1. Clear map 1, activate map 1 (load default: snmp will become OFF)
2. Unregister all card, register all card with protection mode
3. Check all card are working
4. Construct map , adjust clock mode=SSM
5. Store configure
6. Upload configure
7. Send data path
8. Tributary card reset (MIB: cold/warm)
9. Check data path won’t unsync
10. XCU Downgrade to previous version (V1.15.01.0053)
11. XCU Upgrade to current version (V1.15.02.0001)
12. Check download version is correct
13. XCU Reset (standby cold/warm)
14. Check data path is sync., no any bit error,unsync sec.
15. XCU Reset (working warm/cold)
16. Check data path won’t unsync (working warm : no bit error , working cold: unsync sec<2)
17. Clear map 1
18. Retrieve configure
19. Send data path
20. Check data path won’t unsync
21. Power on/off
22. Send data path
23. Check data path won’t unsync

I first need to report the V4150 regression testing plan. The presentation is divided into two parts. The first part is an introduction to the testing environment, and the second part is an introduction to the testing items.

In the section on the testing environment, two types of circuit connections are introduced. The first type is Y protection, and the second type is 1+1 protection. The circuit construction, card types, and clock sources are the same for both types of connections. My cards are classified into two categories: the first category includes T1 and T3, and the second category includes T1 and B155. In the second part, there will be more detailed testing combinations for card functionalities. Additionally, I initially conducted the testing using the US standard.

Next, I will present my testing architecture diagram. In terms of the architecture, the initial step is to reset the settings to their default values before starting the tests. Then, card registration takes place, which can be either in a protected or unprotected state. Following that, the card parameters are set, circuits are constructed, clock sources are configured, and the testing begins. Once these steps are completed, the data is saved and uploaded. Then, the BERT (Bit Error Rate Tester) is initiated. This BERT belongs to the PDH (Plesiochronous Digital Hierarchy) level and starts from T1. During data transmission, various destructive tests are performed, including resetting the motherboard, resetting the cards, upgrading/downgrading versions, power on/off, and port enable/disable. The sub-card and motherboard statuses are checked, as well as the data transmission conditions. After completing these steps, the sub-cards are loaded with default settings, and circuits are deleted. Subsequently, the functionalities of downloading configuration and retrieving are tested. This outlines the general flow of the process.

Afterward, the plan is divided into several cases. These testing items will be discussed in more detail, and some protection combinations will be listed.

Lastly, there is a schedule for both manual and automated testing. The manual testing will be conducted until July 15th, and for the automated testing, it is divided into two parts. The first part is the estimated time for setting up the environment, which is expected to be completed by July 31st, considering the large volume of materials involved. The second part is when the automated testing will begin. During this period, there may be challenges related to the testing process or card hardware. It is hoped that in the following month, these issues can be resolved, and a complete round of testing can be performed.