Program Assignment 2:
Static Timing Analysis

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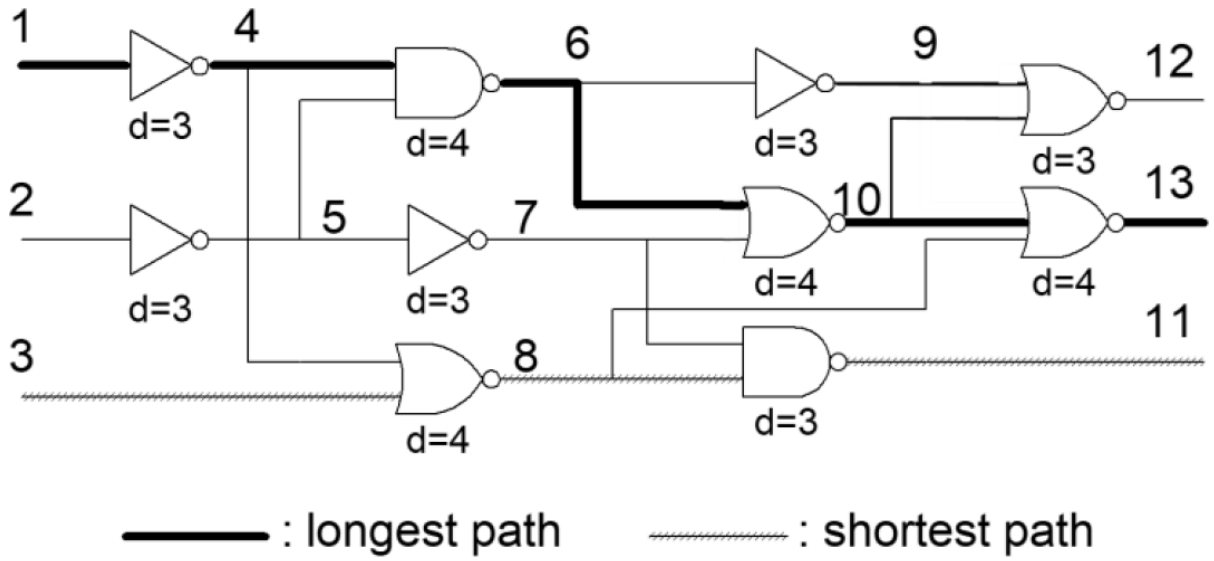
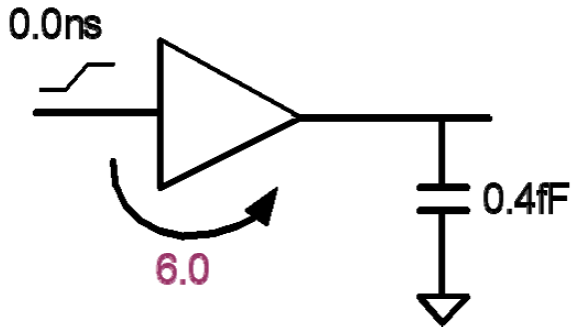
Delay Calculation

- Given a gate-level netlist
  - Determine propagation delay and output transition time (slew) of each gate
  - Find the longest path and the shortest path



Delay Calculation on a Cell

- Lookup table
  - Table Input
    - Input transition time (slew)
    - Output capacitance
  - Table output
    - Delay
    - Output transition time (slew)

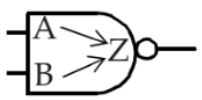


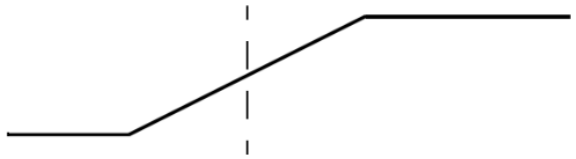
Input Transition (ns) \ Total Output Load (fF)	0.2	0.3	0.4	0.5
0	3	4.5	6	7
0.1	5	8	10.7	13

Cell Delay (ps)

Delay Calculation on Multi-input Cell

- Multiple timing arcs (delay and slew) may be found, input transition time is defined by the input that arrives latest





(a) Slew at pin Z due to A->Z arc.

(b) Slew at pin Z due to B->Z arc.

  - In this example, signal of input pin “B” will define the input transition time of this gate

Worst-case Output Calculation

- After you get the input transition time and output loading, calculate the propagation delay of both output situations (output = 0 and output = 1)

- The one that has larger propagation delay will be the worst-case output, then output transition time is defined according to worst-case output
  - If the output is 0, output transition time is defined by its output falling time
  - If the output is 1, output transition time is defined by its output rising time

Boundary Condition & Assumption

- Input transition time set to **0ns**
- Output loading set to **0.03pF**
- Wire Delay set to **0.005ns**