SOC_Lab2　311510207　江尹凡

- **Brief introduction about the overall system**

設計濾波器試著搭配不同的 interface 跑整個流程，觀察不同

interface 的差異

- **What is observed & learned**

Differences between MAXI and Stream interface

Stream 少了 address 的概念，所以在握手上也不用握地址，但因為沒有地址，所以必須搭配 DMA 做使用

MAXI: address、data 有各自獨立的通道，藉由握手後傳輸。

Differences between csim and cosim

c-sim:　testbench、kernel 都是 c code，compile 後變.exe 跑在 host-cpu 上。

co-sim :　testbench 還是 c code，但 kernel 是 verilog (跑在 simulation 裡面)，tesbench、kernel 會是不同的 process 互相交換 data，比較 testbench kernel 分開跑。

Screen dump

FIRN11MAXI

C_sim

fir_n11_maxi_csim - 記事本

檔案(F) 編輯(E) 格式(O) 檢視(V) 說明

```
INFO: [SIM 2] *************** CSIM start ***************
INFO: [SIM 4] CSIM will launch GCC as the compiler.
   Compiling ../../../FIRTester.cpp in debug mode
   Generating csim.exe
>> Start test!
>> Comparing against output data...
>> Test passed!
-----------------------
INFO: [SIM 1] CSim done with 0 errors.
INFO: [SIM 3] *************** CSIM finish ***************
```

Synthesis Summary Report

```
================================================================
== Performance Estimates
================================================================
+ Timing:
    * Summary:
    +--------+----------+----------+------------+
    |  Clock |  Target  | Estimated| Uncertainty|
    +--------+----------+----------+------------+
    |ap_clk  |  10.00 ns|  7.300 ns|     2.70 ns|
    +--------+----------+----------+------------+

+ Latency:
    * Summary:
    +---------+---------+----------+----------+-----+-----+---------+
    |  Latency (cycles) |  Latency (absolute) |  Interval | Pipeline|
    |   min   |   max   |    min   |    max   | min | max |   Type  |
    +---------+---------+----------+----------+-----+-----+---------+
    |        ?|        ?|         ?|         ?|    ?|    ?|       no|
    +---------+---------+----------+----------+-----+-----+---------+
```

Performence

```
+ Performance & Resource Estimates:

    PS: '+' for module; 'o' for loop; '*' for dataflow
    +---------------------------------+-----+------+---------+---------+----------+---------+------+----------+-------+----------+-----------+-----------+-----+
    |              Modules            | Issue|      | Latency | Latency| Iteration|         | Trip |          |       |          |           |           |     |
    |              & Loops            | Type | Slack| (cycles)|  (ns)  |  Latency | Interval| Count| Pipelined|  BRAM  |    DSP   |     FF    |    LUT    | URAM|
    +---------------------------------+-----+------+---------+---------+----------+---------+------+----------+-------+----------+-----------+-----------+-----+
    |+ fir_n11_maxi                   |     -|  0.00|        -|        -|         -|        -|     -|        no|  4 (1%)|  33 (15%)|  4624 (4%)|  2606 (4%)|    -|
    | + fir_n11_maxi_Pipeline_XFER_LOOP |     -|  0.00|        -|        -|         -|        -|     -|        no|       -|  33 (15%)|  2975 (2%)|  1221 (2%)|    -|
    |  o XFER_LOOP                    |     -|  7.30|        -|        -|        21|        1|     -|       yes|       -|         -|          -|          -|    -|
    +---------------------------------+-----+------+---------+---------+----------+---------+------+----------+-------+----------+-----------+-----------+-----+
```

Utilization

== Utilization Estimates

* Summary:

Name	BRAM_18K	DSP	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	40	-
FIFO	-	-	-	-	-
Instance	4	33	4099	2391	-
Memory	-	-	-	-	-
Multiplexer	-	-	-	175	-
Register	-	-	525	-	-
Total	4	33	4624	2606	0
Available	280	220	106400	53200	0
Utilization (%)	1	15	4	4	0

+ Detail:
    * Instance:

Instance	Module	BRAM_18K	DSP	FF	LUT	URAM
control_s_axi_U	control_s_axi	0	0	294	436	0
grp_fir_n11_maxi_Pipeline_XFER_LOOP_fu_238	fir_n11_maxi_Pipeline_XFER_LOOP	0	33	2975	1221	0
gmem_m_axi_U	gmem_m_axi	4	0	830	734	0
Total		4	33	4099	2391	0

Interface

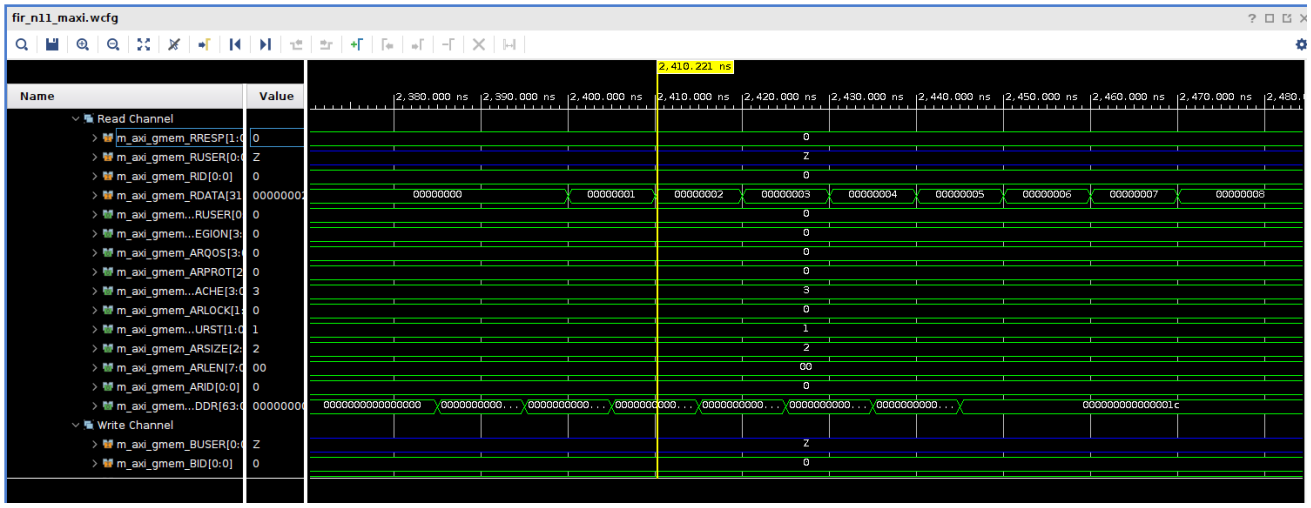
== Interface

* Summary:

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
s_axi_control_AWVALID	in	1	s_axi	control	array
s_axi_control_AWREADY	out	1	s_axi	control	array
s_axi_control_AWADDR	in	7	s_axi	control	array
s_axi_control_WVALID	in	1	s_axi	control	array
s_axi_control_WREADY	out	1	s_axi	control	array
s_axi_control_WDATA	in	32	s_axi	control	array
s_axi_control_WSTRB	in	4	s_axi	control	array
s_axi_control_ARVALID	in	1	s_axi	control	array
s_axi_control_ARREADY	out	1	s_axi	control	array
s_axi_control_ARADDR	in	7	s_axi	control	array
s_axi_control_RVALID	out	1	s_axi	control	array
s_axi_control_RREADY	in	1	s_axi	control	array
s_axi_control_RDATA	out	32	s_axi	control	array
s_axi_control_RRESP	out	2	s_axi	control	array
s_axi_control_BVALID	out	1	s_axi	control	array
s_axi_control_BREADY	in	1	s_axi	control	array
s_axi_control_BRESP	out	2	s_axi	control	array
ap_clk	in	1	ap_ctrl_hs	fir_n11_maxi	return value
ap_rst_n	in	1	ap_ctrl_hs	fir_n11_maxi	return value
interrupt	out	1	ap_ctrl_hs	fir_n11_maxi	return value
m_axi_gmem_AWVALID	out	1	m_axi	gmem	pointer
m_axi_gmem_AWREADY	in	1	m_axi	gmem	pointer
m_axi_gmem_AWADDR	out	64	m_axi	gmem	pointer
m_axi_gmem_AWID	out	1	m_axi	gmem	pointer
m_axi_gmem_AWLEN	out	8	m_axi	gmem	pointer
m_axi_gmem_AWSIZE	out	3	m_axi	gmem	pointer
m_axi_gmem_AWBURST	out	2	m_axi	gmem	pointer
m_axi_gmem_AWLOCK	out	2	m_axi	gmem	pointer
m_axi_gmem_AWCACHE	out	4	m_axi	gmem	pointer
m_axi_gmem_AWPROT	out	3	m_axi	gmem	pointer
m_axi_gmem_AWQOS	out	4	m_axi	gmem	pointer
m_axi_gmem_AWREGION	out	4	m_axi	gmem	pointer
m_axi_gmem_AWUSER	out	1	m_axi	gmem	pointer
m_axi_gmem_WVALID	out	1	m_axi	gmem	pointer
m_axi_gmem_WREADY	in	1	m_axi	gmem	pointer
m_axi_gmem_WDATA	out	32	m_axi	gmem	pointer
m_axi_gmem_WSTRB	out	4	m_axi	gmem	pointer
m_axi_gmem_WLAST	out	1	m_axi	gmem	pointer
m_axi_gmem_WID	out	1	m_axi	gmem	pointer
m_axi_gmem_WUSER	out	1	m_axi	gmem	pointer
m_axi_gmem_ARVALID	out	1	m_axi	gmem	pointer
m_axi_gmem_ARREADY	in	1	m_axi	gmem	pointer
m_axi_gmem_ARADDR	out	64	m_axi	gmem	pointer
m_axi_gmem_ARID	out	1	m_axi	gmem	pointer
m_axi_gmem_ARLEN	out	8	m_axi	gmem	pointer
m_axi_gmem_ARSIZE	out	3	m_axi	gmem	pointer
m_axi_gmem_ARBURST	out	2	m_axi	gmem	pointer
m_axi_gmem_ARLOCK	out	2	m_axi	gmem	pointer
m_axi_gmem_ARCACHE	out	4	m_axi	gmem	pointer
m_axi_gmem_ARPROT	out	3	m_axi	gmem	pointer
m_axi_gmem_ARQOS	out	4	m_axi	gmem	pointer
m_axi_gmem_ARREGION	out	4	m_axi	gmem	pointer
m_axi_gmem_ARUSER	out	1	m_axi	gmem	pointer
m_axi_gmem_RVALID	in	1	m_axi	gmem	pointer
m_axi_gmem_RREADY	out	1	m_axi	gmem	pointer
m_axi_gmem_RDATA	in	32	m_axi	gmem	pointer
m_axi_gmem_RLAST	in	1	m_axi	gmem	pointer
m_axi_gmem_RID	in	1	m_axi	gmem	pointer
m_axi_gmem_RUSER	in	1	m_axi	gmem	pointer
m_axi_gmem_RRESP	in	2	m_axi	gmem	pointer
m_axi_gmem_BVALID	in	1	m_axi	gmem	pointer
m_axi_gmem_BREADY	out	1	m_axi	gmem	pointer
m_axi_gmem_BRESP	in	2	m_axi	gmem	pointer
m_axi_gmem_BID	in	1	m_axi	gmem	pointer
m_axi_gmem_BUSER	in	1	m_axi	gmem	pointer

Co-simulation transcript/waveform

```
-----------------------
INFO: [COSIM 212-1000] *** C/RTL co-simulation finished: PASS ***
INFO: [COSIM 212-211] II is measurable only when transaction number is greater than 1 in RTL simulation. Otherwise, they will be marked as all NA. If user wants to calculate them, please
INFO: [HLS 200-111] Finished Command cosim_design CPU user time: 14.55 seconds. CPU system time: 2.5 seconds. Elapsed time: 19.39 seconds; current allocated memory: 11.129 MB.
INFO: [HLS 200-112] Total CPU user time: 16.31 seconds. Total CPU system time: 2.8 seconds. Total elapsed time: 21.45 seconds; peak allocated memory: 1.101 GB.
Finished C/RTL cosimulation.
```

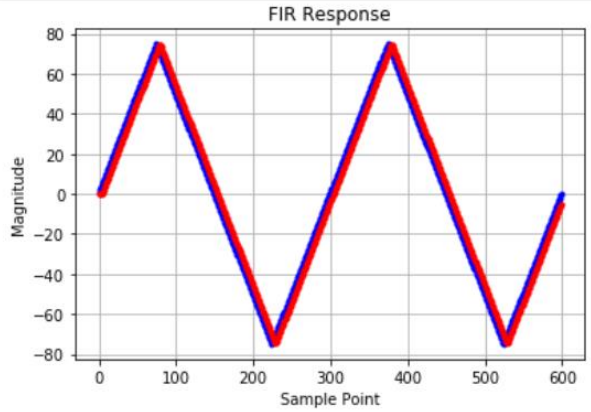


Jupyter Notebook execution results

In [1]:

```
# coding: utf-8

# In[ ]:


from __future__ import print_function

import sys, os
import numpy as np
from time import time
import matplotlib.pyplot as plt

sys.path.append('/home/xilinx')
os.environ['XILINX_XRT'] = '/usr'
from pynq import Overlay
from pynq import allocate

if __name__ == "__main__":
    print("Entry:", sys.argv[0])
    print("System argument(s):", len(sys.argv))

    print("Start of \"" + sys.argv[0] + "\"")

    ol = Overlay("FIRN11MAXI.bit")
    ipFIRN11 = ol.fir_n11_maxi_0

    fiSamples = open("samples_triangular_wave.txt", "r+")
    numSamples = 0
    line = fiSamples.readline()
    while line:
        numSamples = numSamples + 1
        line = fiSamples.readline()

    inBuffer0 = allocate(shape=(numSamples,), dtype=np.int32)
    outBuffer0 = allocate(shape=(numSamples,), dtype=np.int32)
    fiSamples.seek(0)
    for i in range(numSamples):
        line = fiSamples.readline()
        inBuffer0[i] = int(line)
    fiSamples.close()

    numTaps = 11
    n32Taps = [0, -10, -9, 23, 56, 63, 56, 23, -9, -10, 0]
    #n32Taps = [1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1]
    n32DCGain = 0
    timeKernelStart = time()
    for i in range(numTaps):
        n32DCGain = n32DCGain + n32Taps[i]
        ipFIRN11.write(0x40 + i * 4, n32Taps[i])
    if n32DCGain < 0:
        n32DCGain = 0 - n32DCGain
    ipFIRN11.write(0x28, len(inBuffer0) * 4)
    ipFIRN11.write(0x10, inBuffer0.device_address)
    ipFIRN11.write(0x1C, outBuffer0.device_address)
    ipFIRN11.write(0x00, 0x01)
    while (ipFIRN11.read(0x00) & 0x4) == 0x0:
        continue
    timeKernelEnd = time()
```

```
print("Kernel execution time: " + str(timeKernelEnd - timeKernelStart) + " s")

plt.title("FIR Response")
plt.xlabel("Sample Point")
plt.ylabel("Magnitude")
xSeq = range(len(inBuffer0))
if n32DCGain == 0:
    plt.plot(xSeq, inBuffer0, 'b.', xSeq, outBuffer0, 'r.')
else:
    plt.plot(xSeq, inBuffer0, 'b.', xSeq, outBuffer0 / n32DCGain, 'r.')
plt.grid(True)
plt.show() # In Jupyter, press Tab + Shift keys to show plot then redo run

print("============================")
print("Exit process")
```




```
============================
Exit process
```

FIRN11Stream

C_sim

fir_n11_strm_csim - 記事本

檔案(F) 編輯(E) 格式(O) 檢視(V) 說明

```
INFO: [SIM 2] *************** CSIM start ***************
INFO: [SIM 4] CSIM will launch GCC as the compiler.
   Compiling ../../../FIRTester.cpp in debug mode
   Compiling ../../../FIR.cpp in debug mode
   Generating csim.exe
>> Start test!
>> Comparing against output data...
>> Test passed!
-----------------------
INFO [HLS SIM]: The maximum depth reached by any hls::stream() instance in the design is 600
INFO: [SIM 1] CSim done with 0 errors.
INFO: [SIM 3] *************** CSIM finish ***************
```

Synthesis Summary Report

```
================================================================
== Vitis HLS Report for 'fir_n11_strm'
================================================================
* Date:           Tue Oct  3 09:18:24 2023

* Version:        2023.1 (Build 3854077 on May  4 2023)
* Project:        Lab2_1
* Solution:       solution1 (Vivado IP Flow Target)
* Product family: zynq
* Target device:  xc7z020-clg400-1


================================================================
== Performance Estimates
================================================================
+ Timing:
    * Summary:
    +--------+----------+----------+------------+
    |  Clock |  Target  | Estimated| Uncertainty|
    +--------+----------+----------+------------+
    |ap_clk  |  10.00 ns|  7.936 ns|     2.70 ns|
    +--------+----------+----------+------------+
```

Performence

```
================================================================
== Synthesis Summary Report of 'fir_n11_strm'
================================================================
+ General Information:
    * Date:           Tue Oct  3 09:18:25 2023
    * Version:        2023.1 (Build 3854077 on May  4 2023)
    * Project:        Lab2_1
    * Solution:       solution1 (Vivado IP Flow Target)
    * Product family: zynq
    * Target device:  xc7z020-clg400-1


+ Performance & Resource Estimates:

    PS: '+' for module; 'o' for loop; '*' for dataflow
    +---------------------------------+--------+------+---------+---------+----------+---------+------+----------+------+--------+----------+----------+-----+
    |             Modules             |  Issue |      | Latency | Latency| Iteration|         | Trip |          |      |        |          |          |     |
    |             & Loops             |  Type  | Slack | (cycles)|  (ns)  |  Latency | Interval| Count| Pipelined| BRAM |   DSP  |    FF    |    LUT   | URAM|
    +---------------------------------+--------+------+---------+---------+----------+---------+------+----------+------+--------+----------+----------+-----+
    |+ fir_n11_strm                   |  Timing|  -0.64|        -|        -|         -|        -|     -|        no|     -|  3 (1%)|  1118 (1%)|  951 (1%)|    -|
    | + fir_n11_strm_Pipeline_XFER_LOOP  |  Timing|  -0.64|        -|        -|         -|        -|     -|        no|     -|  3 (1%)|  928 (~0%)|  695 (1%)|    -|
    |  o XFER_LOOP                    |      II|   7.30|        -|        -|        15|       11|     -|       yes|     -|       -|         -|         -|    -|
    +---------------------------------+--------+------+---------+---------+----------+---------+------+----------+------+--------+----------+----------+-----+
```

Utilization

```
================================================================
== Utilization Estimates
================================================================
* Summary:
+-----------------+---------+-----+--------+-------+-----+
|       Name      | BRAM_18K| DSP |   FF   |  LUT  | URAM|
+-----------------+---------+-----+--------+-------+-----+
|DSP              |        -|    -|       -|      -|    -|
|Expression       |        -|    -|       0|     42|    -|
|FIFO             |        -|    -|       -|      -|    -|
|Instance         |        0|    3|    1082|    875|    -|
|Memory           |        -|    -|       -|      -|    -|
|Multiplexer      |        -|    -|       -|     34|    -|
|Register         |        -|    -|      36|      -|    -|
+-----------------+---------+-----+--------+-------+-----+
|Total            |        0|    3|    1118|    951|    0|
+-----------------+---------+-----+--------+-------+-----+
|Available        |      280|  220|  106400|  53200|    0|
+-----------------+---------+-----+--------+-------+-----+
|Utilization (%)  |        0|    1|       1|      1|    0|
+-----------------+---------+-----+--------+-------+-----+

+ Detail:
    * Instance:
    +-----------------------------------------+---------------------------------+---------+----+-----+-----+-----+
    |                 Instance                |              Module             | BRAM_18K| DSP|  FF | LUT | URAM|
    +-----------------------------------------+---------------------------------+---------+----+-----+-----+-----+
    |control_s_axi_U                          |control_s_axi                    |        0|   0|  154|  180|    0|
    |grp_fir_n11_strm_Pipeline_XFER_LOOP_fu_118  |fir_n11_strm_Pipeline_XFER_LOOP  |        0|   3|  928|  695|    0|
    +-----------------------------------------+---------------------------------+---------+----+-----+-----+-----+
    |Total                                    |                                 |        0|   3| 1082|  875|    0|
    +-----------------------------------------+---------------------------------+---------+----+-----+-----+-----+
```

Interface

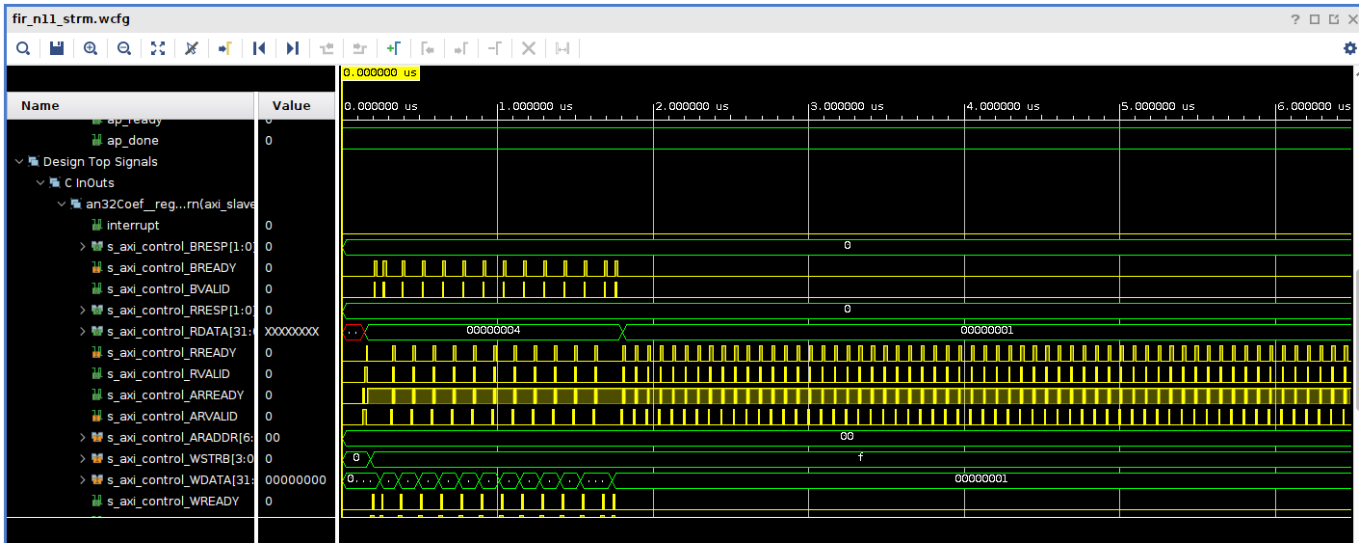
== Interface

* Summary:

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
s_axi_control_AWVALID	in	1	s_axi	control	array
s_axi_control_AWREADY	out	1	s_axi	control	array
s_axi_control_AWADDR	in	7	s_axi	control	array
s_axi_control_WVALID	in	1	s_axi	control	array
s_axi_control_WREADY	out	1	s_axi	control	array
s_axi_control_WDATA	in	32	s_axi	control	array
s_axi_control_WSTRB	in	4	s_axi	control	array
s_axi_control_ARVALID	in	1	s_axi	control	array
s_axi_control_ARREADY	out	1	s_axi	control	array
s_axi_control_ARADDR	in	7	s_axi	control	array
s_axi_control_RVALID	out	1	s_axi	control	array
s_axi_control_RREADY	in	1	s_axi	control	array
s_axi_control_RDATA	out	32	s_axi	control	array
s_axi_control_RRESP	out	2	s_axi	control	array
s_axi_control_BVALID	out	1	s_axi	control	array
s_axi_control_BREADY	in	1	s_axi	control	array
s_axi_control_BRESP	out	2	s_axi	control	array
ap_clk	in	1	ap_ctrl_hs	fir_n11_strm	return value
ap_rst_n	in	1	ap_ctrl_hs	fir_n11_strm	return value
interrupt	out	1	ap_ctrl_hs	fir_n11_strm	return value
pstrmInput_TDATA	in	32	axis	pstrmInput_V_data_V	pointer
pstrmInput_TVALID	in	1	axis	pstrmInput_V_dest_V	pointer
pstrmInput_TREADY	out	1	axis	pstrmInput_V_dest_V	pointer
pstrmInput_TDEST	in	1	axis	pstrmInput_V_dest_V	pointer
pstrmInput_TKEEP	in	4	axis	pstrmInput_V_keep_V	pointer
pstrmInput_TSTRB	in	4	axis	pstrmInput_V_strb_V	pointer
pstrmInput_TUSER	in	1	axis	pstrmInput_V_user_V	pointer
pstrmInput_TLAST	in	1	axis	pstrmInput_V_last_V	pointer
pstrmInput_TID	in	1	axis	pstrmInput_V_id_V	pointer
pstrmOutput_TDATA	out	32	axis	pstrmOutput_V_data_V	pointer
pstrmOutput_TVALID	out	1	axis	pstrmOutput_V_dest_V	pointer
pstrmOutput_TREADY	in	1	axis	pstrmOutput_V_dest_V	pointer
pstrmOutput_TDEST	out	1	axis	pstrmOutput_V_dest_V	pointer
pstrmOutput_TKEEP	out	4	axis	pstrmOutput_V_keep_V	pointer
pstrmOutput_TSTRB	out	4	axis	pstrmOutput_V_strb_V	pointer
pstrmOutput_TUSER	out	1	axis	pstrmOutput_V_user_V	pointer
pstrmOutput_TLAST	out	1	axis	pstrmOutput_V_last_V	pointer
pstrmOutput_TID	out	1	axis	pstrmOutput_V_id_V	pointer

Co-simulation transcript/waveform

```
-----------------------
INFO [HLS SIM]: The maximum depth reached by any hls::stream() instance in the design is 600
INFO: [COSIM 212-1000] *** C/RTL co-simulation finished: PASS ***
INFO: [COSIM 212-211] II is measurable only when transaction number is greater than 1 in RTL simulation. Otherwise, they will be marked as all NA. If user wants to calculate them, ple
INFO: [HLS 200-111] Finished Command cosim_design CPU user time: 14.53 seconds. CPU system time: 1.5 seconds. Elapsed time: 17.03 seconds; current allocated memory: 12.328 MB.
INFO: [HLS 200-112] Total CPU user time: 16.3 seconds. Total CPU system time: 1.79 seconds. Total elapsed time: 19.11 seconds; peak allocated memory: 1.102 GB.
Finished C/RTL cosimulation.
```



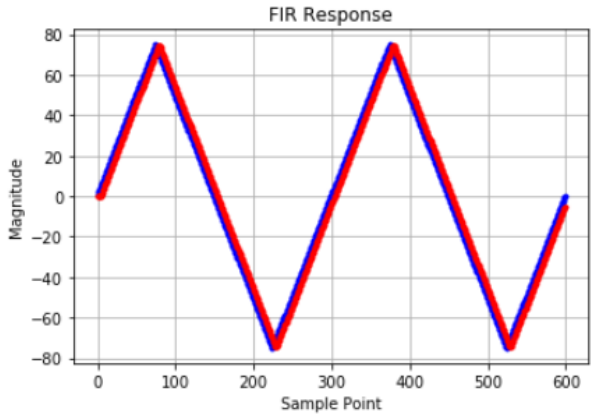
Jupyter Notebook execution results

In [2]:

```
# coding: utf-8

# In[3]:


from __future__ import print_function

import sys, os
import numpy as np
from time import time
import matplotlib.pyplot as plt

sys.path.append('/home/xilinx')
os.environ['XILINX_XRT'] = '/usr'
from pynq import Overlay
from pynq import allocate

if __name__ == "__main__":
    print("Entry:", sys.argv[0])
    print("System argument(s):", len(sys.argv))

    print("Start of \"" + sys.argv[0] + "\"")

    ol = Overlay("FIRN11Stream.bit")
    ipFIRN11 = ol.fir_n11_strm_0
    ipDMAIn = ol.axi_dma_in0
    ipDMAOut = ol.axi_dma_out0

    fiSamples = open("samples_triangular_wave.txt", "r+")
    numSamples = 0
    line = fiSamples.readline()
    while line:
        numSamples = numSamples + 1
        line = fiSamples.readline()

    inBuffer0 = allocate(shape=(numSamples,), dtype=np.int32)
    outBuffer0 = allocate(shape=(numSamples,), dtype=np.int32)
    fiSamples.seek(0)
    for i in range(numSamples):
        line = fiSamples.readline()
        inBuffer0[i] = int(line)
    fiSamples.close()

    numTaps = 11
    n32Taps = [0, -10, -9, 23, 56, 63, 56, 23, -9, -10, 0]
    #n32Taps = [1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1]
    n32DCGain = 0
    timeKernelStart = time()
    for i in range(numTaps):
        n32DCGain = n32DCGain + n32Taps[i]
        ipFIRN11.write(0x40 + i * 4, n32Taps[i])
    if n32DCGain < 0:
        n32DCGain = 0 - n32DCGain
    ipFIRN11.write(0x10, len(inBuffer0) * 4)
    ipFIRN11.write(0x00, 0x01)
    ipDMAIn.sendchannel.transfer(inBuffer0)
    ipDMAOut.recvchannel.transfer(outBuffer0)
    ipDMAIn.sendchannel.wait()
```

```
    ipDMAOut.recvchannel.wait()
    timeKernelEnd = time()
    print("Kernel execution time: " + str(timeKernelEnd - timeKernelStart) + " s")

    plt.title("FIR Response")
    plt.xlabel("Sample Point")
    plt.ylabel("Magnitude")
    xSeq = range(len(inBuffer0))
    if n32DCGain == 0:
        plt.plot(xSeq, inBuffer0, 'b.', xSeq, outBuffer0, 'r.')
    else:
        plt.plot(xSeq, inBuffer0, 'b.', xSeq, outBuffer0 / n32DCGain, 'r.')
    plt.grid(True)
    plt.show() # In Jupyter, press Tab + Shift keys to show plot then redo run

    print("============================")
    print("Exit process")
```

```
Entry: /usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_la
uncher.py
System argument(s): 3
Start of "/usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel
_launcher.py"
Kernel execution time: 0.0016837120056152344 s
```




```
============================
Exit process
```

In [ ]: