NYCU 電子研究所 系統晶片設計 LAB D

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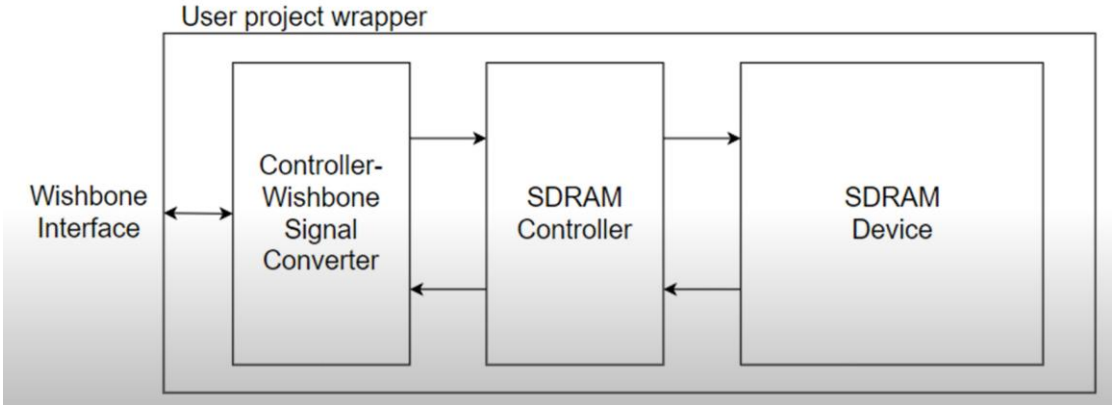
- Introduction

  此次 Lab 與 4-1 十分相似，只是需要把 4-1 中的 BRAM 換成 SDRAM+SDRAM-controller，如下圖所示。

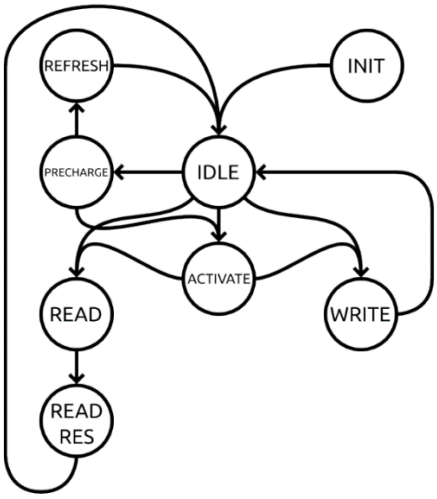


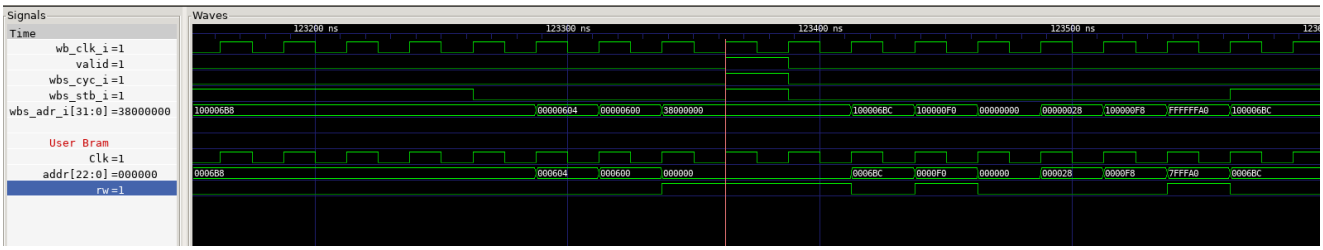
  由於 SDRAM-controller 無法直接與 wishbone 做溝通，因此中間需要再透過一個 converter 來做轉換。

  - SDRAM Device
    - sdram_cle, sdram_cs, sdram_cas, sdram_ras, sdram_we
    - sdram_dqm, sdram_ba, sdram_a
    - sdram_dqi, sdram_dqo
  - User interface
    - user_addr
    - rw
    - data_in, data_out
    - busy
    - in_valid, out_valid

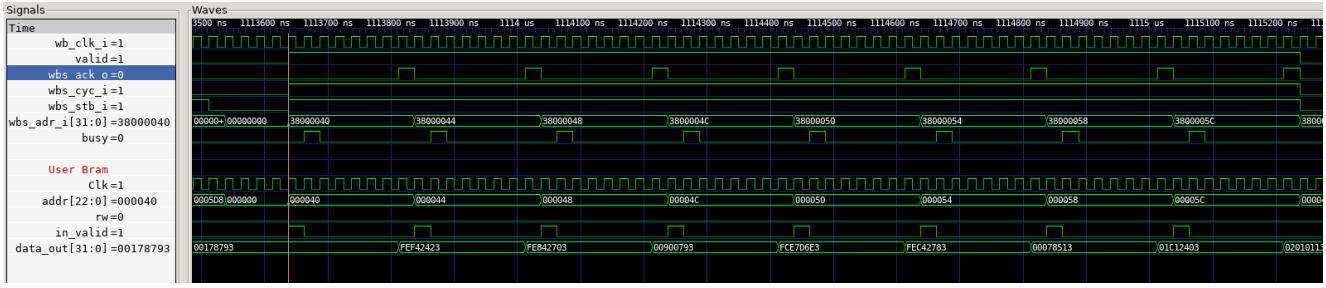
SDRAM Controller

- INIT→IDLE
- IDLE→ACTIVATE→WRITE→IDLE
- IDLE→ACTIVATE→READ→READ_RES →IDLE
- IDLE→WRITE→IDLE
- IDLE→READ→READ_RES→IDLE
- IDLE→PRECHARE→ACTIVATE→WRITE →IDLE
- IDLE→PRECHARE→ACTIVATE→READ →READ_RES→IDLE
- IDLE→PRECHARE→REFRESH→IDLE





write



read (連續讀取) 經觀察可發現，本實驗中會連續讀取 8 筆 code 資訊，且地址為連續

- The behavior model refer to Micron MT48LC64M4A2
  - 16 Meg x 4 x 4 banks