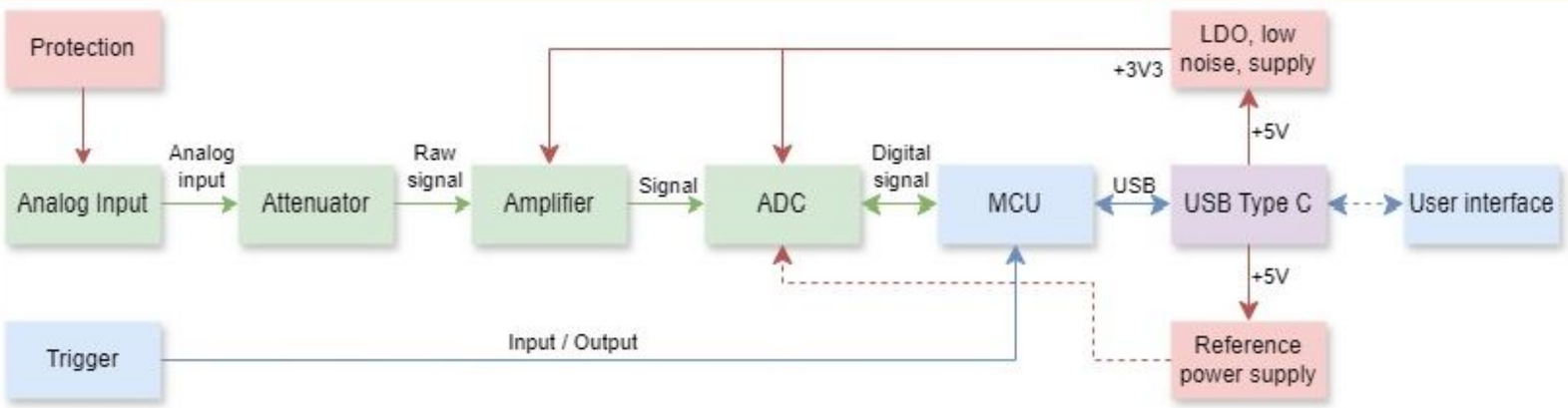
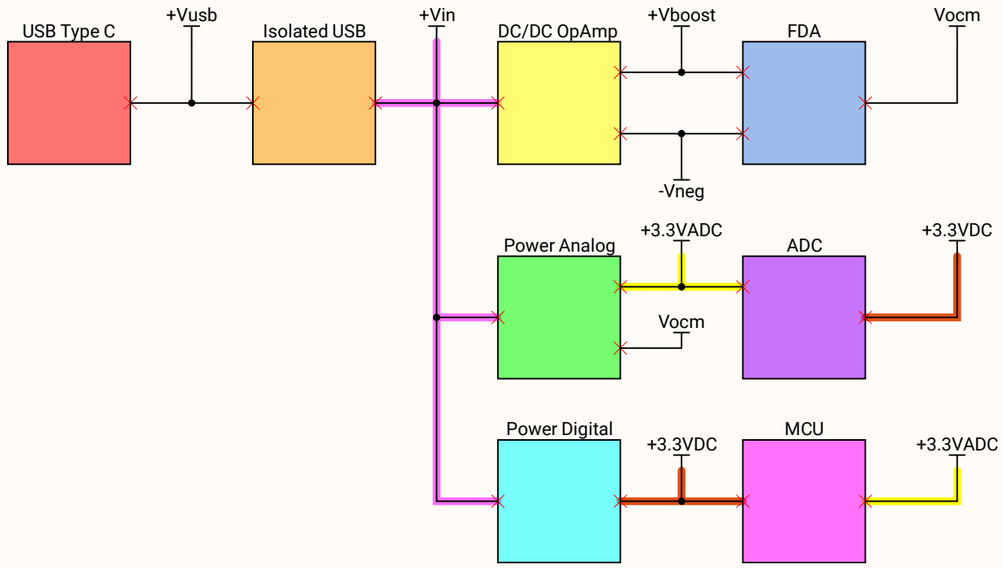
Block Diagram



Power Tree



Pins Function Table

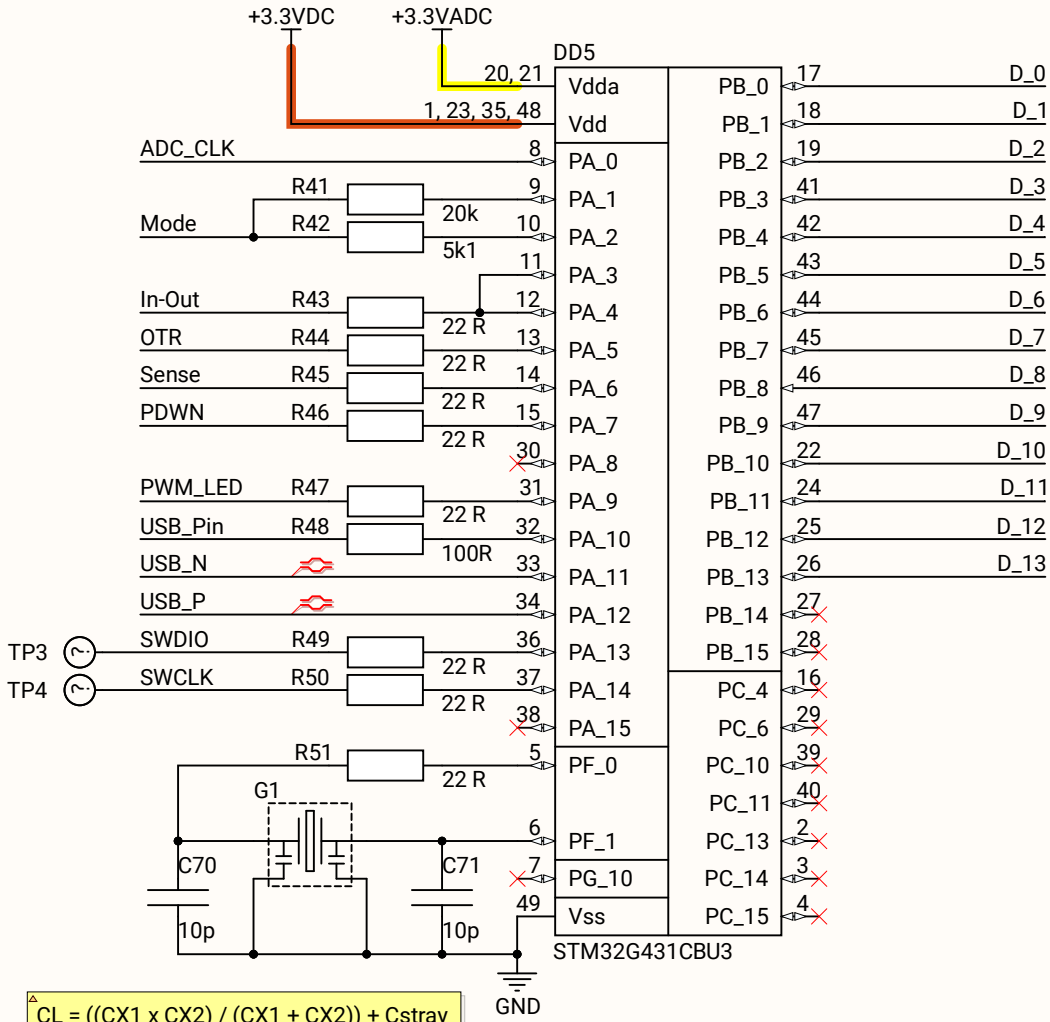
#	Port	Pin	Function	Name	Comment
1	N/A	N/A	Power	Vdd	
2	C	13	NC	N/A	
3	C	14	NC	N/A	
4	C	15	NC	N/A	
5	F	0	OSC+	N/A	
6	F	1	OSC-	N/A	
7	G	0	NC	N/A	
8	A	0	TIM2_1	ADC_CLK	Up to 20 MHz
9	A	1	Output	Mode_1	Twos Complement
10	A	2	Output	Mode_2	Offset Binary
11	A	3	Comp2_Inp	Trigger	
12	A	4	DAC1_1	Trigger_Out	
13	A	5	Input	OTR	From ADC
14	A	6	Output	Sense	Need to be open drain
15	A	7	Output	PDWN	ADC on/off
16	C	4	NC	N/A	
17	B	0	Input	D0	From ADC data line
18	B	1	Input	D1	From ADC data line
19	B	2	Input	D2	From ADC data line
20	N/A	N/A	Power	Vdda	
21	N/A	N/A	Power	Vdda	
22	B	10	Input	D10	From ADC data line
23	N/A	N/A	Power	Vdd	
24	B	11	Input	D11	From ADC data line
25	B	12	Input	D12	From ADC data line
26	B	13	Input	D13	From ADC data line
27	B	14	NC	N/A	
28	B	15	NC	N/A	
29	C	6	NC	N/A	
30	A	8	NC	N/A	
31	A	9	TIM1_2	PWM_LED	For WS2812
32	A	10	Output	USB_Pin	Reboot USB isolator
33	A	11	USB	USB_N	
34	A	12	USB	USB_P	
35	N/A	N/A	Power	Vdd	
36	A	13	SWDIO	SWDIO	
37	A	14	SWCLK	SWCLK	
38	A	15	NC	N/A	
39	C	10	NC	N/A	
40	C	11	NC	N/A	
41	B	3	Input	D3	From ADC data line
42	B	4	Input	D4	From ADC data line
43	B	5	Input	D5	From ADC data line
44	B	6	Input	D6	From ADC data line
45	B	7	Input	D7	From ADC data line
46	B	8	Input	D8	From ADC data line
47	B	9	Input	D9	From ADC data line
48	N/A	N/A	Power	Vdd	
49	N/A	N/A	Vss	GND	

History

Revision	Date	Description
ver 0.1	24.02.2024	Initial draft
ver 0.2	29.03.2024	Finilised version uploaded

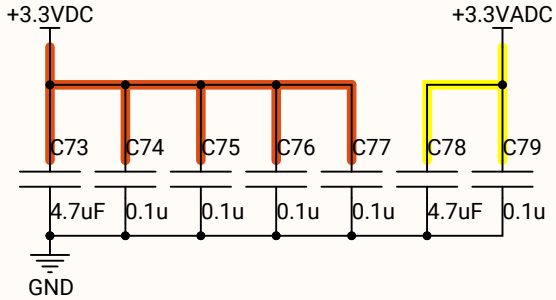
Part Number: '	Rev.: '		Germany, Berlin
Material:	Name: UScope Project		
Units: '		Format: A3	Document: ' / Revision: '
Reviewer: *	Date:	Scale:	Weight: / Page № 1 / Pages: 4

MCU

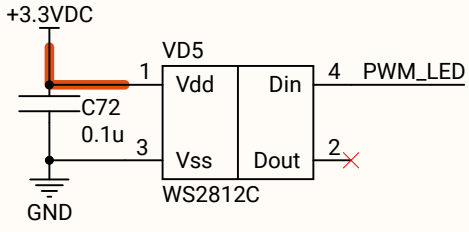


CL = ((CX1 x CX2) / (CX1 + CX2)) + Cstray
CX1 = CX2 = 2*(10 - 5) = 10pF

Decoupling capacitors



LED



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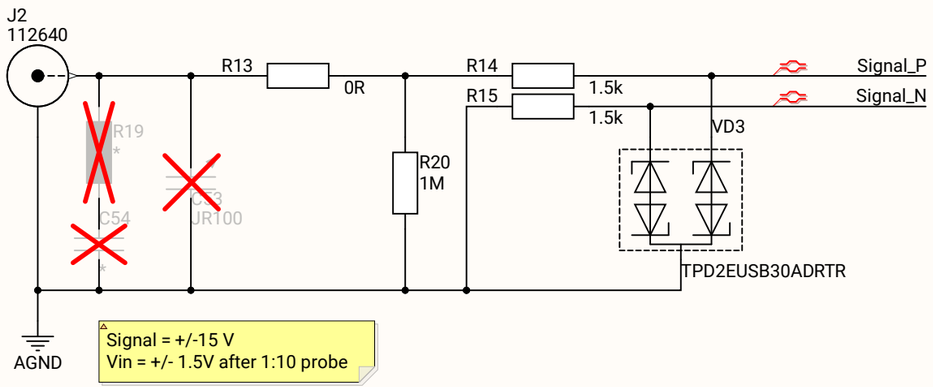
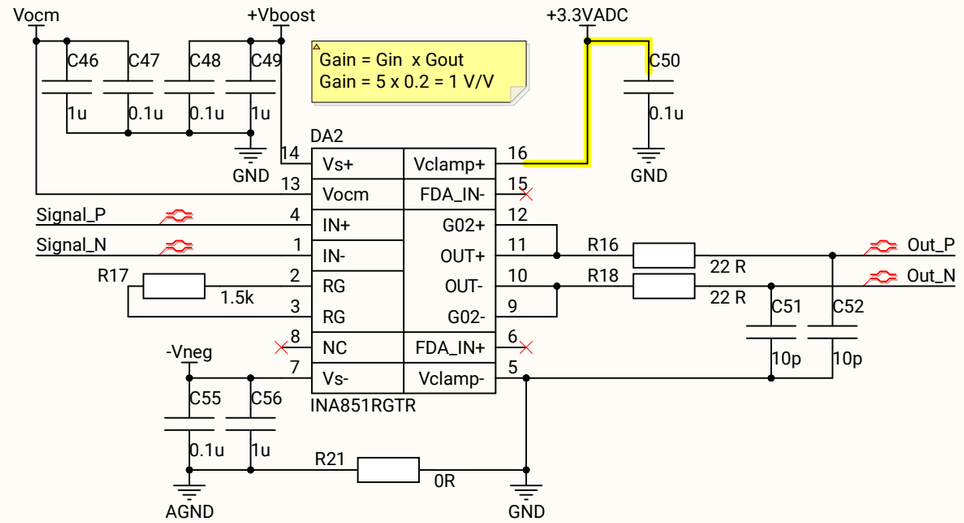
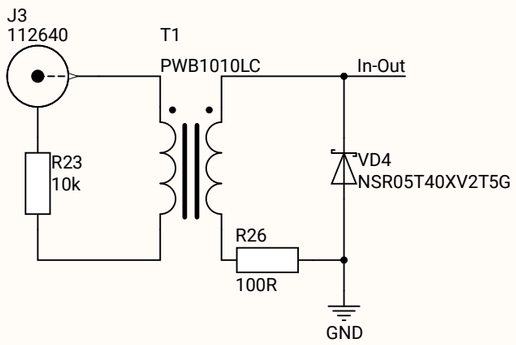
Input



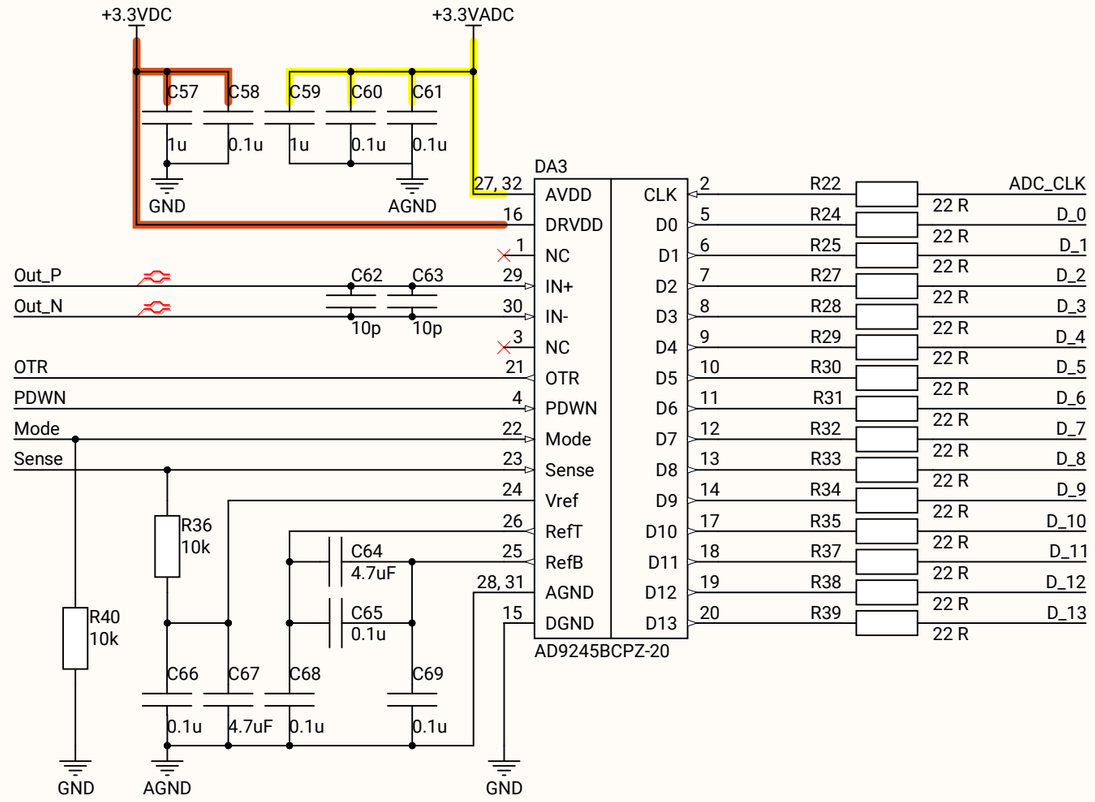
FDA



Input - Output



ADC



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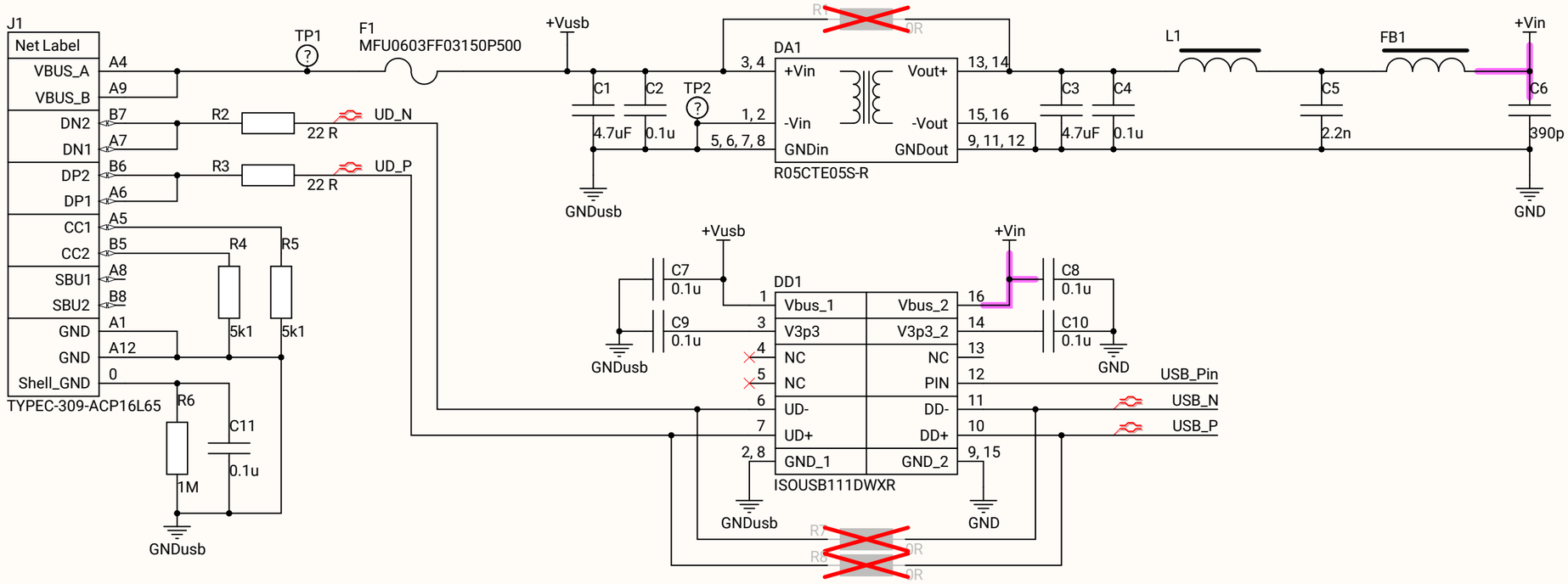
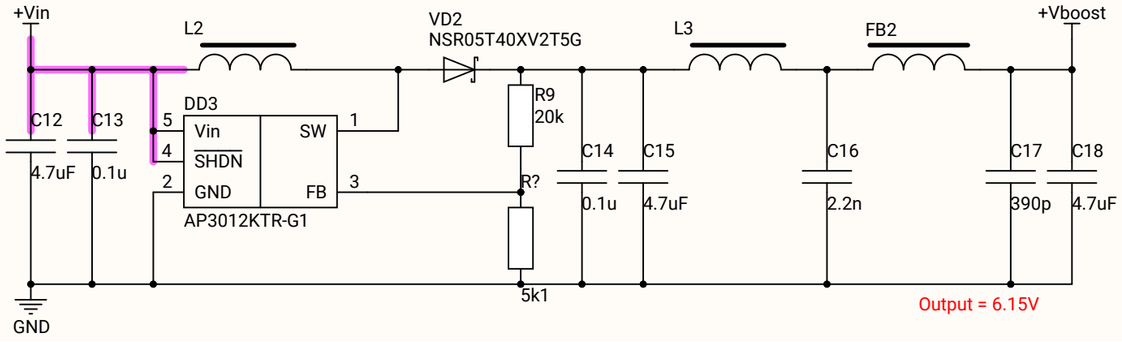
USB

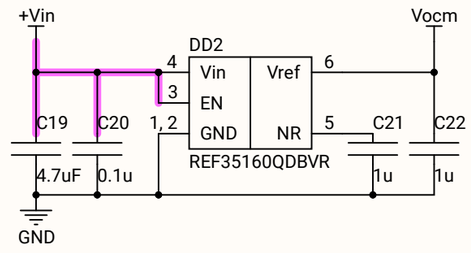
Isolation of USB



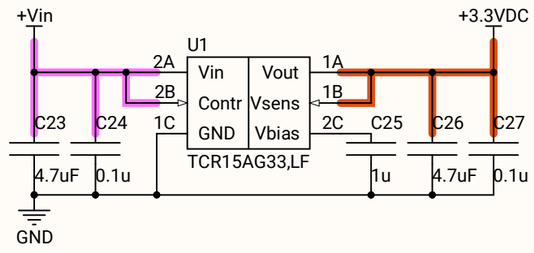
Boost



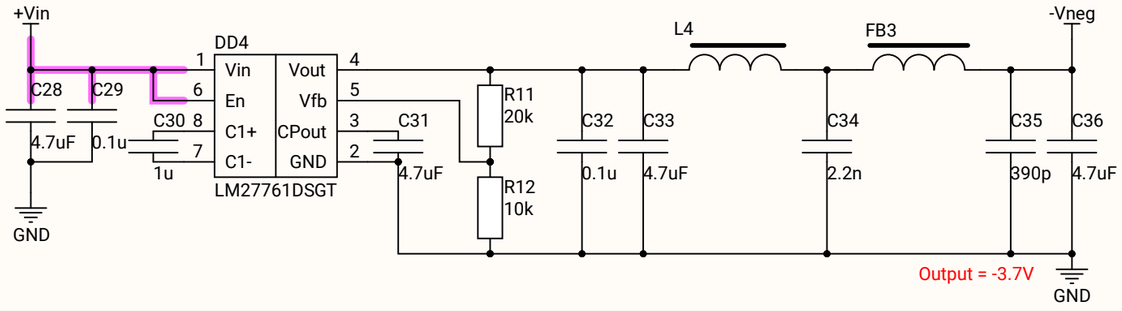
References Supply



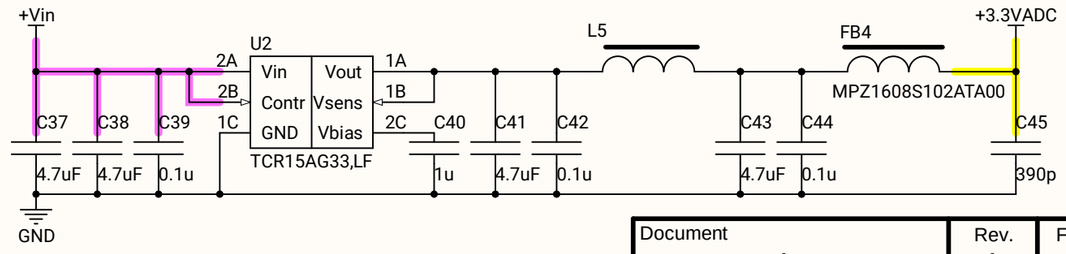
Power Digital



Invertor



Power Analog



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