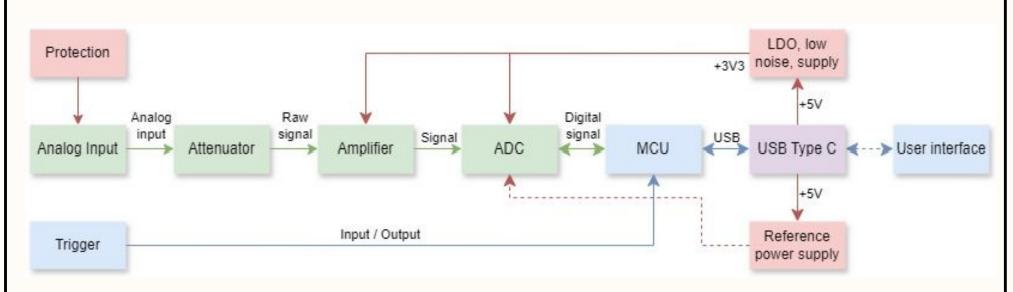
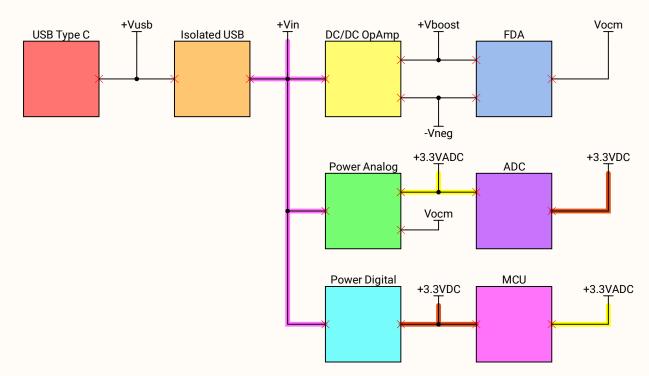
# Block Diagram



### Power Tree



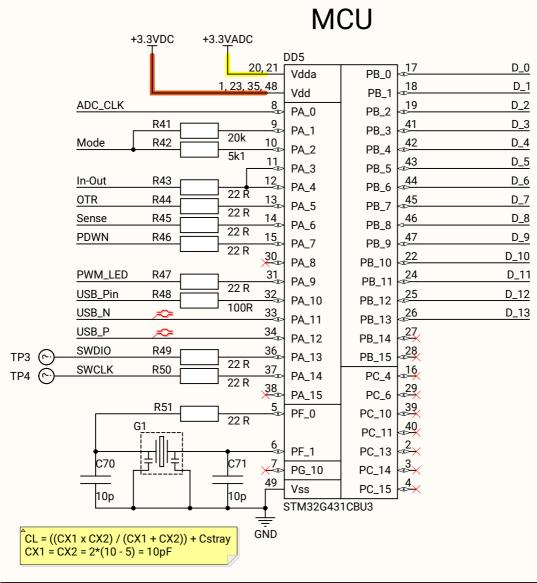
## History

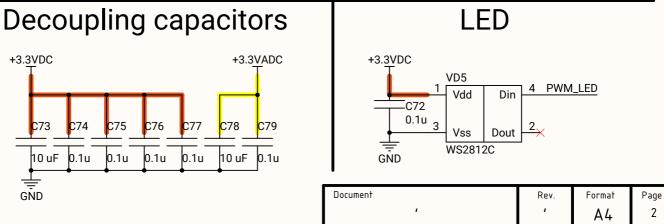
Revision	Date	Description
ver 0.1	24.02.2024	Initial draft
ver 0.2	29.03.2024	Finilised version uploaded

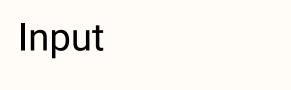
### Pins Function Table

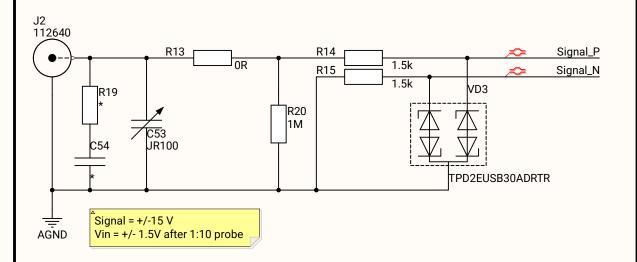
#	Port	Pin	Function	Name	Comment	
1	N/A	N/A	Power	Vdd		
2	С	13	NC	N/A		
3	С	14	NC	N/A		
4	С	15	NC	N/A		
5	F	0	OSC+	N/A		
6	F	1	OSC-	N/A		
7	G	0	NC	N/A		
8	Α	0	TIM2_1	ADC_CLK	Up to 20 MHz	
9	Α	1	Output	Mode_1	Twos Complement	
10	Α	2	Output	Mode_2	Offset Binary	
11	Α	3	Comp2_Inp	Trigger	-	
12	Α	4	DAC1_1	Trigger_Out		
13	Α	5	Input	OTR	From ADC	
14	Α	6	Output	Sense	Need to be open drain	
15	Α	7	Output	PDWN	ADC on/off	
16	С	4	NC	N/A		
17	В	0	Input	D0	From ADC data line	
18	В	1	Input	D1	From ADC data line	
19	В	2	Input	D2	From ADC data line	
20	N/A	N/A	Power	Vdda		
21	N/A	N/A	Power	Vdda		
22	В	10	Input	D10	From ADC data line	
23	N/A	N/A	Power	Vdd		
24	В	11	Input	D11	From ADC data line	
25	В	12	Input	D12	From ADC data line	
26	В	13	Input	D13	From ADC data line	
27	В	14	NC	N/A		
28	В	15	NC	N/A		
29	С	6	NC	N/A		
30	Α	8	NC	N/A		
31	Α	9	TIM1_2	PWM_LED	For WS2812	
32	Α	10	Output	USB_Pin	Reboot USB isolator	
33	Α	11	USB	USB_N		
34	Α	12	USB	USB_P		
35	N/A	N/A	Power	Vdd		
36	Α	13	SWDIO	SWDIO		
37	Α	14	SWCLK	SWCLK		
38	Α	15	NC	N/A		
39	С	10	NC	N/A		
40	С	11	NC	N/A		
41	В	3	Input	D3	From ADC data line	
42	В	4	Input	D4	From ADC data line	
43	В	5	Input	D5	From ADC data line	
44	В	6	Input	D6	From ADC data line	
45	В	7	Input	D7	From ADC data line	
46	В	8	Input	D8	From ADC data line	
47	В	9	Input	D9	From ADC data line	
48	N/A	N/A	Power	Vdd		
49	N/A	N/A	Vss	GND		
L				5.15		

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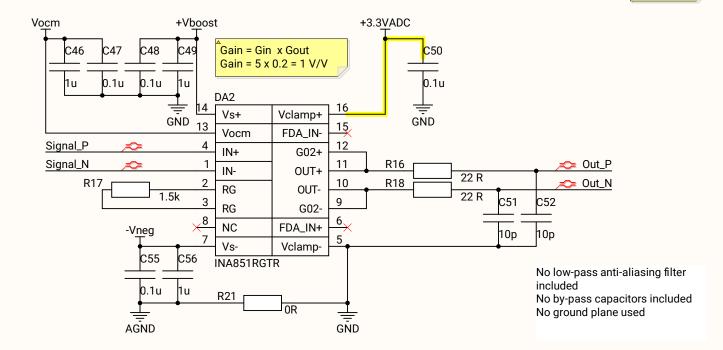




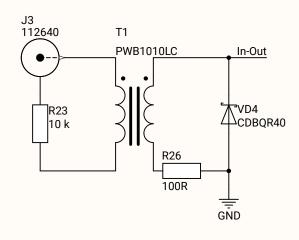


#### FDA

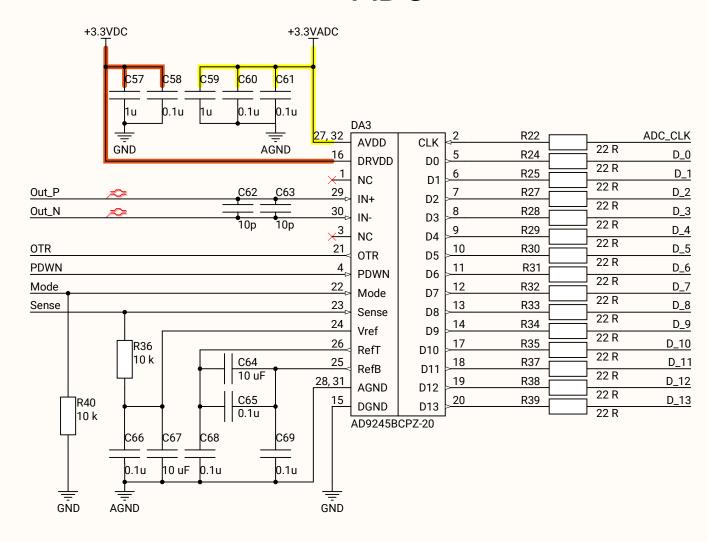




#### Input - Output



#### ADC



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