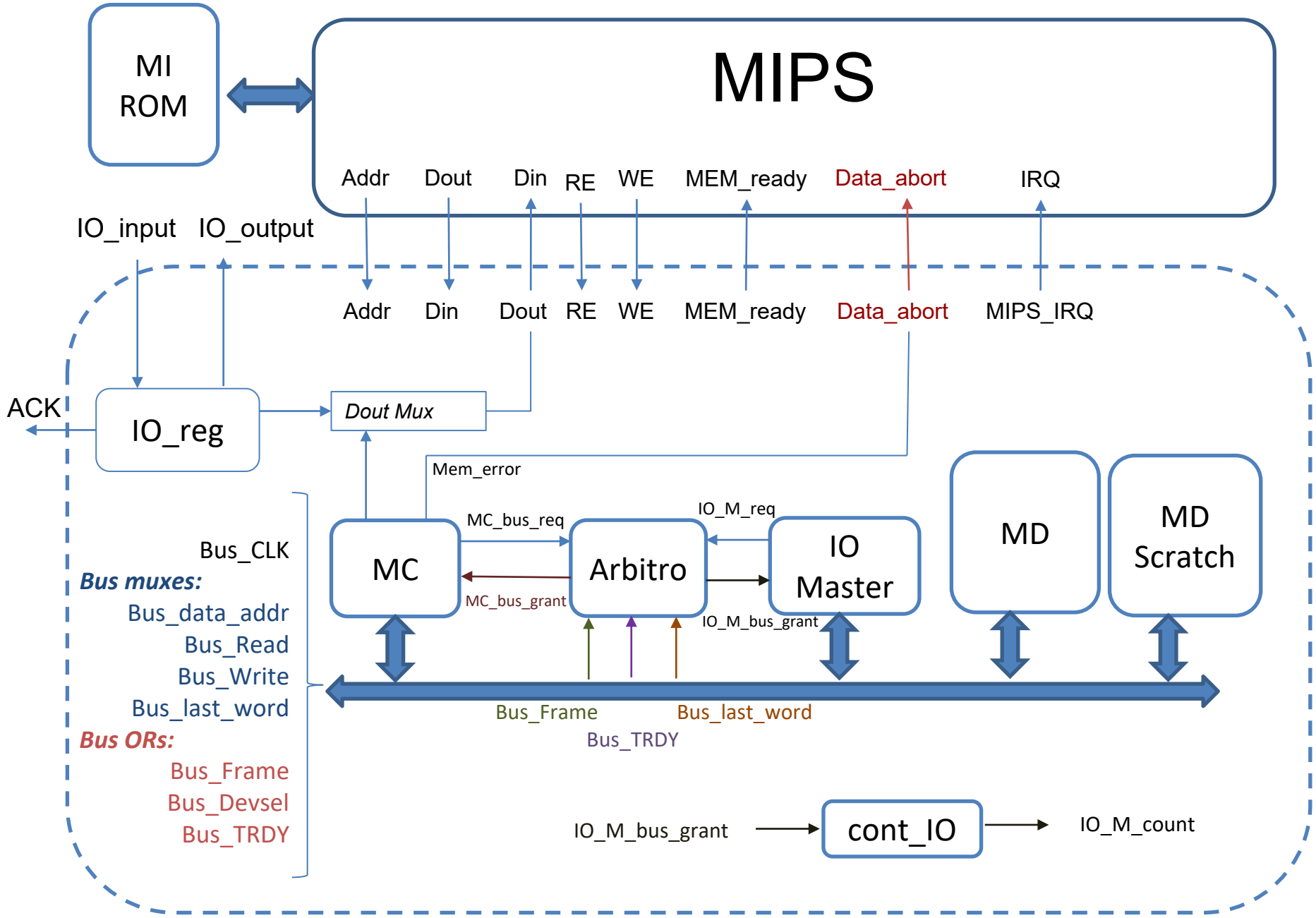
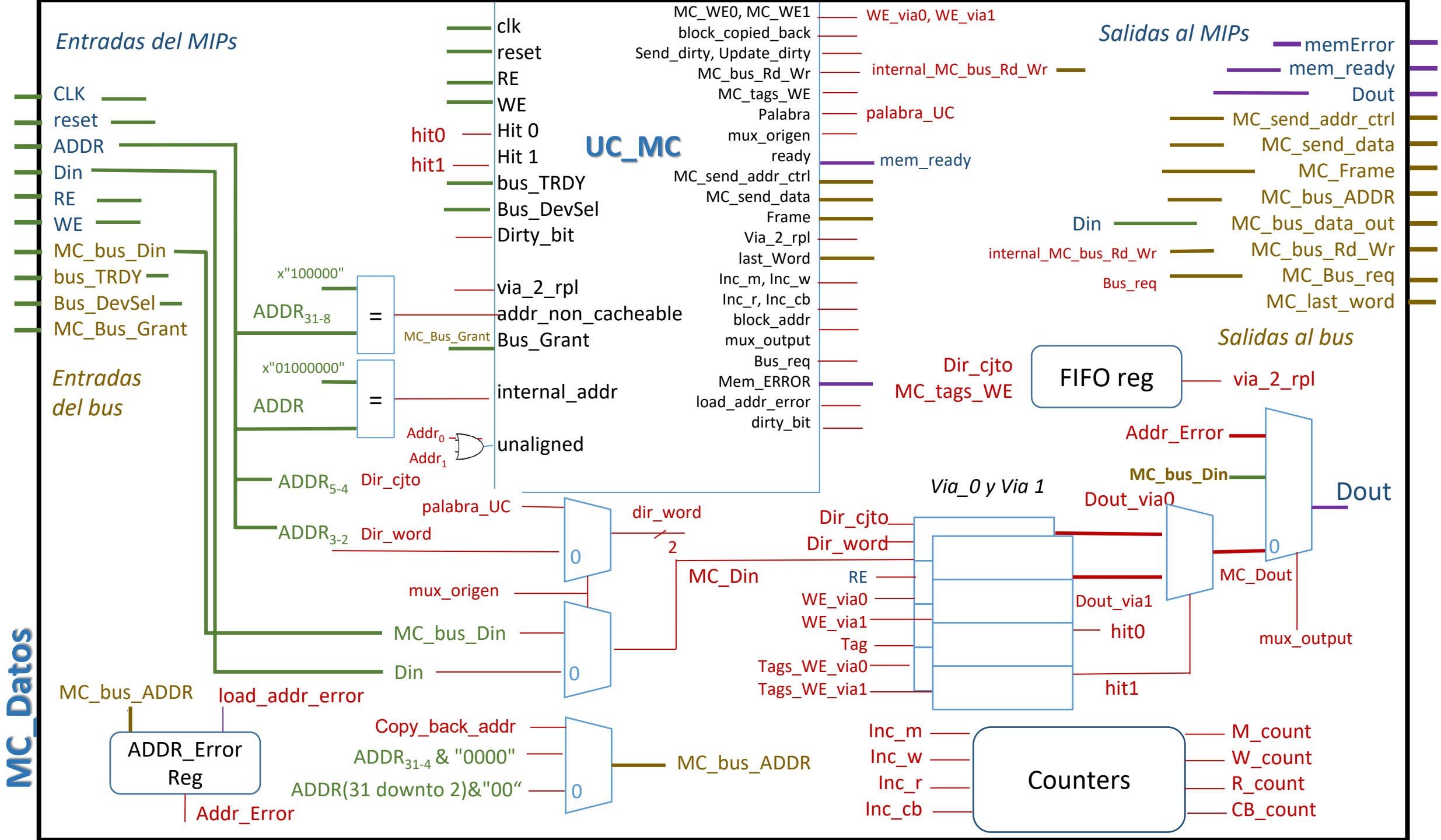

MI
ROM
MIPS
Addr
Dout
Din
RE
WE
MEM_ready
Data_abort
IRQ
IO_input
IO_output
Addr
Din
Dout
RE
WE
MEM_ready
Data_abort
MIPS_IRQ
ACK
IO_reg
Dout Mux
Mem_error
MC_bus_req
IO_M_req
MC
Arbitro
IO
Master
MD
MD
Scratch
MC_bus_grant
IO_M_bus_grant
Bus_CLK
Bus muxes:
Bus_data_addr
Bus_Read
Bus_Write
Bus_last_word
Bus ORs:
Bus_Frame
Bus_Devsel
Bus_TRDY
Bus_Frame
Bus_last_word
Bus_TRDY
IO_M_bus_grant
cont_IO
IO_M_count


Entradas del MIPs
CLK
reset
ADDR
Din
RE
WE
MC_bus_Din
bus_TRDY
Bus_DevSel
MC_Bus_Grant
Entradas del bus
clk
reset
RE
WE
hit0
Hit 0
hit1
Hit 1
bus_TRDY
Bus_DevSel
Dirty_bit
UC_MC
via_2_rpl
addr_non_cacheable
Bus_Grant
internal_addr
unaligned
MC_WE0, MC_WE1
block_copied_back
Send_dirty, Update_dirty
MC_bus_Rd_Wr
MC_tags_WE
Palabra
mux_origen
ready
MC_send_addr_ctrl
MC_send_data
Frame
Via_2_rpl
last_Word
Inc_m, Inc_w
Inc_r, Inc_cb
block_addr
mux_output
Bus_req
Mem_ERROR
load_addr_error
dirty_bit
WE_via0, WE_via1
internal_MC_bus_Rd_Wr
palabra_UC
mem_ready
Salidas al MIPs
memError
mem_ready
Dout
MC_send_addr_ctrl
MC_send_data
MC_Frame
MC_bus_ADDR
MC_bus_data_out
MC_bus_Rd_Wr
MC_Bus_req
MC_last_word
Din
internal_MC_bus_Rd_Wr
Bus_req
Salidas al bus
Dir_cjto
MC_tags_WE
FIFO reg
via_2_rpl
x"100000"
ADDR31-8
=
MC_Bus_Grant
x"01000000"
ADDR
=
Addr0
Addr1
ADDR5-4
Dir_cjto
ADDR3-2
Dir_word
palabra_UC
dir_word
2
0
mux_origen
MC_bus_Din
Din
0
MC_Din
Via_0 y Via 1
Dir_cjto
Dir_word
RE
WE_via0
WE_via1
Tag
Tags_WE_via0
Tags_WE_via1
Dout_via1
hit0
hit1
Addr_Error
MC_bus_Din
Dout_via0
Dout
0
MC_Dout
mux_output
MC_Datos
MC_bus_ADDR
load_addr_error
ADDR_Error Reg
Addr_Error
Copy_back_addr
ADDR31-4 & "0000"
ADDR(31 downto 2)&"00“
0
MC_bus_ADDR
Inc_m
Inc_w
Inc_r
Inc_cb
Counters
M_count
W_count
R_count
CB_count