
GC49C501G1-SJ20I

4-bit Turbo Microcontroller

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1 GC49C501G1-SJ20I Overview

1.1 General Description

GC49C501G1-SJ20I is a 4-bit reduced 8051 Microcontroller.

GC49C501G1-SJ20I has 14 programmable I/O ports, Watchdog timer, POR (Power-On Reset), built-in I.R. LED Driver, and LVD (Low Voltage Detector) as peripherals. In addition, it contains an internal ring oscillator, which can generate the 8 MHz system clock signal instead of a crystal oscillator.

GC49C501G1-SJ20I operates over the extended -40°C to +85°C temperature range, and is available in the 20-pin SOP package.

1.2 Features

- ◆ CPU
 - ✓ 4-bit reduced 8051 architecture
 - ✓ Continuous program addressing, not paged.
 - ✓ 51 instructions including push, pop and logic inst.
 - ✓ Instruction cycle : $F_{SYS}/6$
 - ✓ Multi-level subroutine nesting with RAM based stack.
- ◆ On-chip Memories
 - ✓ FLASH : 1024 bytes (including 128 EEPROM)
 - ✓ RAM : 64 nibbles (including stack)
- ◆ ISP (In System Programming) of FLASH
- ◆ IAP (In Application Programming) of FLASH
- ◆ I/O Ports
 - ✓ P0 : 4-bit parallel I/O (Open drain output)
 - ✓ P1 : Parallel I/O (Open drain output) 2-bit
 - ✓ P2, P3 : 4-bit parallel/bit-selectable I/O (Open drain output)
- ◆ REM output (Remote control transmitter)
 - ✓ Built-in Transistor for I.R. LED Drive

- ✓ $I_{OL} = 300 \text{ mA (Max.)}$ at $V_{DD} = 3\text{V}$ and $V_O = 0.4\text{V}$
- ◆ Carrier Pulse Generation : 7 types
- ◆ Built-in Oscillator
 - ✓ Crystal/Ceramic resonator
 - ✓ Internal oscillator : 8MHz
- ◆ Built-in Reset
 - ✓ Power-on Reset, Power-fail Reset
 - ✓ WDT (Watch-Dog Timer) Reset
 - ✓ Clock switching reset
- ◆ Power Management
 - ✓ Power-down (stop) mode
 - ✓ Release stop by input changes
 - ✓ Sleep mode
- ◆ Power Consumption
 - ✓ Stop mode : $< 0.1\mu\text{A (Typ.)}$ at 2.0V
 $1 \mu\text{A (Max.)}$ at 5.0V
 - ✓ Normal mode : $400 \mu\text{A (Typ.)}$ at 2.0V, $F_{SYS} = 4 \text{ MHz}$
- ◆ Operating frequency vs. voltage
 - ✓ Max. $F_{OSC} = 10 \text{ MHz}$ ($2.7 \text{ V} \leq V_{DD} \leq 5.5\text{V}$)
 - ✓ Max. $F_{OSC} = 5 \text{ MHz}$ ($1.8 \text{ V} \leq V_{DD} < 2.7\text{V}$)
- ◆ Operating temperature : $-40 \text{ }^{\circ}\text{C} \sim 85 \text{ }^{\circ}\text{C}$
- ◆ ESD protection
 - ✓ HBM : 2,000V (JESD22-A114E)
 - ✓ MM : 200V (JESD22-A115-A)
 - ✓ CDM : 800V (JESD22-C101-C)
- ◆ Latch-up protection up to $\pm 200\text{mA}$
- ◆ Package
 - ✓ 20-pin SOIC (JEDEC)

1.3 Applications

- ◆ Remote Controller

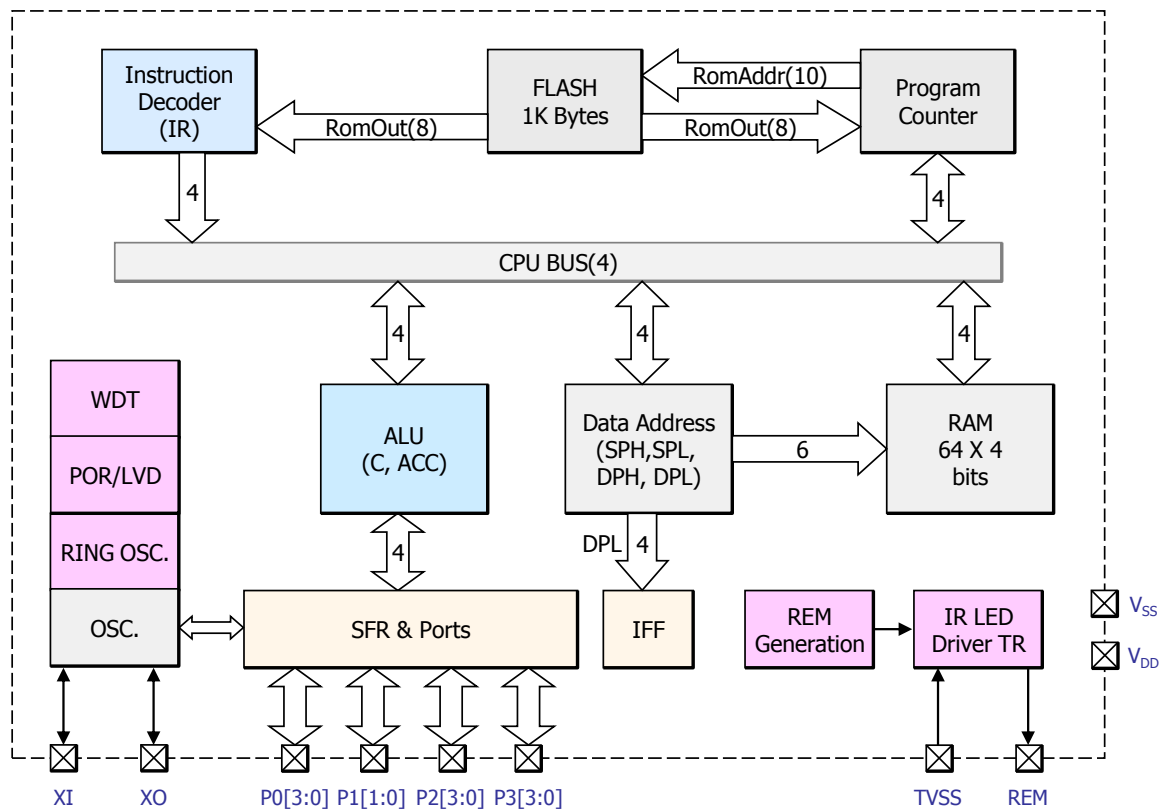
1.4 Product Family Guide

Product	Mask-ROM [Byte]	Flash (EEPROM) [Byte]	RAM [Nibble]	Package	I/O Pins	Other Peripherals
GC49C501G1-SO24I	-	1k (128)	64	24-SOIC	18	WDT IAP ISP LVD POR Ring Oscillator I.R. LED Driver
GC49C501G1-SJ20I	-	1k (128)	64	20-SOIC (JEDEC)	14	
GC41C501G1-SO24I	1k	-	64	24-SOIC	18	
GC41C501G1-SJ20I	1k	-	64	20-SOIC (JEDEC)	14	

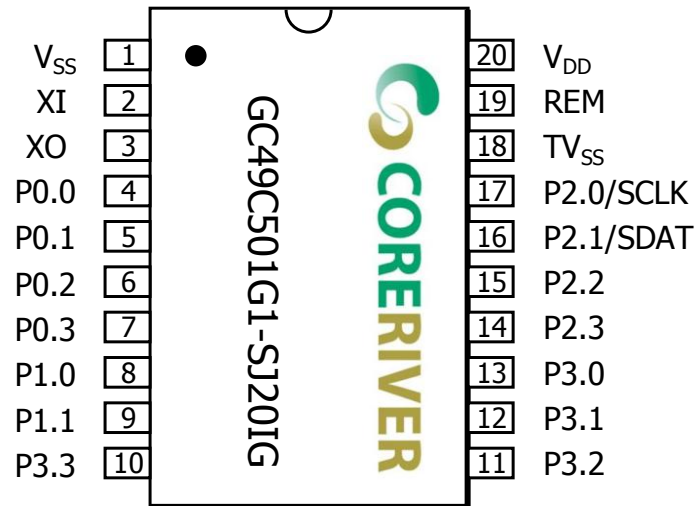
2 Block Diagram

Figure shows the block diagram of **GC49C501G1-SJ20I**. Programs reside in the internal program memory (Embedded Flash Memory). Data are read from or written to data memory (SRAM) or special function registers (SFRs).

The internal registers of **GC49C501G1-SJ20I** are configured as part of the on-chip RAM: therefore each register has an address.



3 Pin Configuration



24-pin SOIC Package Diagram

4 Pin Description

Pin No.	Name	Type	Description	Share Pins
1	V _{SS}	GND	Ground	
2	XI	Input	Input to the inverting oscillator amplifier.	
3	XO	Output	Output from the inverting oscillator amplifier.	
4	P0.0	I/O	General I/O	
5	P0.1	I/O	General I/O	
6	P0.2	I/O	General I/O	
7	P0.3	I/O	General I/O	
8	P1.0	I/O	General I/O	
9	P1.1	I/O	General I/O	
10	P3.3	I/O	General I/O	
11	P3.2	I/O	General I/O	
12	P3.1	I/O	General I/O	
13	P3.0	I/O	General I/O	
14	P2.3	I/O	General I/O	
15	P2.2	I/O	General I/O	
16	P2.1	I/O	General I/O	SDAT
17	P2.0	I/O	General I/O	SCLK
18	TV _{SS}	GND	Ground for IR LED drive Transistor	
19	REM	Output	Output for IR LED drive Transistor. The transistor is n-channel device.	
20	V _{DD}	PWR	Power Supply	

5 Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}	DC supply voltage	-0.5 to 6.5V	V
V_{IN}	DC input voltage	-0.5 to $V_{DD} + 0.5$	V
V_{OUT}	DC output Voltage	-0.5 to $V_{DD} + 0.5$	V
I_{OH}	DC output high current	One I/O pin active: -25	mA
		All I/O pins active: -100	mA
I_{OL}	DC output low current	One I/O pin active: 30	mA
		All I/O pins active: 150	mA
T_{STG}	Storage temperature	-55 to 125	°C

6 Recommended Operating Conditions

Symbol	Parameter	Rating	Unit
V_{DD}	DC supply voltage	1.8 to 5.5	V
T_A	Industrial temperature range	-40 to 85	°C

7 DC Characteristics

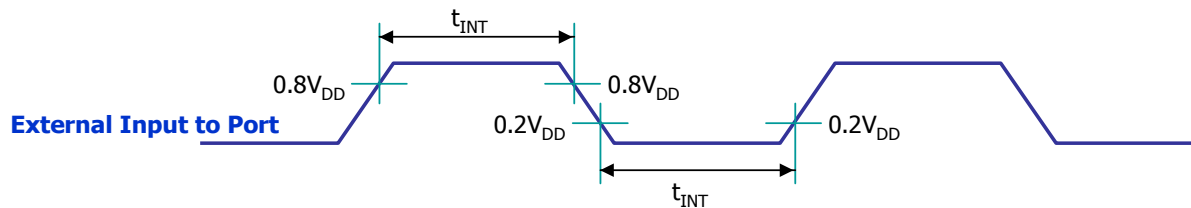
($T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$, $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$ unless otherwise specified)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min.	Typ.	Max.	
Input low voltage	V_{IL1}	P0, P1, P2, P3	$V_{DD} = 1.8\text{V} \sim 5.5\text{V}$	-0.5	-	$0.2V_{DD} - 0.1$	V
Input high voltage	V_{IH1}	P0, P1, P2, P3	$V_{DD} = 1.8\text{V} \sim 5.5\text{V}$	$0.2V_{DD} + 1.0$	-	$V_{DD} + 0.5$	V
Input high leakage current	I_{IH}	All pins except XI, XO	$V_{IN} = V_{DD}$	-1	-	+1	μA
Output low voltage	V_{OL}	P0, P1, P2, P3	$I_{OL} = 20\text{mA} @ V_{DD} = 5\text{V}$ ($I_{OL} = 3\text{mA} @ V_{DD} = 2.2\text{V}$)	-	-	$0.3V_{DD}$	V
Output low voltage	V_{OL2}	REM	$I_{OL} = 280\text{mA} @ V_{DD} = 3\text{V}$	-	-	0.4	V
Output high voltage	V_{OH}	P2 (push-pull output)	$I_{OH} = -15\text{mA} @ V_{DD} = 5\text{V}$	$0.7V_{DD}$	-	-	V
Output high voltage	V_{OHP}	Pull-up current	$I_{OHP} = -40\mu\text{A} @ V_{DD} = 5\text{V}$ ($I_{OHP} = -15\mu\text{A} @ V_{DD} = 2.2\text{V}$)	$0.7V_{DD}$	-	-	V
Pin capacitance	C_{IO}	All	$V_{DD} = 5\text{V}$	-	10	-	pF

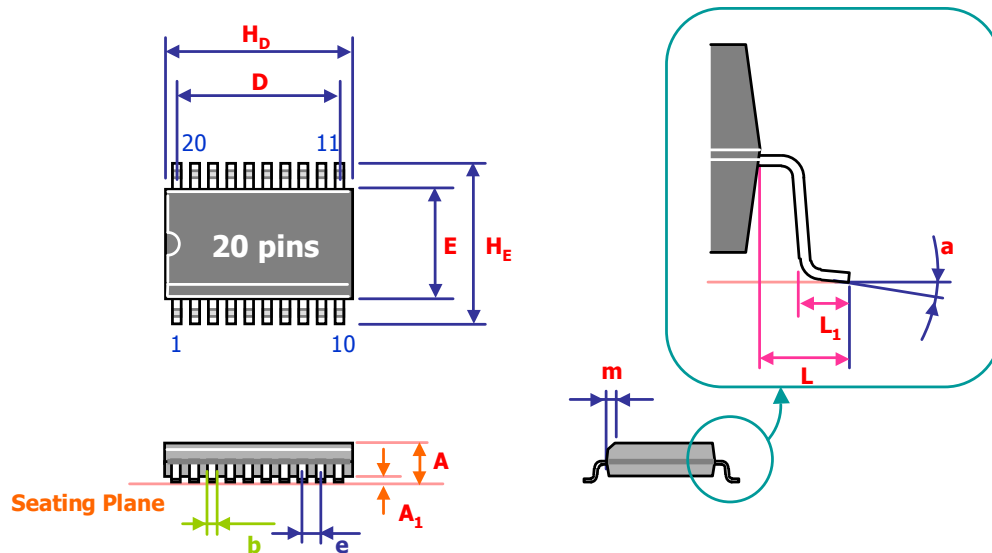
8 AC Characteristics

($T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min.	Typ.	Max.	
Operating Frequency (Internal Clock)	F_{OSC}		$2.7\text{V} \leq V_{\text{DD}} \leq 5.5\text{V}$	-	-	10	MHz
			$1.8\text{V} \leq V_{\text{DD}} \leq 2.7\text{V}$	-	-	5	
Operating Frequency (External Clock)	F_{OSC}	XI, XO	$2.7\text{V} \leq V_{\text{DD}} \leq 5.5\text{V}$	-	-	10	MHz
			$1.8\text{V} \leq V_{\text{DD}} \leq 2.7\text{V}$	-	-	5	
System Frequency	F_{SYS}		$1.8\text{V} \leq V_{\text{DD}} \leq 5.5\text{V}$	1/64	-	1	F_{OSC}
External Input Width	t_{INT}	P0, P1, P2, P3	$1.8\text{V} \leq V_{\text{DD}} \leq 5.5\text{V}$	12	-	-	F_{SYS}



9 20-pin SOIC Package Dimension



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.106	-	-	2.7
A ₁	0.004	-	-	0.1	-	-
b	0.013	0.016	0.020	0.324	0.4	0.51
E	0.264	0.295	0.324	6.71	7.5	8.23
H _D	0.495	0.504	0.512	12.57	12.8	13
H _E	0.394	0.406	0.419	10.0	10.3	10.643
L	0.016	-	0.052	0.406	-	1.32
a	0°	-	8°	0°	-	8°
e	0.050 BSC			1.27 BSC		

Notes:

1. Dimension D & E include mold mismatch and are determined at the mold parting line.
2. General appearance spec. should be based on final visual inspection spec.