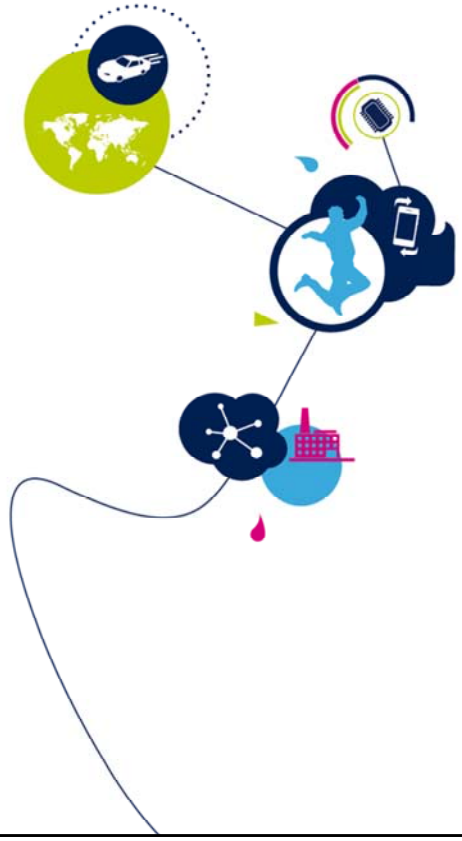
STM32MP1- PWR

Power Controller
Revision 2.0



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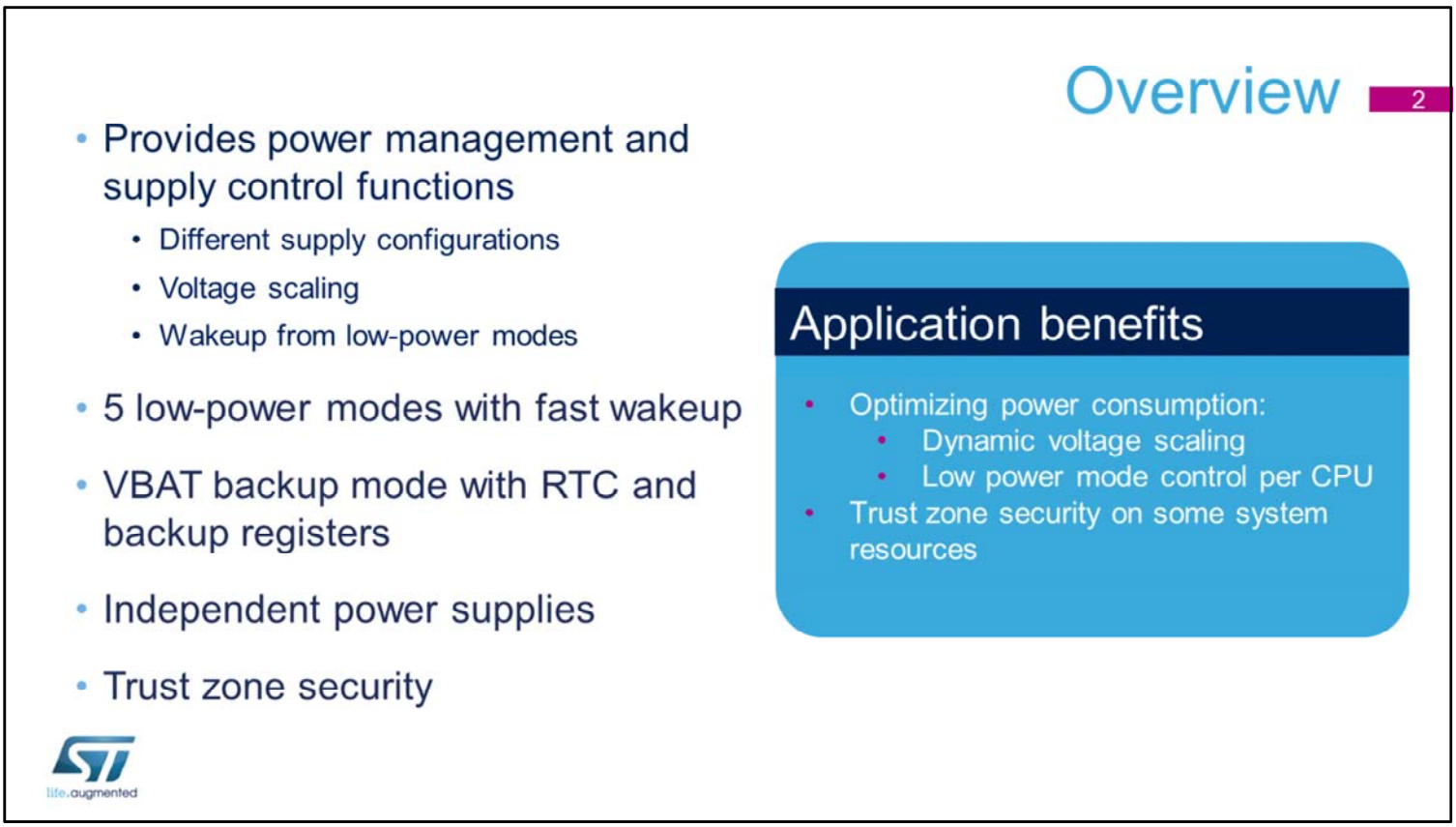
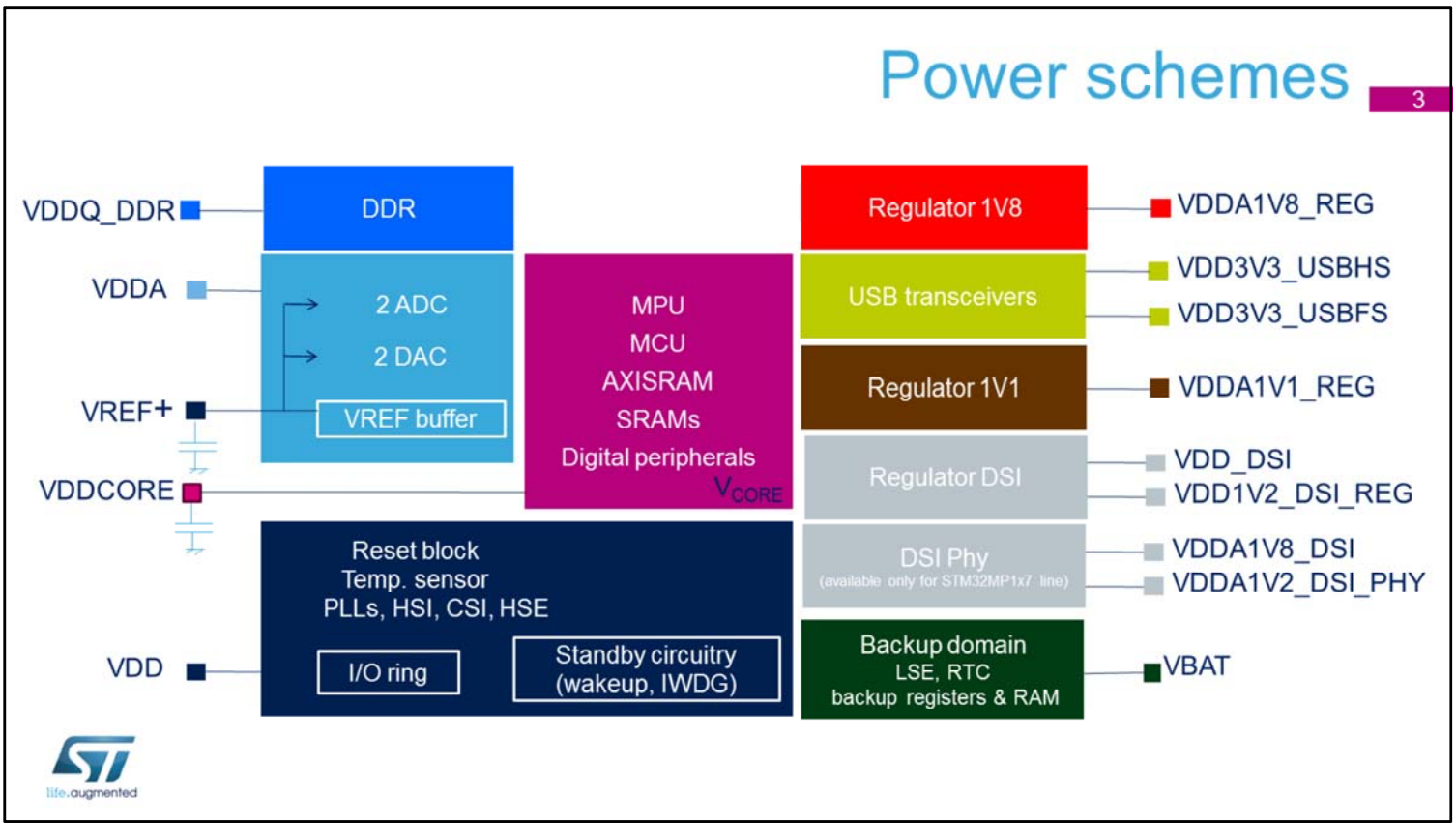
Hello, and welcome to this presentation of the STM32MP1 power controller. The STM32MP1's power management functions and all power modes will also be covered in this presentation.



The STM32MP1 microcontroller has several key features related to power management including several low-power modes, where it is still possible to wake up the CPUs individually with an event on an I/O as well as a large number of peripherals that can wake up from the various low-power modes.
Several power supplies are independent, allowing reduction of the device power consumption while some peripherals are supplied at other voltages.
Thanks to the large number of power modes and independent power domains, STM32MP1 devices offer high flexibility to minimize the power consumption and adjust it depending on active peripherals, required performance and needed wake-up sources.
Some system resources can be secured.

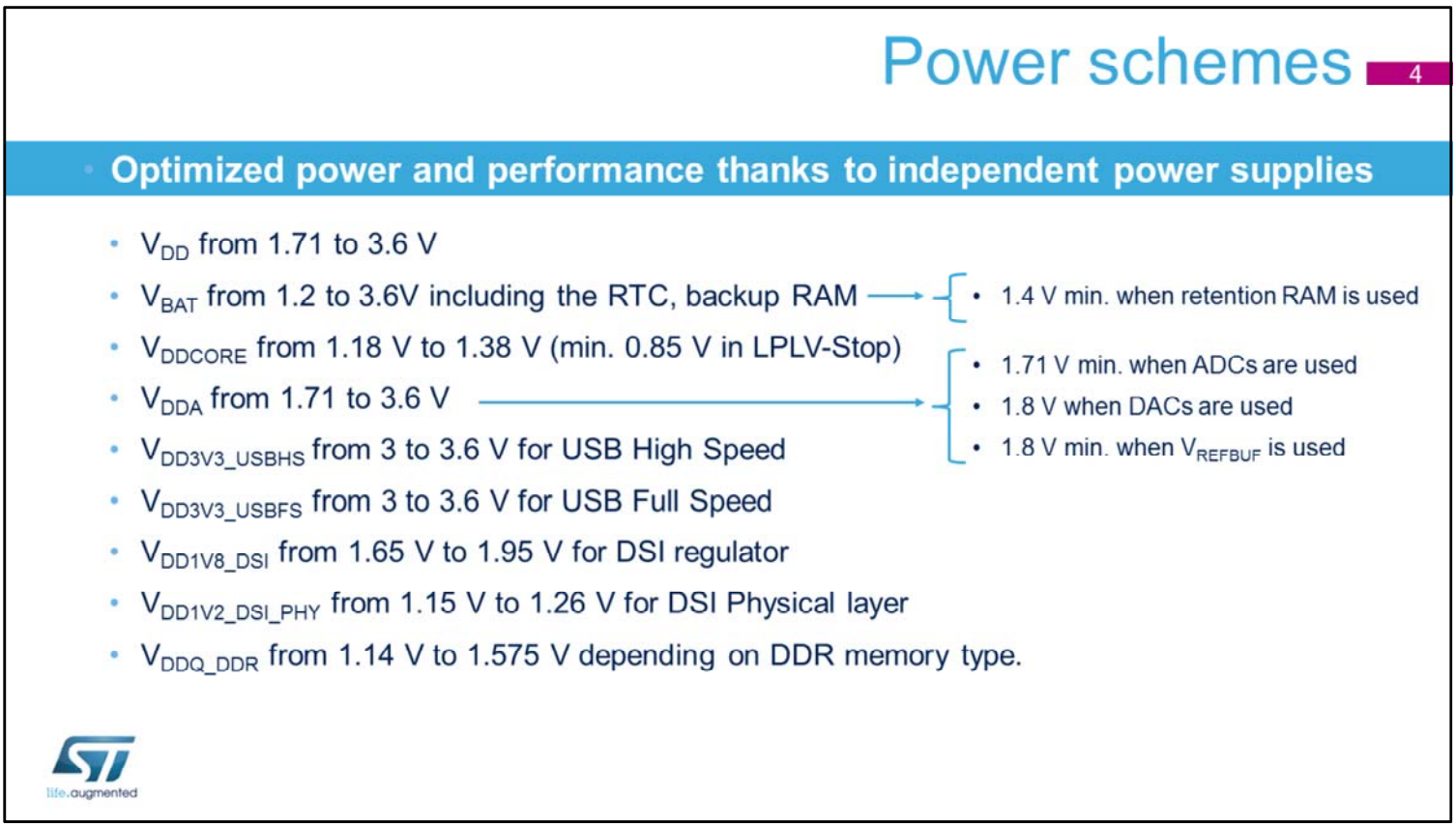


STM32MP1 devices have several independent power supplies, which can be set at different voltages or tied together. The main power supply is VDD, supplying all I/Os. VDD also supplies the reset block, temperature sensor and all internal clock sources. In addition, it supplies the Standby circuitry which includes the wakeup logic and independent watchdog. The VDDCORE directly provide the VCORE supply. VCORE supplies (MPU Cortex-A7, MCU Cortex-M4) with most of the digital peripherals and the AXI RAMs and SRAMs.. The DDR interface has its dedicated VDDQ_DDR supply.

The STM32MP1 features several independent supplies for peripherals: VDDA for the analog peripherals, VDD3V3_USBHS and VDD3V3_USBFS for the USB transceivers, VDDA1V8_DSI and VDD1V2_DSI_PHY for the DSI interface. The VREF+ pin provides the reference voltage to the analog-to-digital and to digital-to-analog converters

and can be used as an external buffer reference for the application.
A backup battery can be connected to the VBAT pin to supply the backup domain.

Furthermore the STM32MP1 microcontroller incorporates various regulators which provide the various voltage levels for the USB and DSI interfaces.



The main power supply VDD ensures full featured operation in all power modes from 1.71 up to 3.6 V, allowing to be supplied by an external 1.8 V regulator. Other independent supplies are provided for peripherals operating at a different voltage.

A backup domain is supplied by VBAT, which must be greater than 1.2 V. The backup domain contains the RTC, the 32.768-kHz LSE external oscillator, the backup registers, and the backup RAM. When the retention RAM is used, VBAT must be at the least greater than 1.4 V.

The digital core is directly supplied from VDDCORE at typical 1.2V in Run mode up to 650MHz, typical 1.34V in Run mode up to 800MHz and typical 0.9 V in LPLV-Stop mode.

The analog power supply VDDA can be connected to any voltage other than VDD. When an analog-to-digital converter is used, the VDDA voltage must be greater than 1.71 V. When a digital-to-analog converter or Vrefbuff is used, VDDA

must be greater than 1.8 V.
The USB interfaces have their individual supplies VDD3V3_USBHS and VDD3V3_USBFS.
The DSI interface requires 2 supplies, VDD1V8_DIS and VDD1V2_DSI_PHY.
The DDR interface is supplied from the individual VDDQ_DDR.

Power schemes

Independent voltage reference supplies for analog performance

- V_{REF+} : reference voltage for ADCs and DACs
  - It can be provided either by an external reference voltage or by the internal voltage reference buffer.
  - VREF+ pin, and thus the internal voltage reference. It is not available on all package, this pin is then double-bonded with V_{DDA} which can be connected to an external reference. With this configuration, the internal voltage reference buffer is not available.

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The ADC and DAC voltage references can be provided either by an external supply voltage or by the internal reference buffer. This allows the converters performance to be improved by providing an isolated and independent reference voltage.

Backup domain regulators

6

- Used to regulate the V_{SW} supply to the Backup RAM and Retention RAM supply level.
- The Backup RAM and Retention RAM have each their own regulator.
  - When V_{CORE} is present
    - Backup domain regulators are off. (Allows to reduce backup battery consumption)
    - Backup RAM and Retention RAM are supplied from V_{CORE}.
  - When V_{CORE} is absent (Standby or V_{BAT} mode) and backup regulators are enabled
    - Backup domain regulator are on.
    - Backup RAM and Retention RAM are supplied from V_{BKUP}.
  - When V_{CORE} is absent (Standby or V_{BAT} mode) and backup regulator are disabled
    - Backup domain regulators are off.
    - Backup RAM and Retention RAM are powered down. (data lost)

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The Backup regulators are used to keep the context of the Backup RAM and Retention RAM in Standby and VBAT modes. Each RAM has its dedicated regulator. The backup RAM regulator is enabled by the BREN bit in the PWR register CR2. The retention RAM regulator is enabled by the RREN bit in PWR register CR2.
When a regulator is enabled, its supply level is checked to be ready, before the system enters Standby mode.

Other regulators

- USB regulators
  - Used to supply the USB interfaces. Can't supply external logic.
  - See USB training
- DSI regulator
  - Used to supply the DSI interface. Can't supply external logic.
  - See DSI training

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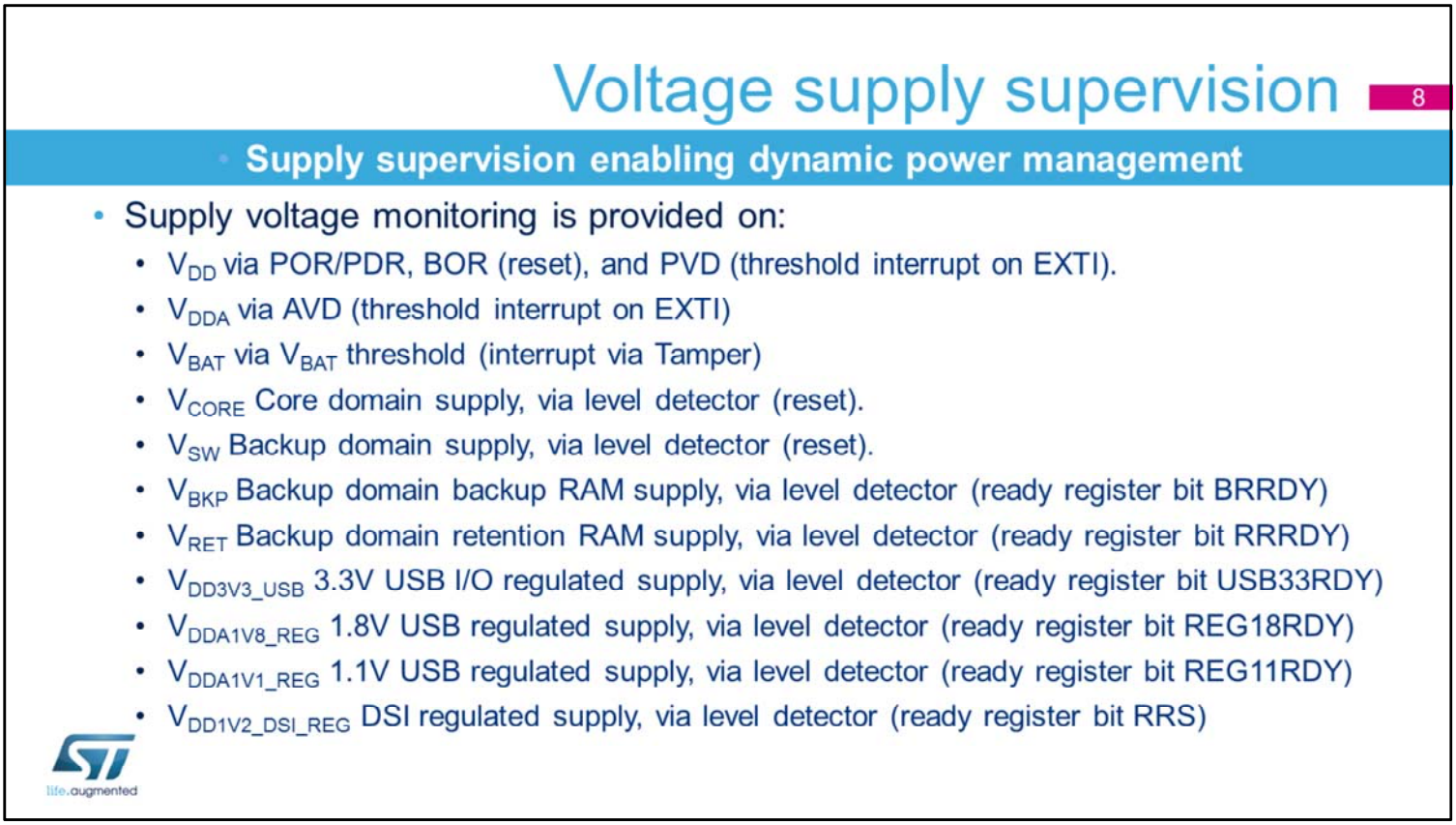
Independent USB regulators generate the V_{DDA1V8_REG} and V_{DDA1V1_REG} supplies from VDD.
The DSI regulator generates the $V_{DD1V2\_DSI\_REG}$ supply from VDD_DSI.



The power supply supervisor ensures dynamic power supply management.
STM32MP1 devices embed power management on main VDD, analog VDDA, VBAT supply input, VCORE domain, Backup VSW domain, Backup regulator VBKP, retention regulator VRET supply, USB interface VDD3V3_USB supply, and regulators supplies VDDA1V8_REG, VDDA1V1_REG and VDD1V2_DSI_REG supplies.
The main VDD supervisor handles reset management and voltage detection via the programmable voltage detector (PVD) when VDD crosses the selected threshold. The PVD can be enabled in all modes except Standby modes. 7 thresholds can be selected by software. In addition, comparisons can be done with an external pin.
The analog VDDA supervisor handles voltage detection via the analog voltage detector (AVD) when VDDA crosses the selected threshold. The AVD can be enabled in all modes except Standby mode. 4 thresholds can be selected by

software.
The VBAT supply voltage is monitored to detect when VBAT crosses the minimum and maximum thresholds. The VBAT voltage detection function can be enabled in all modes.
The main VCORE supervisor handles reset management detection.
The Backup domain VSW supervisor handles reset management when the supply drops below the operating level.
The Backup RAM regulator VBKP supply supervisor verifies that the regulator is ready to supply the backup RAM, before entering Standby mode.
The Retention RAM regulator VRET supply supervisor verifies that the regulator is ready to supply the retention RAM, before entering Standby mode.
The USB interface VDD33USB supply supervisor verifies that the USB interface supply is present. The USB supervision can be enabled in all modes except Standby modes.
The USB and DSI Regulators VDDA1V8_REG, VDD1V1_REG, and VDD1V2_DSI_REG supplies supervisors verify that the regulator is ready to supply the interface.

POR/PDR & BOR

9

Safe and ultra-low-power reset management

- POR (Power On Reset)
  - Supervises V_{DD}.
  - Fixed level to disable reset when V_{DD} level rises above threshold.
- PDR
  - Supervises V_{DD}.
  - Fixed level to generate reset when V_{DD} level drops below threshold.
  - Can be enabled/disabled with PDR_ON input pin.
- BOR
  - Supervises V_{DD}.
  - Provides 4 selectable levels from V_{BOR0} = 1.63 V to V_{BOR3} = 2.6 V through option bits **BOR_LEV[2:0]**, generates reset when V_{DD} level drops below threshold.
  - Can be disabled with system option bits.

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The V_{DD} power supply supervisor guarantees a safe and ultra-low power reset management.
STM32MP1 devices embed an ultra-low-power brown-out reset (BOR) which is always enabled in all power modes. The BOR ensures reset generation as soon as the MCU drops below the selected threshold, regardless of the V_{DD} slope. Four thresholds from typical 1.63 V to 2.6 V are selected by option byte programmed in Flash memory.

Temperature supervision

- Temperature threshold
  - Supervises junction temperature.
  - Can be enabled/disabled with register bit MONEN.
  - Provides TEMPH and TEMPL register flags, connected to Tamper wakeup interrupt.

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The temperature supervisor detects when the junction temperature crosses the minimum and maximum thresholds. The temperature detection function can be enabled in all modes.

VBAT supervision

- Backup battery threshold
  - Supervises backup battery supply level.
  - Can be enabled/disabled with register bit MONEN.
  - Provides VBATH and VBATL register flags, connected to Tamper wakeup interrupt.

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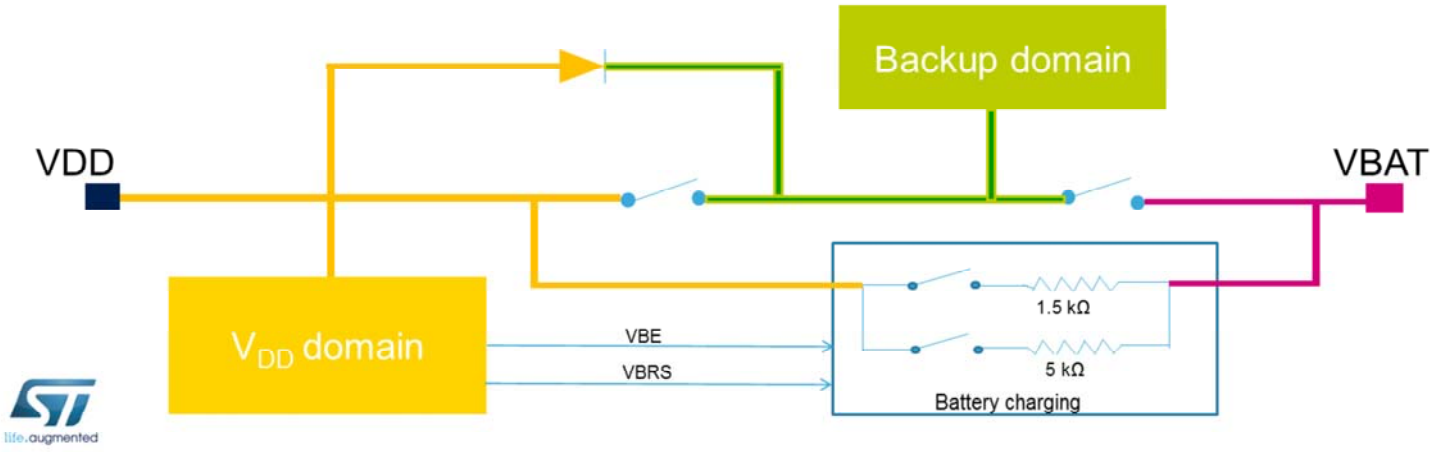
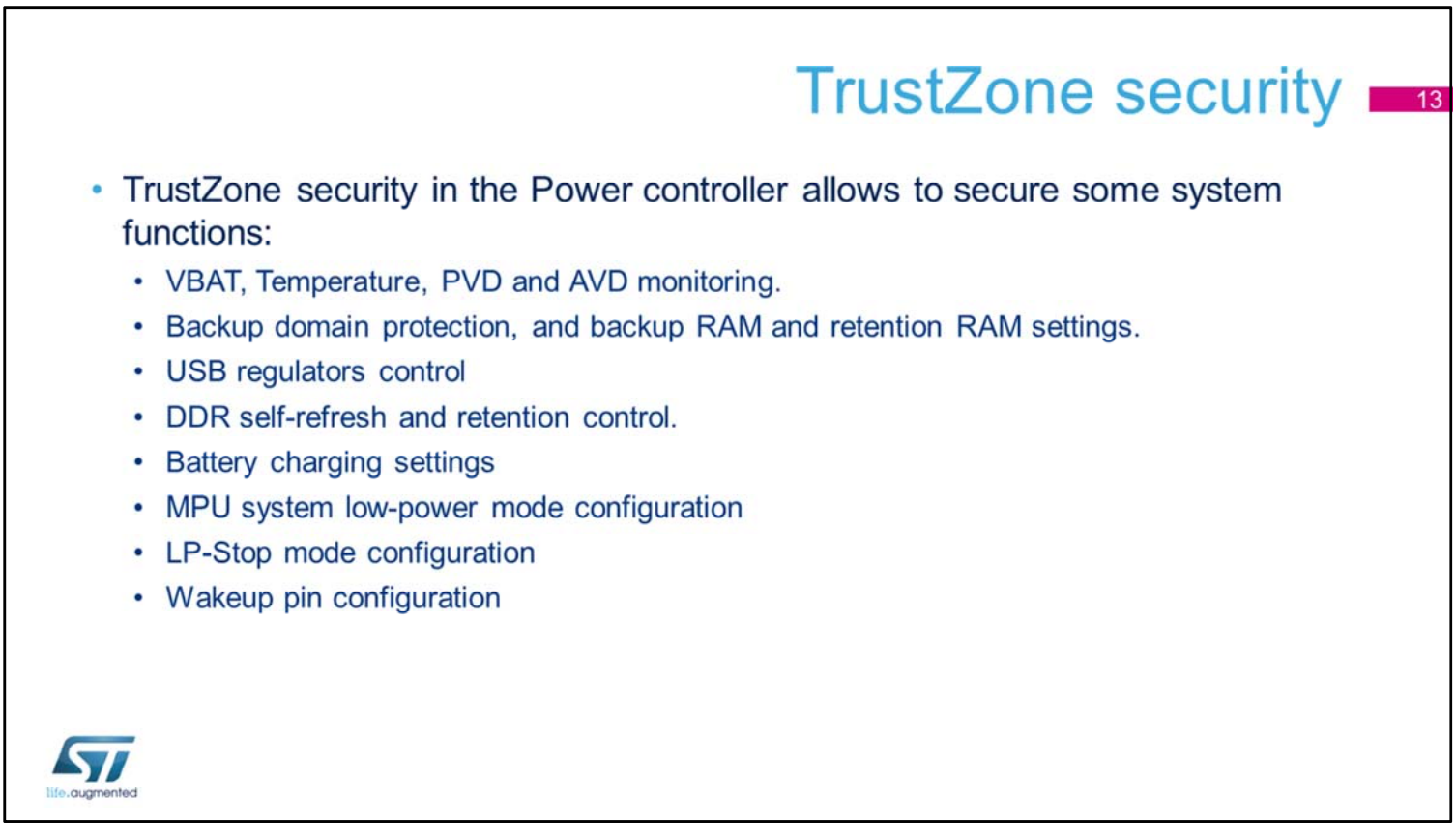
The backup battery supervisor detects when the backup battery supply level crosses the minimum and maximum thresholds. The backup battery detection function can be enabled in all modes.

V_{BAT} battery charging

- A backup battery connected to V_{BAT} can be charged from V_{DD}.
  - Enabled by application Software
  - Selection between 2 charging resistor values (5 kOhm or 1.5 kOhm)
  - Automatically disabled when entering V_{BAT} mode.



The battery charging feature can charge a super-cap connected to the VBAT pin through an internal resistor when the V_{DD} supply is present. The charging is enabled by software and is done either through a 5k Ohm or 1.5 kOhm resistor depending on software. Battery charging is automatically disabled in VBAT mode.



The following features can be made TrustZone secure, they are either all secure or all non-secure.

- Backup battery voltage monitoring, temperature monitoring, Programmable voltage detector, analog peripheral voltage detector.
- Backup domain protection, and backup and retention RAM settings.
- USB regulators control
- DDR self-refresh and retention settings
- Backup battery charging settings
- MPU system low- power mode configuration
- LP-Stop and LPLV-Stop mode configuration
- Individual per wakeup pin configuration

CPU operating modes

Mode	Description
CRun	CPU Active ➔ CPU, CPU-sub system bus matrix(s), CPU enabled peripheral clock(s) active.
CSleep	CPU Sleep ➔ CPU clock stopped, CPU-sub system bus matrix(s), CPU sleep enabled peripheral clock(s) active.
CStop	CPU Deepsleep ➔ CPU, CPU-sub system bus matrix(s), CPU peripheral clock(s) stopped.
CStandby	MPU Deepsleep ➔ MPU, MPU-sub system bus matrix(s), MPU peripheral clock(s) stopped.

- CPU operating modes are directly controlled from the CPU
  - Entering low-power modes
    - CSleep is entered by executing WFI/WFE or on return from ISR. (DEEPSLEEP = 0)
    - CStop/CStandby is entered by executing WFI/WFE or on return from ISR. (DEEPSLEEP = 1)
  - Exiting low-power modes
    - CSleep with a NVIC interrupt, or RXEV event
    - CStop
      - When the system is in Run or Stop mode with a NVIC interrupt, or RXEV event.
      - When the system is in Standby mode with reset.
    - CStandby with a MPU reset.

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The CPU entering low-power mode is controlled by the WFI and WFE, and the DEEPSLEEP bit allows the mode selection in between CSleep and CStop/CStandby modes. When the CPU enters CStop/CSTandby mode, the system operating mode depends on the other CPU.
CSleep mode is exited with a NVIC interrupt or RX event. The way CStop mode is exited depends on the system mode. When the system is in Run or Stop mode, Cstop mode is exited with a NVIC interrupt or RX event. When the system is in Standby mode, CStop is exited with a reset.
The MPU exits from CStandby mode with a reset.
A CPU event input (rxev) wakes up the CPU after a WFE.

System operating modes

Mode	Description
Run	System clock is active and forwarded to the system.
Stop	System clock is stopped.
Standby	System is powered down. (Backup domain may be kept active)

- System operating modes controlled from the CPUs and wakeup sources.
  - Run when a CPU is in CRun or CSleep mode or a wakeup source is active.
  - Stop when the CPUs are in CStop mode and all wakeup sources are cleared, and at least one PDDS bit selects Stop mode.
  - Standby when the CPUs are in CStop mode and all wakeup sources are cleared, and all PDDS bits select Standby mode.

The STM32MP1 system operating mode is controlled from both CPUs. The system only enters Stop or Standby mode when both CPUs are in CStop mode and there is no active wakeup source.
The system only enters Standby mode when all the PDDS bits selects Standby mode.

Sleep mode

All peripherals available and fastest wakeup time

- CPU is stopped, each peripheral clock can be gated ON or OFF
- Entered by executing **WFI** (Wait For Interrupt) or **WFE** (Wait For Event)
- Two mechanisms to enter this mode:
  - **Sleep Now**: MCU enters Sleep mode as soon as WFI/WFE instructions are executed
  - **Sleep on Exit**: MCU enters Sleep mode as soon as it exits the lowest priority ISR
    - The stack is not popped before entering Sleep mode, it will not be pushed when the next interrupt occurs, saving running time.
  - **Controlled by Cortex-M System Control Register [SLEEPONEXIT]**

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Sleep and Low-power sleep modes enable all peripherals to be used and features the fastest wakeup time.
In these modes, the CPU is stopped and each peripheral clock can be configured by software to be gated ON or OFF during the Sleep and Low-power sleep modes.
These modes are entered by executing the assembler instruction Wait for Interrupt or Wait for Event. When executed in Low-power run mode, the device enters Low-power sleep mode.
Depending on the SLEEPONEXIT bit configuration in the CortexM4 System Control Register, the MCU enters Sleep mode as soon as the instruction is executed, or as soon as it exits the lowest priority Interrupt Sub Routine. This last configuration saves time and consumption by removing the need to pop and push the stack.

Stop modes

Lowest power modes with full retention

- All memory and all peripheral register data is retained
- All high-speed clocks are stopped
- LSE (32.768 kHz external oscillator) and LSI (32 kHz internal oscillator) can be enabled
- Several peripherals can be active and wake up from Stop modes
- System clock at wakeup to the MPU is restored and the MCU receives the HSI.
- LP-Stop and LPLV-Stop power consumption is lower compared to Stop mode. But those modes support a reduced number of peripherals with wakeup capability.

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STM32MP1 devices features three Stop modes: Stop, LP-Stop and LPLV-Stop, which are the lowest power modes with full retention and fast wakeup time to Run mode.
The contents of SRAMs and all peripherals registers are preserved in all Stop modes.
All high speed clocks are stopped.
The 32.768 kHz external oscillator and 32 kHz internal oscillator can be enabled.
Several peripherals can be active and wake up from Stop modes.
The MPU system clock on wake-up is restored and the MCU will receive the HSI clock.
LP-Stop and LPLV-Stop power consumption is lower than the consumption for Stop mode, but those modes support less active wakeup peripherals.

Stop modes comparison

18

	Stop	LP-Stop	LPLV-Stop
Consumption	25 °C, 3,3 V		
	high	medium	low
Wakeup time	short	medium	long
Regulator	Regulator Main mode	Regulator Low-power mode	
	Normal supply level		Low-voltage level
Peripherals	RTC, GPIO, BOR, PVD, AVD, VBATH/L, TEMPH/L, LSECSS, DTS, IWDG, LPTIM, USB-OTG, CEC, ETH, MDIOS, USART, I2C, SPI, and DBG		RTC, GPIO, BOR, PVD, AVD, VBATH/L, TEMPH/L, LSECSS, DTS, IWDG

When comparing Stop modes:
Stop power consumption is higher than the LP-Stop and LPLV-Stop consumption, but the wakeup time is shorter.
For Stop and LP-Stop modes, the number of active wakeup peripherals is higher.
Stop and LP-Stop modes keeps the V_{CORE} domain at the same supply level as Run mode, allowing a very short wake-up time at the expense of a higher consumption than LPLV-Stop mode.
LP-Stop mode allows the external power supply unit to be placed in low-power mode, reducing overall system power consumption.
LPLV-Stop mode allows the external power supply unit to be placed in low-power mode and supplies a lower Vddcore level, reducing the STM32MP1 and overall system power consumption.
Stop and LP-Stop modes support the same number of active wakeup peripherals, where LPLV-Stop mode supports a

reduced sub-set.

Standby mode

19

Lowest power mode with Backup RAM retention, switch to V_{BAT} and I/O control

- By default: no RAM nor registers retention (voltage regulators in power down). backup registers always retained.
- Possibility to retain 4 Kbytes of Backup RAM
- Possibility to retain 64 Kbytes of Retention RAM
- Ultra Low Power BOR always ON: safe reset regardless of V_{DD} slope.
- 5 wakeup pins: the polarity of each of the 5 wakeup pins is configurable
- MPU clock restored and MCU wakeup clock is the HSI clock.

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The Standby mode is the lowest power mode in which 4 Kbytes of Backup RAM and 64 Kbytes of retention RAM can be retained, the automatic switch from VDD to VBAT is supported.
By default, the voltage regulators are in Power down mode and the SRAMs and the peripherals registers are lost. The backup registers are always retained.
Thanks to software, it is possible to retain the Backup RAM and the Retention RAM.
The ultra-low-power brown-out reset is always ON to ensure a safe reset regardless of the VDD slope.
5 wakeup pins are available to wake up the device from Standby mode. The polarity of each of them is configurable.
The MPU system clock is restored at wakeup, and the MCU system clock selects the HSI clock.

VBAT mode

RTC still running and backup registers preserved in case of V_{DD} loss

- Backup domain contains:
  - RTC clocked by 32.768 kHz LSE oscillator, including **3 tamper pins**
  - **Backup registers**
  - RCC_BDCR register
  - 4 Kbyte Backup memory, when backup regulator is enabled.
  - 64 Kbyte Retention memory, when retention regulator is enabled.
- Automatic internal switch between V_{BAT} and V_{DD} when V_{DD} is powered down and powered on.
- Internal connection to ADC for voltage monitoring ($V_{BAT}/4$)
- V_{BAT} charging

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The backup domain allows us to keep the RTC functional and to preserve the backup registers in case the VDD supply is down, thanks to a backup battery connected to the VBAT pin.
The backup domain contains the RTC clocked by the low-speed external oscillator at 32.768 kHz. 3 tamper pins are functional in VBAT mode, and will erase the backup registers also included in the VBAT domain, in case of intrusion detection.
The backup domain also contains the RTC clock control logic.
In case VDD drops below a certain threshold, the backup domain power supply automatically switches to VBAT. When VDD is back to normal, the backup domain power supply automatically switches back to VDD.
The VBAT voltage is internally connected to an ADC input channel in order to monitor the backup battery level.
When VDD is present, the battery connected to VBAT can

be charged from the VDD supply.

CPU wakes up from CStop mode

- To know from which system low-power mode the CPU wakes up, flags are provided. Each CPU has its own set of flags.
  - STOPF - System has been in Stop mode, after the CPU entered CStop.
    - Wakeup interrupt to the CPU will be pending in EXTI or peripheral.
    - The system may already be in Run mode due to the other CPU.
  - SBF- System has been in Standby mode, after the CPU entered CStop
    - CPU starts from reset, there is no wakeup interrupt pending in the EXTI.
    - The system may actually be in Stop ,mode or already in Run mode due to the other CPU.
- The CPU flags are supposed to be cleared by firmware when the CPU wakes up.

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When a CPU wakes up from its CStop mode, it has to know from which mode the system has woken up. For this, each CPU has dedicated flag bits Standby flag and Stop flag. These bits inform the CPU about the state of the system, and which parts may need to be reinitialized.

MPU wakes up from CStandby mode

- When ever the MPU wakes up from CStandby mode, the MPUSBF flag is set, next to any system STOPF or SBF flag.
- The MPU flags are supposed to be cleared by firmware when the MPU wakes up.

When the MPU wakes up from CStandby mode, it is informed by the MPU Standby Flag. The system modes at wakeup are available in the STOP flag and STANDBY flag.

Wakeup

- The CPU wakeup state depends on the system state

System Mode	MPU mode	MCU mode	SBF	STOPF	MPUSBF	Comment	MPU wakeup	MCU wakeup
Run	CRun / CStop	CRun / CStop	0	0	0	System contents retained	ISR/Event	ISR/Event
	CStandby		0	0	1		Reset	
Stop	CStop	CStop	0	1	0	System contents retained, system clock stopped	ISR/Event	ISR/Event
	CStandby		0	1	1		Reset	
Standby	CStandby		1	0	1	System contents lost	Reset	Reset
VBAT	n.a.	n.a.						

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This table gives an overview of the MPU and MCU wakeup state versus the system operating mode and how they are signaled by the wakeup flag bits. It also shows how the MPU and MCU were awaken, through an interrupt or an event, or a CPU reset.

PWR interrupts

Interrupt event	Description	Availability
WKUP[6:1]	Wakeup from Standby mode. Wakeup from Stop mode via event signal to EXTI	Run, Stop and Standby
PVDO	Wakeup from Stop mode via event signal to EXTI	Run and Stop
AVDO	Wakeup from Stop mode via event signal to EXTI	Run and Stop
VBATH, VBATL	Wakeup from Standby mode & STOP mode via RTC Tamper Interrupt	Run, Stop and Standby
TEMPH, TEMPL	Wakeup from Standby mode & STOP mode via RTC Tamper Interrupt	Run, Stop and Standby

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Here a summary of the PWR control related interrupts.

Debug information

- The DBGMCU_CR register enables debugging in Stop and Standby mode:
  - DBGSTOP: when set, the processor clock and associated bus matrix clocks are kept active in Stop mode.
  - DBGSTANDBY: When set, the digital part is not powered down in Standby mode, and the processor clock and associated bus matrix clocks are kept active.
    When exiting from Standby mode, a reset is generated.
- When DBGSTOP or DBGSTANDBY is enabled, the connection with the debugger is kept during the related Stop or Standby mode.
  After wakeup, debugging is still possible.

The Debug Control Register is used to enable debugging in Stop and Standby modes. When the related bit is set, the CPU clock and bus matrix clock is kept active, and the regulator is kept ON in normal mode to supply the core logic. This maintains the connection with the debugger during the low-power modes, and keeps the debugging alive during and after wakeup. Remember to clear these bits when the device is not under debug, because the consumption is higher in all low-power modes when these bits are set, due to the fact they force the regulator to remain enabled and keep clocks active.

Related peripherals

- Refer to the following list of peripheral trainings for more details about their dependencies with the power modes:
  - Reset and clock control (RCC)
  - Interrupts (NVIC and EXTI)
  - Digital-to-analog converter (DAC)
  - Low-power timer (LPTIM)
  - Independent watchdog (IWDG)
  - Real-time clock (RTC)
  - Inter-integrated circuit (I2C) interface
  - Universal synchronous asynchronous receiver transmitter (USART)
  - Low-power universal asynchronous receiver transmitter (LPUART)
  - USB-HS and USB-FS interfaces
  - DSI interface

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In addition to this training, you can refer to the Reset and Clock Control and Interrupts trainings as well as those for all the peripherals with wakeup from Stop and Standby capability.