

NCE P-Channel Enhancement Mode Power MOSFET

Description

The NCE01P30K uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications. It is ESD protected.

General Features

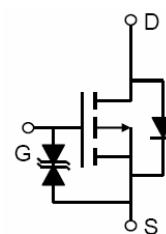
- $V_{DS} = -100V, I_D = -30A$
- $R_{DS(ON)} < 58m\Omega @ V_{GS} = -10V$ (Typ: $44m\Omega$)
- $R_{DS(ON)} < 65m\Omega @ V_{GS} = -4.5V$ (Typ: $48m\Omega$)
- Super high dense cell design
- Advanced trench process technology
- Reliable and rugged
- High density cell design for ultra low On-Resistance

Application

- Portable equipment and battery powered systems

100% UIS TESTED!

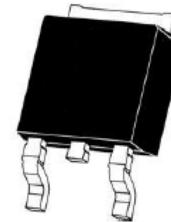
100% ΔV_{ds} TESTED!



Schematic diagram



Marking and pin assignment



TO-252-2L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE01P30K	NCE01P30K	TO-252-2L	-	-	-

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	-30	A
Drain Current-Continuous($T_C=100^\circ C$)	$I_D (100^\circ C)$	-21	A
Pulsed Drain Current	I_{DM}	-150	A
Maximum Power Dissipation	P_D	120	W
Single pulse avalanche energy ^(Note 5)	E_{AS}	420	mJ
Derating factor		0.8	W/ $^\circ C$
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	1.25	$^\circ C/W$
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Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

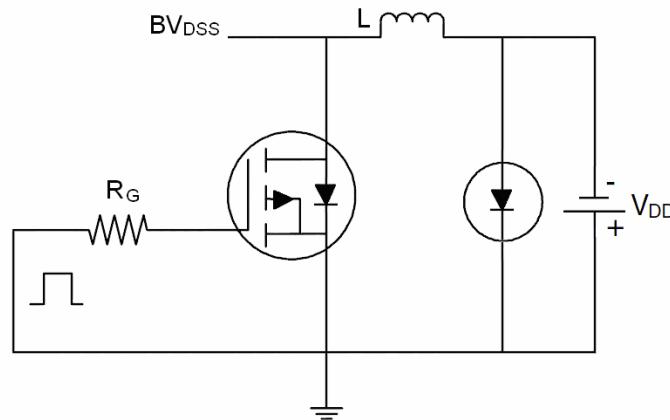
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=-250\mu\text{A}$	-100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}}=-100\text{V}, V_{\text{GS}}=0\text{V}$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{\text{GS}}=\pm20\text{V}, V_{\text{DS}}=0\text{V}$	-	-	±10	μA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=-250\mu\text{A}$	-1.5	-1.9	-2.5	V
Drain-Source On-State Resistance	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}}=-10\text{V}, I_{\text{D}}=-15\text{A}$	-	44	58	$\text{m}\Omega$
		$V_{\text{GS}}=-4.5\text{V}, I_{\text{D}}=-15\text{A}$	-	48	65	$\text{m}\Omega$
Forward Transconductance	g_{FS}	$V_{\text{DS}}=-50\text{V}, I_{\text{D}}=-10\text{A}$	5	-	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C_{iss}	$V_{\text{DS}}=-50\text{V}, V_{\text{GS}}=0\text{V}, F=1.0\text{MHz}$	-	8049	-	PF
Output Capacitance	C_{oss}		-	184.5	-	PF
Reverse Transfer Capacitance	C_{rss}		-	179	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}}=-50\text{V}, I_{\text{D}}=-15\text{A}, V_{\text{GS}}=-10\text{V}, R_{\text{GEN}}=9.1\Omega$	-	17	-	nS
Turn-on Rise Time	t_{r}		-	80	-	nS
Turn-Off Delay Time	$t_{\text{d}(\text{off})}$		-	45	-	nS
Turn-Off Fall Time	t_{f}		-	65	-	nS
Total Gate Charge	Q_g	$V_{\text{DS}}=-50\text{V}, I_{\text{D}}=-15\text{A}, V_{\text{GS}}=-10\text{V}$	-	120	-	nC
Gate-Source Charge	Q_{gs}		-	22	-	nC
Gate-Drain Charge	Q_{gd}		-	26.4	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V_{SD}	$V_{\text{GS}}=0\text{V}, I_{\text{S}}=-10\text{A}$	-	-	-1.2	V
Diode Forward Current ^(Note 2)	I_{S}	-	-	-	-30	A
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ\text{C}, IF = -15\text{A}$ $di/dt = 100\text{A}/\mu\text{s}$ ^(Note 3)	-	90	-	nS
Reverse Recovery Charge	Q_{rr}		-	150	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

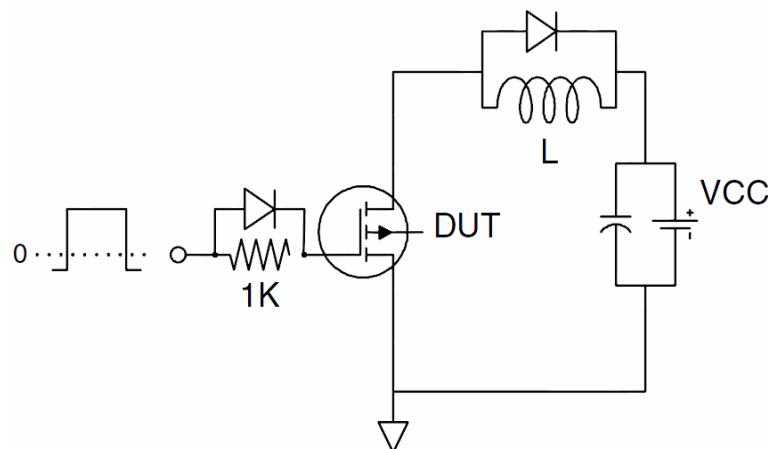
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_j=25^\circ\text{C}, V_{\text{DD}}=-50\text{V}, V_G=-10\text{V}, L=0.5\text{mH}, R_g=25\Omega$

Test Circuit

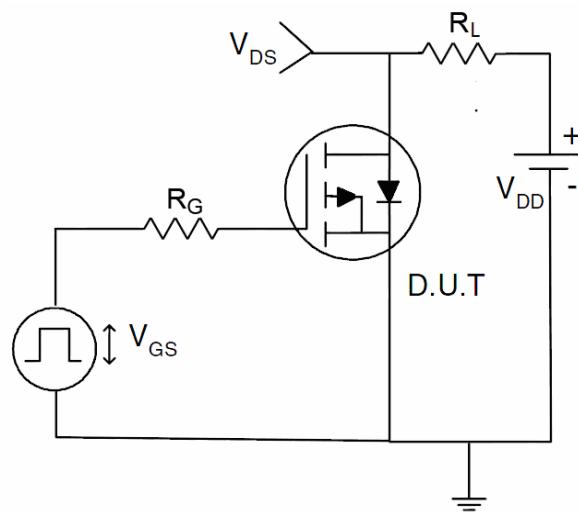
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

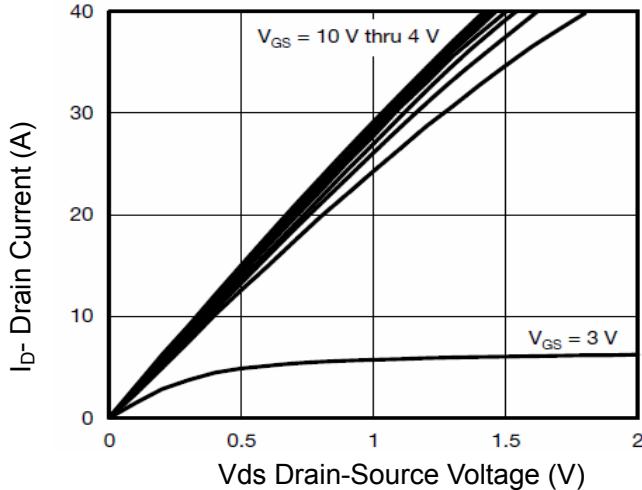


Figure 1 Output Characteristics

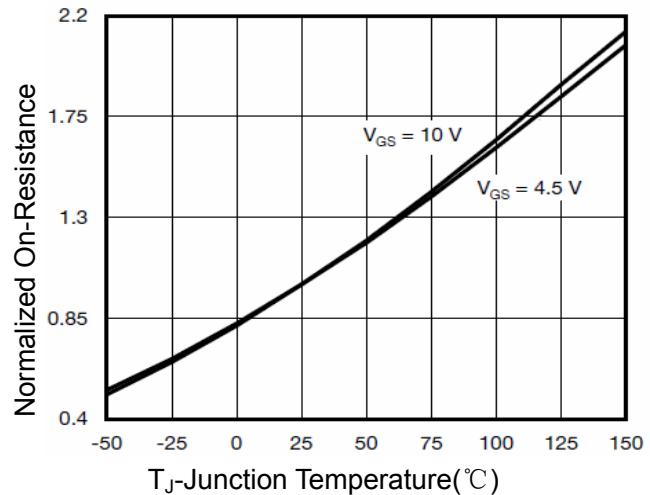


Figure 4 Rdson-JunctionTemperature

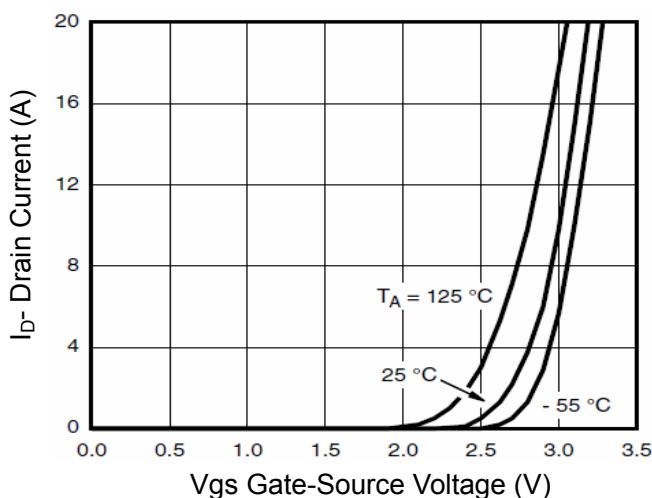


Figure 2 Transfer Characteristics

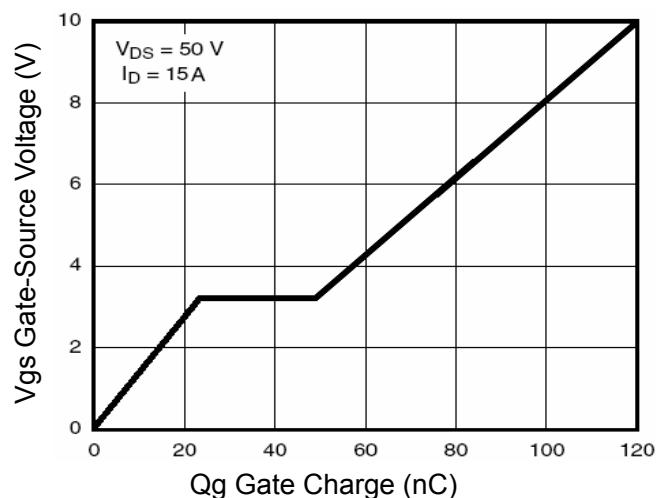


Figure 5 Gate Charge

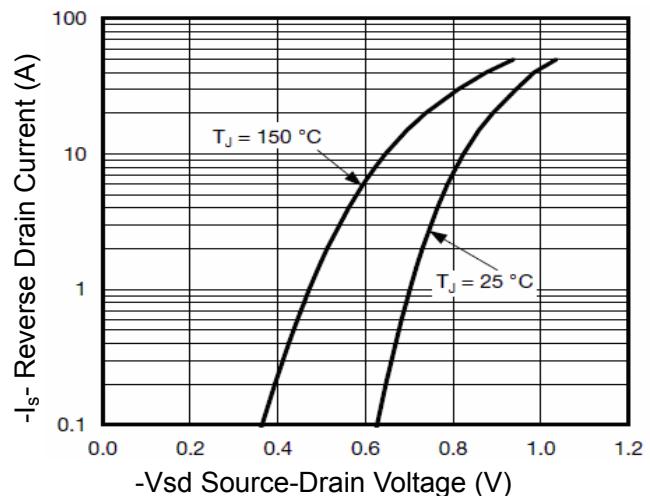


Figure 6 Source- Drain Diode Forward

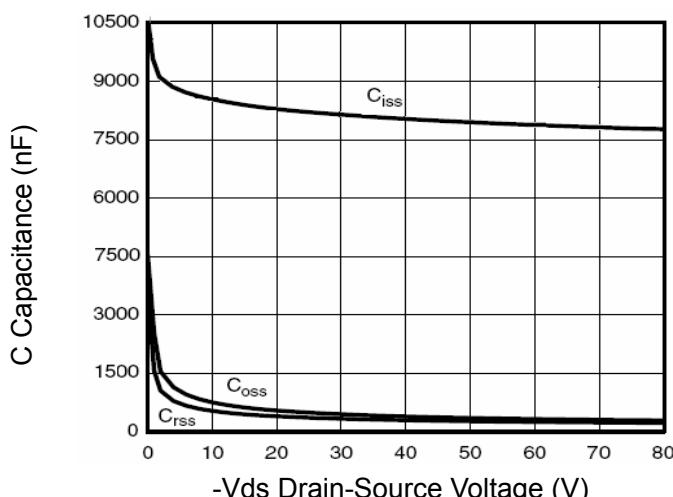


Figure 7 Capacitance vs Vds

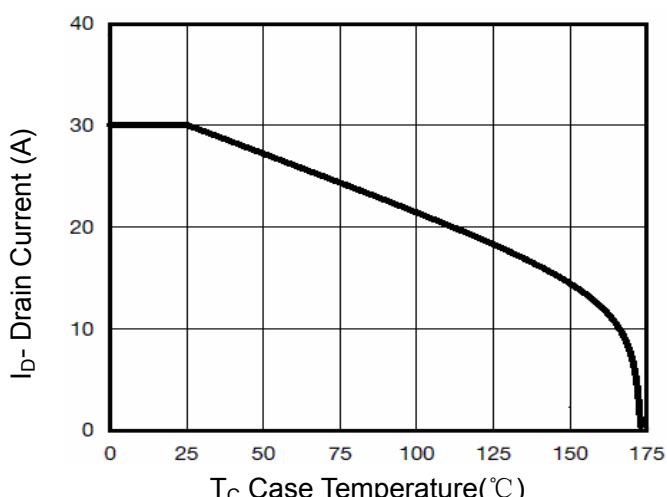


Figure 9 Drain Current vs Case Temperature

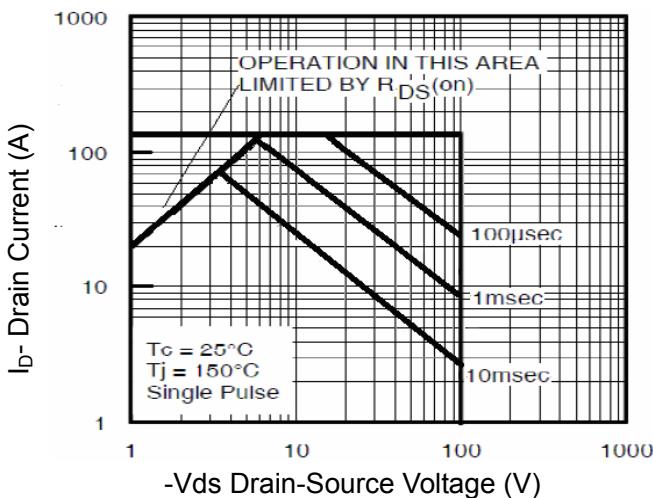


Figure 8 Safe Operation Area

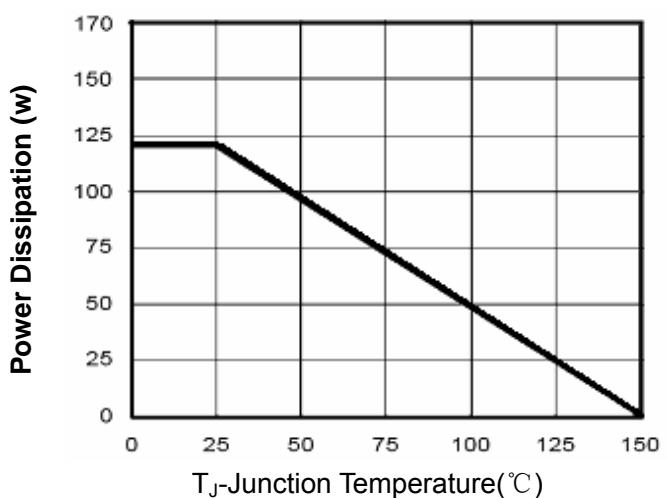


Figure 10 Power De-rating

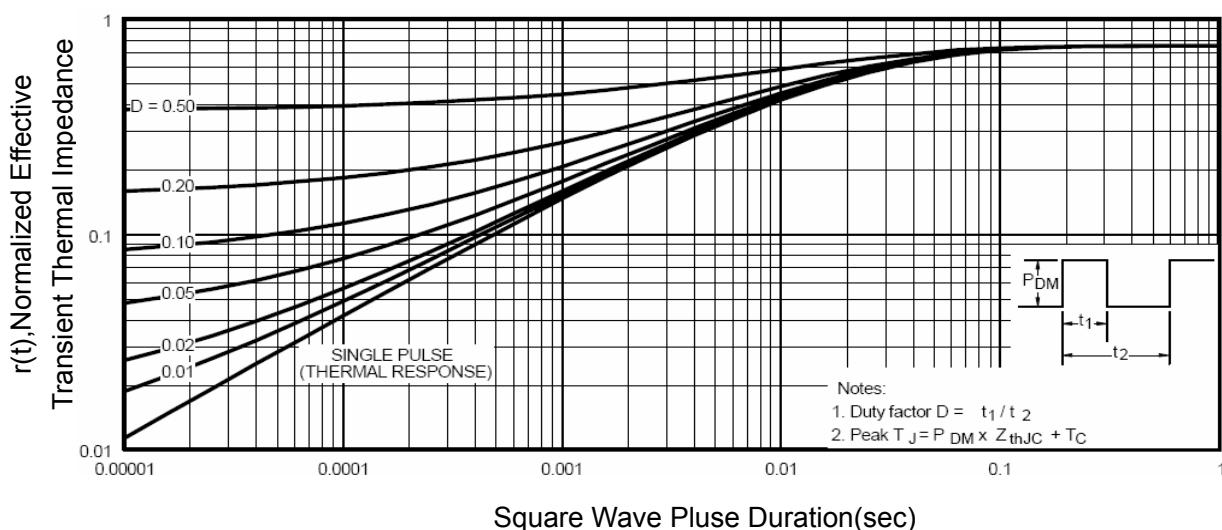
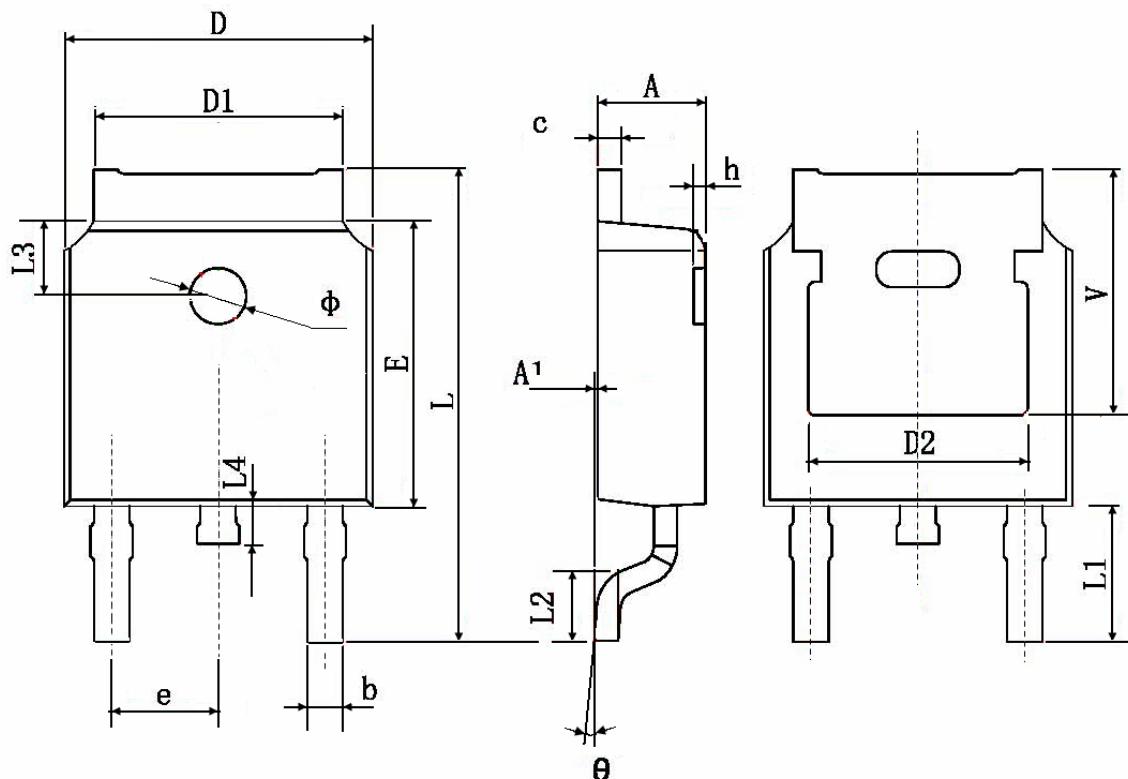


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-252 Package Information


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	

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