

NCE N-Channel Super Trench Power MOSFET

Description

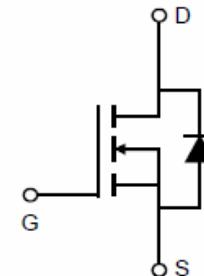
The NCEP3090GU uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

General Features

- $V_{DS} = 30V, I_D = 90A$
- $R_{DS(ON)} = 2m\Omega$ (typical) @ $V_{GS} = 10V$
- $R_{DS(ON)} = 3.1m\Omega$ (typical) @ $V_{GS} = 4.5V$
- Excellent gate charge $\times R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 150 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

Application

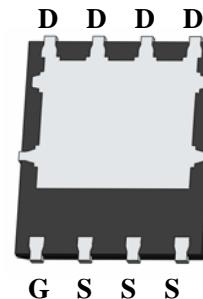
- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification



Schematic Diagram



Top View



Bottom View

100% UIS TESTED!

100% ΔV_{ds} TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCEP3090GU	NCEP3090GU	DFN5X6-8L	-	-	-

Absolute Maximum Ratings ($T_c=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	90	A
Drain Current-Continuous($T_c=100^\circ C$)	$I_D (100^\circ C)$	63.6	A
Pulsed Drain Current	I_{DM}	360	A
Maximum Power Dissipation	P_D	70	W
Derating factor		0.56	W/°C
Single pulse avalanche energy (Note 5)	E_{AS}	500	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	°C

**Thermal Characteristic**

Thermal Resistance, Junction-to-Case ^(Note 2)	R _{θJC}	1.8	°C/W
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Electrical Characteristics (T_C=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	V _{DSS}	V _{GS} =0V, I _D =250μA	30	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.0	1.5	2.0	V
Drain-Source On-State Resistance	R _{DSON}	V _{GS} =10V, I _D =20A	-	2	2.3	mΩ
		V _{GS} =4.5V, I _D =20A	-	3.1	3.6	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =20A	-	60	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, F=1.0MHz	-	2100	-	PF
Output Capacitance	C _{oss}		-	773	-	PF
Reverse Transfer Capacitance	C _{rss}		-	15.5	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =15V, I _D =20A V _{GS} =10V, R _G =1.6Ω	-	7.5	-	nS
Turn-on Rise Time	t _r		-	4.0	-	nS
Turn-Off Delay Time	t _{d(off)}		-	37	-	nS
Turn-Off Fall Time	t _f		-	7.5	-	nS
Total Gate Charge	Q _g	V _{DS} =15V, I _D =20A, V _{GS} =10V	-	34.8	-	nC
Gate-Source Charge	Q _{gs}		-	6.2	-	nC
Gate-Drain Charge	Q _{gd}		-	5.1	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V, I _S =20A	-	-	1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	90	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = I _S di/dt = 100A/μs ^(Note 3)	-	14	-	nS
Reverse Recovery Charge	Q _{rr}		-	21	-	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition : T_J=25°C, V_{DD}=20V, V_G=10V, L=0.5mH, R_G=25Ω

Typical Electrical and Thermal Characteristics

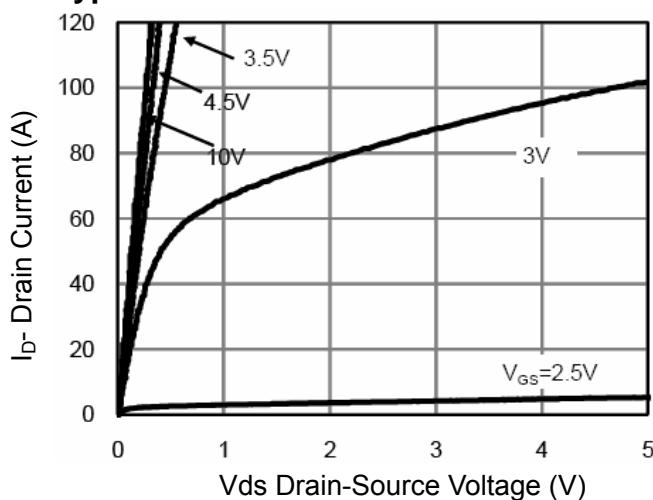


Figure 1 Output Characteristics

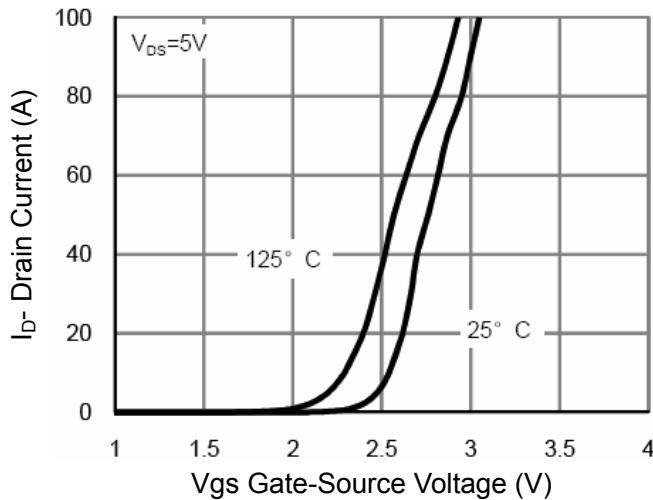


Figure 2 Transfer Characteristics

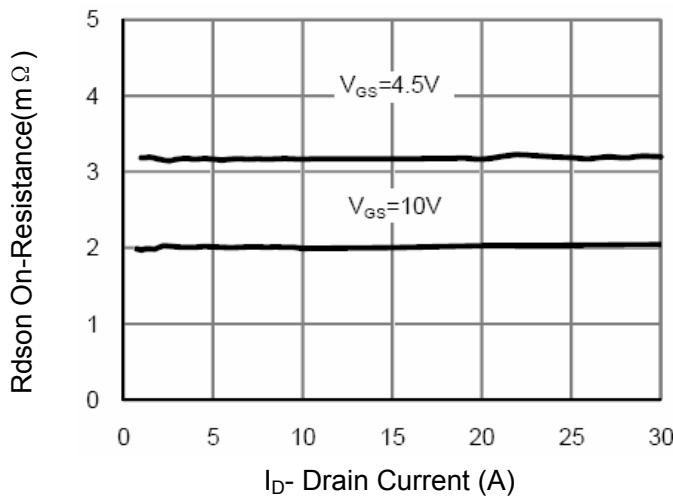


Figure 3 Rdson- Drain Current

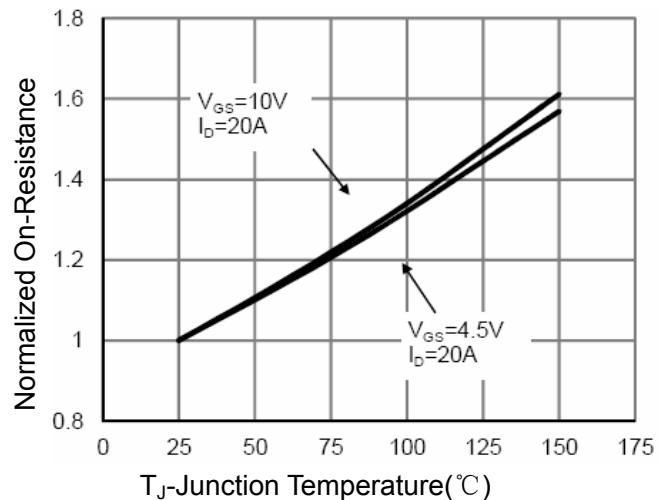


Figure 4 Rdson-Junction Temperature

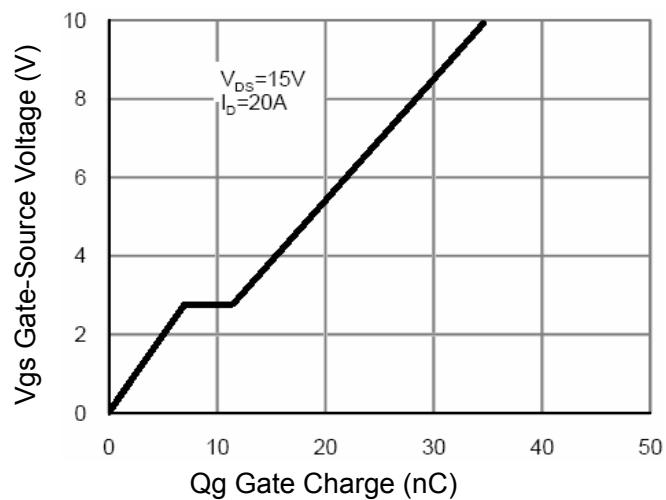


Figure 5 Gate Charge

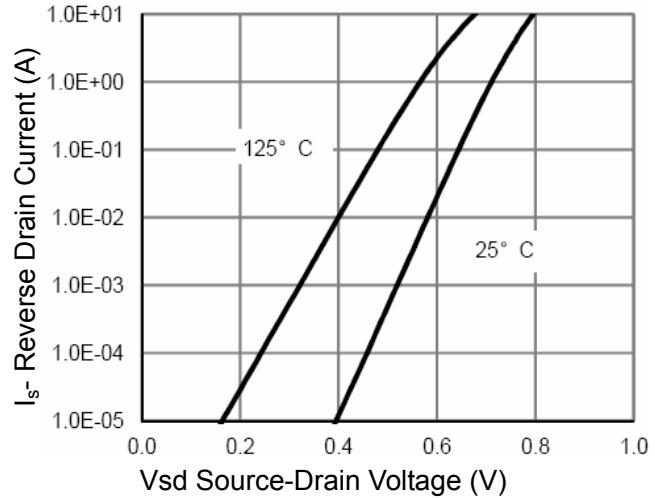


Figure 6 Source- Drain Diode Forward

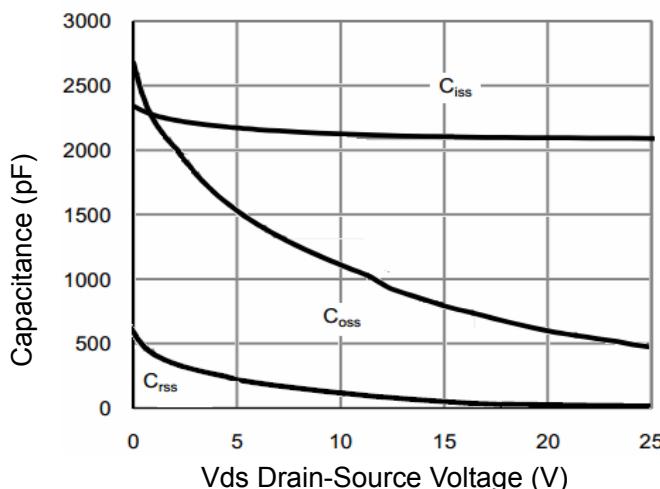


Figure 7 Capacitance vs Vds

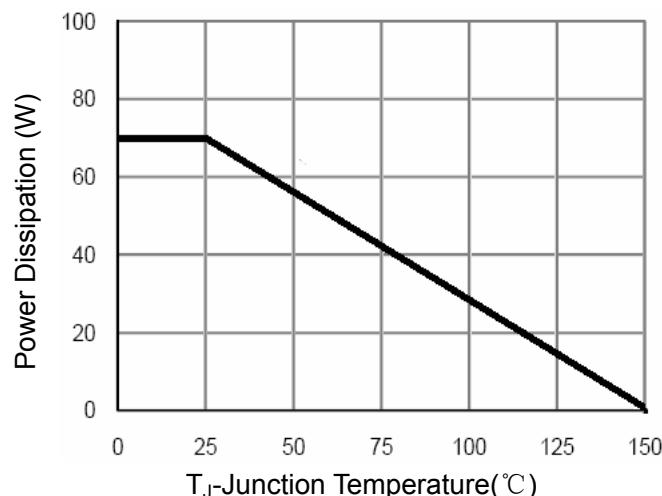


Figure 9 Power De-rating

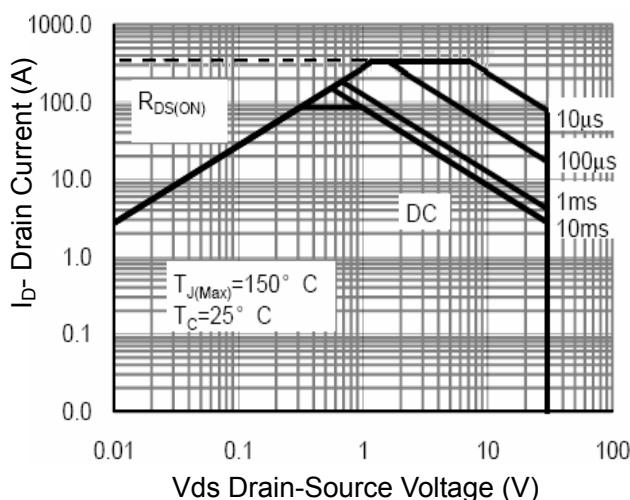


Figure 8 Safe Operation Area

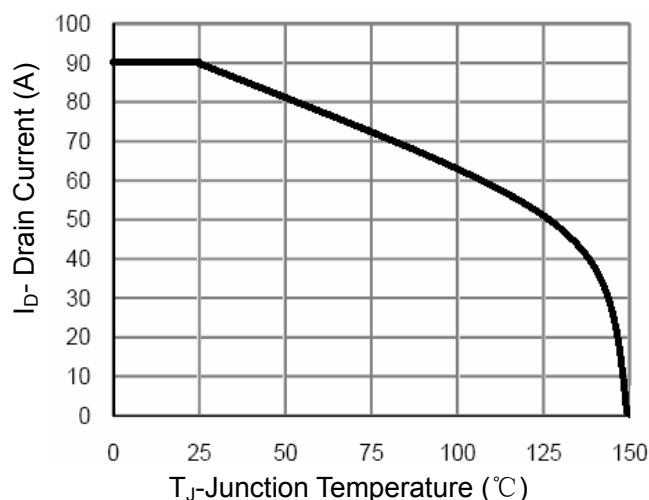


Figure 10 Current De-rating

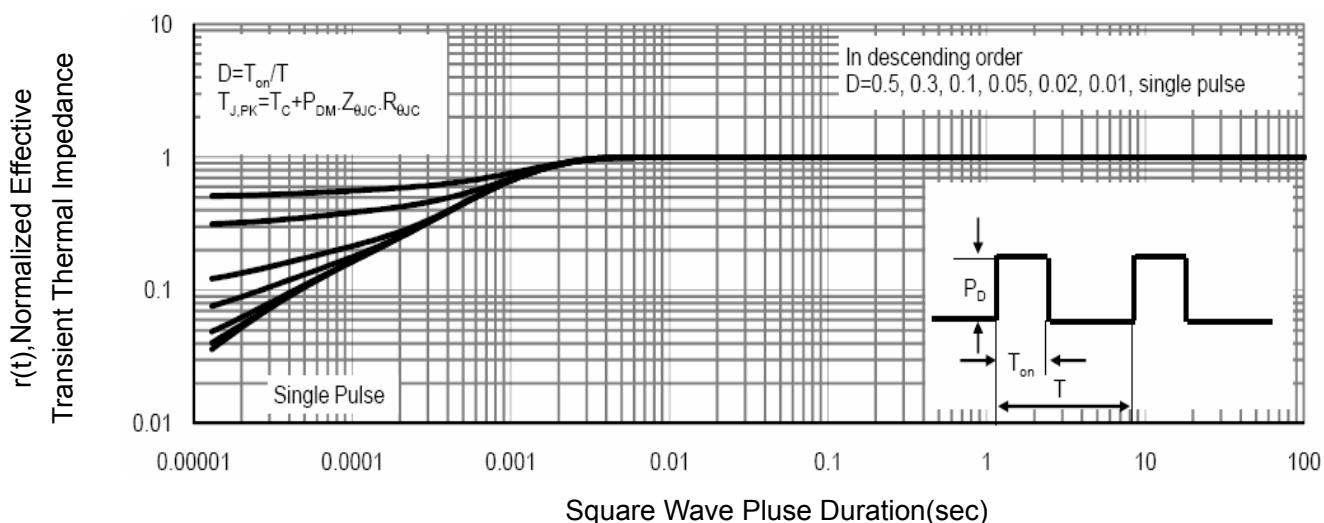
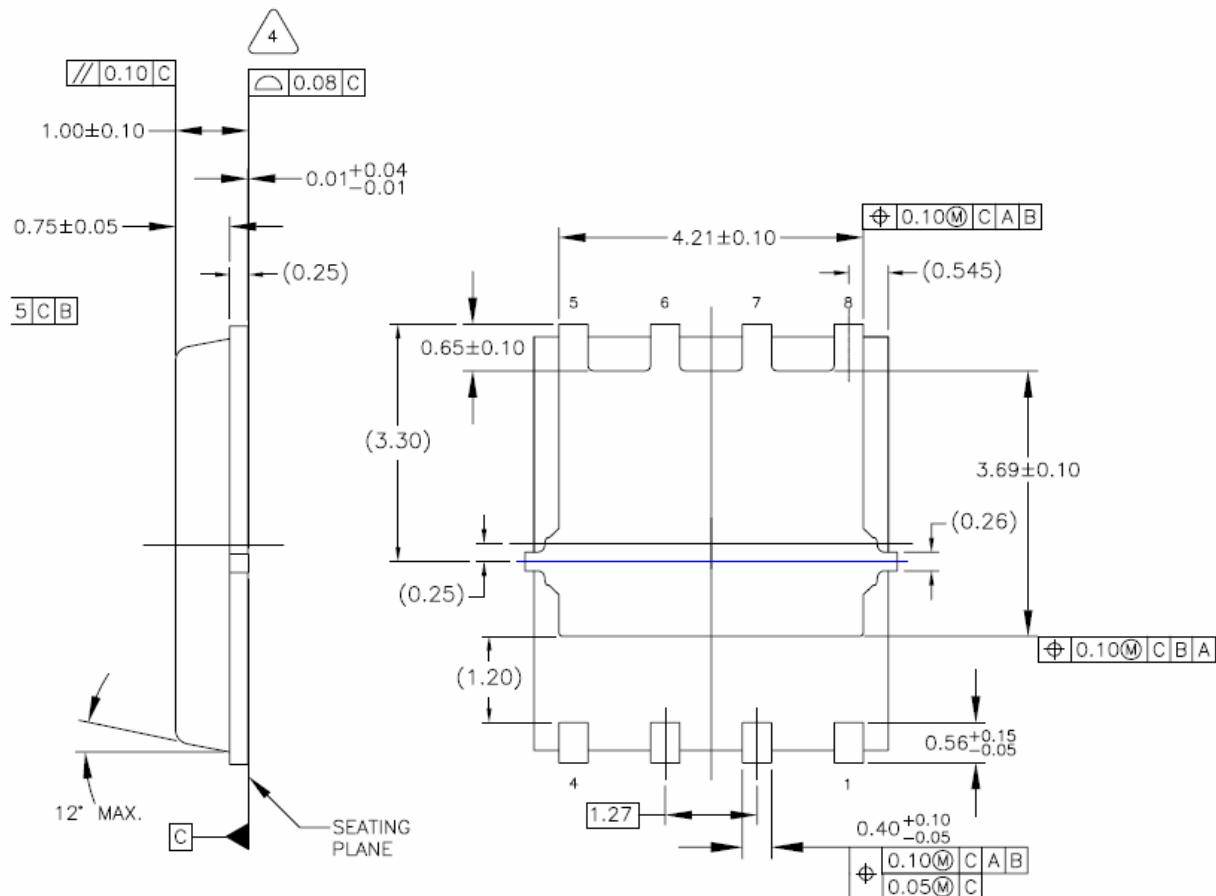
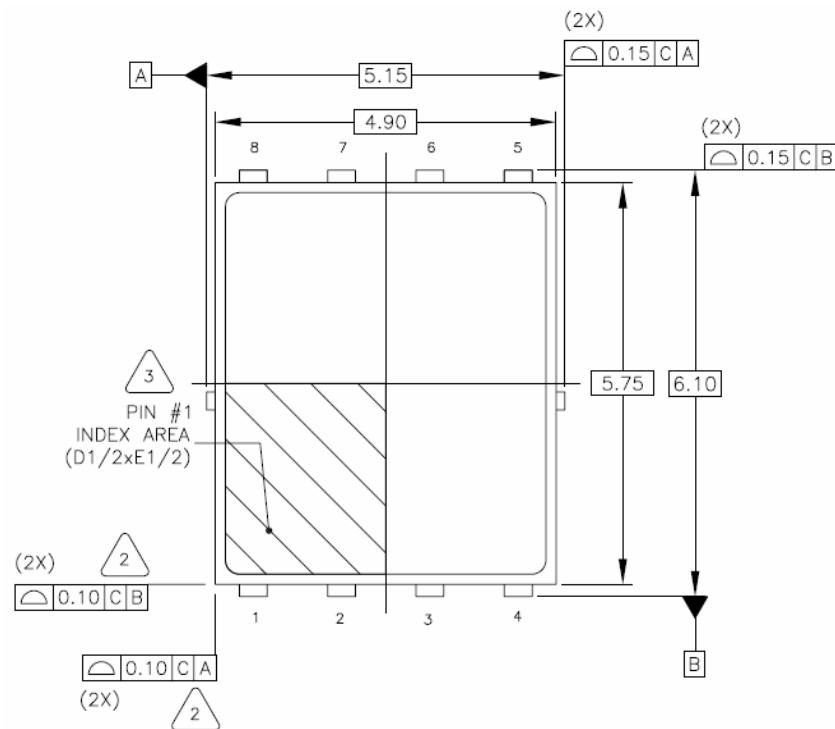


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN5X6-8L Package Information




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