

# SW7203 Register List

## 1. History

V1.0: initial version for IC version 1

## 2. Register

Note: reserved bits should not be modified

### 2.1. REG 0x01: Version info

Bit	Description	R/W	Default
7-3	/	/	/
2-0	IC Version	R	0x1

### 2.2. REG 0x02: IRQ EN 1

Bit	Description	R/W	Default
7	/	/	/
6	vsys_ovp_irq_dis 0: enable vsys ovp irq 1: disable vsys ovp irq	W/R	0x0
5	charger_overtime_irq_dis 0: enable charger overtime irq 1: disable charger overtime irq	W/R	0x0
4	charger_full_irq_dis 0: enable charger full irq 1: disable charger full irq	W/R	0x0
3	indtb_plug_in_irq_dis 0: enable indtb plug in irq 1: disable indtb plug in irq	W/R	0x0
2	indtb_plug_out_irq_dis 0: enable indtb plug out irq 1: disable indtb plug out irq	W/R	0x0
1	indta2_plug_in_irq_dis 0: enable indta2 plug in irq 1: disable indta2 plug in irq	W/R	0x0
0	indta1_plug_in_irq_dis 0: enable indta1 plug in irq 1: disable indta1 plug in irq	W/R	0x0

### 2.3. REG 0x03: IRQ EN 2

Bit	Description	R/W	Default
7	Thermal_shutdown_irq_dis 0: enable Thermal shutdown irq 1: disable Thermal shutdown irq	R/W	0x0
6	ntc_otp_irq_dis 0: enable ntc otp irq 1: disable ntc otp irq	R/W	0x0
5	vbus_ovp_irq_dis 0: enable vbus ovp irq 1: disable vbus ovp irq	R/W	0x0
4	vbat_ovp_irq_dis 0: enable vbat ovp irq 1: disable vbat ovp irq	R/W	0x0
3	vbat_uvlo_irq_dis 0: enable vbat uvlo irq 1: disable vbat uvlo irq	R/W	0x0
2	vbus_scp_irq_dis 0: enable vbus scp irq 1: disable vbus scp irq	R/W	0x0
1	vbus_olp_irq_dis 0: enable vbus olp irq 1: disable vbus olp irq	R/W	0x0
0	vsys_uvp_irq_dis 0: enable vsys_uvp irq 1: disable vsys_uvp irq	R/W	0x0

### 2.4. REG 0x04: IRQ Trigger Event 1

Bit	Description	R/W	Default
7	/	/	/
6	vsys_ovp_pending_bit Charger can restart if write 1 to clear this bit from host when adapter in. 0: nothing 1: vsys ovp	R/W	0x0
5	charger_overtime_pending_bit Write 1 to clear this bit from host. 0: nothing	R/W	0x0

	1: charger overtime		
4	charger_full_pending_bit Write 1 to clear this bit from host. 0: nothing 1: charger full	R/W	0x0
3	indtb_plug_in_pending_bit Write 1 to clear this bit from host. 0: nothing 1: indtb plug in	R/W	0x0
2	indtb_plug_out_pending_bit Write 1 to clear this bit from host. 0: nothing 1: indtb plug out	R/W	0x0
1	indta2_plug_in_pending_bit Write 1 to clear this bit from host. 0: nothing 1: indta2 plug in	R/W	0x0
0	indta1_plug_in_pending_bit Write 1 to clear this bit from host. 0: nothing 1: indta1 plug in	R/W	0x0

## 2.5. REG 0x05: IRQ Trigger Event 2

Bit	Description	R/W	Default
7	Thermal_shutdown_pending_bit Write 1 to clear this bit from host. 0: nothing 1: Thermal shutdown	R/W	0x0
6	ntc_otp_pending_bit Write 1 to clear this bit from host. 0: nothing 1: Ntc otp	R/W	0x0
5	vbus_ovp_pending_bit Write 1 to clear this bit from host. 0: nothing 1: vbus ovp	R/W	0x0
4	vbat_ovp_pending_bit Write 1 to clear this bit from host. 0: nothing 1: vbat ovp	R/W	0x0
3	vbat_uvlo_pending_bit	R/W	0x0

	Write 1 to clear this bit from host. 0: nothing 1: uvlo		
2	vbus_scp_pending_bit Write 1 to clear this bit from host. 0: nothing 1: vbus scp	R/W	0x0
1	vbus_olp_pending_bit Write 1 to clear this bit from host. 0: nothing 1: vbus olp	R/W	0x0
0	vsys_uvp_pending_bit Write 1 to clear this bit from host. 0: nothing 1: vsys_uvp	R/W	0x0

## 2.6. REG 0x06: System Status

Bit	Description	R/W	Default
7	charger_on 0: charger off 1: charger on-line	R	0x0
6	discharge_on 0: discharge off 1: discharge on-line	R	0x0
5-3	/	/	/
2	62368_limit_startup The function of 62368 reduce current and voltage is active. 0: nothing 1: reduce charge current and charge voltage according to 62368 settings	R	0x0
1	chg_mode_ibat_dischg Battery discharge to VSYS in charger mode. 0: bat discharge in charger mode 1: bat charger in charger mode	R	0x0
0	vbusb_existing 0: adapter disconnect 1: adapter on-line	R	0x0

## 2.7. REG 0x0C: Fast discharge Control

Bit	Description	R/W	Default
7-4	/	/	/
3	vbus_fast_dischg_en Vbus discharge for 500mS. It will close discharge automatically after 500mS .write 0 to close Vbus discharge earlier from host even discharge within 500mS. 0: disable vbus fast discharge 1: enable vbus fast discharge	W/R	0x0
2	indtb_fast_dischg_en Indtb discharge for 500mS. It will close discharge automatically after 500mS .write 0 to close Indtb discharge earlier from host even discharge within 500mS. 0: disable indtb fast discharge 1: enable indtb fast discharge	W/R	0x0
1	indta1_fast_dischg_en Indta1 discharge for 500mS. It will close discharge automatically after 500mS .write 0 to close Indta1 discharge earlier from host even discharge within 500mS. 0: disable indta1 fast discharge 1: enable indta1 fast discharge	W/R	0x0
0	indta2_fast_dischg_en Indta2 discharge for 500mS. It will close discharge automatically after 500mS .write 0 to close Indta2 discharge earlier from host even discharge within 500mS. 0: disable indta2 fast discharge 1: enable indta2 fast discharge	W/R	0x0

## 2.8. REG 0x0D: Work Mode Control

Bit	Description	R/W	Default
7-5	/	/	/
4	chg_en Before opening the charging, Indtb need to link to Vbus. 0: disable charger 1: enable charger	W/R	0x0
3-1	/	/	/
0	dischg_en 0: disable discharge 1: enable discharge	W/R	0x0

## 2.9. REG 0x0F: IC Reset Check

Bit	Description	R/W	Default
7-1	/	/	/
0	IC_reset_check This bit register can assist the MCU to determine whether reset occurs; after the chip is powered up, the bit is set to 1, and the MCU will query the bit regularly. If the bit is 0, the reset occurs on the chip.	R/W	0x0

## 2.10. REG 0x10: ADC Data Type

Bit	Description	R/W	Default
7-6	adc_filter_time 0: 10mS 1: 20mS 2: 40mS 3: 80mS	R/W	0x0
5-4	/	/	/
3-0	adc_data_type ADC data type selection 0: Vbat voltage ( $V_{bat} = \text{Adc\_data}[11:0] * 7.5\text{mV}$ ) 1: Vbus voltage ( $V_{bus} = \text{Adc\_data}[11:0] * 7.5\text{mV}$ ) 2~3: Reserved 4: Vbat charger current ( $I_{bat\_CHG} = \text{Adc\_data}[11:0] * 5\text{mA}$ ) 5: Vbus charger current ( $I_{bus\_CHG} = \text{Adc\_data}[11:0] * 5\text{mA}$ ) 6: Vbat discharge current ( $I_{bat\_DISCHG} = \text{Adc\_data}[11:0] * 5\text{mA}$ ) 7: Vbus discharge curr ( $I_{bus\_DISCHG} = \text{Adc\_data}[11:0] * 5\text{mA}$ ) 8: Tdie ( $TDIE = (\text{Adc\_data}[11:0] - 1839) / 6.82^{\circ}\text{C}$ ) 9: Rntc= $N * 1.1 / 40\text{K}\Omega$ 10: Vsys voltage ( $V_{SYS} = \text{Adc\_data}[11:0] * 7.5\text{mV}$ ) 11-15: Reserved	R/W	0x0

## 2.11. REG 0x11: ADC Data High 8Bit

Bit	Description	R/W	Default
7-0	adc_data[11:4] ADC Data High 8Bit	R	0x0

## 2.12. REG 0x12: ADC Data Low 4Bit

Bit	Description	R/W	Default
7-4	/	/	/
3-0	adc_data[3:0] ADC Data Low 4Bit	R	0x0

## 2.13. REG 0x18: Indt Control/Standby

Bit	Description	R/W	Default
7-5	/	/	/
4	standby_dis Shutdown in low-power mode enable 0: enable standby mode 1: disable standby mode	R/W	0x0
3-2	/	/	/
1	indta1_en Indta1 plug in detection enable 0: disable 1: enable	R/W	0x0
0	indta2_en Indta2 plug in detection enable 0: disable 1: enable	R/W	0x0

## 2.14. REG 0x19: Powerpath Control

Bit	Description	R/W	Default
7-3	/	/	/
2	gateb_en NMOS drive gateb enable 0: disable 1: enable	R/W	0x0
1	gatea1_en NMOS drive gatea1 enable 0: disable 1: enable	R/W	0x0
0	gatea2_en NMOS drive gatea2 enable 0: disable 1: enable	R/W	0x0

## 2.15. REG 0x1A: I2C Address

Bit	Description	R/W	Default
7-2	/	/	/
1-0	i2c_addr I2c address choose, 7bit 0: 0x3C (read 0x79, write 0x78) 1: 0x38 (read 0x71, write 0x70) 2: 0x1C (read 0x39, write 0x38) 3: 0x18 (read 0x31, write 0x30)	R/W	0x0

## 2.16. REG 0x20: Discharge Setting 1

Bit	Description	R/W	Default
7-6	pwm_freq Switch frequency setting in charger mode and discharge mode. 0: 300KHz 1: 200KHz 2: 400KHz 3: 800KHz	R/W	0x0
5	force_pwm 0: pfm mode in light load 1: force pwm mode in light load	R/W	0x0
4-3	/	/	/
2	ntc_dis Ntc over temp protection enable. 0: enable ntc over temp protection 1: disable ntc over temp protection	R/W	0x0
1	minton Set minton for power mos. 0: Low side mos minimal passthrough time is 112nS, high side mos minimal passthrough time is 133nS. 1: Low side mos minimal passthrough time is 58nS, high side mos minimal passthrough time is 81nS.	R/W	0x0
0	fb_ext_set Vbus output voltage mode selection 0: I2c set 1: Fb set	R/W	0x0

## 2.17. REG 0x21: Discharge Setting 2

Bit	Description	R/W	Default
7-6	deadtime_HS1 0: 60nS 1: 20nS 2: 40nS 3: 80nS	R/W	0x2
5-4	deadtime_LS1 0: 60nS 1: 20nS 2: 40nS 3: 60nS	R/W	0x2
3-2	deadtime_HS2 0: 60nS 1: 20nS 2: 40nS 3: 80nS	R/W	0x2
1-0	deadtime_LS2 0: 60nS 1: 20nS 2: 40nS 3: 60nS	R/W	0x2

## 2.18. REG 0x22: Discharge Setting 3

Bit	Description	R/W	Default
7-6	M2_rdson_set 0: 2.5mR 1: 5mR 2: 7.5mR 3: 10mR	R/W	0x3
5-4	Lset Set by LSET pin resistance for first power on. 0: 1uH 1: 2.2uH 2: 3.3uH 3: 4.7uH	R/W	0x0
3-0	/	/	/

## 2.19. REG 0x23: Discharge Vbus Vol High 8 Bits

Bit	Description	R/W	Default
7-0	dischg_vbus[10:3] To set the discharge output voltage limit, write to REG0x23() and REG0x24() using the data with 10mV/step. There is fixed offset voltage 3V for all codes. The range is clamped in digital core at minimal 3V and maximum 22V during normal discharge operation. Any write above 22 V is ignored. Write dischg_vbus[10:3] first and write dischg_vbus[2:0] next.	R/W	0x00

## 2.20. REG 0x24: Discharge Vbus Vol Low 3 Bits

Bit	Description	R/W	Default
7-3	/	/	/
2-0	dischg_vbus[2:0] Reference for REG0x23.	R/W	0x0

## 2.21. REG 0x25: Discharge Ibus Limit

Bit	Description	R/W	Default
7	/	/	/
6-0	dischg_ibus_limit[6:0] To set the discharge output current limit, write to REG0x25() using the data with 50mA/step. There is fixed offset current 0.5A for all codes. The range is clamped in digital core at minimal 0.5A and maximum 6.85A during normal discharge operation.	R/W	0x60

## 2.22. REG 0x26: Discharge Ibat Limit

Bit	Description	R/W	Default
7	/	/	/
6-0	dischg_ibat_limit[6:0] To set the discharge input current limit, write to REG0x26() using the data with 100mA/step. There is fixed offset current 0.1A for all codes. The range is clamped in digital core at minimal 0.1A and maximum 12A during normal discharge operation. Any write	R/W	0x77

	above 12A is ignored.		
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## 2.23. REG 0x27: Bat Uvlo

Bit	Description	R/W	Default
7	/	/	/
6-0	bat_uvlo[6:0] To set the discharge bat uvlo voltage limit, write to REG0x27() using the data with 100mV/step. There is fixed offset voltage 2.7V for all codes. The range is clamped in digital core at minimal 2.7V and maximum 13.2V during normal discharge operation. Any write above 13.2V is ignored.	R/W	0x03

## 2.24. REG 0x28: Bat Uvlo Hys

Bit	Description	R/W	Default
7-5	/	/	/
4-0	bat_uvlo_hys[4:0] To set the discharge bat uvlo hys voltage limit, write to REG0x28() using the data with 100mV/step. There is fixed offset voltage 0.4V for all codes. The range is clamped in digital core at minimal 0.4V and maximum 2V during normal discharge operation. Any write above 2 V is ignored.	R/W	0x00

## 2.25. REG 0x30: Charger Setting 1

Bit	Description	R/W	Default
7	vbus_uvlo_disable_charger Clear charger enable when adppter out. 0: clean charger enable flag when Vbus uvlo 1: nothing	R/W	0x0
6	charger_done_dis Stop charger enable when vbat reach charge voltage setting. 0: enable charger done 1: disable charger done	R/W	0x0
5-4	/	/	/
3-2	chg_end_cur Charger current set when charger full. 0: 100mA	R/W	0x0

	1: 200mA 2: 300mA 3: 400mA		
1-0	cell_numb Cell_numb is set by BSET pin resistance for first power on. 0: 1 cell 1: 2 cells 2: 3 cells 3: 4 cells	R/W	0x0

## 2.26. REG 0x31: Charger Setting 2

Bit	Description	R/W	Default
7-4	/	/	/
3-2	Thermal_shutdown_setting. 0: 120°C 1: 130°C 2: 140°C 3: 150°C	R/W	0x3
1-0	ocp_cur Trigger RCS OCP or M2 OCP when inductor peak current clamp to this value in charger mode or discharge mode. 0: 12A 1: 14A 2: 16A 3: 18A	R/W	0x3

## 2.27. REG 0x32: Charger Setting 3

Bit	Description	R/W	Default
7	62368_dis 0: enable 62368 mode 1: disable 62368 mode	R/W	0x0
6	62368_reduce_ibat_only Reduce ibus enable when it is in 62368 status. 0: reduce ibus and ibat 1: reduce ibat only	R/W	0x0
5	/	/	/
4	chg_overtime_dis 0: enable charger overtime 1: disable charger overtime	R/W	0x0

3-2	chg_trk_overtime_set Trickle charger overtime setting. 0: 30min 1: 1h 2: 2h 3: 4h	R/W	0x3
1-0	chg_cc_overtime_set Constant charger overtime setting 0: 12h 1: 24h 2: 48h 3: 72h	R/W	0x3

## 2.28. REG 0x33: Charger Setting 4

Bit	Description	R/W	Default
7-6	62368_cold_chg_cur_reduce 62368 reduce charger current when in cold. 0: ibus and ibat reduce to 1/2 1: ibus and ibat reduce to 1/4 2: nothing 3: no use	R/W	0x0
5-4	62368_hot_chg_cur_reduce 62368 reduce charger current when in hot. 0: ibus and ibat reduce to 1/2 1: ibus and ibat reduce to 1/4 2: nothing 3: no use	R/W	0x0
3	62368_cold_chg_vol_reduce 62368 reduce chargevoltage when in cold. 0: charger voltage reduce cell number * 0.1V 1: nothing	R/W	0x0
2	62368_hot_chg_vol_reduce 62368 reduce chargevoltage when in hot. 0: charger voltage reduce cell number * 0.1V 1: nothing	R/W	0x0
1	62368_cold_temp_hys 0: 5°C 1: 10°C	R/W	0x0
0	62368_hot_temp_hys 0: 5°C 1: 10°C	R/W	0x0

## 2.29. REG 0x34: Charger Vbat Vol High 8 Bits

Bit	Description	R/W	Default
7-0	chg_vol[10:3] To set the output charge voltage, write a 11-bit ChargeVoltage register command (REG0x34() and REG0x35()) using the data with 10mV/step. There is fixed offset voltage 3V for all codes. The charger provides charge voltage range from 3 V to 19.2 V, Any write above 19.2 V is ignored. Upon POR, REG0x34() and REG0x35() is by default set as 4.2V for 1 cell, 8.4V for 2 cells, 12.6V for 3 cells or 16.8V for 4 cells. Write chg_vol [10:3] first and write chg_vol [2:0] next.	R/W	0x00

## 2.30. REG 0x35: Charger Vbat Vol Low 3 Bits

Bit	Description	R/W	Default
7-3	/	/	/
2-0	chg_vol[2:0] Reference for REG 0x34.	R/W	0x00

## 2.31. REG 0x36: Trickle Vol

Bit	Description	R/W	Default
7	/	/	/
6-0	trickle_vol_threshold[6:0] To set the trickle_vol threshold, write a 7-bit trickle_vol threshold register command (REG0x36()) using the data with 100mV/step. There is fixed offset voltage 2.5V for all codes. The charger provides trickle_vol threshold range from 2.5 V to 13.2 V, Any write above 13.2 V is ignored. Upon POR, REG0x36() is by default set as 2.9V for 1 cell, 5.8V for 2 cells, 8.7V for 3 cells or 11.6V for 4 cells.	R/W	0x00

## 2.32. REG 0x37: Trickle Vol Hys/Trickle Cur

Bit	Description	R/W	Default
3-2	trickle_cur 0: 100mA 1: 200mA	R/W	0x0

	2: 300mA 3: 400mA		
1-0	trickle_vol_hys Upon POR, REG0x37() is by default set as 0.1V for 1 cell, 0.2V for 2 cells, 0.3V for 3 cells or 0.4V for 4 cells. 0: 0.1V 1: 0.2V 2: 0.3V 3: 0.4V	R/W	0x0

### 2.33. REG 0x38: Charger Hold Vol

Bit	Description	R/W	Default
7-0	chg_hold threshold[7:0] To set the input voltage limit, write a 8-bit InputVoltage register command (REG0x38()) using the data with 100mV/step. There is fixed offset voltage 4V for all codes. The charger provides input voltage range from 4 V to 20 V, Any write above 20V is ignored. If the input voltage drops more than the InputVoltage register allows, the device enters VINDPM and reduces the charge current.	R/W	0x04

### 2.34. REG 0x39: Charger Ibus Limit

Bit	Description	R/W	Default
7	/	/	/
6-0	chg_ibus_limit[6:0] To set the charge input current limit, write to REG0x39() using the data with 50mA/step. There is fixed offset current 0.5A for all codes. The range is clamped in digital core at minimal 0.5A and maximum 6.85A during normal discharge operation.	R/W	0x40

### 2.35. REG 0x3A: Charger Ibat Limit

Bit	Description	R/W	Default
7	/	/	/
6-0	chg_ibat_limit[6:0] To set the charge output current limit, write to REG0x3A() using the data with 100mA/step. There is fixed offset current 0.1A for all codes.	R/W	0x00

	The range is clamped in digital core at minimal 0.1A and maximum 12A during normal charge operation. Any write above 12 A is ignored.		
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### 2.36. REG 0x40: Nvdc Setting 1

Bit	Description	R/W	Default
7	/	/	/
6	learn_en Learn mode allows the battery to discharge and converter to shut off while the adapter is present . It calibrates the battery gas gauge over a complete discharge/charge cycle. 0: disable learn mode 1: enable learn mode	R/W	0x0
5-2	/	/	/
1-0	vsys_vth Vsys over load threshold for battery cell num. 0: 6V (2-4S) or 3.1V (1S) 1: 5.75V (2-4S) or 2.85V (1S) 2: 6.25V (2-4S) or 3.35V (1S) 3: 6.5V (2-4S) or 3.6V (1S)	R/W	0x0

### 2.37. REG 0x41: Nvdc Setting 2

Bit	Description	R/W	Default
7-1	/	/	/
4-0	ibat_ldo[4:0] To set the charge output ldo current limit, write to REG0x41() using the data with 100mA/step. There is fixed offset current 0.1A for all codes. The range is clamped in digital core at minimal 0.1A and maximum 2A during normal charge operation. Any write above 2 A is ignored.	R/W	0x0

### 2.38. REG 0x42: Vsys Min Vol

Bit	Description	R/W	Default
7	/	/	/
6-0	vsys_min[6:0] To set the vsys_min voltage, write a 7-bit vsys_min voltage register command (REG0x42()) using the data with 200mV/step.	R/W	0x0

	There is fixed offset voltage 3V for all codes. The charger provides vsys_min voltage range from 3 V to 16.6 V, Any write above 16.6 V is ignored. Upon POR, REG0x42() is by default set as 3.6V for 1 cell, 6.2V for 2 cells, 9.2V for 3 cells or 12.2V for 4 cells.		
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### 2.39. REG 0x43: Ntc Setting 1

Bit	Description	R/W	Default
7-6	dischg_ntc_h Discharge ntc hot threshold. 0: 50°C 1: 55°C 2: 60°C 3: 65°C	R/W	0x0
5-4	dischg_ntc_l Discharge ntc cold threshold. 0: -10°C 1: -5°C 2: 0°C 3: -20°C	R/W	0x0
3-2	chg_ntc_h Charger ntc hot threshold. 0: 45°C 1: 40°C 2: 50°C 3: 55°C	R/W	0x0
1-0	chg_ntc_l Charger ntc cold threshold. 0: 0°C 1: 10°C 2: 5°C 3: -5°C	R/W	0x0

### 2.40. REG 0x44: Ntc Setting 2

Bit	Description	R/W	Default
7-2	/	/	/
1-0	ntc_i_flag Current flow from ntc pin. 0: 20uA	R	0x0

	1: 40uA		
	2: 80uA		
	3: Reserved		

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