图纸编号	图纸名称		
1	Title Page		
2	Block_Digram		
3	PowerRail		
4	HDMI/UART/RJ45		
5	Peripheral		
6	DIMM 200		
7			
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13			
14			
15			

修改记录:

_	日期	修改人	说明
1	2019-08-12	Jack	创建
2	2020-03-23	Hans	修改为V11 版本



AIGO_C5MB_V11 Schematic

TEAM: AIGO_C5

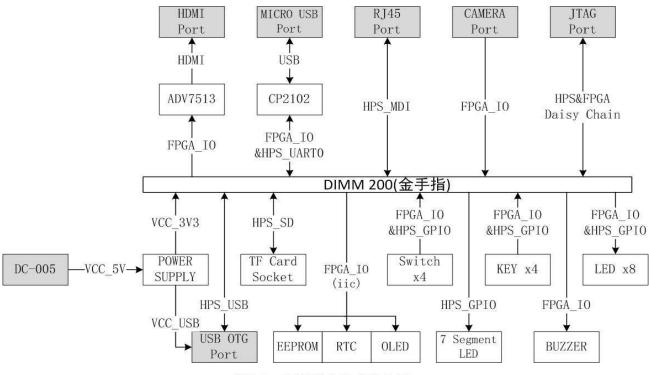
DESIGN: Hans

CHECK: Jack

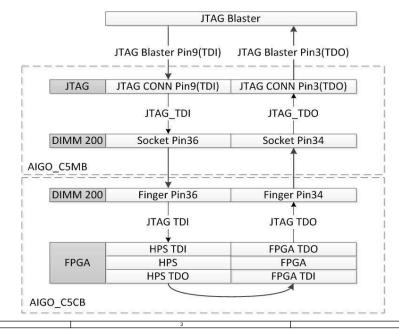
DATE: 2020/03/23

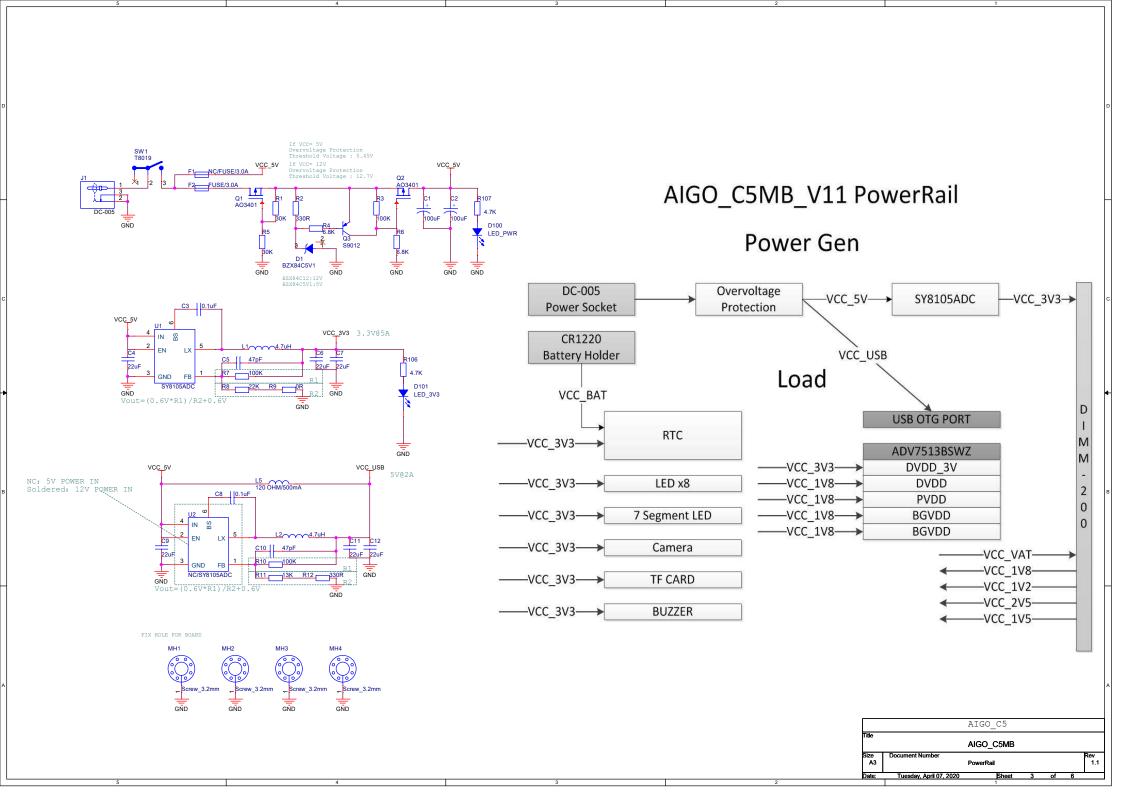
		AIGO_C5				
Title		AIGO_C5MB				
Size A3	Document Number	Title Page				Rev 1.1
Date:	Monday, March 23, 2020	Sheet	1	of	6	

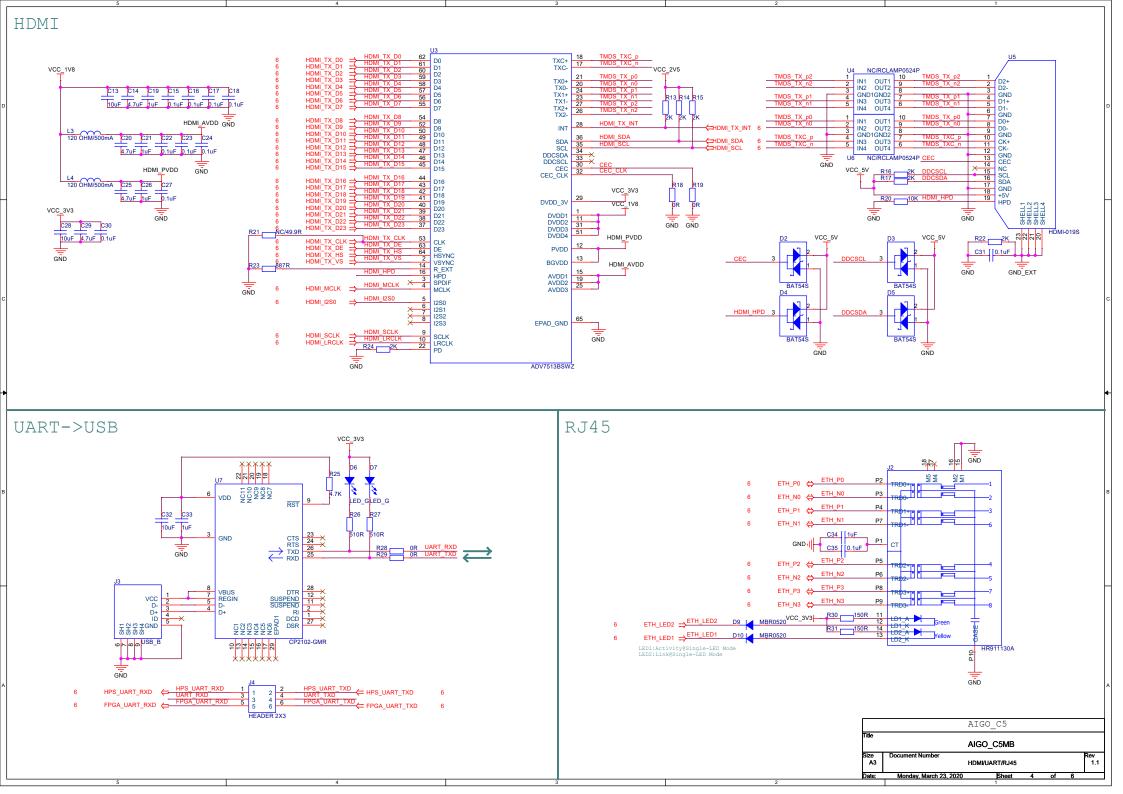
AIGO_C5MB_V11 Block Diagram

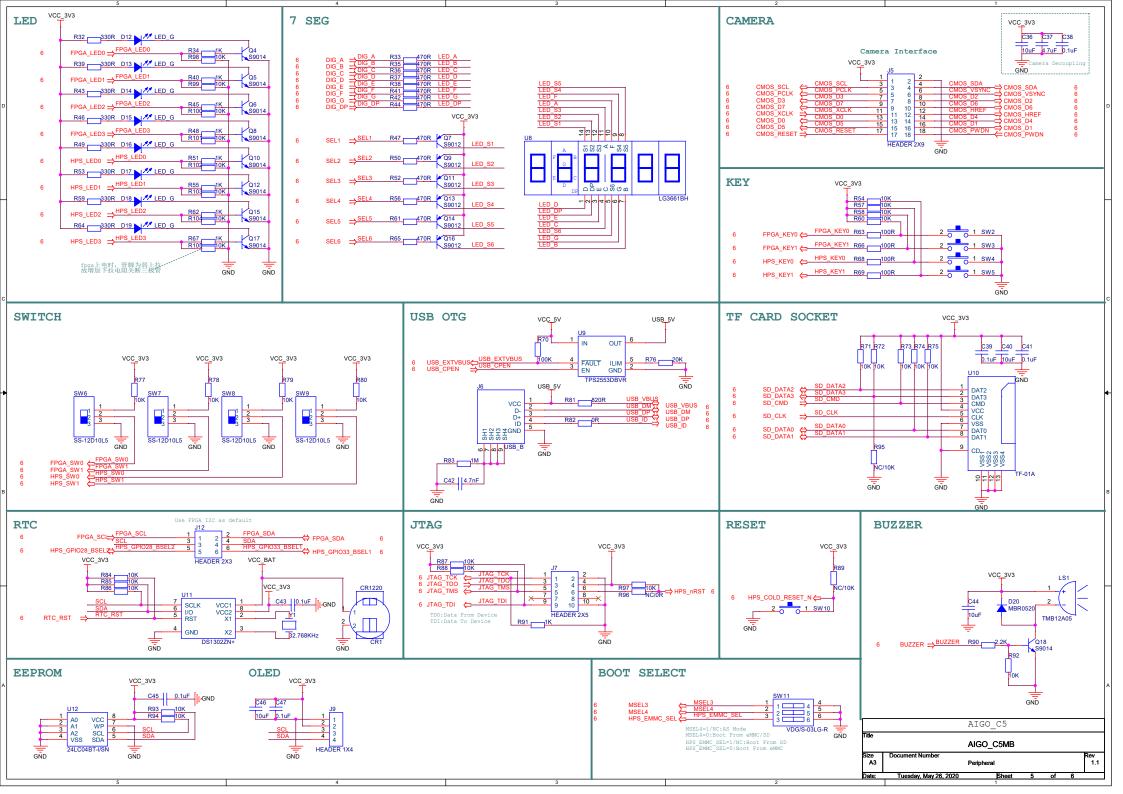


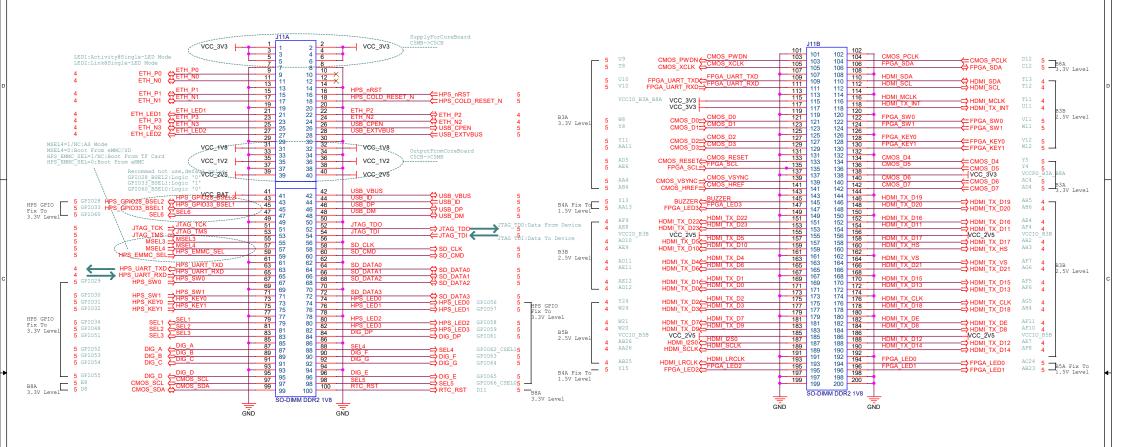
AIGO_C5CB&MB JTAG Flow











Supported Voltage Ranges

Power	Direction	Range	Current	Annotation
VCC_3V3	MB->CB	3.3V	TBD	core board main power
VCCIO B3B	MB->CB	1.2-2.5V	TBD	Bank 3B IO Power
VCCIO_B5B	MB->CB	1.2-3.3V	TBD	Bank 5B IO Power
VCCPD_B5B	MB->CB	1.2-3.3V(*)	TBD	Bank 5B IO Pre Driver
VCCIO B3A B8A	MB->CB	1.2-3.3V	TBD	Bank 3A/8A IO Power
VCCPD B3A B8A	MB->CB	2.5-3.3V(*)	TBD	Bank 3A/8A IO Pre Driver
VCC BAT	MB->CB	2.0-3.6V	TBD	Backup Battery Power
VCC_1V2	CB->MB	1.2V	TBD	1A max
VCC 1V8	CB->MB	1.8V	TBD	1A max
VCC_2V5	CB->MB	2.5V	TBD	1.5A max

(*)if VCCIO B5B>=2.5V,VCCPD B5B=VCCIO B5B if VCCIO B5B<2.5V,VCCPD B5B=2.5V (*)if VCCIO B3A B8A>=2.5V,VCCPD B3A B8A=VCCIO B3A B8A if VCCIO B3A B8A<2.5V,VCCPD B3A B8A=2.5V

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