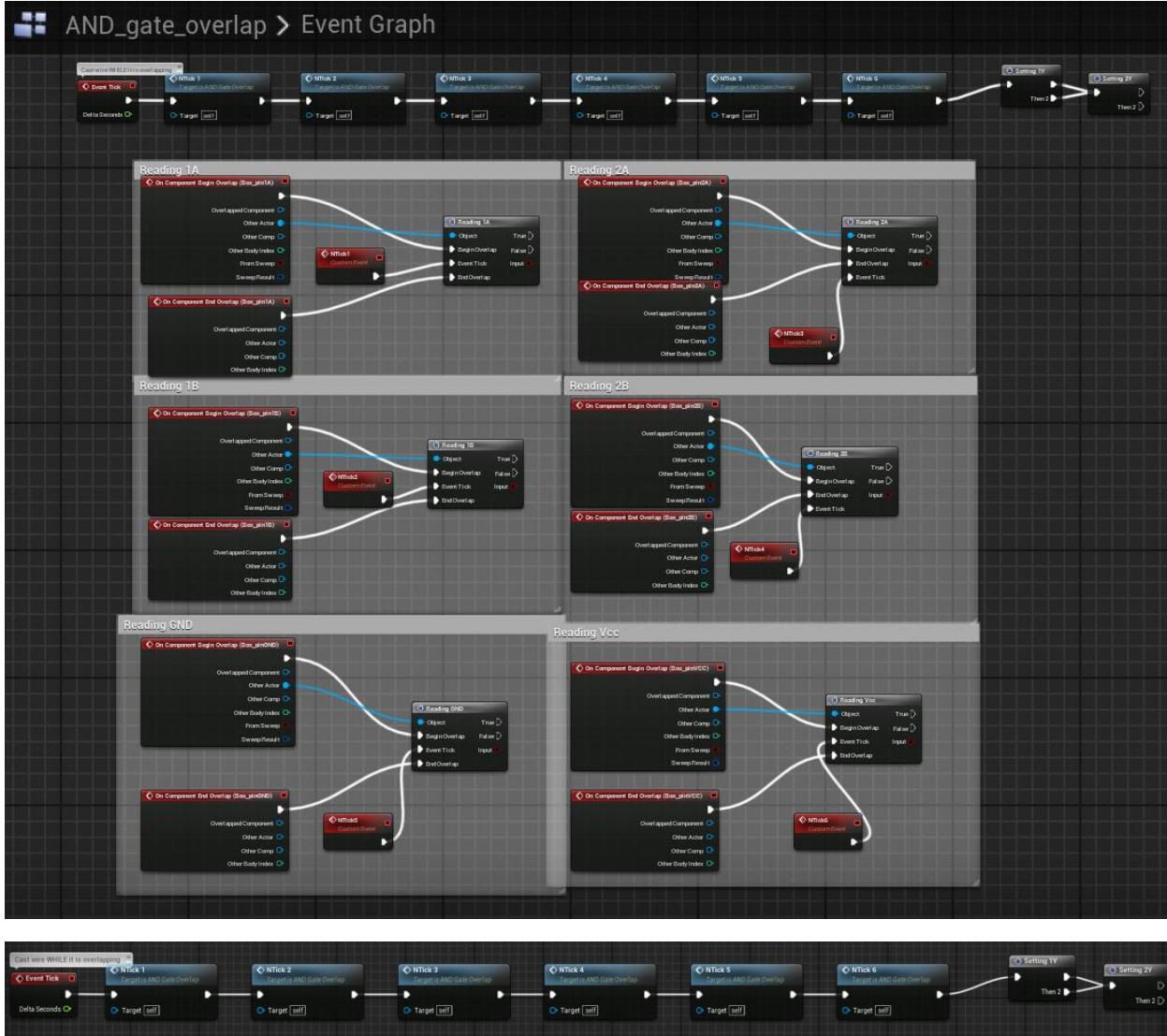
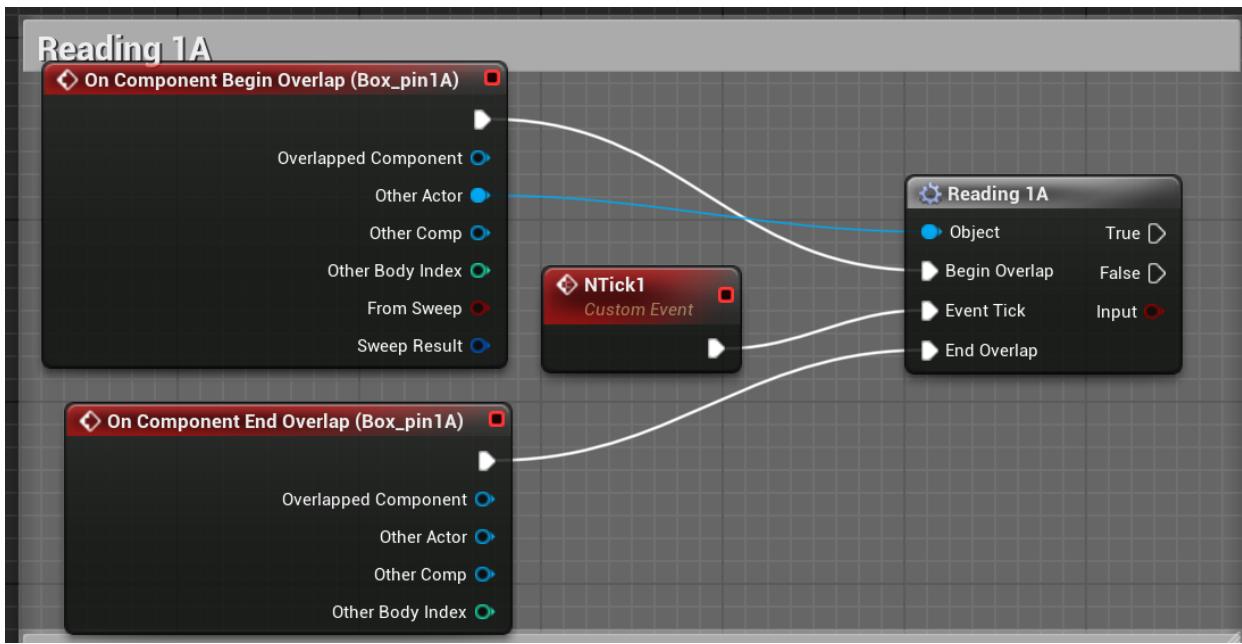


Design: Michael DiNardi, Acacia Mastropao

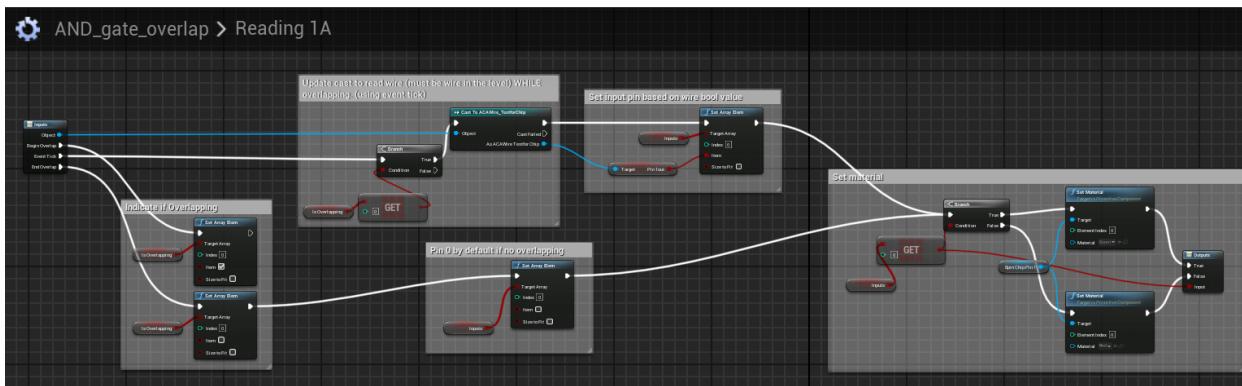
AND gate overlap (same event graph for all overlap chips except NOT gate which has different number of inputs and outputs. Additionally, the Event ticks have different names on different graphs)



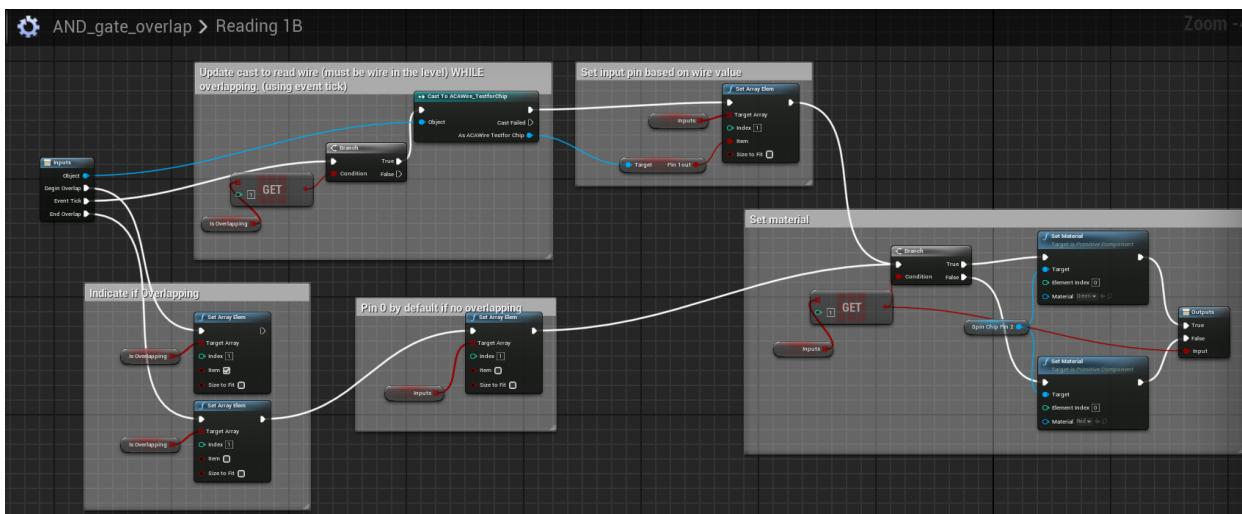


(same basic connection for each Reading box in the screenshot above but replaced with specific Reading xx, NTickx and On Component Begin/End Overlap (Box_pinxx))

Reading 1A (same for all overlap chips)

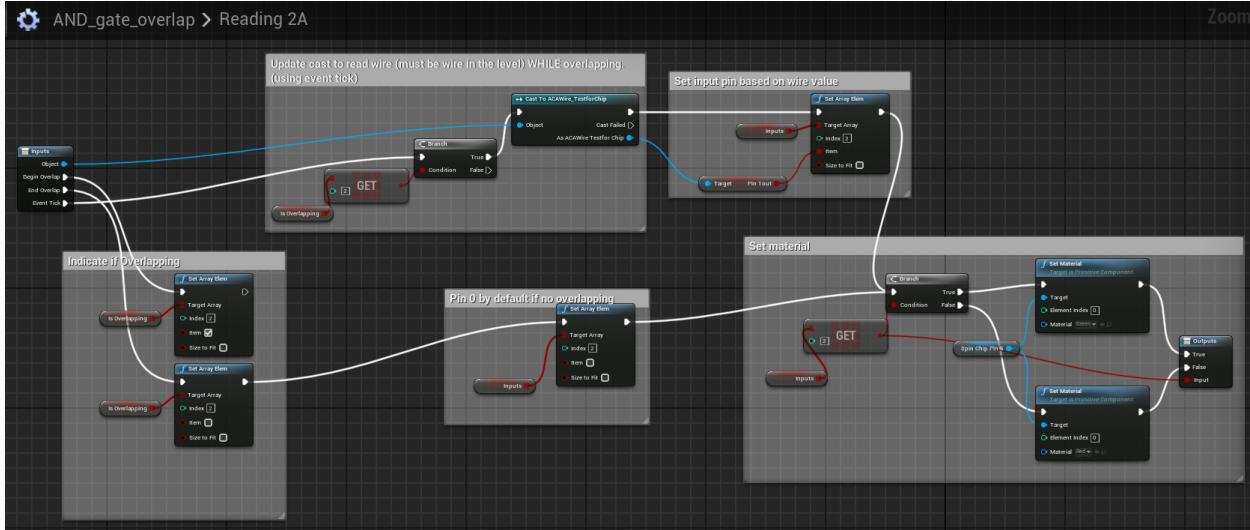


Reading 1B (same for all overlap chips (except NOT gate which has no Read 1B))

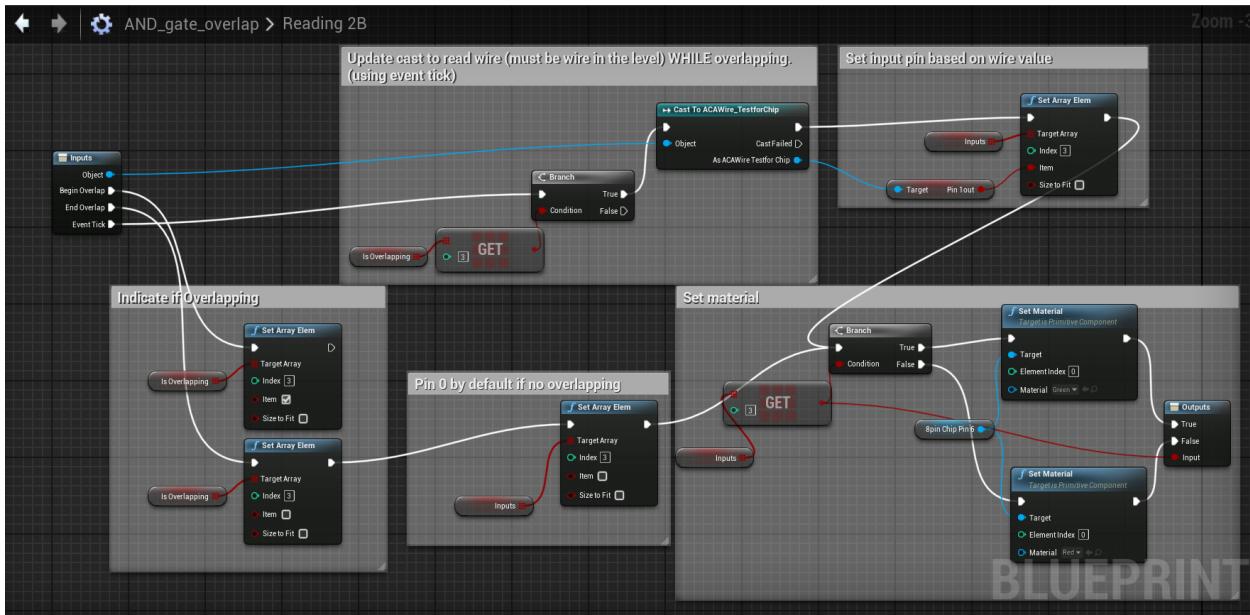


Reading 1A, 1B, 2A, 2B, Vcc have same blueprint except for the isOverlapping and Input Array Indexes, and the Set material target changes according to the pin that is being read.

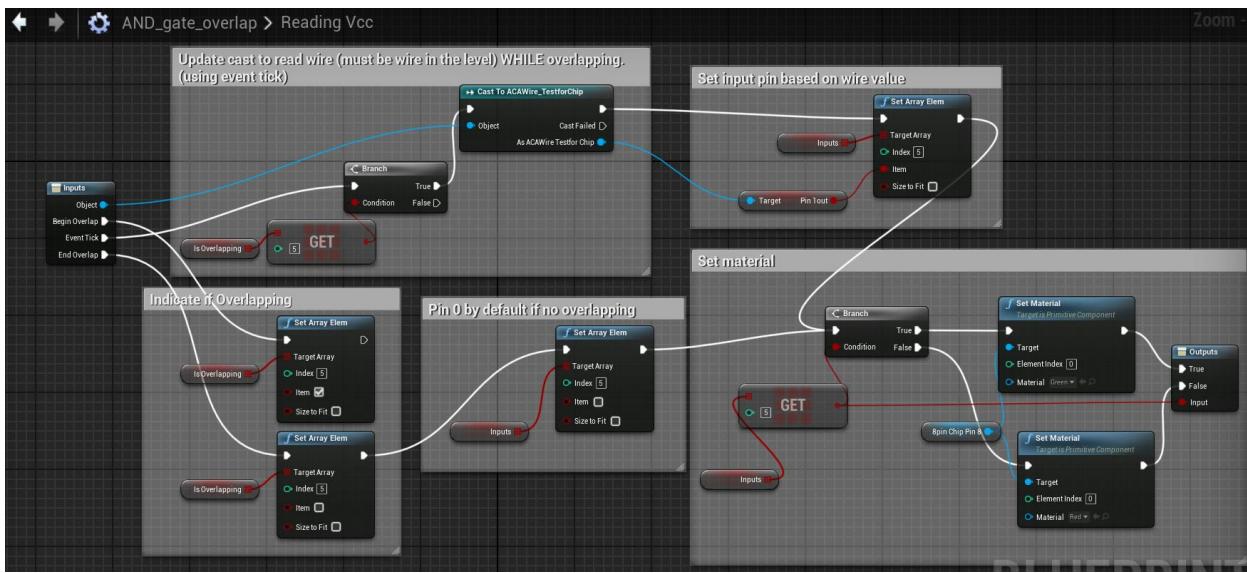
Reading 2A (same for all overlap chips (except NOT gate which has different array index))



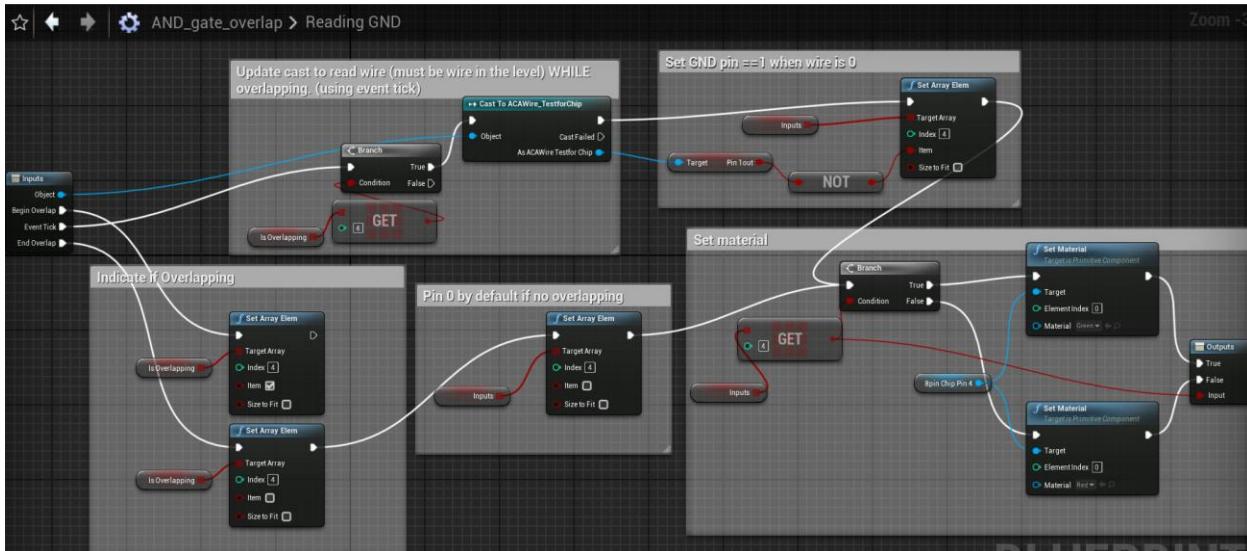
Reading 2B (same for all overlap chips (except NOT gate which has no Reading 2B))



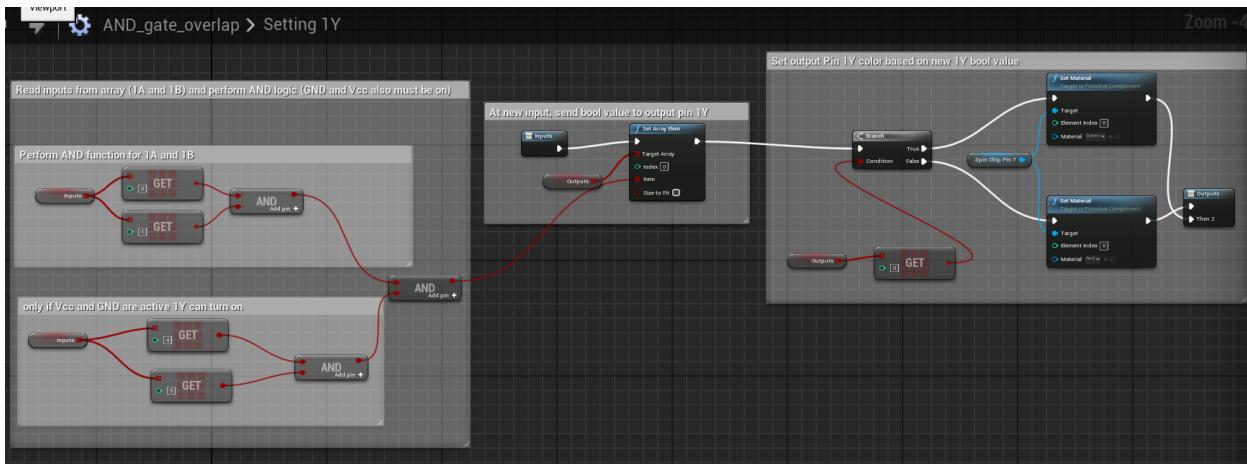
Reading Vcc (same for all overlap chips)



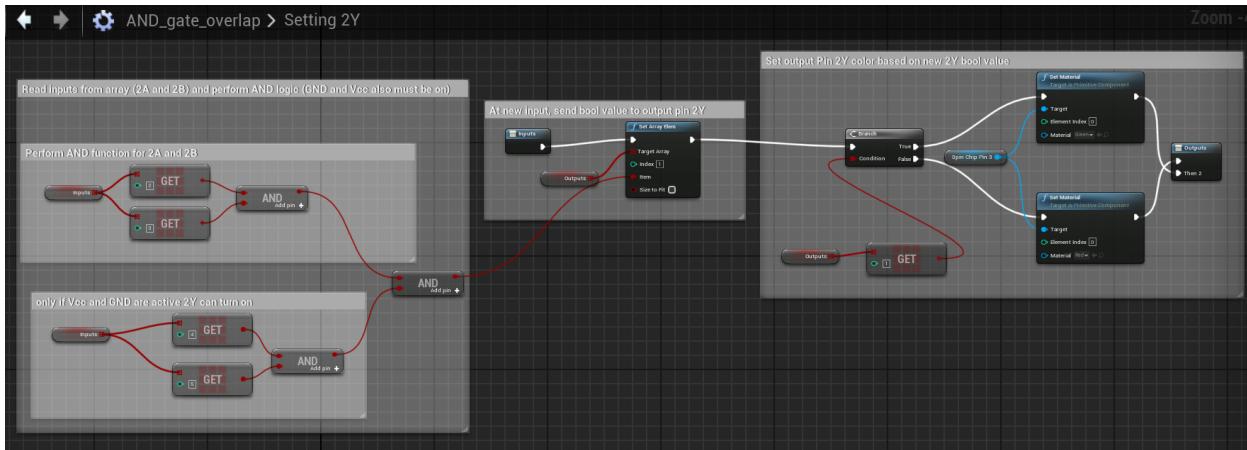
Reading GND (same for all overlap chips) (different from rest of Read Macros because it NOTs wire input)



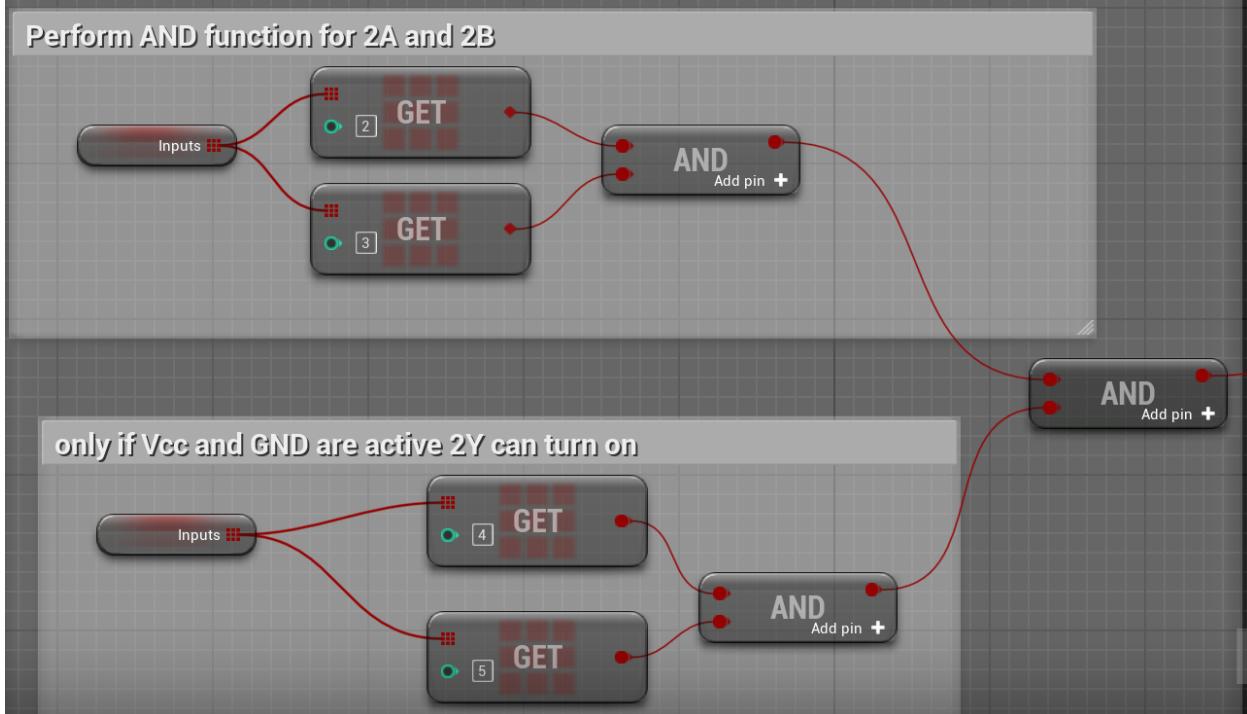
AND Setting 1Y. Setting 1Y same as Setting 2Y except for Index values and Set material pin Target



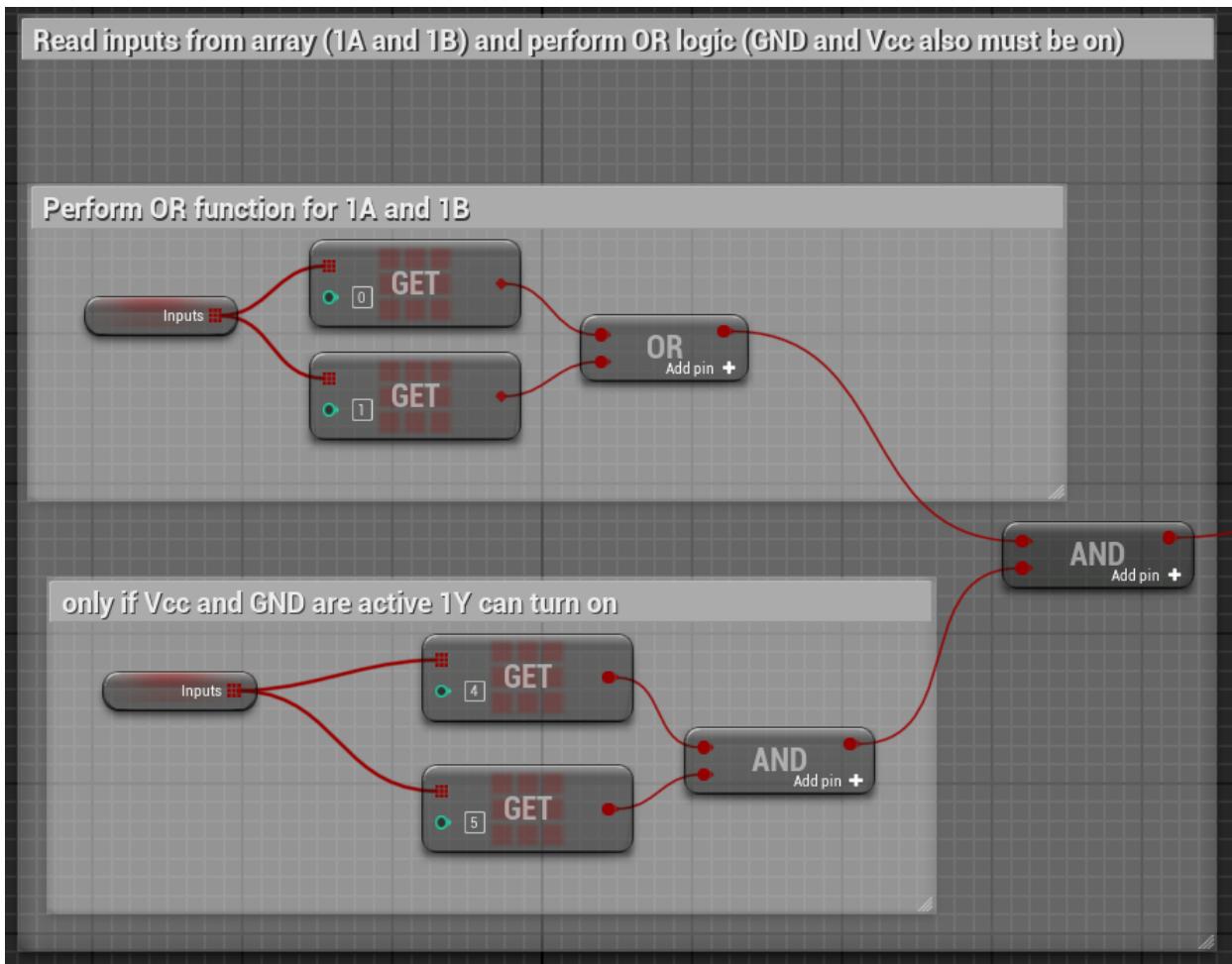
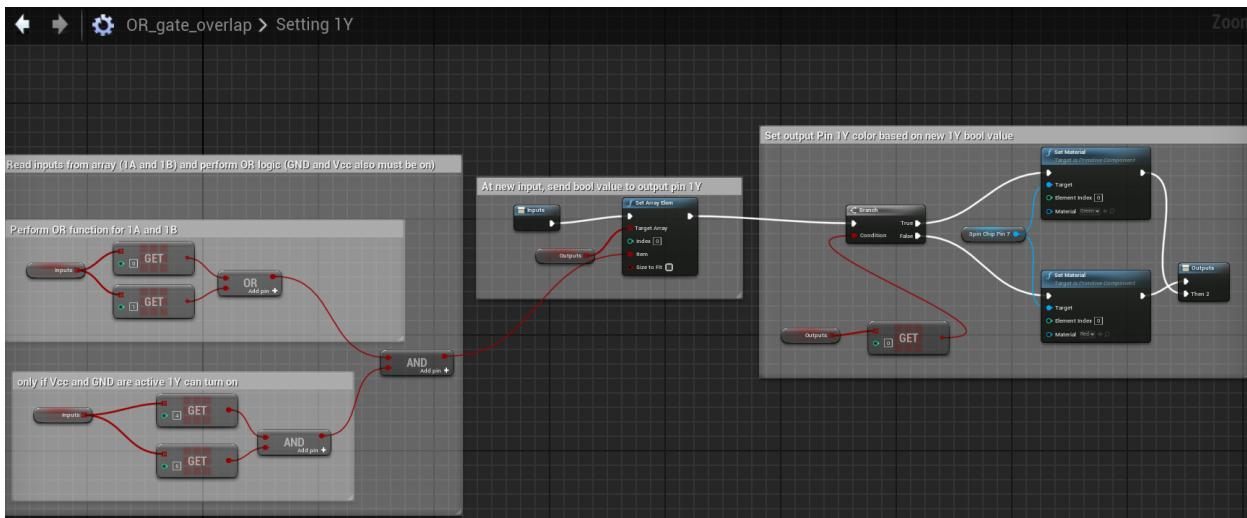
AND Setting 2Y



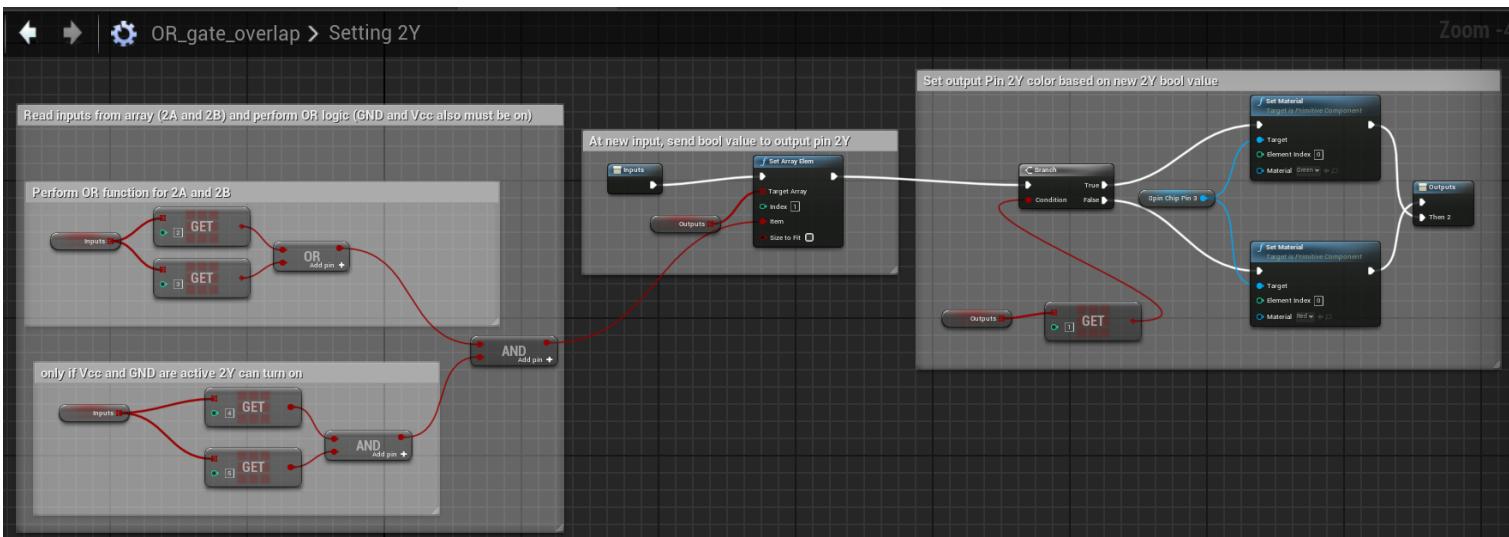
AND 2Y performing Boolean function



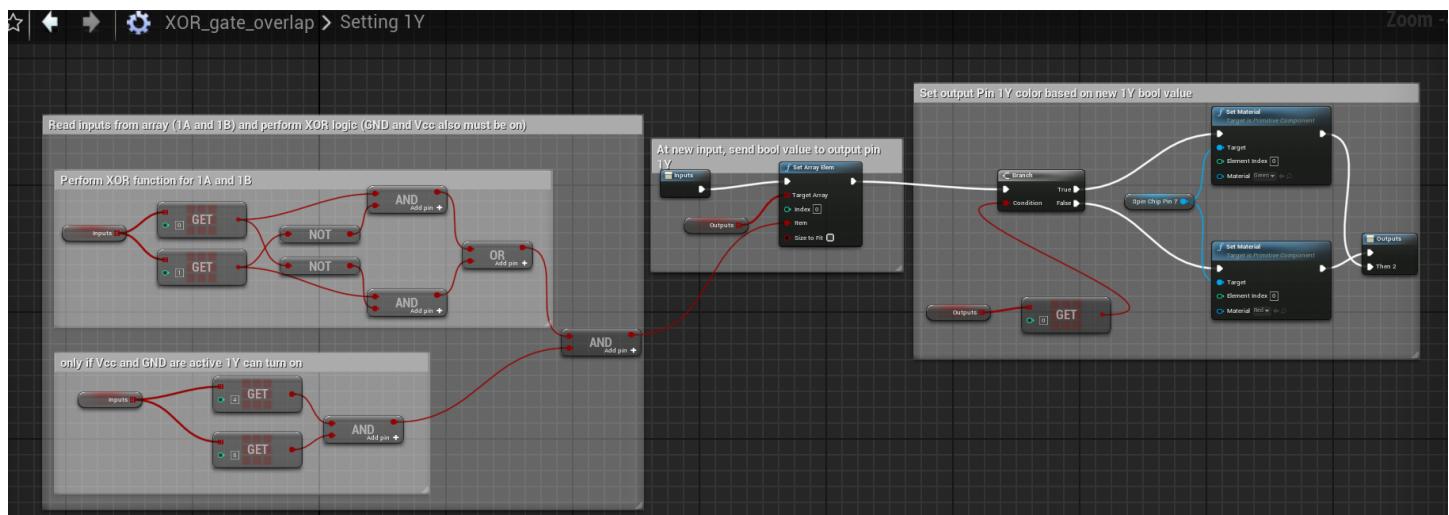
OR Setting 1Y



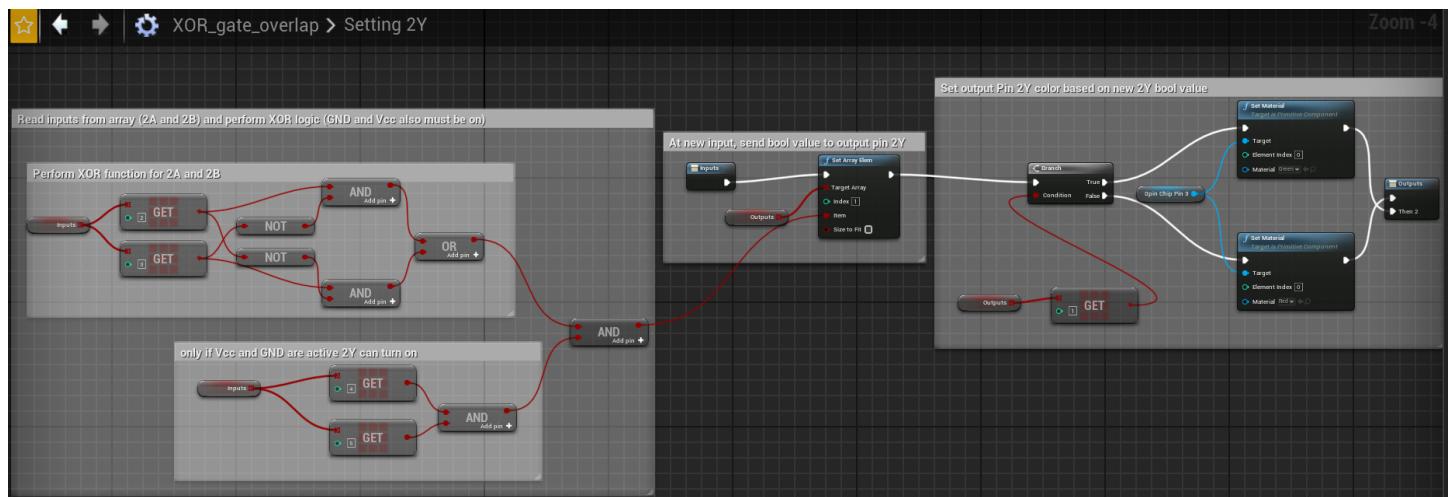
OR Setting 2Y



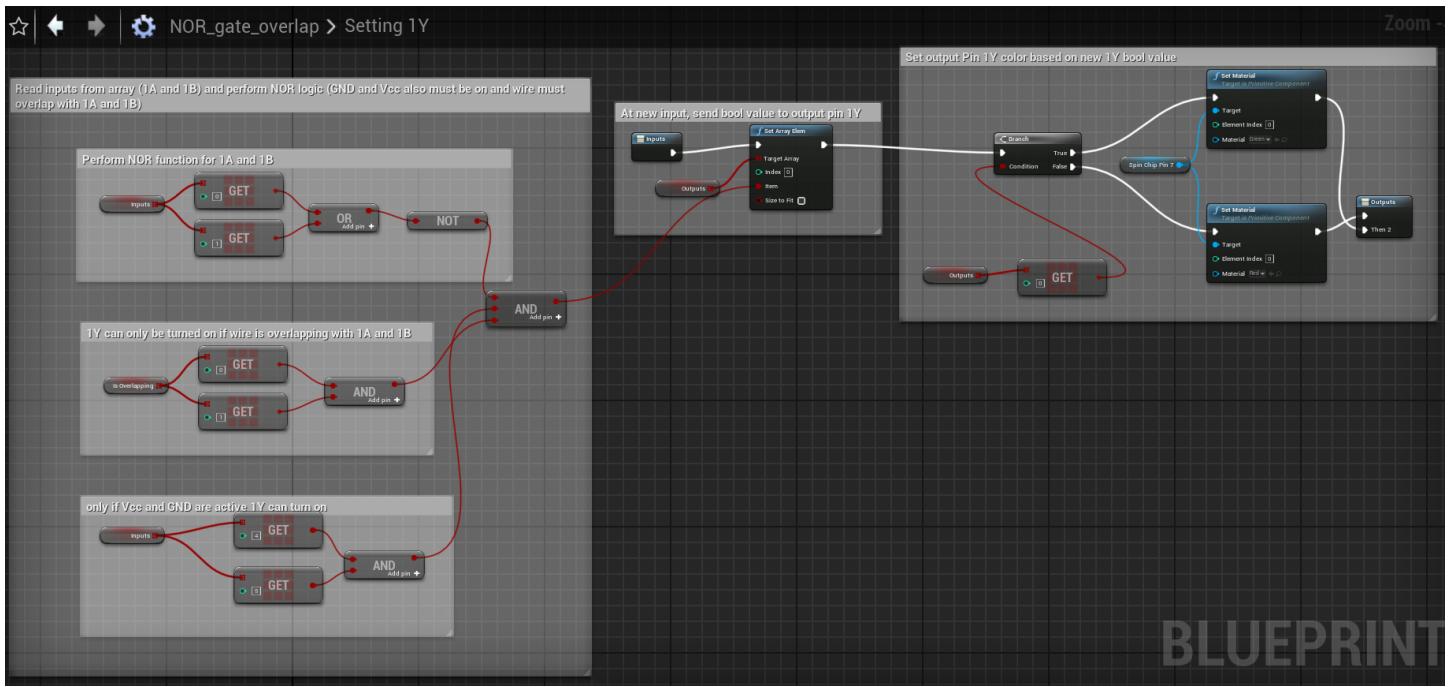
XOR Setting 1Y



XOR Setting 2Y

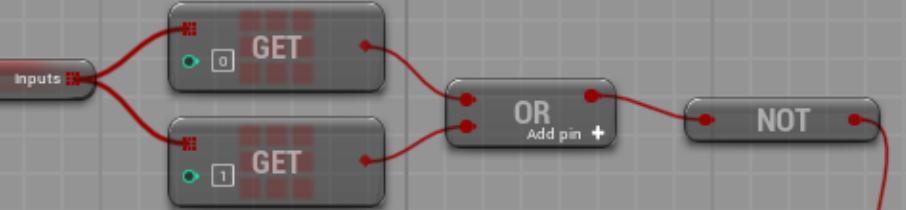


NOR Setting 1Y



Read inputs from array (1A and 1B) and perform NOR logic (GND and Vcc also must be on and wire must overlap with 1A and 1B)

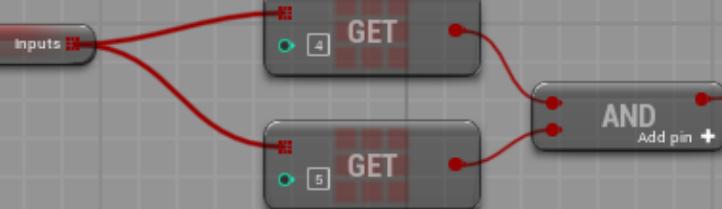
Perform NOR function for 1A and 1B



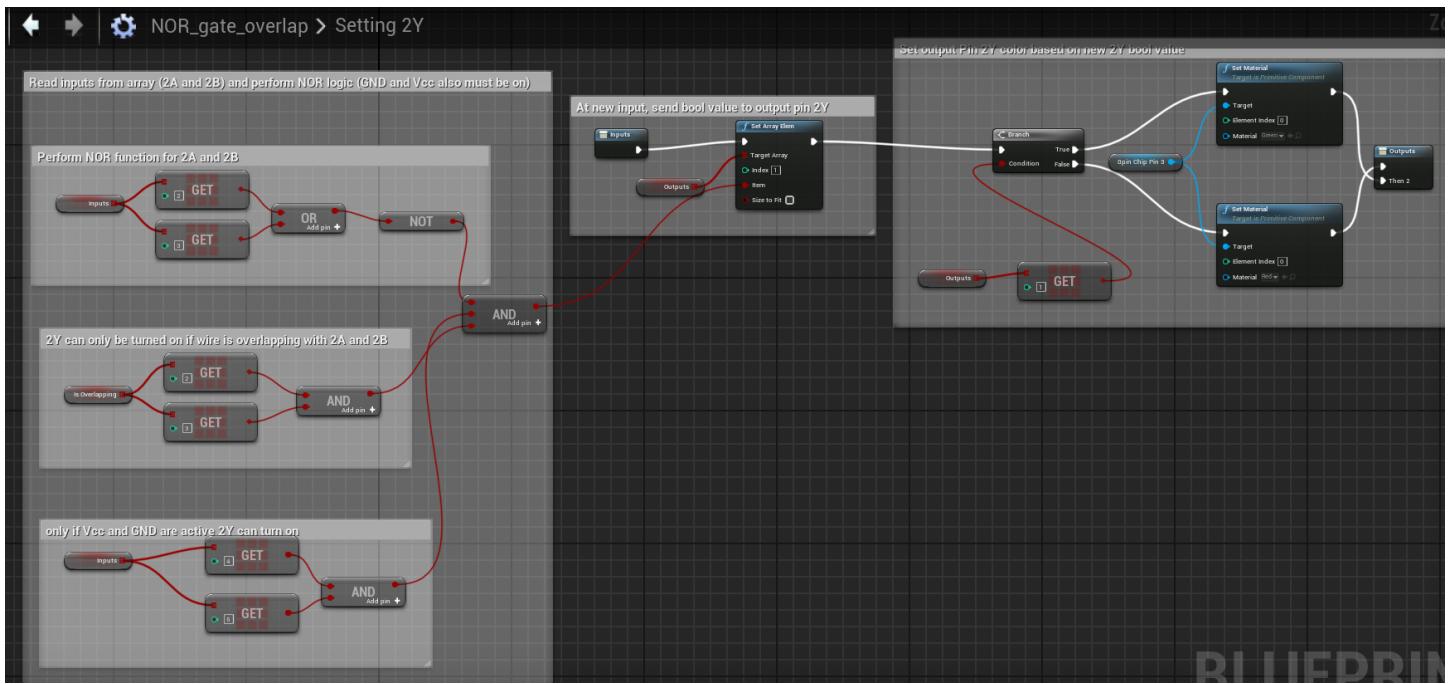
1Y can only be turned on if wire is overlapping with 1A and 1B



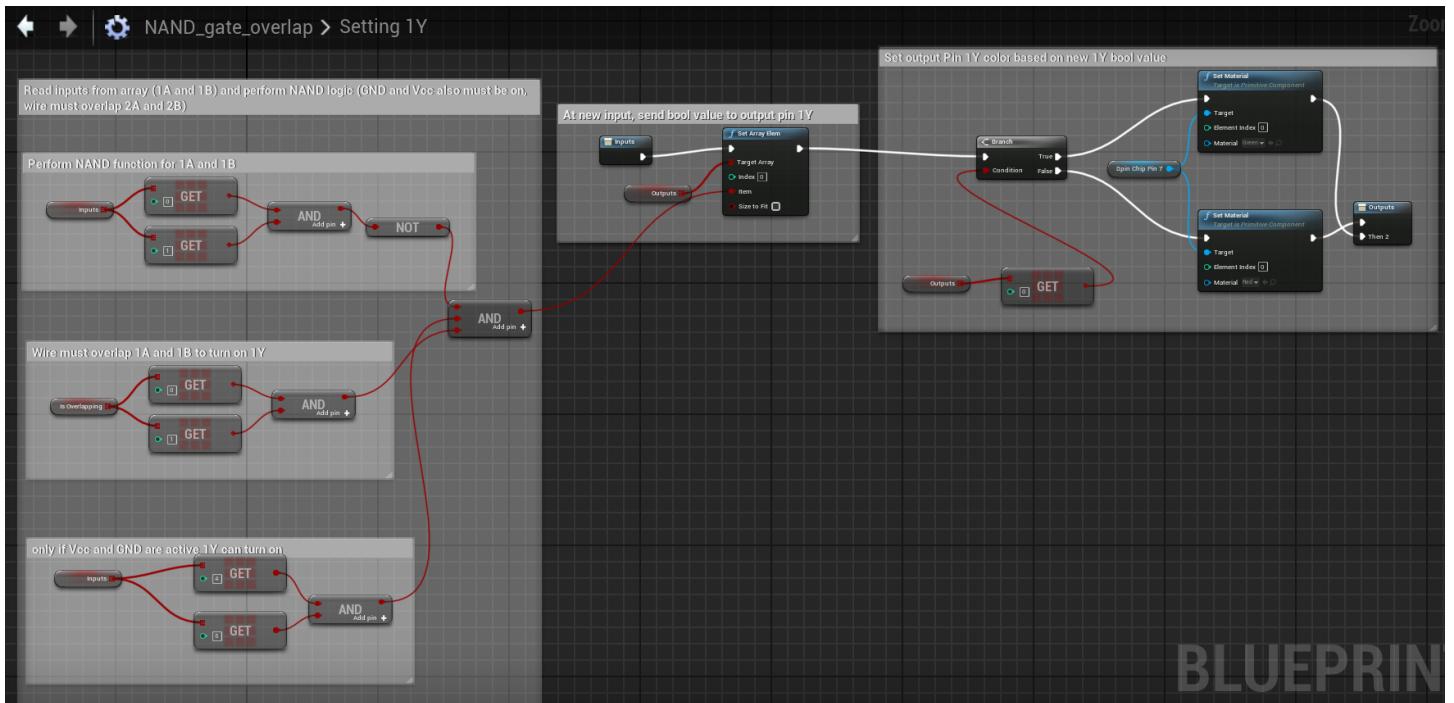
only if Vcc and GND are active 1Y can turn on



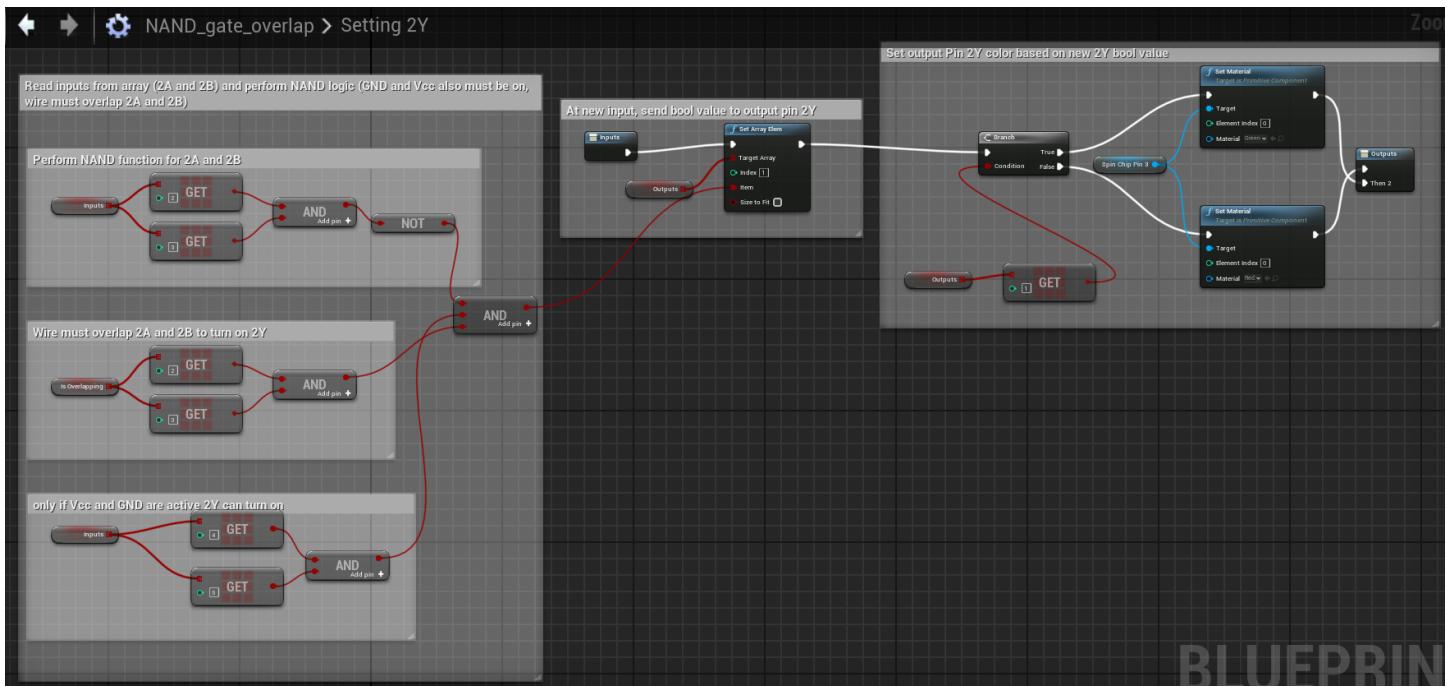
NOR Setting 2Y



NAND Setting 1Y



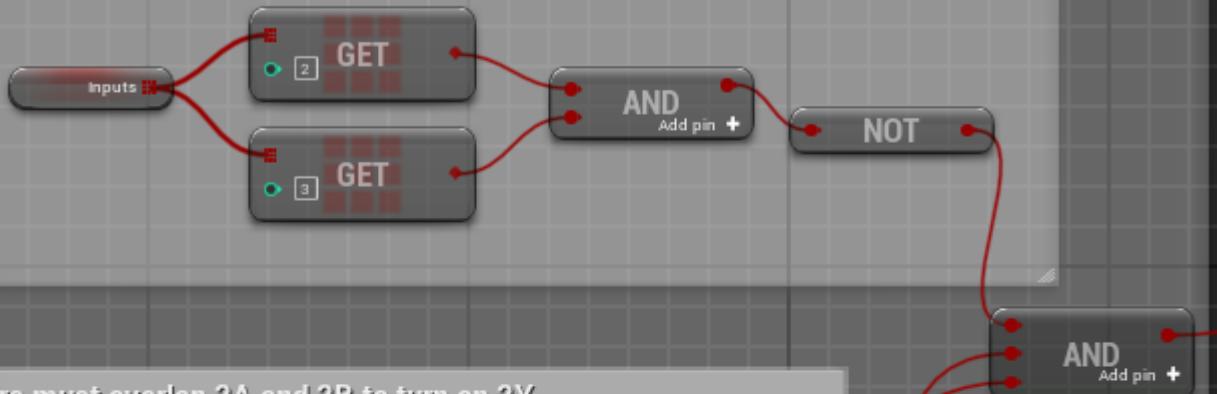
NAND Setting 2Y



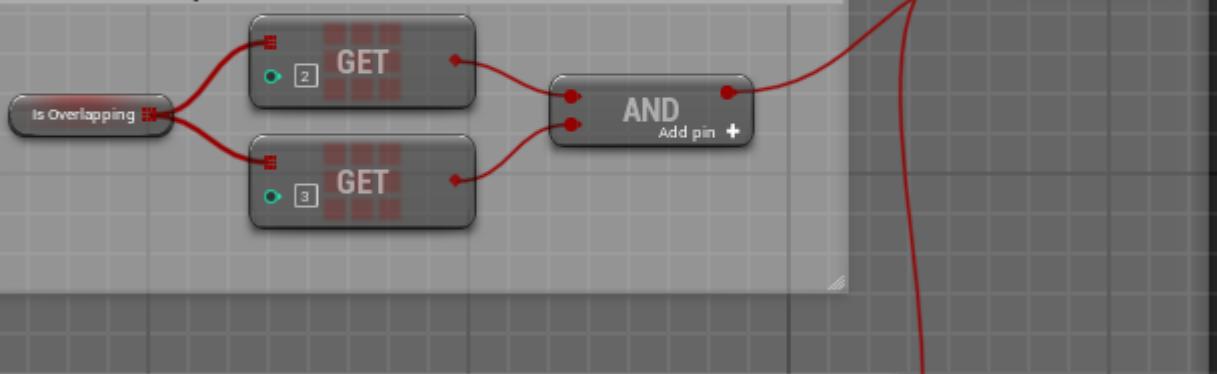
BI UFPRI

Read inputs from array (2A and 2B) and perform NAND logic (GND and Vcc also must be on, wire must overlap 2A and 2B)

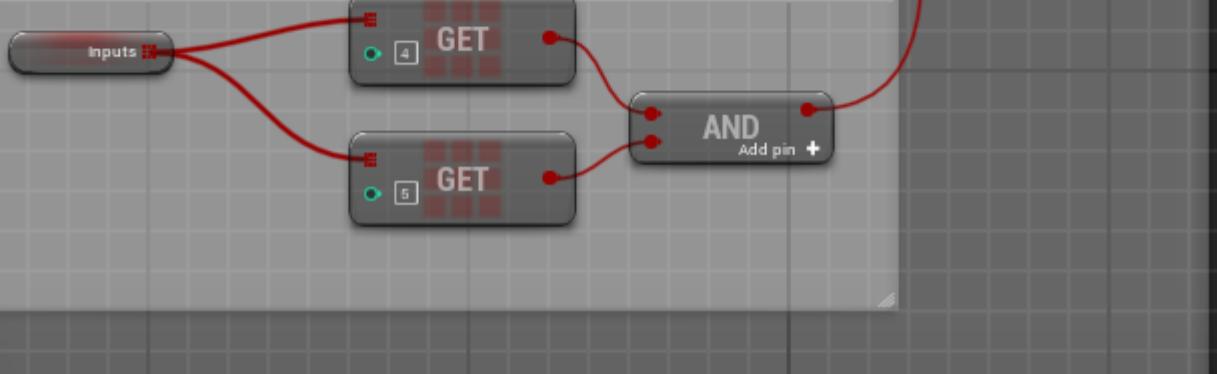
Perform NAND function for 2A and 2B



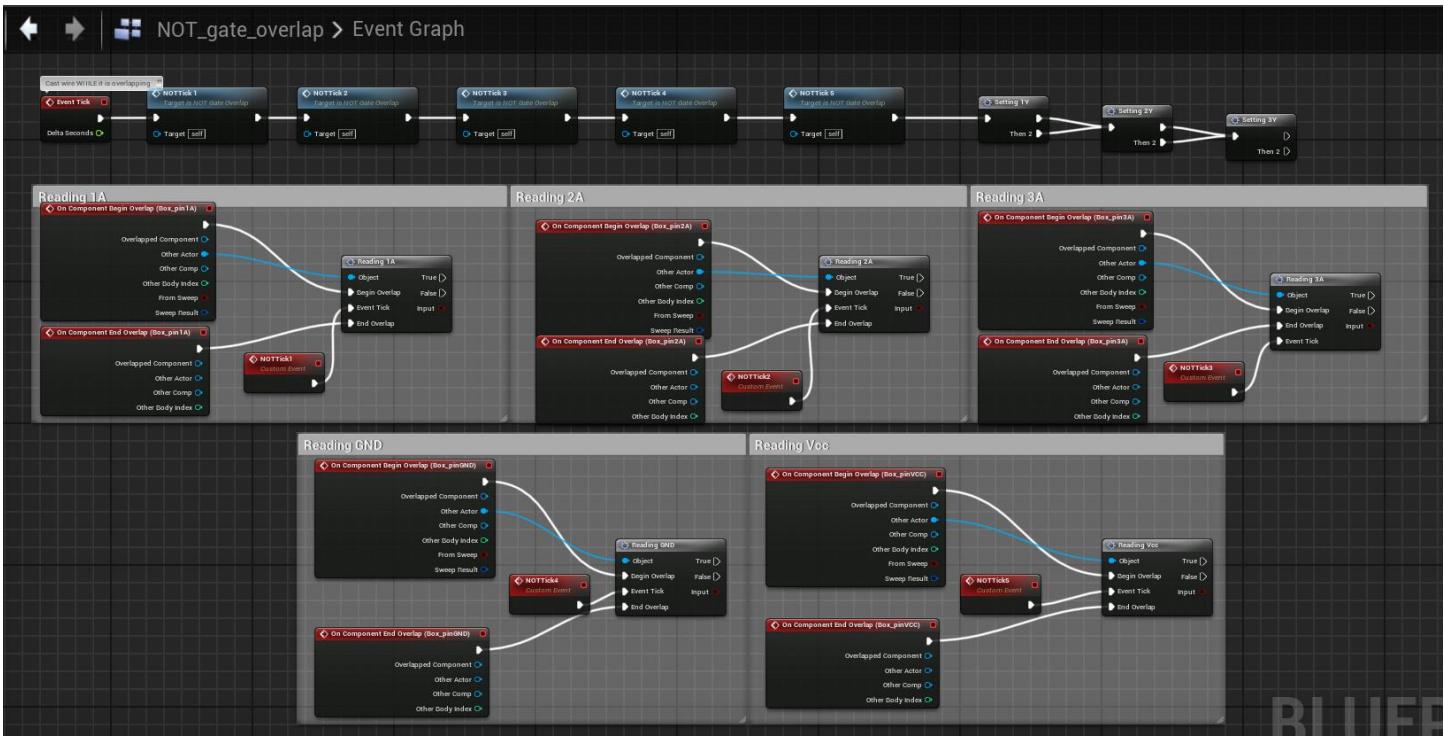
Wire must overlap 2A and 2B to turn on 2Y



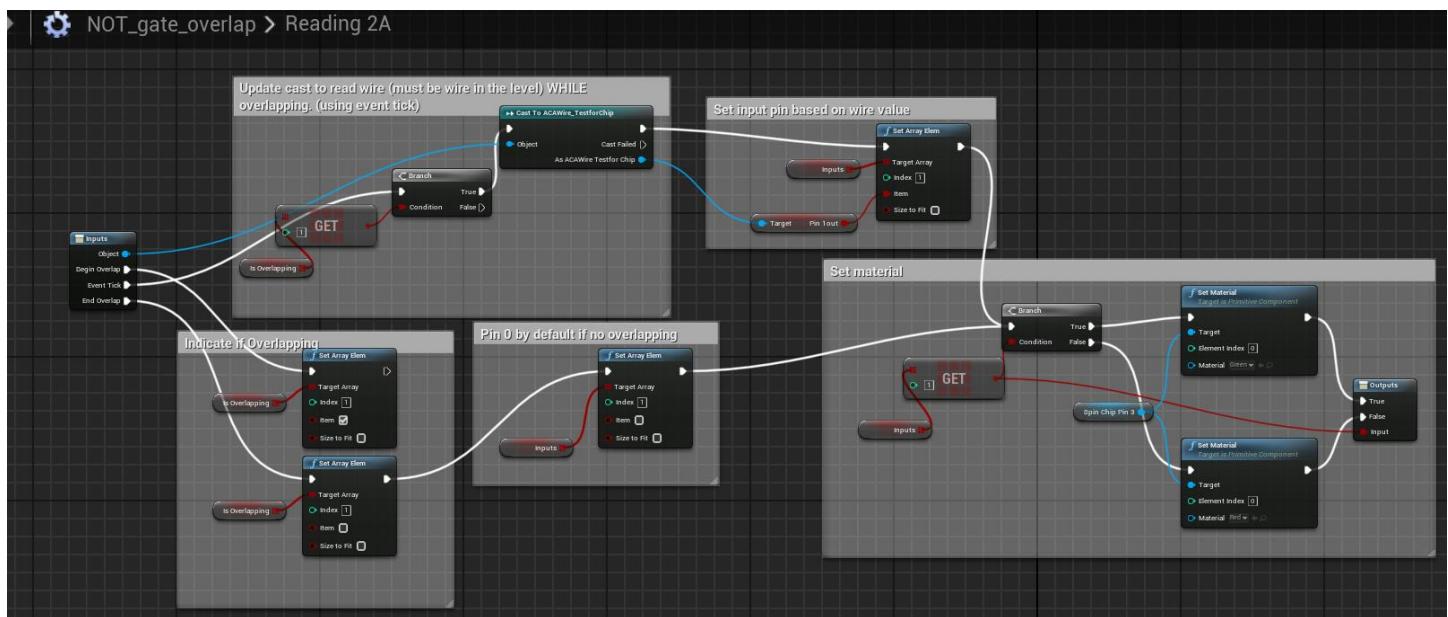
only if Vcc and GND are active 2Y can turn on



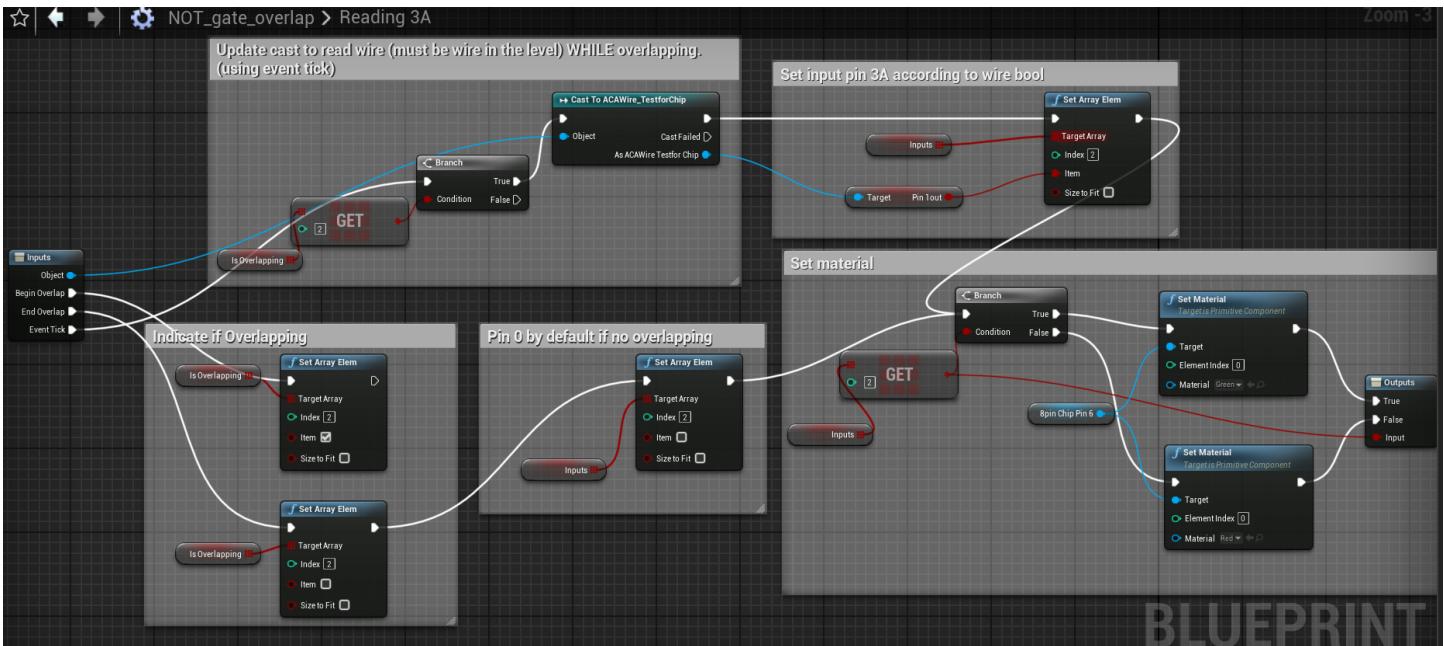
NOT Overlap Ship Event Graph



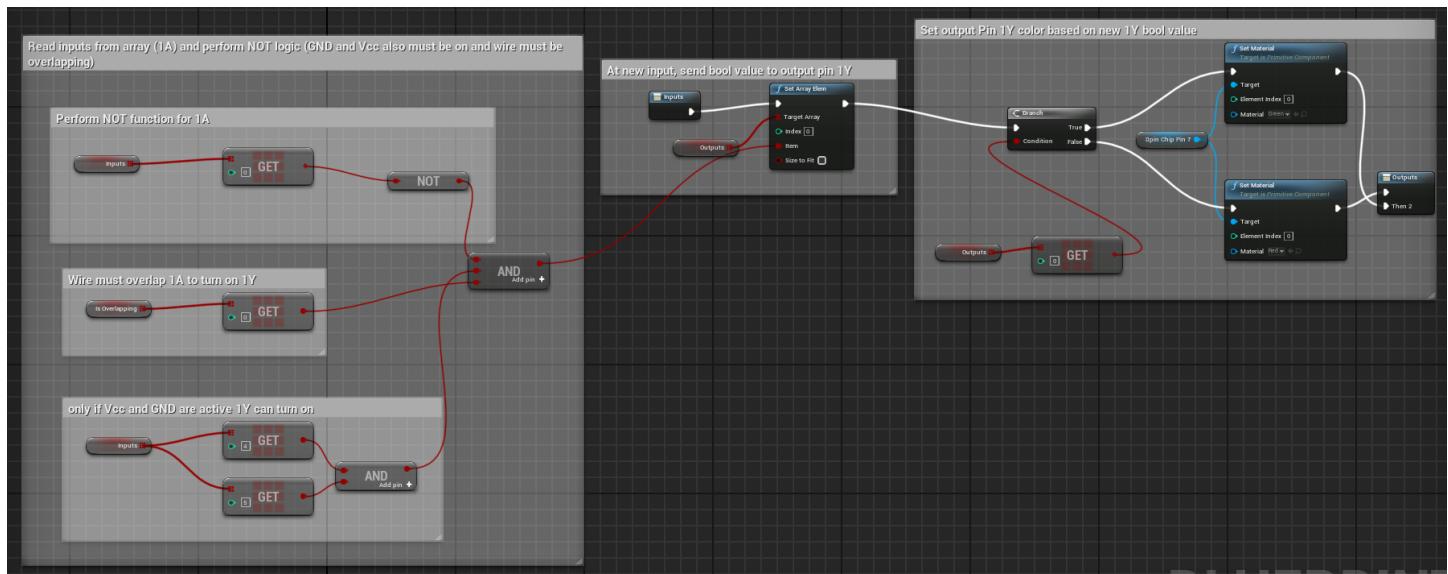
NOT Reading 2A



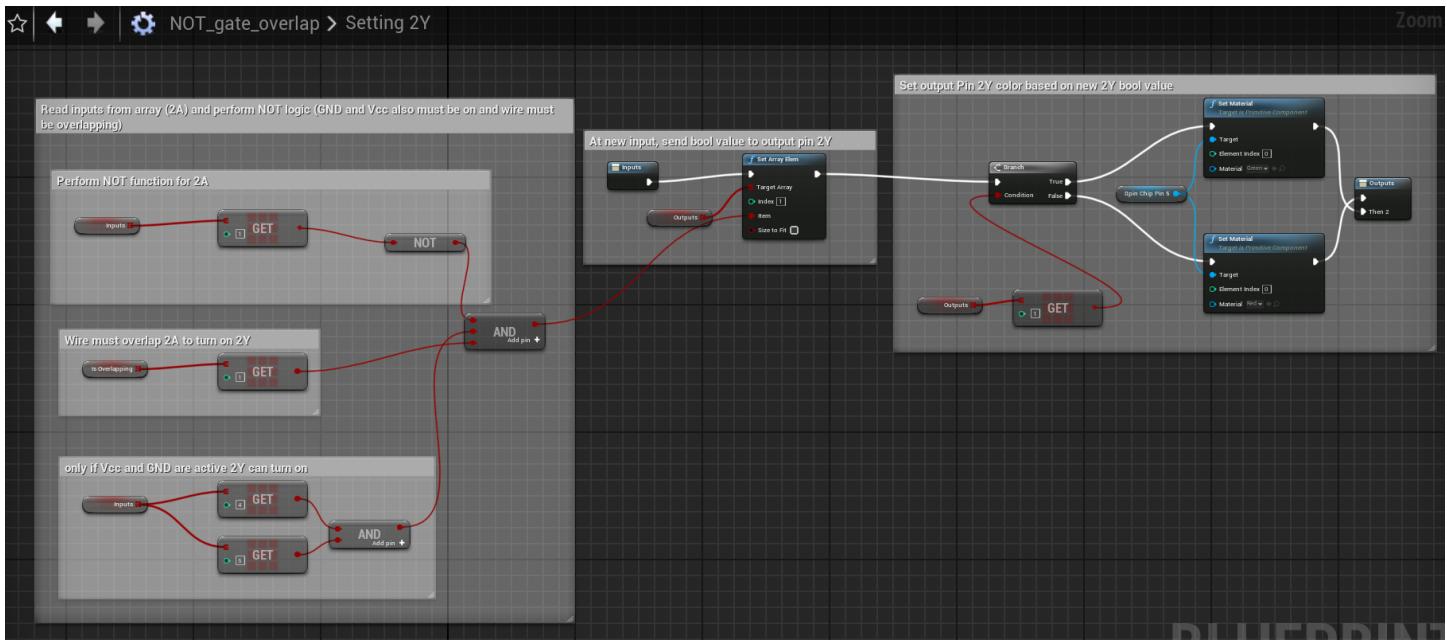
NOT Reading 3A



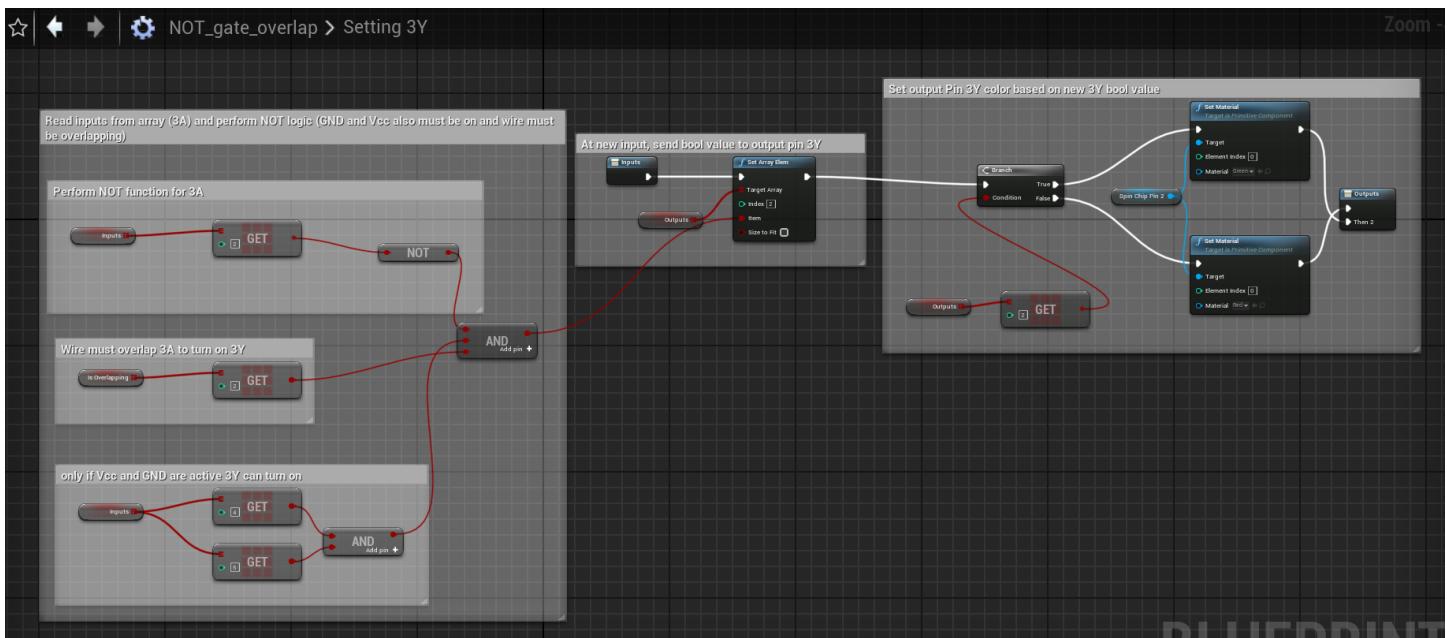
NOT Setting 1Y



NOT Setting 2Y



NOT Setting 3Y



Read inputs from array (3A) and perform NOT logic (GND and Vcc also must be on and wire must be overlapping)

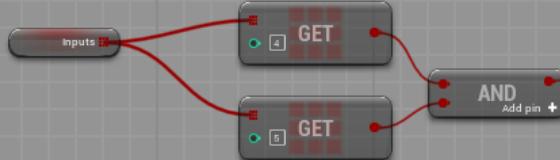
Perform NOT function for 3A



Wire must overlap 3A to turn on 3Y



only if Vcc and GND are active 3Y can turn on



At new input, send bool value to output pin 3Y

