

300MHz to 9GHz High Linearity I/Q Demodulator with Wideband IF Amplifier

FEATURES

- True Zero IF Demodulation
- Wideband Input Matched from 500MHz to 9GHz
- Wide IF Bandwidth: DC to 1GHz (1dB Flatness)
- 37dB Image Rejection, Adjustable to 60dB
- High Total OIP3: 37dBm at 5.8GHz
- 58dBm OIP2 at 5.8GHz, Adjustable to 65dBm
- Max Power Conversion Gain: 9.2dB at 5.8GHz
- Single-Ended RF Input with On-Chip Transformer
- User Adjustable DC Offset Null
- Serial Interface
- IF Amplifier Gain Adjustable in Eight Steps
- IF Amplifier Shutdown/Enable
- Low Power Shutdown Mode
- Operating Temperature Range (T_C): -40°C to 105°C
- 32-Lead 5mm \times 5mm QFN Package

APPLICATIONS

- 5G Base Station Fronthaul/Backhaul Receivers
- Military and Satellite Receivers
- Point-to-Point Broadband Radios
- High Linearity Direct Conversion I/Q SDR
- Test Instrumentation
- DPD Receivers

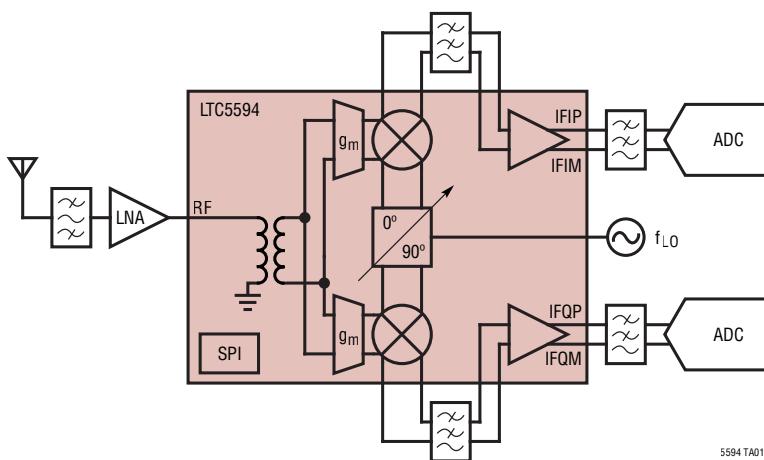
DESCRIPTION

The LTC[®]5594 is a direct conversion quadrature demodulator optimized for high linearity zero-IF and low-IF receiver applications in the 300MHz to 9GHz frequency range. The very wide IF bandwidth of more than 1GHz makes the LTC5594 particularly suited for demodulation of very wideband signals, especially in 5G fronthaul/backhaul receiver applications. The outstanding dynamic range of the LTC5594 makes the device suitable for demanding infrastructure direct conversion applications. Proprietary technology inside the LTC5594 provides the capability to optimize OIP2 to 65dBm, and achieve image rejection better than 60dB. The DC offset control function allows nulling of the DC offset at the A/D converter input, thereby optimizing the dynamic range of true zero-IF receivers that use DC-coupled IF signal paths. The wideband RF and LO input ports make it possible to cover all the major wireless infrastructure frequency bands using a single device. The IF outputs of the LTC5594 are designed to interface directly with most common A/D converter input interfaces. The high OIP3 and high conversion gain of the device eliminate the need for additional amplifiers in the IF signal path.

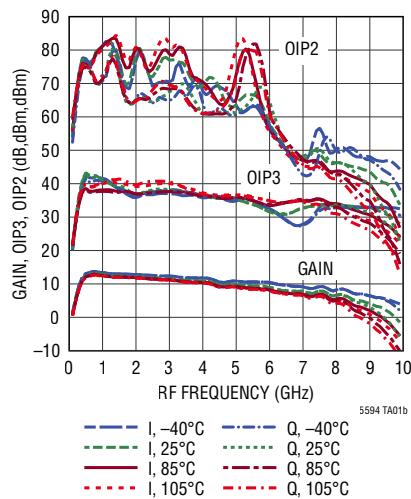
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TYPICAL APPLICATION

Direct Conversion I/Q Receiver



Gain, OIP3, and OIP2 vs Temperature (T_C) (Unoptimized)



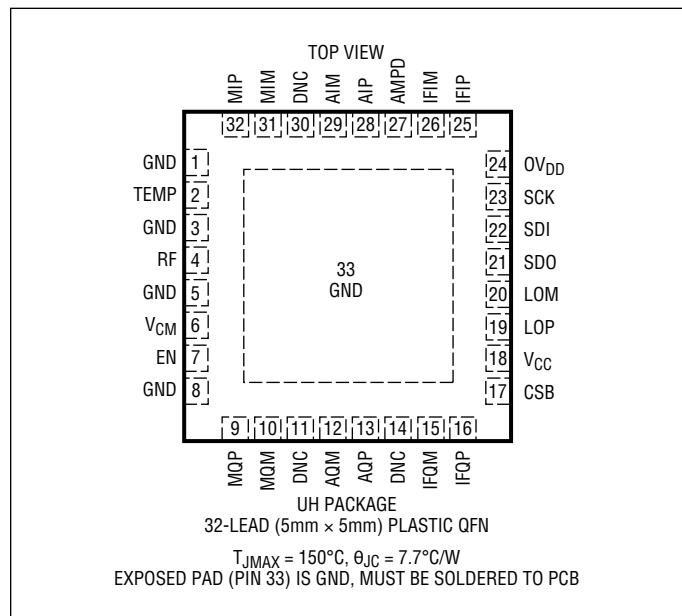
LTC5594

ABSOLUTE MAXIMUM RATINGS

(Note 1)

| | |
|---|--|
| V _{CC} Supply Voltage (Note 23) | -0.3V to 5.5V |
| O _{VDD} , SDO Voltage (Note 20) | -0.3V to 3.8V |
| RF DC Voltage | 1.5V to 2.0V |
| LOP, LOM DC Voltage | 2.1V to 2.8V |
| IFIM, IFIP, IFQP, IFQM DC Voltage | -0.3V to 3.5V |
| AIM, AIP, AQM, AQP | |
| DC Voltage | V _{CC} - 1.7V to V _{CC} - 1.2V |
| MIM, MIP, MQM, MQP | |
| DC Voltage | V _{CC} - 1.7V to V _{CC} - 1.2V |
| Voltage on Any Other Pin | -0.3V to 5.5V |
| LOP, LOM, RF Input Power (Note 19) | +20dBm |
| Output Short Circuit Duration (Notes 16, 19) ... | Indefinite |
| Maximum Junction Temperature (T _{JMAX}) | 150°C |
| Case Operating Temperature | |
| Range (T _C) | -40°C to 105°C |
| Storage Temperature Range | -65°C to 150°C |

PIN CONFIGURATION



ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|------------------|------------------|--------------|---------------------------------|-------------------|
| LTC5594IUH#PBF | LTC5594IUH#TRPBF | 5594 | 32-Lead (5mm x 5mm) Plastic QFN | -40°C to 105°C |

Consult ADI Marketing for parts specified with wider operating temperature ranges.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

$T_C = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$, $OV_{DD} = EN = CSB = 3.3\text{V}$, $SDI = SCK = AMPD = 0\text{V}$,
 $V_{CM} = 0.9\text{V}$, $P_{IF} = 1.5\text{dBm}$ (-1.5dBm/tone for 2-tone tests), $P_{LO} = 6\text{dBm}$, all registers at default values, and all parameters listed for combined performance of demodulator and amplifier unless otherwise noted. (Notes 2, 3, 6, 9, 21, 24)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|-----------------|---|--|-----|------------|-----|-------|
| $f_{RF(RANGE)}$ | RF Input Frequency Range | (Note 12) | | 0.3 to 9.0 | | GHz |
| $f_{LO(RANGE)}$ | LO Input Frequency Range | (Note 12) | | 0.3 to 9.0 | | GHz |
| BW_{IF} | IF Output Bandwidth | -1dB Corner Frequency (Note 22) | | 1.0 | | GHz |
| RL_{RF} | RF Input Return Loss (Note 5) | $f_{RF} = 300\text{MHz}$ to 500MHz $f_{RF} = 500\text{MHz}$ to 9.0GHz | | >10 | | dB |
| RL_{LO} | LO Input Return Loss | $f_{LO} = 300\text{MHz}$ to 9.0GHz | | >10 | | dB |
| $P_{LO(RANGE)}$ | LO Input Power Range | (Note 12) | | -6 to 12 | | dBm |
| G_P | Power Conversion Gain AMPG = 0x06, $R_{LOAD} = 100\Omega$ Differential (Note 8) | $f_{RF} = 400\text{MHz}$ | | 11.5 | | dB |
| | | $f_{RF} = 1900\text{MHz}$ | | 12.3 | | dB |
| | | $f_{RF} = 3500\text{MHz}$ | | 11.0 | | dB |
| | | $f_{RF} = 5800\text{MHz}$ | | 9.2 | | dB |
| | | $f_{RF} = 7200\text{MHz}$ | | 7.0 | | dB |
| | | $f_{RF} = 8500\text{MHz}$ | | 5.2 | | dB |
| NF | Noise Figure, Double Side Band (Note 4) | $f_{RF} = 400\text{MHz}$ | | 15.7 | | dB |
| | | $f_{RF} = 1900\text{MHz}$ | | 16.0 | | dB |
| | | $f_{RF} = 3500\text{MHz}$ | | 17.9 | | dB |
| | | $f_{RF} = 5800\text{MHz}$ | | 21.2 | | dB |
| | | $f_{RF} = 7200\text{MHz}$ | | 23.5 | | dB |
| | | $f_{RF} = 8500\text{MHz}$ | | 28.6 | | dB |
| $NF_{BLOCKING}$ | Noise Figure Under Blocking Conditions Double Side Band, $P_{IF, BLOCKER} = 1.5\text{dBm}$ (Note 7) | $f_{RF} = 400\text{MHz}$ | | 16.7 | | dB |
| | | $f_{RF} = 1900\text{MHz}$ | | 17.0 | | dB |
| | | $f_{RF} = 3500\text{MHz}$ | | 18.9 | | dB |
| | | $f_{RF} = 5800\text{MHz}$ | | 22.2 | | dB |
| | | $f_{RF} = 7200\text{MHz}$ | | 24.5 | | dB |
| | | $f_{RF} = 8500\text{MHz}$ | | 29.6 | | dB |
| OIP3 | Output 3rd Order Intercept Unadjusted/Adjusted | $f_{RF} = 400\text{MHz}$ | | 40/44 | | dBm |
| | | $f_{RF} = 1900\text{MHz}$ | | 37/43 | | dBm |
| | | $f_{RF} = 3500\text{MHz}$ | | 37/42 | | dBm |
| | | $f_{RF} = 5800\text{MHz}$ | | 37/40 | | dBm |
| | | $f_{RF} = 7200\text{MHz}$ | | 33/38 | | dBm |
| | | $f_{RF} = 8500\text{MHz}$ | | 33/35 | | dBm |
| OIP2 | Output 2nd Order Intercept Unadjusted/Adjusted | $f_{RF} = 400\text{MHz}$ | | 75/80 | | dBm |
| | | $f_{RF} = 1900\text{MHz}$ | | 68/75 | | dBm |
| | | $f_{RF} = 3500\text{MHz}$ | | 68/70 | | dBm |
| | | $f_{RF} = 5800\text{MHz}$ | | 58/65 | | dBm |
| | | $f_{RF} = 7200\text{MHz}$ | | 48/55 | | dBm |
| | | $f_{RF} = 8500\text{MHz}$ | | 43/48 | | dBm |
| $IIP3_{DEMOD}$ | Input 3rd Order Intercept without Amplifier Unadjusted | $f_{RF} = 400\text{MHz}$ | | 30 | | dBm |
| | | $f_{RF} = 1900\text{MHz}$ | | 26 | | dBm |
| | | $f_{RF} = 3500\text{MHz}$ | | 27 | | dBm |
| | | $f_{RF} = 5800\text{MHz}$ | | 24 | | dBm |
| | | $f_{RF} = 7200\text{MHz}$ | | 24 | | dBm |
| | | $f_{RF} = 8500\text{MHz}$ | | 27 | | dBm |
| $OIP3_{AMP}$ | Output 3rd Order Intercept, Amplifier Only (Note 17) | $f_{IF} = 10\text{MHz}$ | | 42 | | dBm |
| | | $f_{IF} = 100\text{MHz}$ | | 41 | | dBm |
| | | $f_{IF} = 200\text{MHz}$ | | 38 | | dBm |
| | | $f_{IF} = 300\text{MHz}$ | | 37 | | dBm |
| | | $f_{IF} = 500\text{MHz}$ | | 35 | | dBm |
| | | $f_{IF} = 1000\text{MHz}$ | | 30 | | dBm |

ELECTRICAL CHARACTERISTICS

$T_C = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$, $OV_{DD} = EN = CSB = 3.3\text{V}$, $SDI = SCK = AMPD = 0\text{V}$, $V_{CM} = 0.9\text{V}$, $P_{IF} = 1.5\text{dBm}$ ($-1.5\text{dBm}/\text{tone}$ for 2-tone tests), $P_{LO} = 6\text{dBm}$, all registers at default values, and all parameters listed for combined performance of demodulator and amplifier unless otherwise noted. (Notes 2, 3, 6, 9, 21, 24)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------|---|---|--|-----|-----|--|
| HD2 | 2nd Order Harmonic Distortion Unadjusted/Adjusted | $f_{RF} = 400\text{MHz}$ $f_{RF} = 1900\text{MHz}$ $f_{RF} = 3500\text{MHz}$ $f_{RF} = 5800\text{MHz}$ $f_{RF} = 7200\text{MHz}$ $f_{RF} = 8500\text{MHz}$ | -65 -64 -60 -56 -50 -46 | | | dBc dBc dBc dBc dBc dBc |
| HD3 | 3rd Order Harmonic Distortion Unadjusted/Adjusted | $f_{RF} = 400\text{MHz}$ $f_{RF} = 1900\text{MHz}$ $f_{RF} = 3500\text{MHz}$ $f_{RF} = 5800\text{MHz}$ $f_{RF} = 7200\text{MHz}$ $f_{RF} = 8500\text{MHz}$ | -82 -80 -76 -70 -65 -68 | | | dBc dBc dBc dBc dBc dBc |
| P1dB | Output 1dB Compression Point | $f_{RF} = 400\text{MHz}$ $f_{RF} = 1900\text{MHz}$ $f_{RF} = 3500\text{MHz}$ $f_{RF} = 5800\text{MHz}$ $f_{RF} = 7200\text{MHz}$ $f_{RF} = 8500\text{MHz}$ | 13.2 13.2 13.2 13.2 13.2 13.2 | | | dBm dBm dBm dBm dBm dBm |
| DC _{OFFSET} | DC Offset, Unadjusted (Note 13) | $f_{RF} = 400\text{MHz}$ $f_{RF} = 1900\text{MHz}$ $f_{RF} = 3500\text{MHz}$ $f_{RF} = 5800\text{MHz}$ $f_{RF} = 7200\text{MHz}$ $f_{RF} = 8500\text{MHz}$ | 19 17 17 -26 -63 -19 | | | mV mV mV mV mV mV |
| DC _{OFF(RANGE)} | DC Offset Adjustment Range | DCOI, DCOQ = 0x00 to 0xFF | -75 to 75 | | | mV |
| DC _{OFF(STEP)} | DC Offset Step Size | | 640 | | | μV |
| ΔG | I/Q Gain Mismatch, Unadjusted | $f_{RF} = 400\text{MHz}$ $f_{RF} = 1900\text{MHz}$ $f_{RF} = 3500\text{MHz}$ $f_{RF} = 5800\text{MHz}$ $f_{RF} = 7200\text{MHz}$ $f_{RF} = 8500\text{MHz}$ | 0.05 0.05 0.06 0.06 0.07 0.44 | | | dB dB dB dB dB dB |
| ΔG _(RANGE) | I/Q Gain Mismatch Adjustment Range | GERR = 0x00 to 0x3F | -0.5 to 0.5 | | | dB |
| ΔG _(STEP) | I/Q Gain Mismatch Adjustment Step Size | | 0.016 | | | dB |
| Δϕ | I/Q Phase Mismatch, Unadjusted | $f_{RF} = 400\text{MHz}$ $f_{RF} = 1900\text{MHz}$ $f_{RF} = 3500\text{MHz}$ $f_{RF} = 5800\text{MHz}$ $f_{RF} = 7200\text{MHz}$ $f_{RF} = 8500\text{MHz}$ | 0.9 1.1 3.1 1.6 1.1 1.0 | | | Deg Deg Deg Deg Deg Deg |
| Δϕ _(RANGE) | I/Q Phase Mismatch Adjustment Range | PHA = 0x000 to 0x1FF | -2.5 to 2.5 | | | Deg |
| Δϕ _(STEP) | I/Q Phase Mismatch Adjustment Step Size | | 0.05 | | | Deg |
| IRR | Image Rejection Ratio Unadjusted/Adjusted (Note 10) | $f_{RF} = 400\text{MHz}$ $f_{RF} = 1900\text{MHz}$ $f_{RF} = 3500\text{MHz}$ $f_{RF} = 5800\text{MHz}$ $f_{RF} = 7200\text{MHz}$ $f_{RF} = 8500\text{MHz}$ | 43/70 42/65 33/65 37/60 40/60 33/60 | | | dB dB dB dB dB dB |

ELECTRICAL CHARACTERISTICS

$T_C = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$, $0V_{DD} = EN = CSB = 3.3\text{V}$, $SDI = SCK = AMPD = 0\text{V}$,
 $V_{CM} = 0.9\text{V}$, $P_{IF} = 1.5\text{dBm}$ (-1.5dBm/tone for 2-tone tests), $P_{LO} = 6\text{dBm}$, all registers at default values, and all parameters listed for combined performance of demodulator and amplifier unless otherwise noted. (Notes 2, 3, 6, 9, 21, 24)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------|------------------------------|---|--|-----|-----|-------|
| L_{LEAK} | LO to RF Leakage | $f_{LO} = 400\text{MHz}$ $f_{LO} = 1900\text{MHz}$ $f_{LO} = 3500\text{MHz}$ $f_{LO} = 5800\text{MHz}$ $f_{LO} = 7200\text{MHz}$ $f_{LO} = 8500\text{MHz}$ | -67 -65 -56 -52 -50 -55 | | | dBm |
| R_{LISO} | RF to LO Isolation | $f_{RF} = 400\text{MHz}$ $f_{RF} = 1900\text{MHz}$ $f_{RF} = 3500\text{MHz}$ $f_{RF} = 5800\text{MHz}$ $f_{RF} = 7200\text{MHz}$ $f_{RF} = 8500\text{MHz}$ | 69 57 66 55 57 53 | | | dB |
| R_{IISO} | RF to IF Isolation (Note 18) | $f_{RF} = 400\text{MHz}$ $f_{RF} = 1900\text{MHz}$ $f_{RF} = 3500\text{MHz}$ $f_{RF} = 5800\text{MHz}$ $f_{RF} = 7200\text{MHz}$ $f_{RF} = 8500\text{MHz}$ | 70 48 59 48 40 43 | | | dB |
| L_{IISO} | LO to IF Isolation (Note 18) | $f_{LO} = 400\text{MHz}$ $f_{LO} = 1900\text{MHz}$ $f_{LO} = 3500\text{MHz}$ $f_{LO} = 5800\text{MHz}$ $f_{LO} = 7200\text{MHz}$ $f_{LO} = 8500\text{MHz}$ | 40 29 38 36 33 35 | | | dB |

Power Supply and Other Parameters

| | | | | | | |
|-----------------|---|---|-----------------|-----------------|------|-----------------------------|
| V_{CC} | Supply Voltage | | 4.75 | 5.0 | 5.25 | V |
| I_{CC} | Supply Current | | 450 | 470 | 500 | mA |
| $I_{CC(MIX)}$ | Mixer Supply Current | Amplifier Disabled, $AMPD = 3.3\text{V}$ | 230 | 250 | 270 | mA |
| $I_{CC(OFF)}$ | Shutdown Current | $EN < 0.3\text{V}$ | 20 | 900 | | μA |
| $I_{CC(SLEEP)}$ | Sleep Current | $EDEM = EDC = EADJ = EAMP = 0$ | 4 | | | mA |
| t_{ON} | Turn-On Time (Note 14) | EN Transition from Logic Low to High | 1 | | | μs |
| t_{OFF} | Turn-Off Time (Note 15) | EN Transition from Logic High to Low | 1 | | | μs |
| OV_{DD} | Digital I/O Supply Voltage | | | 1.2 to 3.3 | | V |
| V_{DH} | EN Input High Voltage (On) | | 0.7 • OV_{DD} | | | V |
| V_{DL} | EN Input Low Voltage (Off) | | | 0.3 • OV_{DD} | | V |
| I_{EN} | EN Pin Input Current | $EN = 3.3\text{V}$ | 41 | | | μA |
| V_{TEMP} | TEMP Diode Bias Voltage | $I_{TEMP} = 100\mu\text{A}$ into TEMP Pin, $T_J = 25^\circ\text{C}$ | 0.774 | | | V |
| | TEMP Diode Temperature Slope | $I_{TEMP} = 100\mu\text{A}$ into TEMP Pin | -1.52 | | | $\text{mV}/^\circ\text{C}$ |
| $Z_{MIX(OUT)}$ | Mixer Output Impedance | Differential | 100 0.6 | | | ΩpF |
| $V_{MIX(OUT)}$ | Mixer Output DC Voltage | Common Mode | 3.6 | | | V |
| $Z_{AMP(IN)}$ | Amplifier Input Impedance | Differential | 200 0.2 | | | ΩpF |
| $V_{AMP(IN)}$ | Amplifier DC Input Voltage | Common Mode | 3.6 | | | V |
| $Z_{AMP(OUT)}$ | Amplifier Output Impedance | Differential | 4 0.5 | | | $\text{k}\Omega \text{pF}$ |
| $I_{AMP(SC)}$ | Amplifier DC Output Short Circuit Current | $IFIP = IFIM = IFQP = IFQM = 0\text{V}$ | 100 | | | mA |
| $V_{CM(RANGE)}$ | V_{CM} Pin Voltage Range (Notes 11, 12) | | 0.5 to 2.0 | | | V |

ELECTRICAL CHARACTERISTICS

$T_C = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$, $OV_{DD} = EN = CSB = 3.3\text{V}$, $SDI = SCK = AMPD = 0\text{V}$, $V_{CM} = 0.9\text{V}$, $P_{IF} = 1.5\text{dBm}$ ($-1.5\text{dBm}/\text{tone}$ for 2-tone tests), $P_{LO} = 6\text{dBm}$, all registers at default values, and all parameters listed for combined performance of demodulator and amplifier unless otherwise noted. (Notes 2, 3, 6, 9, 21, 24)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------------|---------------------------|--------------------------|-----------------------|-----------------------|-----|---------------|
| Serial Interface Pins | | | | | | |
| V_{IH} | High Level Input Voltage | CSB, SDI, SCK | $0.7 \bullet OV_{DD}$ | | | V |
| V_{IL} | Low Level Input Voltage | CSB, SDI, SCK | | $0.3 \bullet OV_{DD}$ | | V |
| V_{IHYS} | Input Hysteresis Voltage | CSB, SDI, SCK | | 250 | | mV |
| $I_{IN(SER)}$ | Input Current | CSB, SDI, SCK (Note 19) | | | 10 | μA |
| V_{OH} | High Level Output Voltage | SDO, 10mA Current Sink | $0.7 \bullet OV_{DD}$ | | | V |
| V_{OL} | Low Level Output Voltage | SDO, 10mA Current Source | | $0.3 \bullet OV_{DD}$ | | V |

Serial Interface Timing

| | | | | | |
|-----------|-----------------------|---|----|----|----|
| t_{CKH} | SCK High Time | | 25 | | ns |
| t_{CKL} | SCK Low Time | | 25 | | ns |
| t_{CSS} | CSB Setup Time | | 10 | | ns |
| t_{CSH} | CSB High Time | | 10 | | ns |
| t_{DS} | SDI to SCK Setup Time | | 6 | | ns |
| t_{DH} | SDI to SCK Hold Time | | 6 | | ns |
| t_{DO} | SCK to SDO Time | To $V_{IH}/V_{IL}/\text{Hi-Z}$ with 30pF Load | | 16 | ns |

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime. The voltage on all pins should not exceed $V_{CC} + 0.3\text{V}$ or be less than -0.3V , otherwise damage to the ESD diodes may occur.

Note 2: Tests are performed with the test circuit of Figure 1.

Note 3: The LTC5594 is guaranteed to be functional over the -40°C to 105°C case temperature operating range.

Note 4: DSB noise figure is measured at the baseband frequency of 15MHz with a small-signal noise source without any filtering on the RF input and no other RF signal applied.

Note 5: A 6.8pF shunt capacitor is used on the RF inputs for 300MHz to 500MHz. 0.2pF is used for 500MHz to 9GHz.

Note 6: The differential amplifier outputs (IFIP, IFIM and IFQP, IFQM) are combined using a 180° combiner.

Note 7: Noise figure under blocking conditions ($NF_{BLOCKING}$) is measured at an output frequency of 60MHz with RF input signal at $f_{LO} + 1\text{MHz}$. Both RF and LO input signals are appropriately filtered, as well as the baseband output.

Note 8: Power conversion gain is defined from the RF input to the I or Q output. Power conversion gain is measured with a 100Ω differential load impedance on the I and Q outputs. Any losses due to IF combiner and spectrum analyzer termination have been de-embedded.

Note 9: Input P_{RF} adjusted so that $P_{IF} = -1.5\text{dBm}/\text{tone}$ at the amplifier output. RF tone spacing set at 4MHz with high side LO, $f_{LO} = f_{RF} + 30\text{MHz}$.

Note 10: Image rejection is measured at $f_{IF} = 12\text{MHz}$ and calculated from the measured gain error and phase error.

Note 11: If the V_{CM} pin is left floating, it will self bias to a nominal 0.9V.

Note 12: This is the recommended operating range, operation outside the listed range is possible with degraded performance to some parameters.

Note 13: DC offset measured differentially between IFIP and IFIM and between IFQP and IFQM. The reported value is the mean of the absolute values of the characterization data distribution.

Note 14: IF amplitude is within 10% of final value.

Note 15: IF amplitude is at least 30dB down from its on state.

Note 16: IF outputs shorted to ground.

Note 17: IF tone spacing set at 1MHz.

Note 18: Worst case isolation measured to each IF single-ended port.

Note 19: Guaranteed by design characterization, not tested in production.

Note 20: The voltage on the OV_{DD} pin must never exceed $V_{CC} + 0.3\text{V}$, otherwise damage to the ESD diodes may occur.

Note 21: Refer to Appendix for register definition and default values.

Note 22: Mixer outputs directly connected to amplifier inputs. Bandwidth measured on single amplifier output, I or Q.

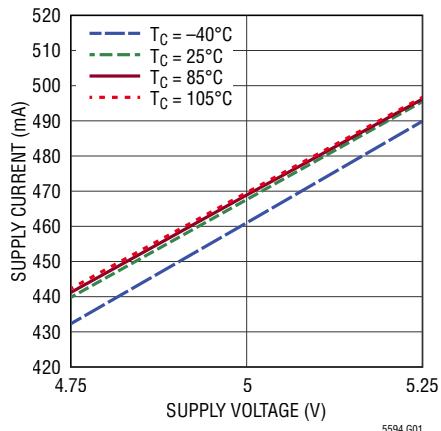
Note 23: V_{CC} should be ramped up slower than 5V/ms to prevent damage.

Note 24: P_{IF} measured at amplifier differential outputs.

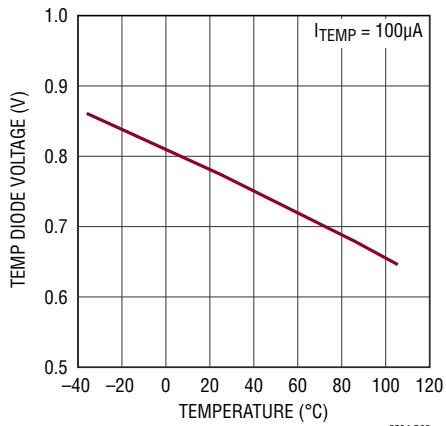
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{CC} = 5V$, $EN = 3.3V$, $T_C = 25^\circ C$, $P_{LO} = 6dBm$,
 HSLO, RF tone spacing = 4MHz, $f_{IF} = 30MHz$, $P_{IF} = -1.5dBm$ per tone, and register defaults. DC Blocks, 50Ω terminations, and
 MACOM H9 180° combiner at amplifier outputs de-embedded from measurement unless otherwise noted. Test circuit shown in
 Figure 1 with 1GHz interstage filter.

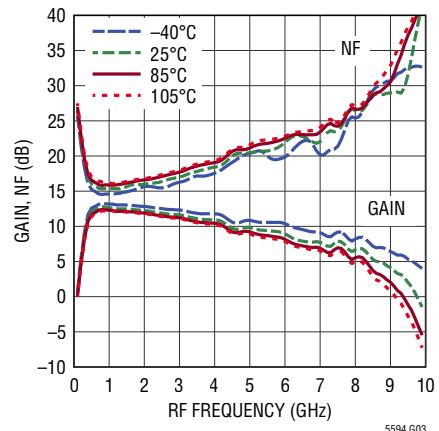
Supply Current vs Supply Voltage



5594 G01

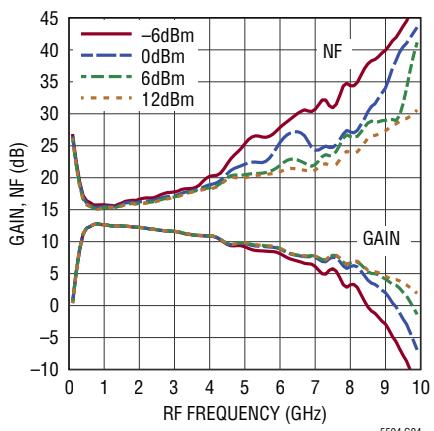
TEMP Diode Voltage vs Junction Temperature (T_J)

5594 G02

Noise Figure and Conversion Gain vs Temperature (T_C)

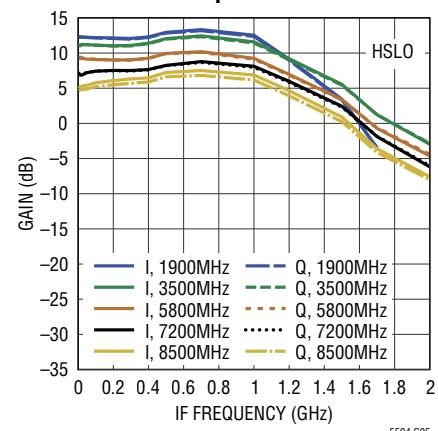
5594 G03

Noise Figure and Conversion Gain vs LO Power



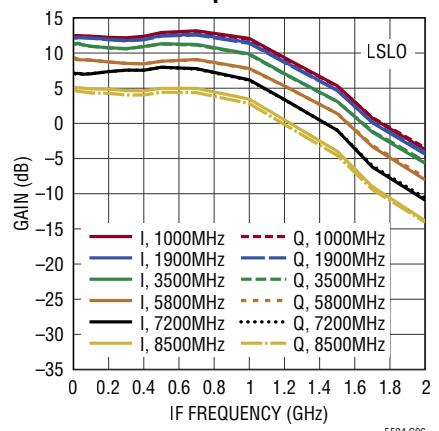
5594 G04

Gain vs IF Frequency for Various Fixed LO Frequencies



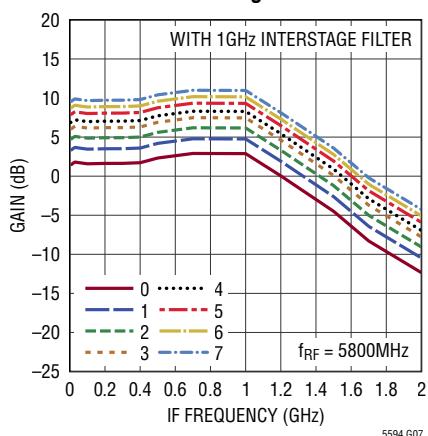
5594 G05

Gain vs IF Frequency for Various Fixed LO Frequencies



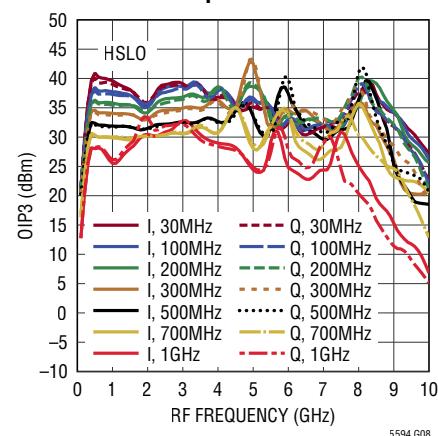
5594 G06

Gain vs AMPG Register Value



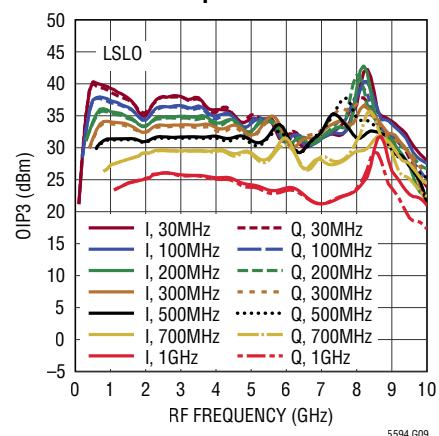
5594 G07

OIP3 vs RF Frequency for Various Fixed IF Frequencies



5594 G08

OIP3 vs RF Frequency for Various Fixed IF Frequencies

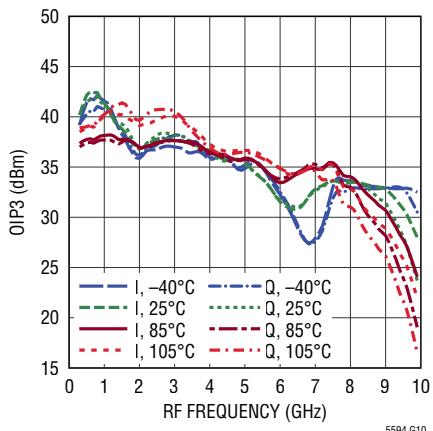


5594 G09

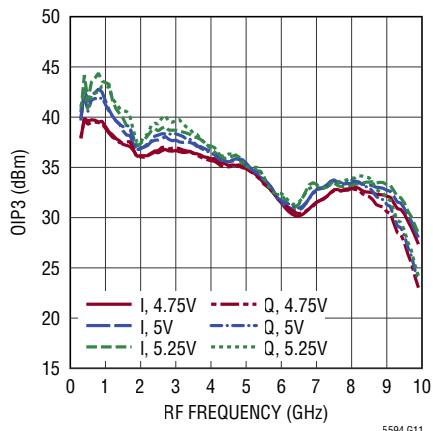
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{CC} = 5V$, $EN = 3.3V$, $T_C = 25^\circ C$, $P_{LO} = 6dBm$, HSLO, RF tone spacing = 4MHz, $f_{IF} = 30MHz$, $P_{IF} = -1.5dBm$ per tone, and register defaults. DC Blocks, 50Ω terminations, and MACOM H9 180° combiner at amplifier outputs de-embedded from measurement unless otherwise noted. Test circuit shown in Figure 1 with 1GHz interstage filter.

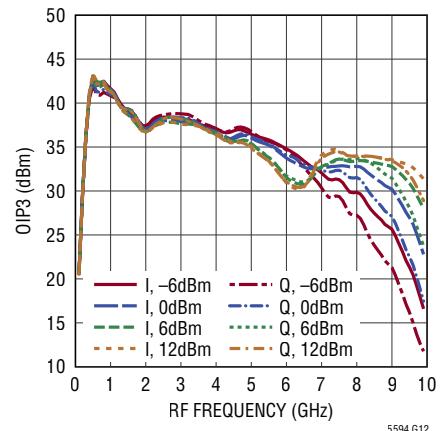
OIP3 vs Temperature (T_C)



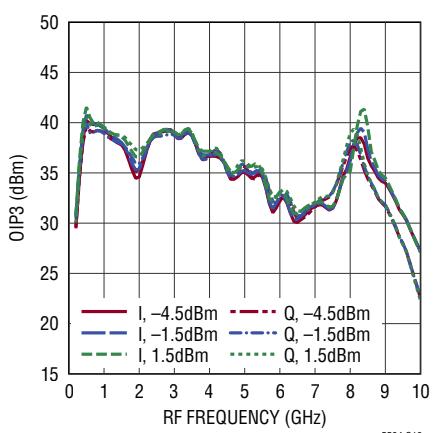
OIP3 vs Supply Voltage (V_{CC})



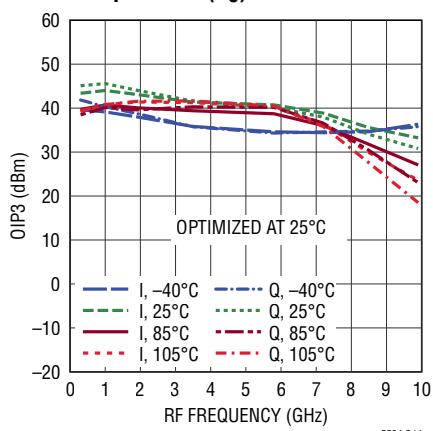
OIP3 vs LO Power



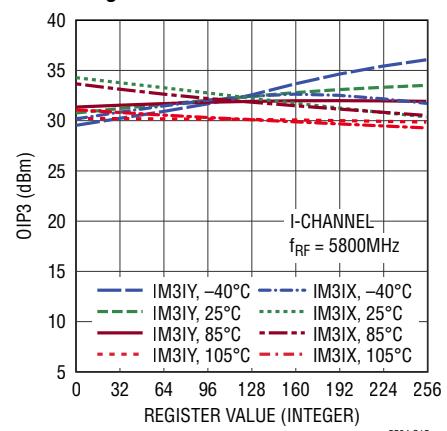
OIP3 vs IF Tone Power



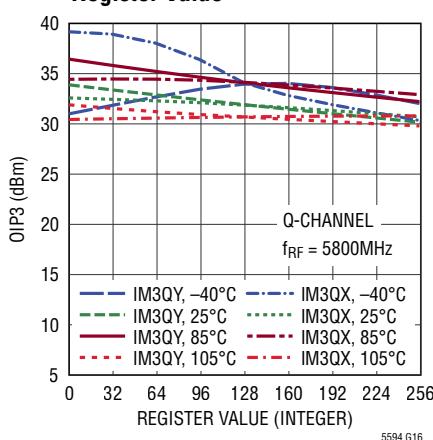
Optimized OIP3 vs Temperature (T_C)



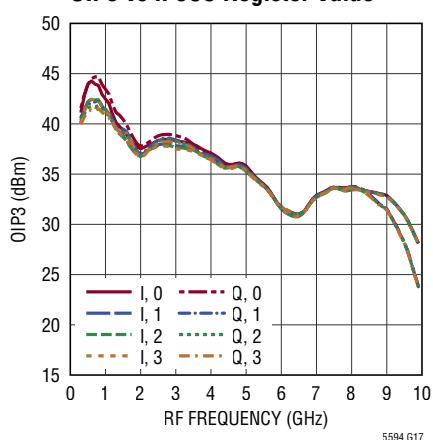
OIP3 vs Temperature (T_C) and Register Value



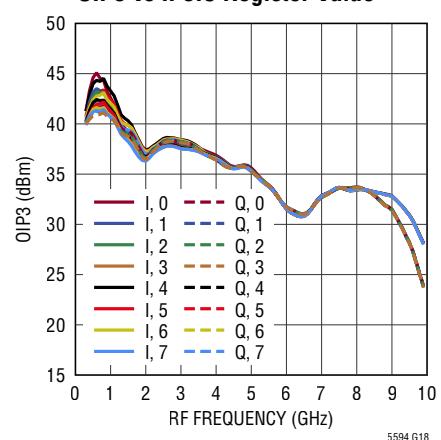
OIP3 vs Temperature (T_C) and Register Value



OIP3 vs IP3CC Register Value



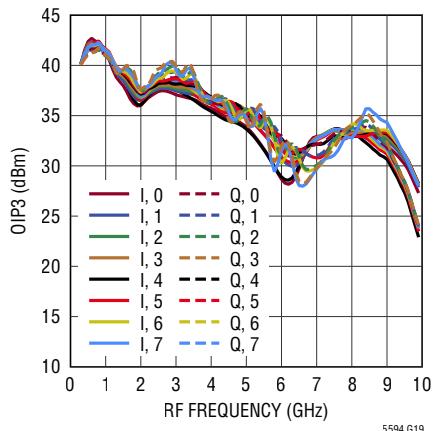
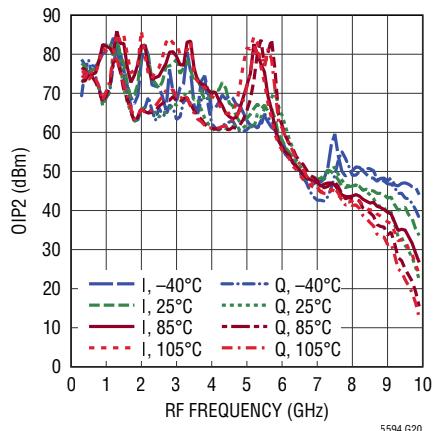
OIP3 vs IP3IC Register Value



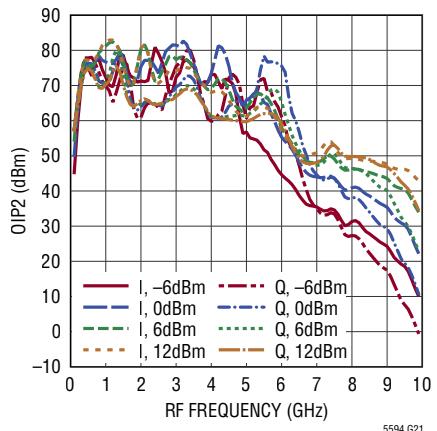
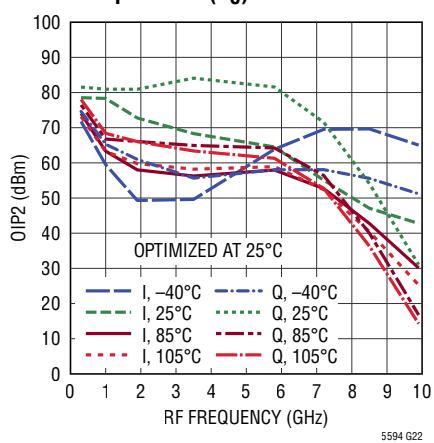
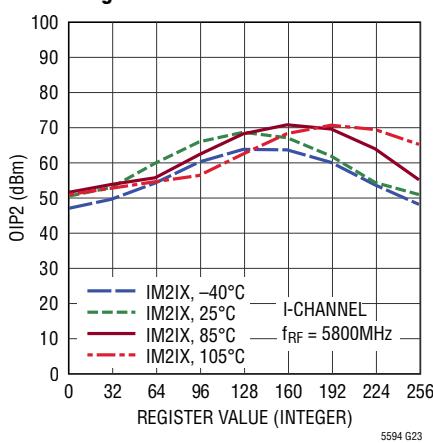
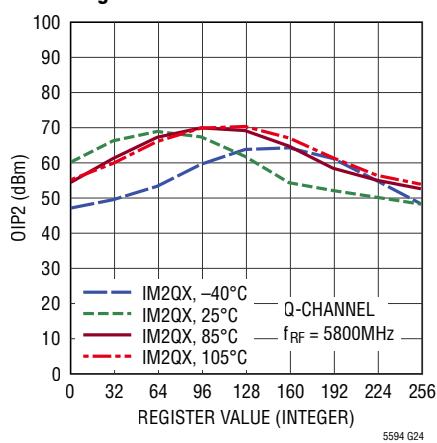
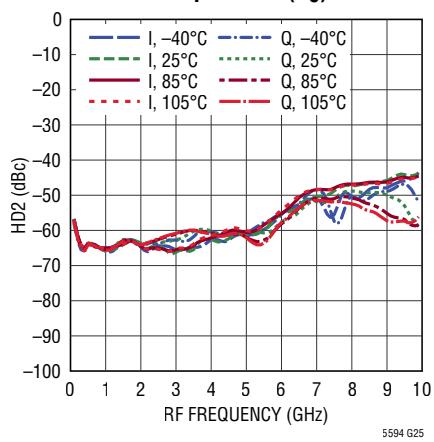
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{CC} = 5V$, $EN = 3.3V$, $T_C = 25^\circ C$, $P_{LO} = 6dBm$,
 HSLO, RF tone spacing = 4MHz, $f_{IF} = 30MHz$, $P_{IF} = -1.5dBm$ per tone, and register defaults. DC Blocks, 50Ω terminations, and
 MACOM H9 180° combiner at amplifier outputs de-embedded from measurement unless otherwise noted. Test circuit shown in
 Figure 1 with 1GHz interstage filter.

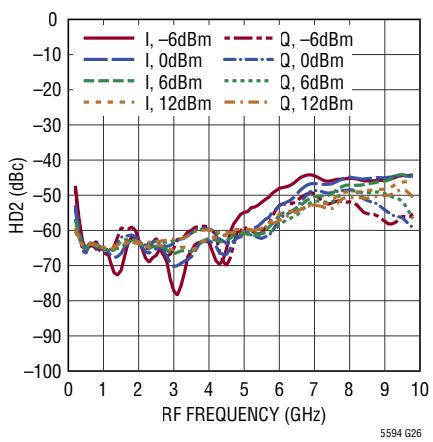
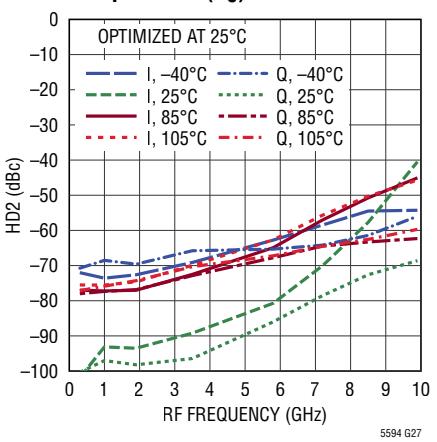
OIP3 vs LVCM Register Value

OIP2 vs Temperature (T_C)

OIP2 vs LO Power

Optimized OIP2 vs Temperature (T_C)OIP2 vs Temperature (T_C) and Register ValueOIP2 vs Temperature (T_C) and Register ValueHD2 vs Temperature (T_C)

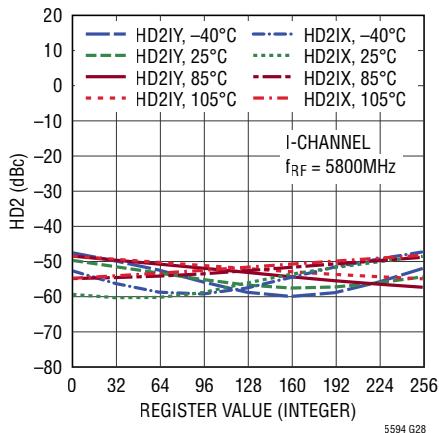
HD2 vs LO Power

Optimized HD2 vs Temperature (T_C)

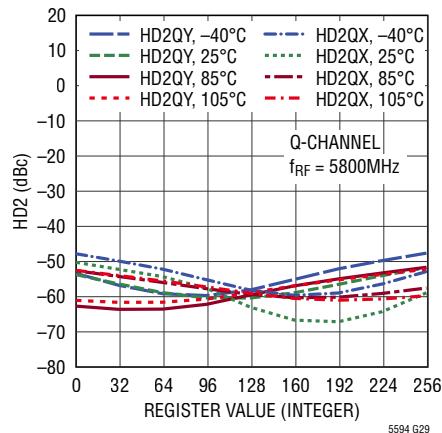
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{CC} = 5V$, $EN = 3.3V$, $T_C = 25^\circ C$, $P_{LO} = 6dBm$,
 HSLO, RF tone spacing = 4MHz, $f_{IF} = 30MHz$, $P_{IF} = -1.5dBm$ per tone, and register defaults. DC Blocks, 50Ω terminations, and
 MACOM H9 180° combiner at amplifier outputs de-embedded from measurement unless otherwise noted. Test circuit shown in
 Figure 1 with 1GHz interstage filter.

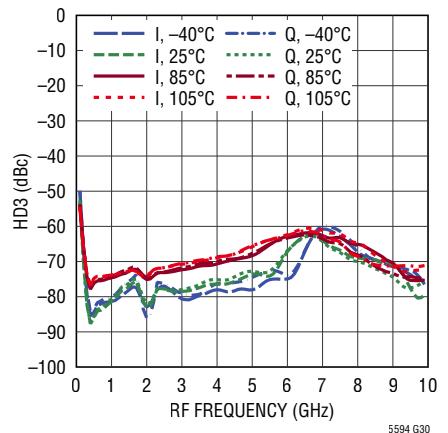
HD2 vs Temperature (T_C) and Register Value



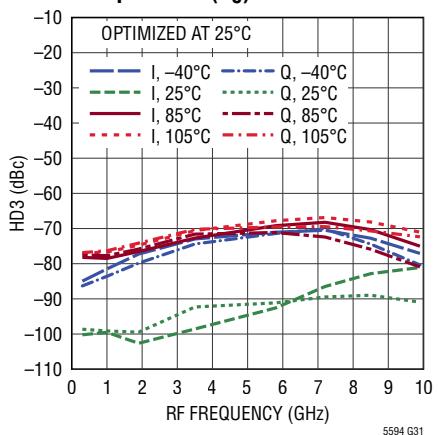
HD2 vs Temperature (T_C) and Register Value



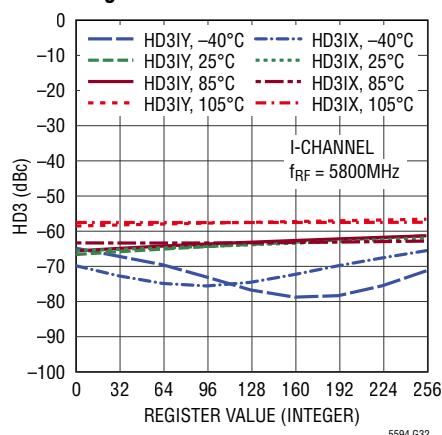
HD3 vs Temperature (T_C)



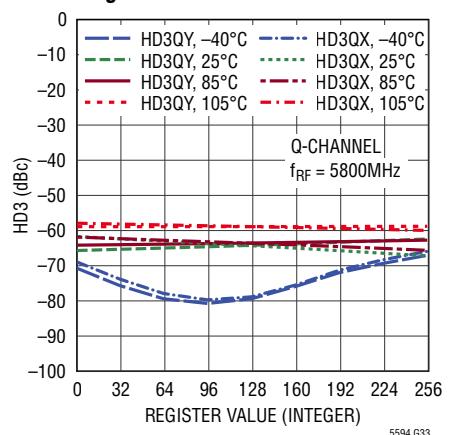
Optimized HD3 vs Temperature (T_C)



HD3 vs Temperature (T_C) and Register Value



HD3 vs Temperature (T_C) and Register Value



Output Referred P1dB

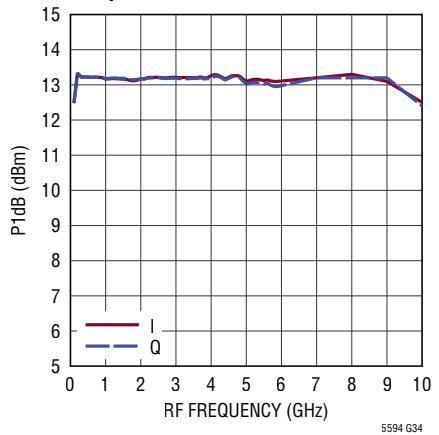


Image Rejection vs Temperature (T_C)

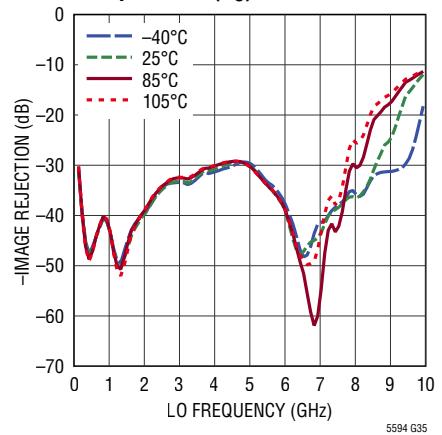
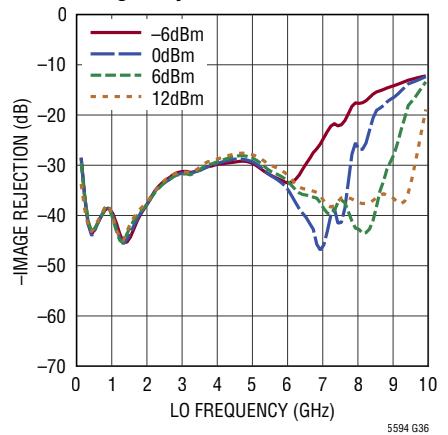
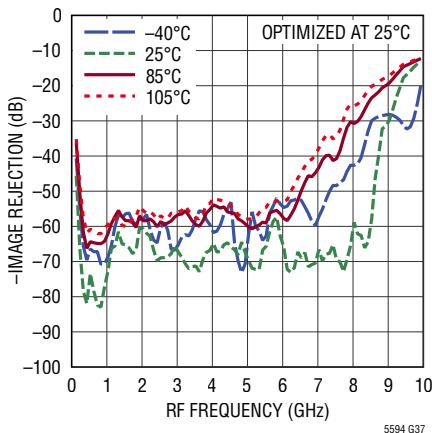


Image Rejection vs LO Power

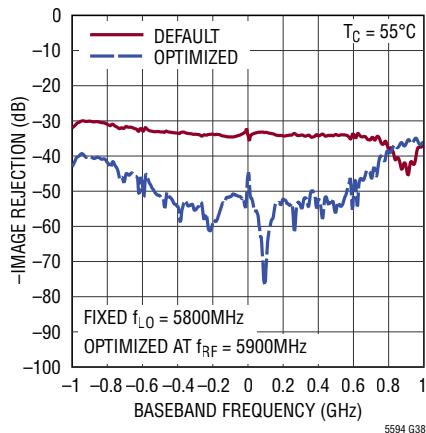
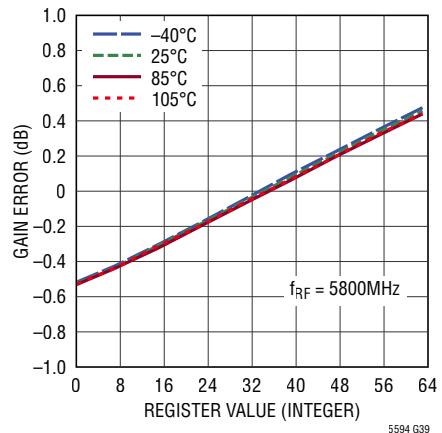
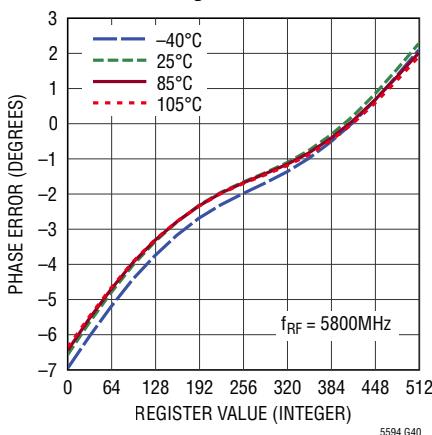
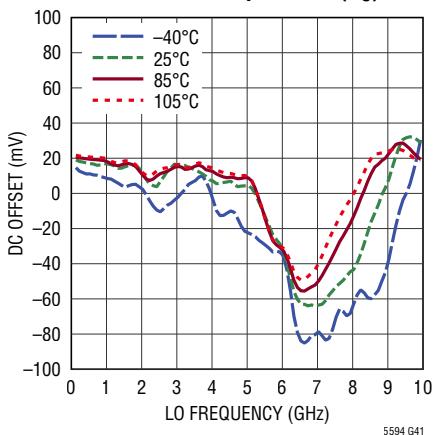


TYPICAL PERFORMANCE CHARACTERISTICS

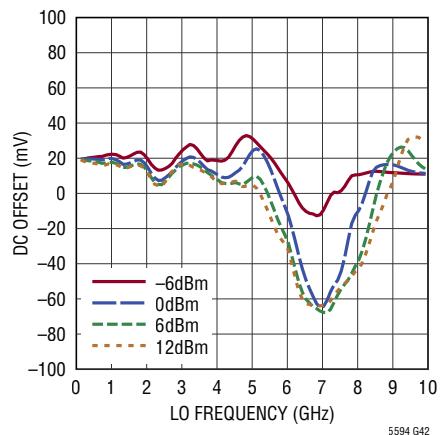
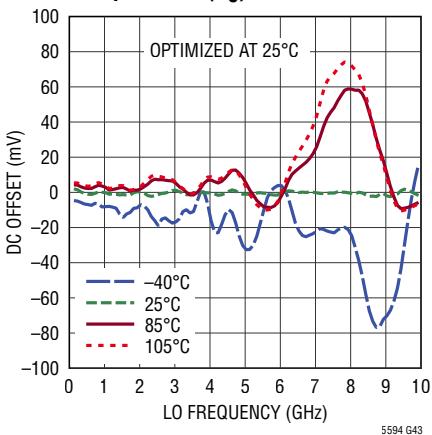
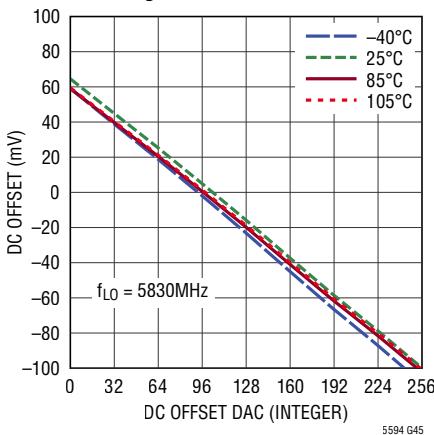
HSLO, RF tone spacing = 4MHz, $f_{IF} = 30\text{MHz}$, $P_{IF} = -1.5\text{dBm}$ per tone, and register defaults. DC Blocks, 50Ω terminations, and MACOM H9 180° combiner at amplifier outputs de-embedded from measurement unless otherwise noted. Test circuit shown in Figure 1 with 1GHz interstage filter.

Optimized Image Rejection vs Temperature (T_C)

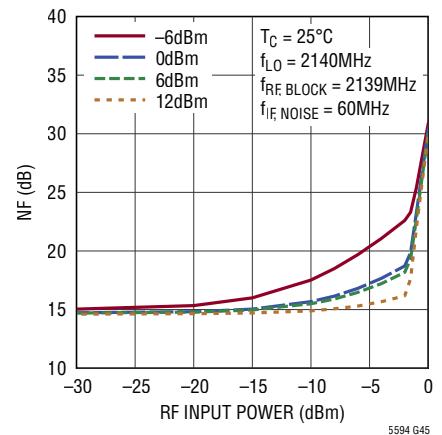
Optimized Image Rejection vs Baseband Frequency

Gain Error vs Temperature (T_C) and GERR Register ValuePhase Error vs Temperature (T_C) and PHA Register ValueDC Offset vs Temperature (T_C)

DC Offset vs LO Power

Optimized DC Offset vs Temperature (T_C)DC Offset vs Temperature (T_C) and Register Value

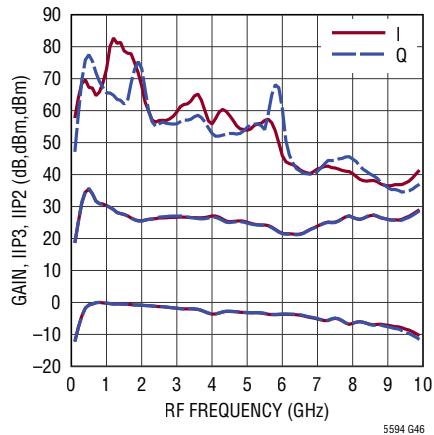
Blocking Noise Figure vs LO Power



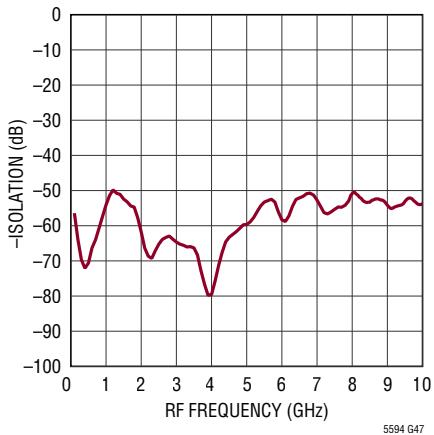
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{CC} = 5V$, $EN = 3.3V$, $T_C = 25^\circ C$, $P_{LO} = 6dBm$,
 HSLO, RF tone spacing = 4MHz, $f_{IF} = 30MHz$, $P_{IF} = -1.5dBm$ per tone, and register defaults. DC Blocks, 50Ω terminations, and
 MACOM H9 180° combiner at amplifier outputs de-embedded from measurement unless otherwise noted. Test circuit shown in
 Figure 1 with 1GHz interstage filter.

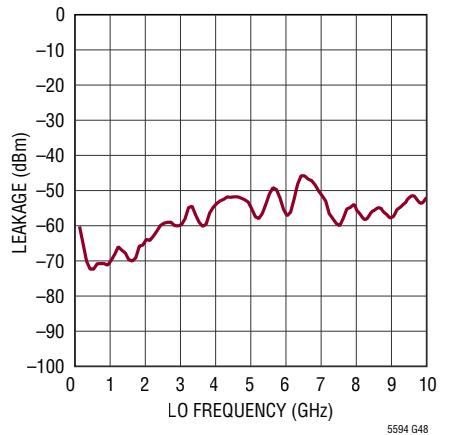
Gain, IIP3, and IIP2 for
Mixer Only



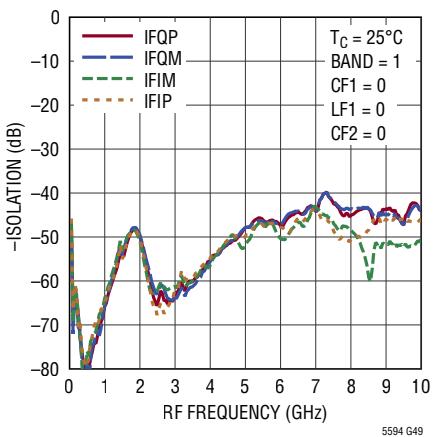
RF to LO Isolation



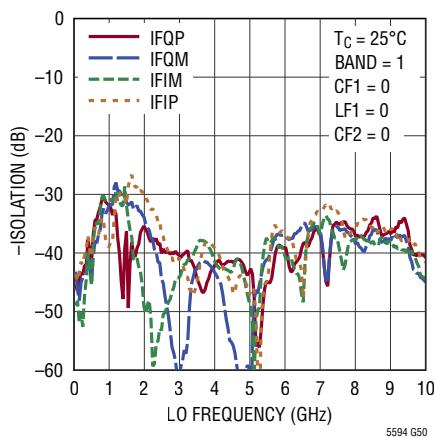
LO to RF Leakage



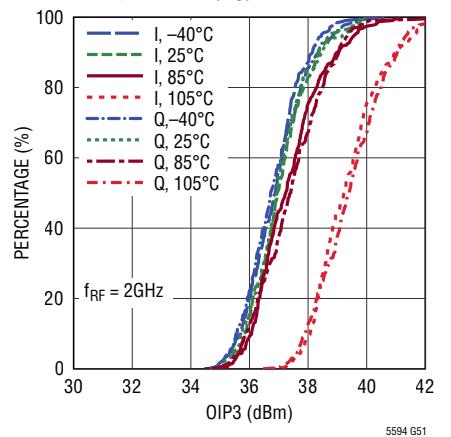
RF to IF Isolation



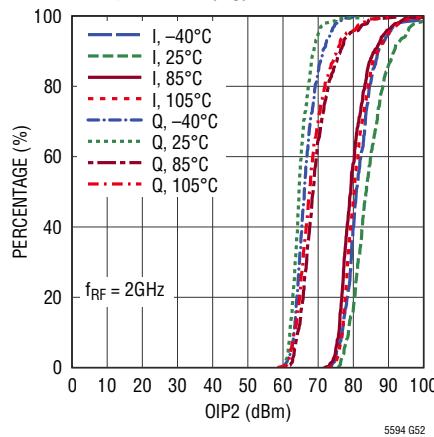
LO to IF Isolation



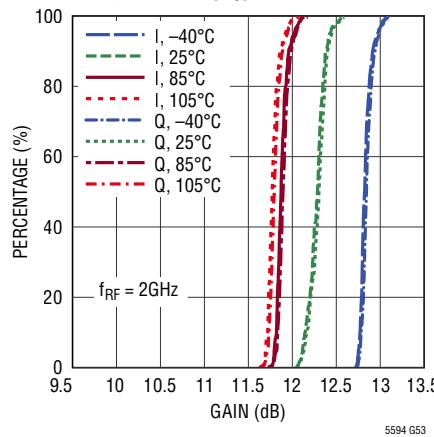
OIP3 Distribution vs
Temperature (T_C)



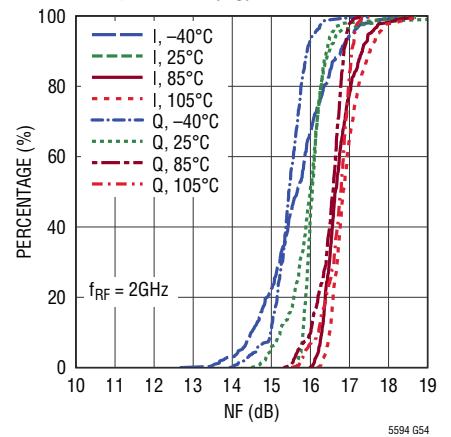
OIP2 Distribution vs
Temperature (T_C)



Conversion Gain Distribution vs
Temperature (T_C)

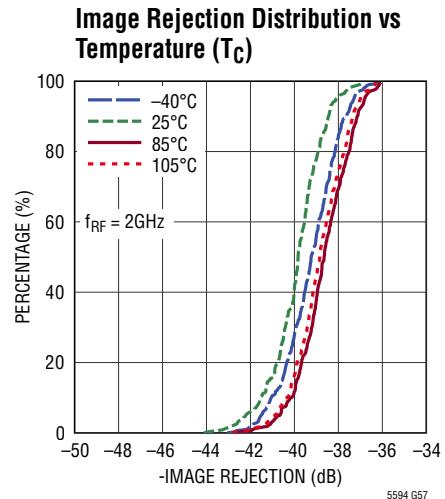
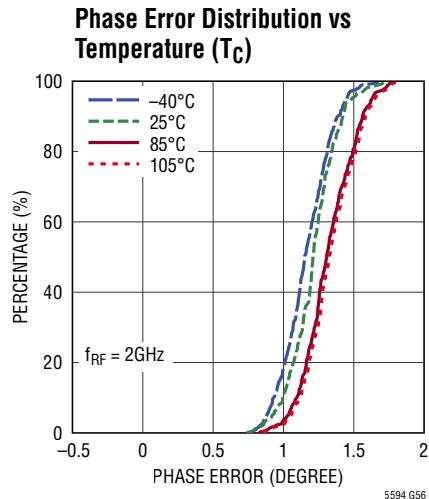
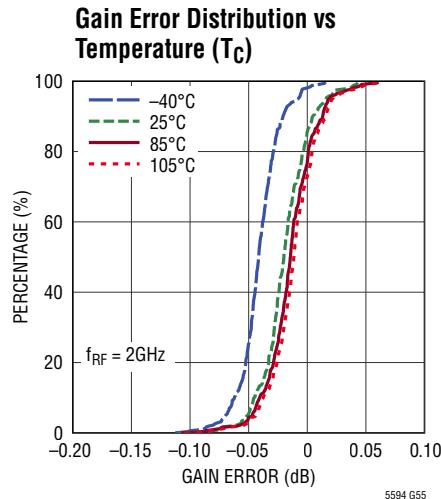


Noise Figure Distribution vs
Temperature (T_C)



TYPICAL PERFORMANCE CHARACTERISTICS

$V_{CC} = 5V$, $EN = 3.3V$, $T_C = 25^\circ C$, $P_{LO} = 6dBm$, HSLO, RF tone spacing = 4MHz, $f_{IF} = 30MHz$, $P_{IF} = -1.5dBm$ per tone, and register defaults. DC Blocks, 50Ω terminations, and MACOM H9 180° combiner at amplifier outputs de-embedded from measurement unless otherwise noted. Test circuit shown in Figure 1 with 1GHz interstage filter.



PIN FUNCTIONS

TEMP (Pin 2): Temperature Monitoring Diode. The diode to ground at this pin can be used to measure the die temperature. A forward bias current of $100\mu A$ can be used into this pin and the forward voltage drop can be measured as a function of die temperature.

RF (Pin 4): 50Ω RF Input. The pin should be DC-blocked with a coupling capacitor; $1000pF$ is recommended.

V_{CM} (Pin 6): IF Amplifier Common Mode Output Voltage Adjust. Source resistance should be $1k$ or lower. If this pin is left unconnected, it will internally self-bias to $0.9V$.

EN (Pin 7): Enable Pin. A logic high on this pin will enable the chip. An internal $200k$ pull-down resistor ensures the chip remains disabled if there is no connection to the pin (open-circuit condition).

MQP, MQM, MIM, MIP (Pins 9, 10, 31, 32): Mixer Differential Output Pins. When connected to the amplifier input pins, the DC bias point is $V_{CC} - 1.4V$ for each pin. A lowpass filter is typically used between the MQM(P) or MIM(P) pins and the AQM(P) or AIM(P) pins to suppress the high frequency mixing products. See the Applications section for more information.

DNC (Pins 11, 14, 30): DO NOT CONNECT. No connection should be made to these pins.

AQM, AQP, AIP, AIM (Pins 12, 13, 28, 29): Amplifier Differential Input Pins. When connected to the mixer output pins, the DC bias point is $V_{CC} - 1.4V$ for each pin. A lowpass filter is typically used between the AQM(P) or AIM(P) pins and the MQM(P) or MIM(P) pins to suppress the high frequency mixing products. See the Applications section for more information.

IFQM, IFQP, IFIP, IFIM (Pins 15, 16, 25, 26): IF Amplifier Output Pins. The current used by the output amplifiers is set by a resistance of 25Ω to 200Ω from each pin to ground and the V_{CM} control voltage.

CSB (Pin 17): Chip Select Bar. When CSB is low, the serial interface is enabled. It can be driven with $1.2V$ to $3.3V$ logic levels.

V_{CC} (Pin 18): Positive Supply Pin. This pin should be bypassed with a $1000pF$ and $4.7\mu F$ capacitor to ground.

LOP, LOM (Pins 19, 20): LO Inputs. External matching is not needed. Can be driven 50Ω single-ended or 100Ω differentially. The LO pins should be DC-blocked with

PIN FUNCTIONS

coupling capacitor; 1000pF is recommended. When driven single-ended, the unused pin should be terminated with 50Ω in series with the DC-blocking capacitor.

SDO (Pin 21): Serial Data Output. This output can accommodate logic levels from 1.2V to 3.3V. During read-mode, data is read out MSB first.

SDI (Pins 22): Serial Data Input. Data is clocked MSB first into the mode-control registers on the rising edge of SCK. SDI can be driven with 1.2V to 3.3V logic levels.

SCK (Pin 23): Serial Clock Input. SDI can be driven with 1.2V to 3.3V logic levels.

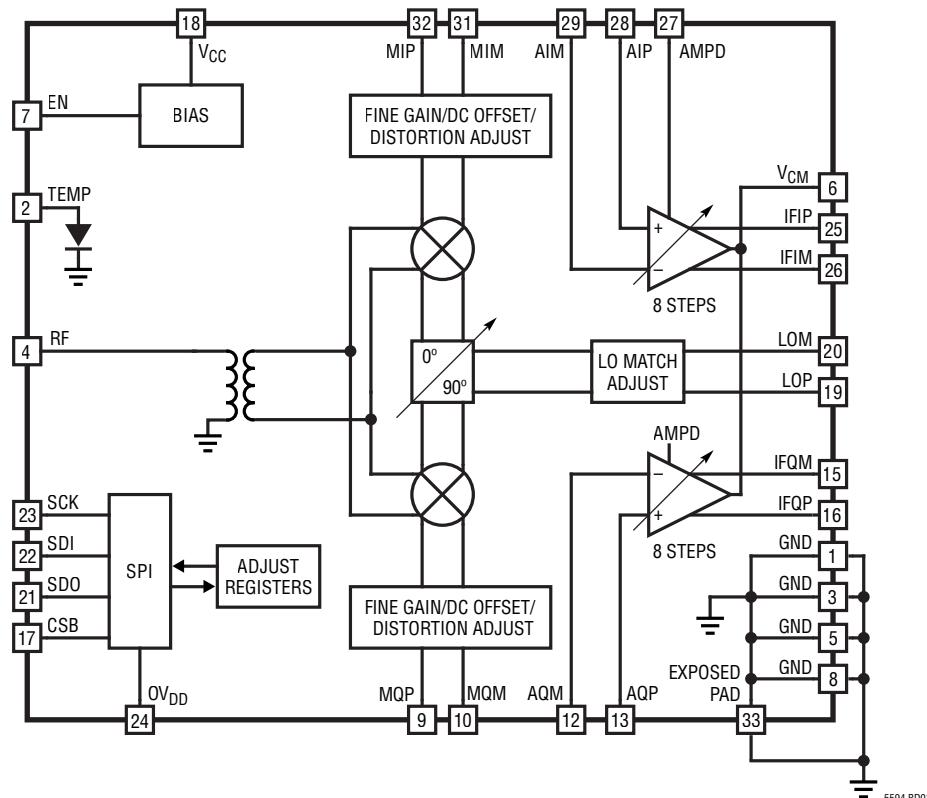
OV_{DD} (Pin 24): Positive Digital Interface Supply Pin. This pin sets the logic levels for the digital interface. 1.2V to 3.3V can be used. This pin should be bypassed with a 1μF

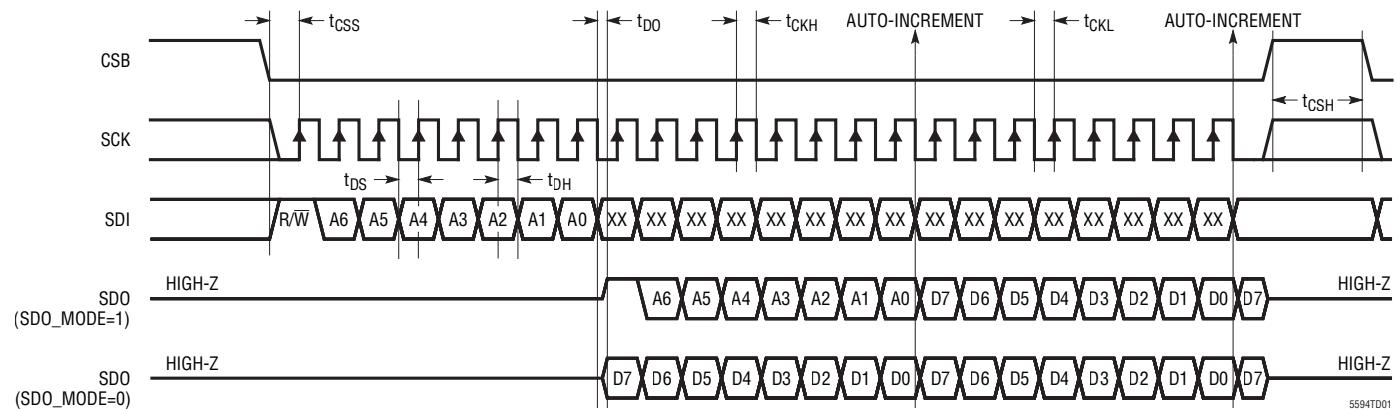
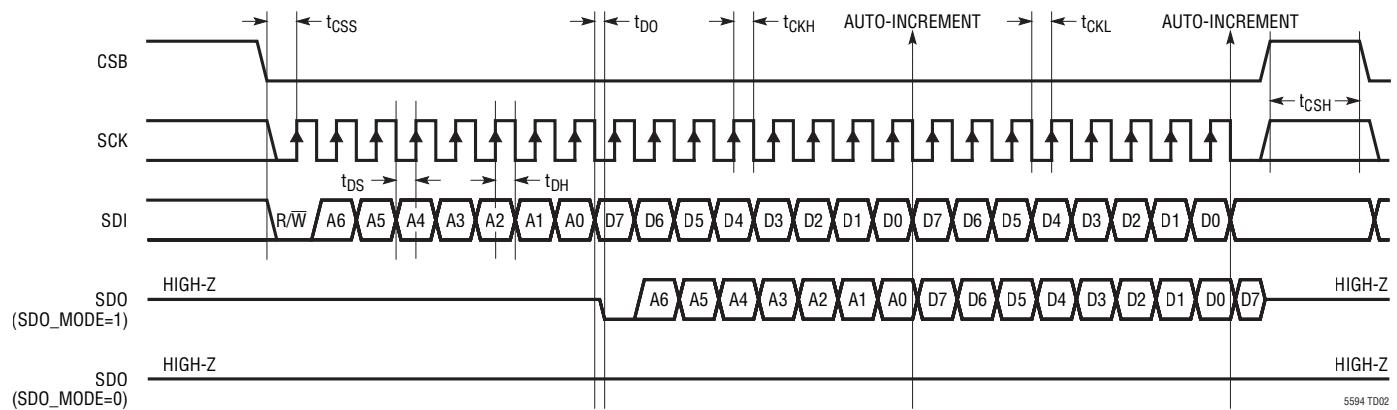
capacitor to ground. The V_{CC} supply must be applied before the OV_{DD} supply to prevent damage to the ESD diodes.

AMPD (Pin 27): IF Amplifier Disable Pin. A logic high on this pin will disable the IF amplifiers. The state of the IF amplifiers is the logical AND of AMPD and the EAMP register. An internal 200k pull-down resistor ensures the IF amplifiers are enabled by default if there is no connection to the pin (open-circuit condition).

GND (Pins 1, 3, 5, 8, Exposed Pad Pin 33): Ground. These pins must be soldered to the circuit board RF ground plane. The backside exposed pad ground connection should have a low inductance connection and good thermal contact to the printed circuit board ground plane using many through-hole vias. See layout information.

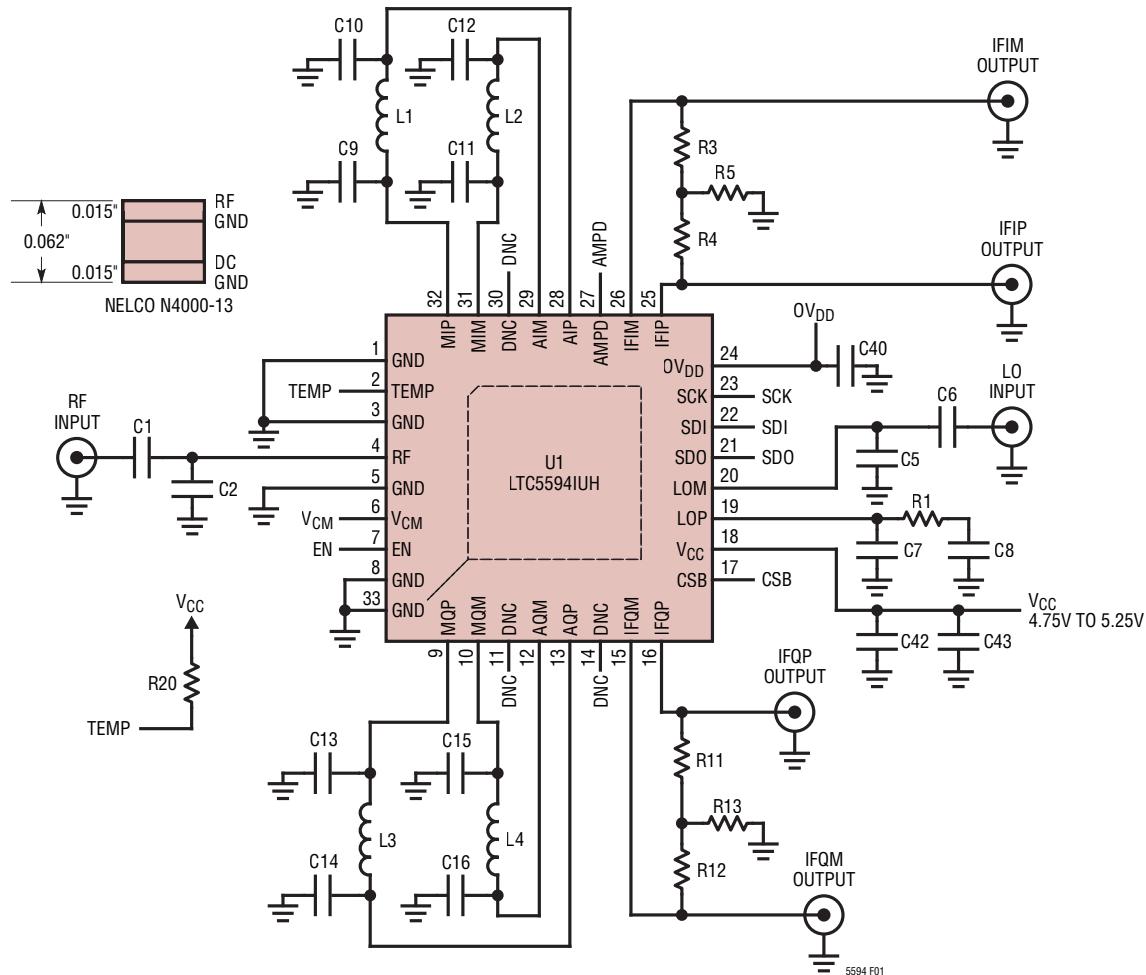
BLOCK DIAGRAM



TIMING DIAGRAMS**SPI Port Timing (Readback Mode)****SPI Port Timing (Write Mode)**

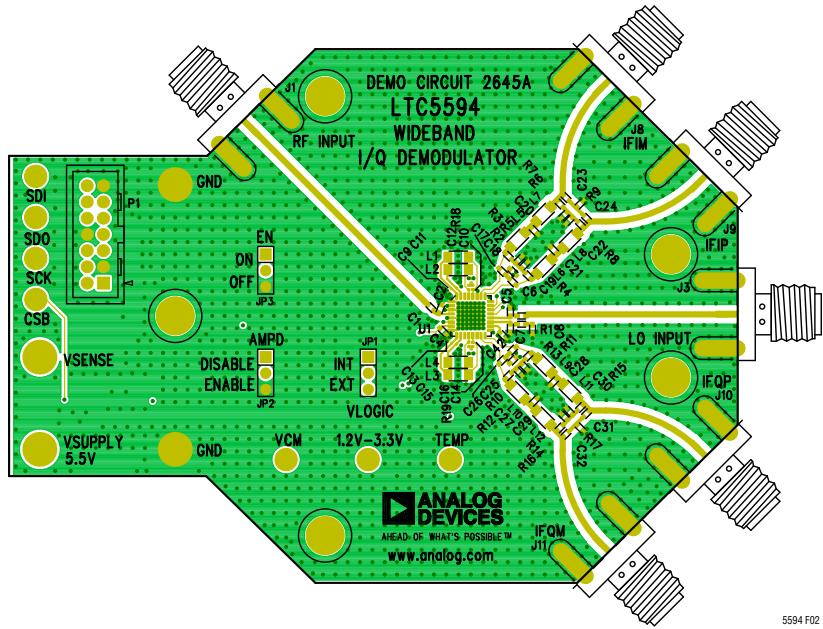
LTC5594

TEST CIRCUIT



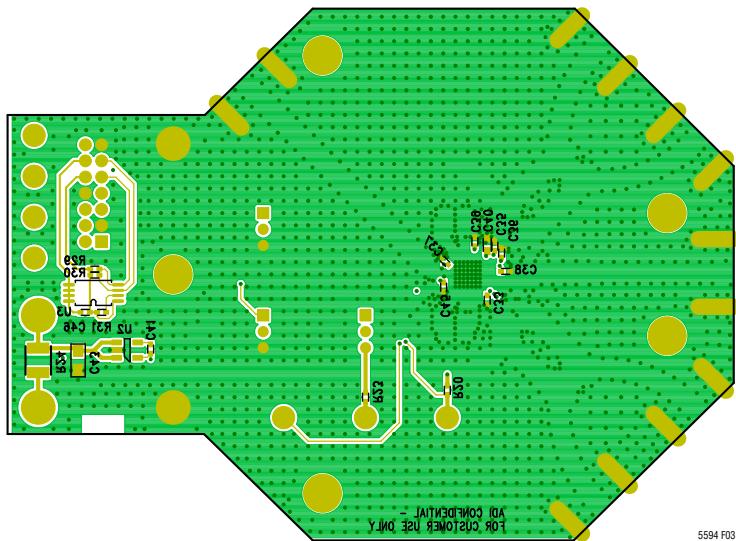
| REF DES | VALUE | SIZE | VENDOR | REF DES | VALUE | SIZE | VENDOR |
|--------------------|--------|------|--------|----------------------|--------|------|-----------|
| C1, C6, C8, C42 | 1000pF | 0402 | Murata | L1 TO L4 | 8.2nH | 0805 | Coilcraft |
| C2 | 0.2pF | 0402 | Murata | R1, R3, R4, R11, R12 | 49.9Ω | 0402 | |
| C5, C7 | 0.3pF | 0402 | Murata | R5, R13 | 0Ω | 0402 | |
| C9, C11, C13, C15 | 1.0pF | 0201 | Murata | R20 | 40.2kΩ | 0402 | |
| C10, C12, C14, C16 | 3.0pF | 0201 | Murata | | | | |
| C40 | 1μF | 0603 | Murata | | | | |
| C43 | 4.7μF | 0805 | Murata | | | | |

Figure 1. Test Circuit Schematic

TEST CIRCUIT

5594 F02

Figure 2. Component Side of Evaluation Board



5594 F03

Figure 3. Bottom Side of Evaluation Board

APPLICATIONS INFORMATION

The LTC5594 is an IQ demodulator designed for high dynamic range receiver applications. It consists of an RF balun, I/Q mixers, quadrature LO amplifiers, IF amplifiers, and correction circuitry for DC offset, image rejection, and nonlinearity.

Operation

As shown in the Block Diagram for the LTC5594, the RF input signal is converted to a differential signal by the on-chip balun transformer before going to the I and Q channel mixers.

The LO inputs are impedance matched using a programmable network, and then accurately shifted in phase by 90° by an internal precision phase shifter. This phase shifter maintains the accurate quadrature relation over the full LO input range from 300MHz to 9GHz. In addition, the phase shifter allows fine tuning of the phase difference between the I- and Q-channel LO with a resolution of around 0.05 degrees to compensate for any phase mismatch between the mixers and phase mismatch introduced into the IF path by any filter component mismatch.

The differential mixer IF output signals are filtered off-chip to remove the $f_{RF} + f_{LO}$ signal and other high frequency mixing products before being applied to the on-chip IF amplifiers. The IF amplifiers have adjustable gain and common mode output voltage to allow for direct interfacing with A/D converters. The gain balance between both IF output channels of the LTC5594 can be fine tuned with a resolution of about 0.016dB in order to compensate for gain mismatches in the IF signal path, either caused

internally by the device or by external amplifiers and filters. The DC offset in both IF channels can be adjusted in order to minimize the accumulated DC offset at the A/D converter input.

The IF gain, gain error and phase error adjust, DC offset adjust, and nonlinearity adjust registers are digitally controlled through a 4-wire serial interface. The register map is detailed in the Appendix.

RF Input Port

Figure 4 shows a simplified schematic of the demodulator's RF input connected to an on-chip balun transformer. External DC voltage should not be applied to the RF input pin. DC current flowing into the pin may cause damage to the chip. Series DC blocking capacitors should be used to couple the RF input pin to the RF signal source. As shown in Figure 5, the RF input port is well matched with return loss greater than 10dB over the frequency range of 500MHz to 9GHz with a 0.2pF capacitor on C2. A 0.1pF capacitor on C3 placed 3mm away from C1 on the 50Ω input transmission line may improve return loss at higher frequencies. The RF pin can also be externally matched over the 300MHz to 500MHz frequency range by changing C2 to 6.8pF. Table 1 shows the impedance and input reflection coefficient for the RF input with C2 = 0.2pF. The input transmission line length is de-embedded from the measurement.

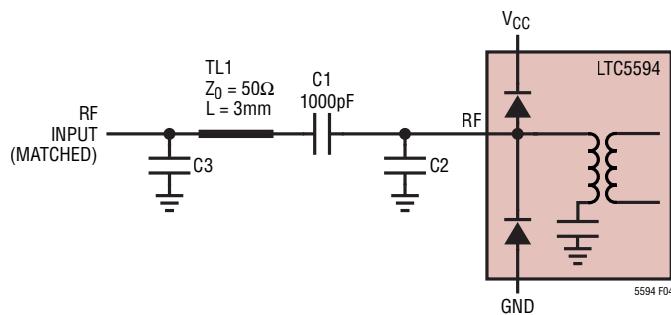


Figure 4. Simplified Schematic of the RF Input with External Matching Components

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Table 1. RF Input Impedance

| FREQUENCY (MHz) | INPUT IMPEDANCE (Ω) | S11 | |
|--------------------|------------------------------|-------|-----------|
| | | MAG | ANGLE (°) |
| 300 | $30.0 + j57.1$ | 0.594 | 122.5 |
| 1000 | $66.8 - j5.3$ | 0.151 | -17.6 |
| 1500 | $49.4 - j10.4$ | 0.092 | -94.0 |
| 2000 | $46.8 + j4.0$ | 0.048 | 133.7 |
| 2500 | $48.9 + j12.8$ | 0.113 | 96.0 |
| 3000 | $56.5 + j10.6$ | 0.111 | 56.5 |
| 3500 | $62.7 - j5.8$ | 0.124 | -24.0 |
| 4000 | $61.5 - j23.6$ | 0.233 | -62.6 |
| 4500 | $55.4 - j30.6$ | 0.278 | -78.5 |
| 5000 | $47.0 - j26.3$ | 0.236 | -97.9 |
| 5500 | $38.6 - j16.1$ | 0.191 | -133.2 |
| 6000 | $33.7 - j7.5$ | 0.206 | -162.0 |
| 7000 | $32.3 - j12.0$ | 0.240 | -155.2 |
| 8000 | $33.9 + j0.1$ | 0.192 | 179.7 |
| 9000 | $48.0 + j44.0$ | 0.404 | 93.6 |

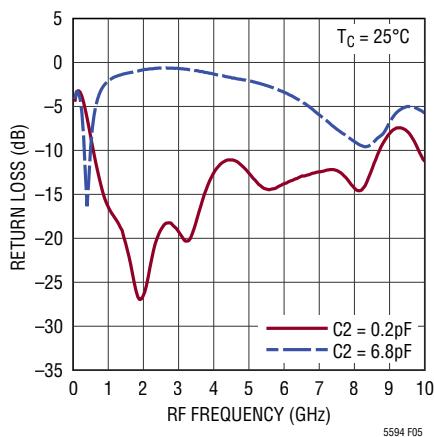


Figure 5. RF Input Return Loss with $C_2 = 0.2\text{pF}$ and 6.8pF

LO Input Port

The demodulator's LO input interface is shown in Figure 6. The input consists of a programmable input match and a high precision quadrature phase shifter which generates 0° and 90° phase shifted LO signals for the LO buffer amplifiers to drive the I/Q mixers. DC blocking capacitors are required on the LOP and LOM inputs. When using a single-ended LO input, it is necessary to terminate the unused LO input (LOP in Figure 6) into 50Ω .

The programmable input match adjust is controlled by the BAND, CF1, LF1, and CF2 registers as detailed in the register map shown in Table 2. The return loss for the register setting in Table 2 is shown in Figure 7.

Table 2. Register Settings for Single-Ended LO Matching

| LO FREQUENCY (MHz) | BAND | CF1 | LF1 | CF2 |
|--------------------|------|-----|-----|-----|
| 300 to 339 | 0 | 31 | 3 | 31 |
| 339 to 398 | 0 | 21 | 3 | 24 |
| 398 to 419 | 0 | 14 | 3 | 23 |
| 419 to 556 | 0 | 17 | 2 | 31 |
| 556 to 625 | 0 | 10 | 2 | 23 |
| 625 to 801 | 0 | 15 | 1 | 31 |
| 801 to 831 | 0 | 14 | 1 | 27 |
| 831 to 1046 | 0 | 8 | 1 | 21 |
| 1046 to 1242 | 1 | 31 | 3 | 31 |
| 1242 to 1411 | 1 | 21 | 3 | 28 |
| 1411 to 1696 | 1 | 17 | 2 | 26 |
| 1696 to 2070 | 1 | 15 | 1 | 31 |
| Default | 1 | 8 | 3 | 3 |
| 2070 to 2470 | 1 | 8 | 1 | 21 |
| 2470 to 2980 | 1 | 2 | 1 | 10 |
| 2980 to 3500 | 1 | 1 | 0 | 19 |
| 3500 to 9000 | 1 | 0 | 0 | 0 |

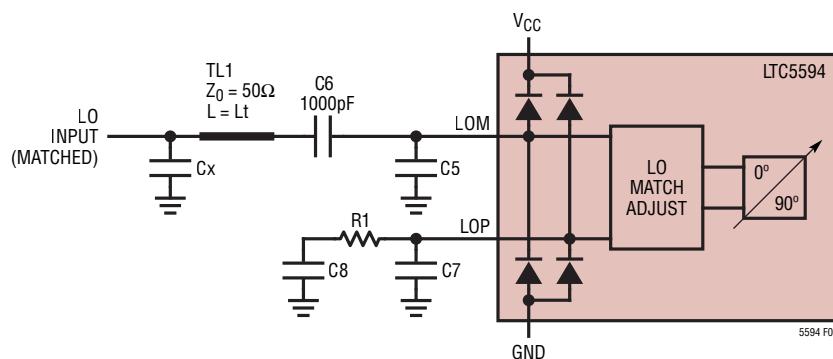


Figure 6. Simplified Schematic of the LO Inputs with Single-Ended Drive

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Figure 8 shows the high band LO input return loss for various input TL1 transmission line lengths for LO input frequencies from 6GHz to 9GHz. Return loss greater than 10dB can be achieved by using a 0.2pF capacitor at Cx on the input 50Ω transmission line. The high band LO input return loss is listed in Table 3 with no capacitor at Cx and BAND, CF1, LF1, and CF2 registers set to 1,0,0,0.

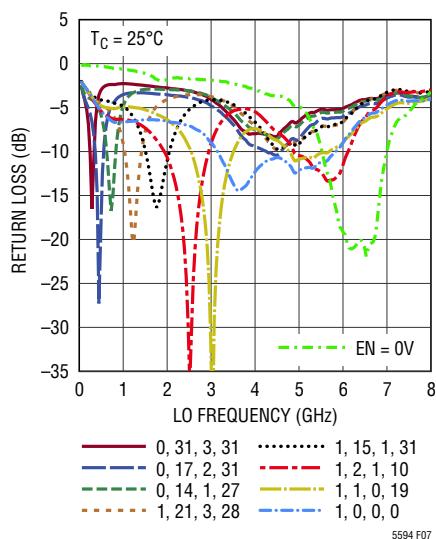


Figure 7. Single-Ended LO Input Return Loss vs BAND, CF1, LF1, and CF2

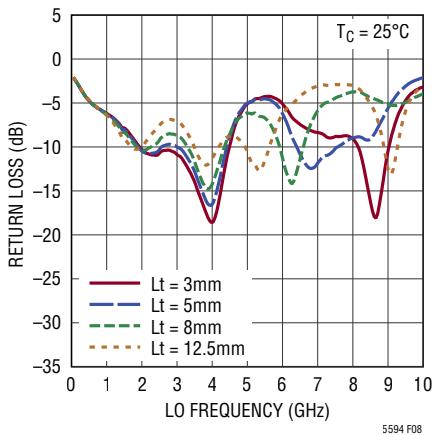


Figure 8. High Band LO Input Return Loss vs Input Transmission Line Length Lt

Table 3. High Band LO Input Impedance

| FREQUENCY (MHz) | INPUT IMPEDANCE (Ω) | S11 | |
|--------------------|---------------------|-------|-----------|
| | | MAG | ANGLE (°) |
| 5000 | 87.2 + j37.9 | 0.436 | 46.4 |
| 5500 | 121.5 + j32.1 | 0.503 | 27.8 |
| 6000 | 132.1 + j5.4 | 0.453 | 4.8 |
| 6500 | 95.2 - j17.7 | 0.347 | -23.8 |
| 7000 | 73.5 - j39.5 | 0.406 | -58.2 |
| 7500 | 69.0 - j47.5 | 0.467 | -66.0 |
| 8000 | 77.8 - j51.9 | 0.531 | -59.9 |
| 8500 | 77.8 - j38.8 | 0.361 | -75.4 |
| 9000 | 58.8 - j38.8 | 0.402 | -122.6 |

Interstage Filter

An interstage IF filter should be used between the MIP (MIM) and AIP (AIM) pins and the MQP (MQM) and AQP (AQM) pins to suppress the large $f_{RF} + f_{LO}$ and other mixing products from the mixer outputs. Without the filter, the linearity of the amplifier can be degraded for the desired signal. Figure 9 shows a recommended lowpass filter. Table 4 shows typical values used for a lowpass response of various bandwidths.

Table 4. Component Values for Interstage Lowpass Filter

| 1dB BW (MHz) | L1, L2 (nH) | C9, C11 (pF) | C10, C12 (pF) |
|--------------|-------------|--------------|---------------|
| 20 | 330 | 39 | 120 |
| 50 | 150 | 15 | 47 |
| 100 | 68 | 10 | 22 |
| 300 | 33 | 4.7 | 6.8 |
| 500 | 22 | 3.0 | 3.0 |
| 1000 | 8.2 | 1.0 | 3.0 |

It is important that the placement of C10 and C12 be as close as possible to the amplifier inputs. Long line lengths on the amplifier inputs can lead to instability. As shown in Figure 10, a 50Ω common mode termination resistance can be used to better ensure stability with long line lengths and/or higher order filtering. The placement of C9 and C11 should be as close as possible to the mixer outputs for effective filtering of the 2xLO, $f_{RF} + f_{LO}$, and other mixing products.

By adjusting the values of the capacitors in the filter, it is possible to add or remove frequency slope of the IF response. The RF input has a frequency slope above 2GHz of approximately -1dB/GHz . If a high side LO (HSLO) is

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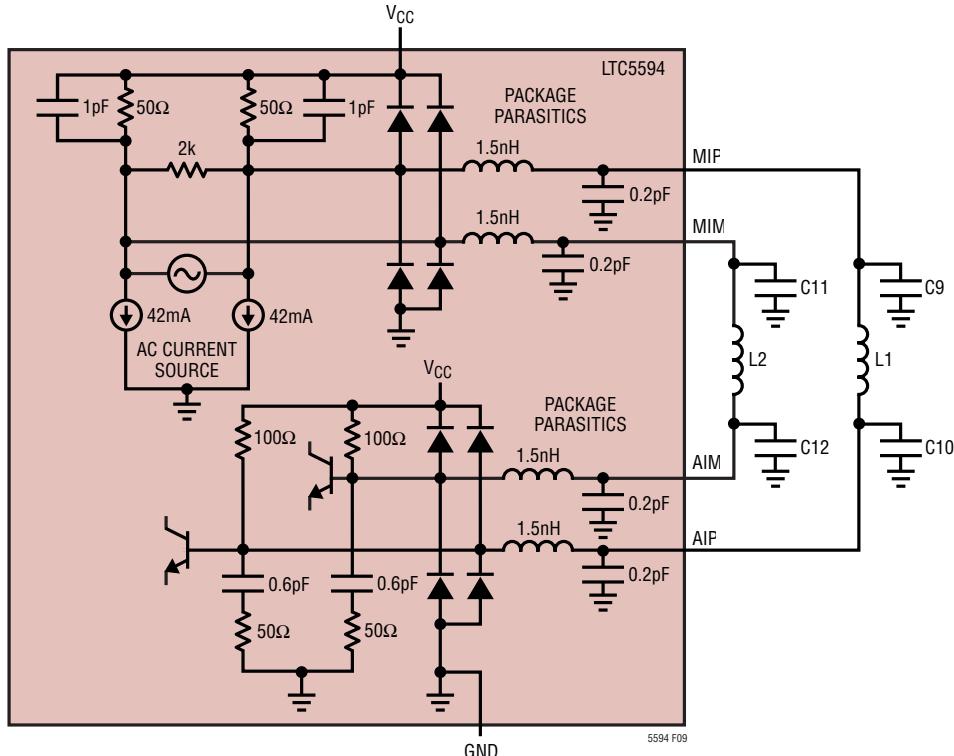


Figure 9. Simplified Schematic of the Mixer Output and IF Amplifier Input with Interstage Filter

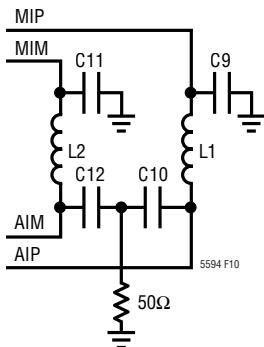


Figure 10. Interstage IF Filter with Common Mode Termination

used, the resulting IF slope will be 1dB/GHz. If a low side LO (LSLO) is used, the resulting IF slope will be $-1\text{dB}/\text{GHz}$. The IF filter component values can be adjusted so that approximately 1dB of peaking or roll-off can be achieved over the filter bandwidth to give an overall flat IF response for the HSLO or LSLO case.

I-Channel and Q-Channel Outputs

The phase relationship between the I-channel output signal and the Q-channel output signal is fixed. When the LO input frequency is higher (or lower) than the RF input frequency, the Q-channel outputs (IFQP, IFQM) lead (or lag) the I-channel outputs (IFIP, IFIM) by 90° .

Figure 11 shows a simplified schematic of the IF amplifier outputs. The current-mode outputs require a terminating resistance to establish a common mode voltage level. The optimum operating current is 18mA per output. A 50Ω termination is recommended on each output for a 0.9V common mode voltage (R_5, R_6). Operation at a higher common mode voltage is possible with the addition of a common mode termination. For example, to operate at 1.8V, an additional common mode resistance of 25Ω ($R_5 = 66.5\Omega$ and $R_6 = 0\Omega$, or $R_5 = R_6 = 43.2\Omega$) would be used to maintain an output current of 18mA. Alternatively, a 100Ω termination to ground on each output can be used for a 1.8V common mode voltage with 6dB more

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conversion gain. To operate at lower common mode voltages, a lower termination resistance can be used on each output at the expense of conversion gain, or a negative supply can be used at the connection of the termination resistors. Figure 12 shows the OIP3 of the amplifier alone with various common mode voltages.

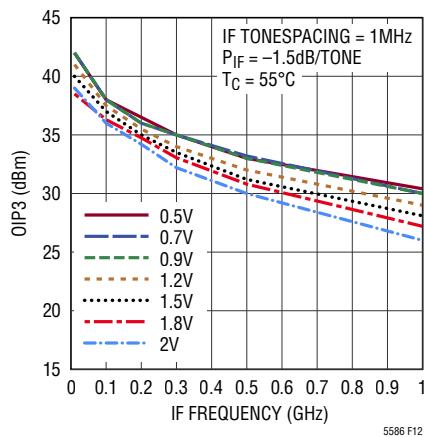


Figure 12. OIP3 of Amplifier Only vs Output Common Mode Voltage (V_{CM})

The amplifier gain can be adjusted in eight steps of roughly 1dB from 8dB to 15dB using the AMPG register. Setting AMPG = 0x7 sets the gain at about 15dB and setting AMPG = 0x0 sets the gain to about 8dB.

A typical anti-alias filter is shown in Figure 11 for interface with an ADC. The parallel combinations of $R3|R7$ and $R4|R8$ set the differential impedance for the ADC. The input and output of the filter contain a common mode termination for high frequencies. These are formed by $C17$, $C18$ and 24.9Ω at the input and $C23$, $C24$ and 24.9Ω at the output. The common mode termination at the amplifier output ensures stability and the common mode termination at the ADC input provides a termination for the high frequency kickback from the sampling capacitors in the ADC. Table 5 shows some typical values vs 1dB cutoff frequency for the anti-alias filter. To optimize the flatness and ripple of the IF band, both the IF interstage filter and the anti-alias filter can be designed together in a simulator including package parasitics. The additional slope due to RF slope and HSLO or LSLO can be compensated by using this method. The layout of the anti-alias filter should be done so that the amplifier outputs and ADC inputs are as close as possible. This is to prevent long line lengths from introducing additional parasitics.

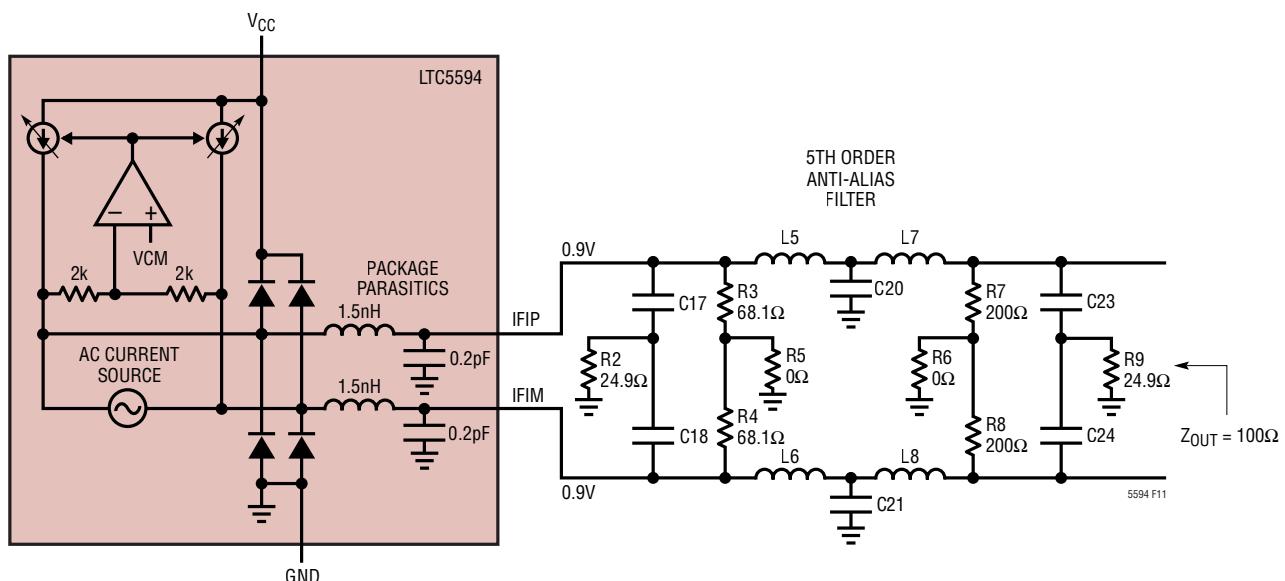


Figure 11. Simplified Schematic of the IF Amplifier Output with Anti-Alias Filter

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Table 5. Component Values for Anti-Alias Lowpass Filter

| 1dB BW (MHz) | L5 – L8 (nH) | C17, C18 (pF) | C20, C21 (pF) | C23, C24 (pF) |
|-----------------|-----------------|------------------|------------------|------------------|
| 20 | 560 | 56 | 180 | 82 |
| 50 | 240 | 22 | 68 | 33 |
| 100 | 120 | 12 | 39 | 22 |
| 300 | 33 | 3.9 | 8.2 | 6.8 |
| 500 | 22 | 1.8 | 6.8 | 3.3 |
| 1000 | 8 | 1.0 | 3.3 | 1.8 |

Tables 6 and 7 show the differential and common mode S-parameters for the amplifier by itself with 50Ω terminations on all ports. In addition, common mode terminations were used on the input and output ports having a value of 2pF in series with 50Ω .

The common mode feedback amplifier holds the common mode output voltage within about 20mV of the V_{CM} pin voltage. The V_{CM} pin interface is shown in Figure 13. The V_{CM} pin should be driven by a voltage source with an output impedance lower than $1\text{k}\Omega$. When the V_{CM} pin is unbiased, the output common mode voltage will be held at a nominal 0.9V given by the internal voltage divider formed by the 40k and 8k resistors. Connecting the V_{CM} pin to an ADC common mode reference pin allows the output common mode voltage of the IF amplifier to track the ADC common mode.

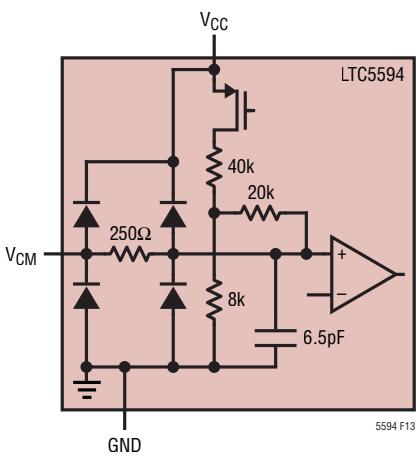


Figure 13. Simplified Schematic of the V_{CM} Input Pin

Table 6. IF Amplifier S-Parameters (Differential-Mode)

| IF (MHz) | S_{11} | | S_{21} | | S_{12} | | S_{22} | |
|-------------|----------|--------|----------|--------|----------|-------|----------|--------|
| | MAG | ANG | MAG | ANG | MAG | ANG | MAG | ANG |
| 0.001 | 0.204 | -179.9 | 2.129 | 180.0 | 1.8e-4 | 164.8 | 0.014 | 178.5 |
| 100 | 0.203 | 176.0 | 2.154 | 171.9 | 5.4e-4 | 118.0 | 0.026 | -120.9 |
| 200 | 0.205 | 172.2 | 2.170 | 163.7 | 1.0e-4 | 102.8 | 0.050 | -112.0 |
| 300 | 0.207 | 168.5 | 2.197 | 155.6 | 1.7e-4 | 92.8 | 0.079 | -113.5 |
| 400 | 0.210 | 164.8 | 2.239 | 147.3 | 2.8e-4 | 93.7 | 0.111 | -118.3 |
| 500 | 0.215 | 160.9 | 2.292 | 138.8 | 3.2e-4 | 95.4 | 0.147 | -125.0 |
| 600 | 0.221 | 157.0 | 2.363 | 130.1 | 4.0e-4 | 92.0 | 0.186 | -132.1 |
| 700 | 0.227 | 153.0 | 2.445 | 121.2 | 5.0e-4 | 92.1 | 0.230 | -140.0 |
| 800 | 0.235 | 149.0 | 2.535 | 112.0 | 5.5e-4 | 86.2 | 0.279 | -148.1 |
| 900 | 0.242 | 144.6 | 2.642 | 102.0 | 6.9e-4 | 93.2 | 0.334 | -157.0 |
| 1000 | 0.251 | 140.6 | 2.770 | 92.3 | 7.9e-4 | 92.7 | 0.396 | -166.2 |
| 1500 | 0.303 | 117.6 | 3.420 | 32.3 | 0.003 | 92.6 | 0.738 | 134.4 |
| 2000 | 0.365 | 90.2 | 3.318 | -45.5 | 0.005 | 33.2 | 0.828 | 70.0 |
| 2500 | 0.385 | 56.1 | 2.232 | -105.2 | 0.005 | -3.1 | 0.666 | 13.1 |
| 3000 | 0.365 | 16.6 | 2.620 | -160.2 | 0.005 | -34.2 | 0.488 | -38.4 |
| 3500 | 0.319 | -28.2 | 1.021 | 157.4 | 0.005 | -61.9 | 0.418 | -94.7 |
| 4000 | 0.307 | -83.4 | 0.742 | 113.3 | 0.005 | -79.5 | 0.409 | -150.6 |

Table 7. IF Amplifier S-Parameters (Common Mode)

| IF (MHz) | S_{11} | | S_{21} | | S_{12} | | S_{22} | |
|-------------|----------|--------|----------|--------|----------|--------|----------|--------|
| | MAG | ANG | MAG | ANG | MAG | ANG | MAG | ANG |
| 0.001 | 0.184 | -138.7 | 9.2e-4 | -112.8 | 0.037 | -65.3 | 0.985 | 179.8 |
| 100 | 0.186 | 172.5 | 0.085 | -118.9 | 0.013 | -68.6 | 0.152 | 126.7 |
| 200 | 0.188 | 166.6 | 0.173 | -134.7 | 0.007 | -91.8 | 0.125 | 116.7 |
| 300 | 0.191 | 160.2 | 0.237 | -150.0 | 0.004 | -113.1 | 0.097 | 97.3 |
| 400 | 0.196 | 154.4 | 0.291 | -163.8 | 0.002 | -145.4 | 0.067 | 75.2 |
| 500 | 0.202 | 148.4 | 0.340 | -176.8 | 0.002 | 170.2 | 0.037 | 43.6 |
| 600 | 0.210 | 142.8 | 0.387 | 170.9 | 0.002 | 137.0 | 0.023 | -38.0 |
| 700 | 0.219 | 137.2 | 0.436 | 159.1 | 0.003 | 118.1 | 0.051 | -97.8 |
| 800 | 0.230 | 132.0 | 0.488 | 147.1 | 0.003 | 107.8 | 0.094 | -121.5 |
| 900 | 0.243 | 126.5 | 0.550 | 134.9 | 0.004 | 106.6 | 0.148 | -137.0 |
| 1000 | 0.252 | 120.9 | 0.612 | 122.2 | 0.006 | 104.8 | 0.211 | -151.3 |
| 1500 | 0.325 | 96.7 | 0.981 | 43.4 | 0.020 | 80.4 | 0.749 | 136.1 |
| 2000 | 0.438 | 72.1 | 0.776 | -46.1 | 0.036 | 18.6 | 1.005 | 55.9 |
| 2500 | 0.549 | 40.1 | 0.496 | -97.1 | 0.041 | -21.9 | 0.873 | 2.9 |
| 3000 | 0.601 | 6.9 | 0.397 | -143.2 | 0.042 | -52.2 | 0.764 | -37.3 |
| 3500 | 0.618 | -27.5 | 0.281 | -175.7 | 0.044 | -80.3 | 0.668 | -72.7 |
| 4000 | 0.595 | -60.3 | 0.254 | 147.3 | 0.046 | -101.2 | 0.620 | -107.0 |

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Temperature Diode

A schematic of the TEMP pin is shown in Figure 14. The temperature diode can be used to directly measure the die temperature. A 40k resistor is recommended to V_{CC} to generate a 100 μ A current source for the diode readout. The temperature slope is about $-1.52\text{mV}/^\circ\text{C}$.

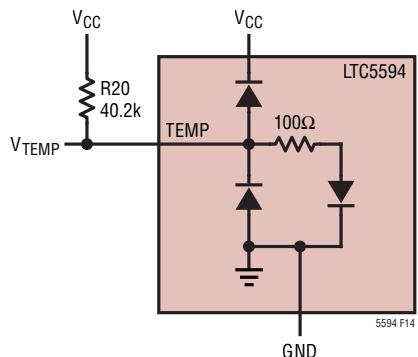


Figure 14. Schematic of the TEMP Pin

Enable Interface

A simplified schematic of the EN pin is shown in Figure 15. The enable voltage necessary to turn on the LTC5594 is $0.7 \cdot \text{OV}_{\text{DD}}$. To disable or turn off the chip, this voltage should be below $0.3 \cdot \text{OV}_{\text{DD}}$. If the EN pin is not connected, the chip is disabled. An internal 200k Ω pull-down keeps the part in shutdown mode if the pin is left floating. The LTC5594 can be put into a lower current sleep mode through the serial interface by writing 0x00 to register 0x16. This will dis-

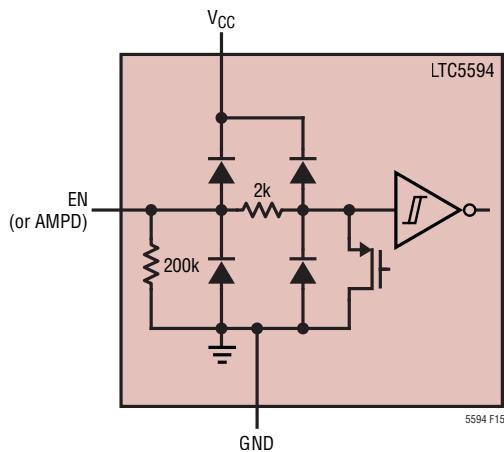


Figure 15. Simplified Schematic of the EN (or AMPD) Pin Interface

able the demodulator, amplifier, DC offset, and nonlinearity adjust circuits which are controlled by the EDEM, EAMP, EDC, and EADJ bits. Alternatively, writing any combination of bits to the four MSB's of register 0x16 will enable or disable the individual circuit blocks.

AMPD Interface

Also shown in Figure 15 is the simplified schematic for the AMPD IF amplifier disable pin. The IF amplifiers are enabled if the logical AND of AMPD and the EAMP register is 1. The IF amplifier state is detailed in Table 8.

Table 8. IF Amplifier State vs Logic Levels

| EAMP Register | AMPD Pin | |
|---------------|----------|-----|
| | 0 | 1 |
| 0 | OFF | OFF |
| 1 | ON | OFF |

Digital Input Pins

Figure 16 shows the simplified schematics for the digital input pins, SCK, CSB, and SDI. These pins should not be left floating, since there is no internal pull-down or pull-up.

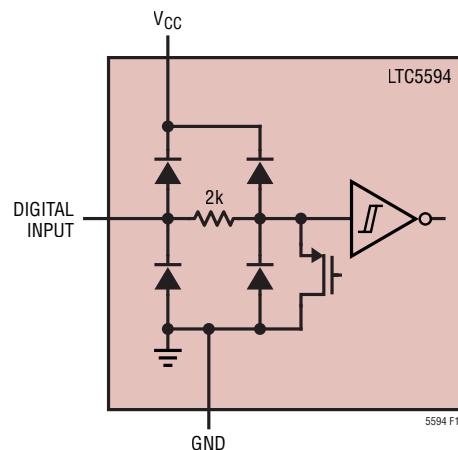


Figure 16. Simplified Schematic of the Digital Input Pins (SCK, CSB, SDI)

OV_{DD} Interface

Figure 17 shows the simplified schematic of the OV_{DD} interface. The OV_{DD} pin supplies the voltage for the digital inputs and SDO pin. By setting the pin at 1.2V to 3.3V, the serial port can function with 1.2V to 3.3V logic levels. It is important that when sequencing the supply voltages for

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the chip that the V_{CC} supply be brought up first before the OV_{DD} supply. This is to prevent the ESD diode connected between OV_{DD} and V_{CC} from getting damaged.

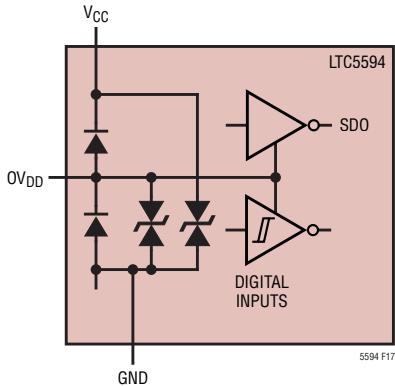


Figure 17. Simplified Schematic of the OV_{DD} Pin Interface

SERIAL PORT

The SPI compatible serial port provides control and monitoring functionality.

Communication Sequence

The serial bus is comprised of CSB, SCK, SDI and SDO. Data transfers to the part are accomplished by the serial bus master device first taking CSB low to enable the LTC5594's port. Input data applied on SDI is clocked on the rising edge of SCK, with all transfers MSB first. The communication burst is terminated by the serial bus master returning CSB high. See the timing diagrams for details.

Data is read from the part during a communication burst using SDO. Readback may be multidrop (more than one LTC5594 or other serial device connected in parallel on the serial bus), as SDO is high impedance (Hi-Z) when CSB = 1.

Single Byte Transfers

The serial port is arranged as a simple memory map, with status and control available in 23 registers as shown in the appendix. All data bursts are comprised of at least two 8-bit bytes. The most significant bit of the first byte is the read/write bit. Setting this bit to 1 puts the serial port into read mode. The next 7 bits of the first byte are address bits and can be set from 0x00 to 0x17. The subsequent byte, or bytes, is data from/to the specified register address. See the timing diagrams for details. Note that the written

data is transferred to the internal register at the falling edge of the 16th clock cycle (parallel load).

Multiple Byte Transfers

More efficient data transfer of multiple bytes is accomplished by using the LTC5594's register address auto-increment feature as shown in the timing diagram. The serial port master sends the destination register address in the first byte and reads or writes data in the second byte as before, but on the third byte the address pointer is auto-incremented by 1 and the serial port master can read or write to subsequent registers. If the register address pointer attempts to increment past 23 (0x17), it is automatically reset to 0.

SDO_MODE Control Bit

The SDO output has two modes of operation as shown in the timing diagram. When register 0x16 control bit SDO_MODE = 0, the SDO pin functions as a normal output which is Hi-Z during a write command. If SDO_MODE = 1, the SDO output is put into a serial repeater mode where SDO echos the command written to SDI before readback of register contents either in read or write mode. This can be used in high bus noise environments where it is necessary to perform error checking on commands sent to the serial port.

A simplified schematic of the SDO output is shown in Figure 18. The OV_{DD} supply sets the logic level of the output, and a 25Ω series resistor limits the output current.

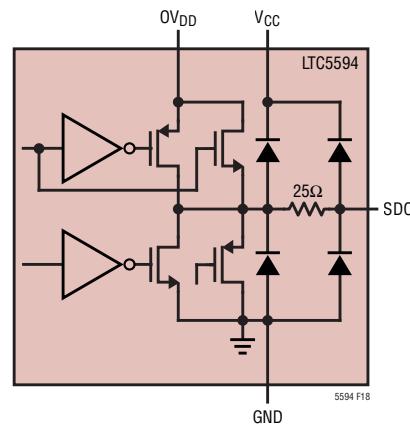


Figure 18. Simplified Schematic of the SDO Pin Interface

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Register Defaults

The register map and defaults are given in Tables 9 and 10 in the Appendix. When the device is powered up, the registers may not be reset to their default values. By writing a 1 to the SRST bit (bit[3]) of register 0x16, the device will go into soft reset and the registers will be reset to their default values.

Impairment Minimization

The LTC5594 contains circuitry for minimizing receiver impairments such as DC offset, phase and gain error, and nonlinearity. An example block diagram of a receiver

application is shown in Figure 19. A 2-tone source signal is applied to the RF input and the I and Q ADC outputs are measured in the digital domain to determine the optimized register settings in the LTC5594 for minimization of the impairments.

Figure 20 shows the nonoptimized baseband spectrum and Figure 21 shows the optimized baseband spectrum for a 2-tone test signal at 5.8GHz.

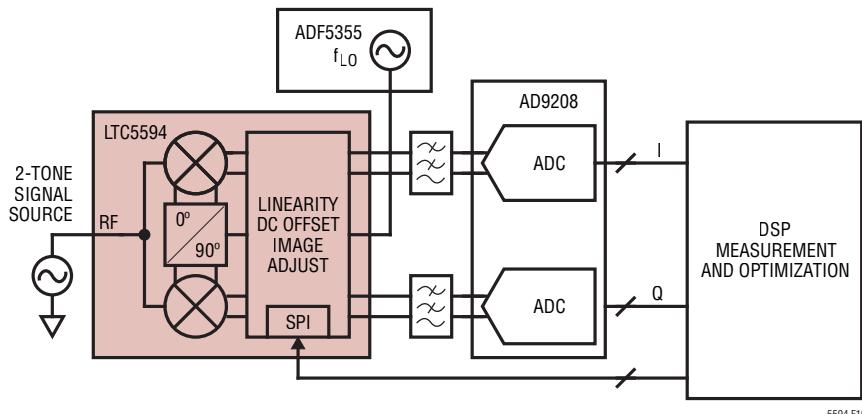


Figure 19. Example Block Diagram of a Receiver with 2-Tone Test Signal for Impairment Minimization

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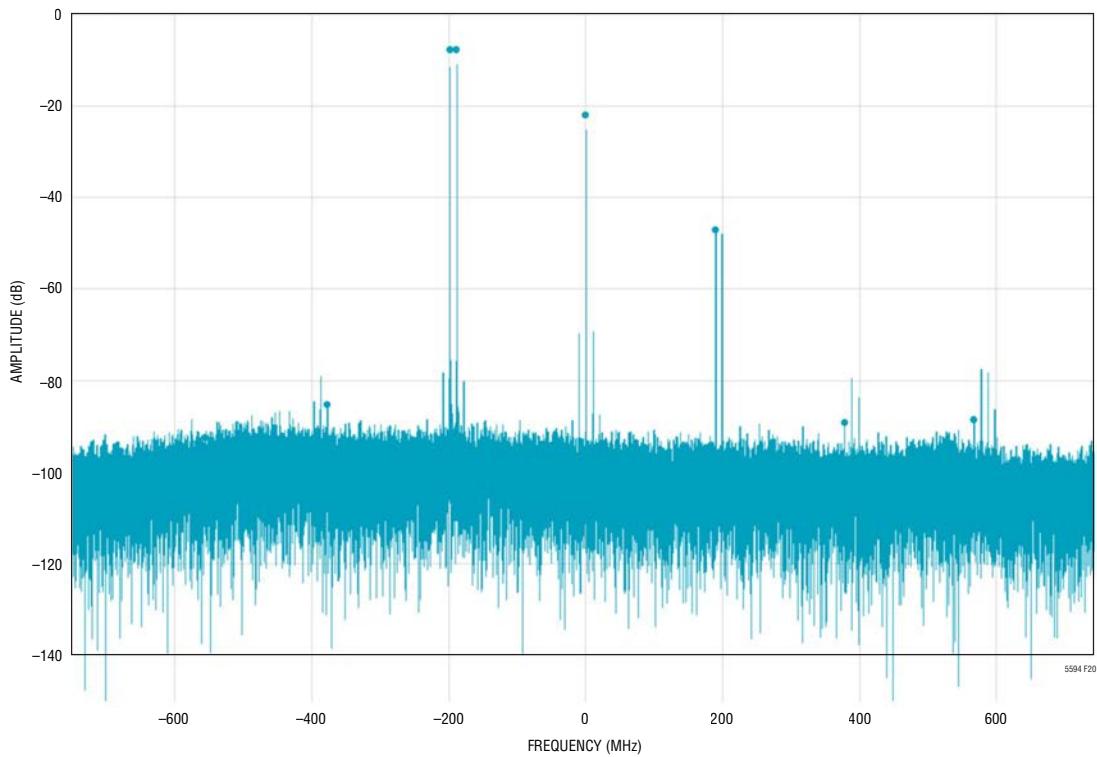


Figure 20. Nonoptimized 2-Tone Spectrum at 5.8GHz with 1GHz Anti-Alias Filter

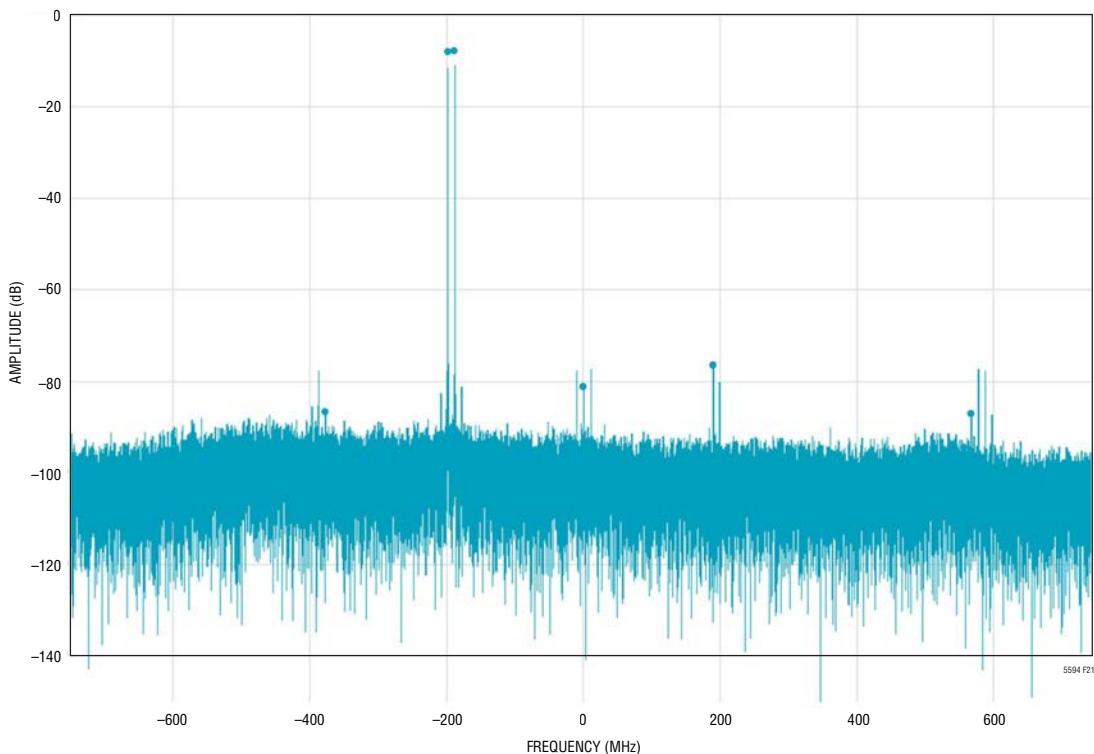


Figure 21. Optimized 2-Tone Spectrum at 5.8GHz with 1GHz Anti-Alias Filter

APPENDIX**Table 9. Serial Port Register Contents**

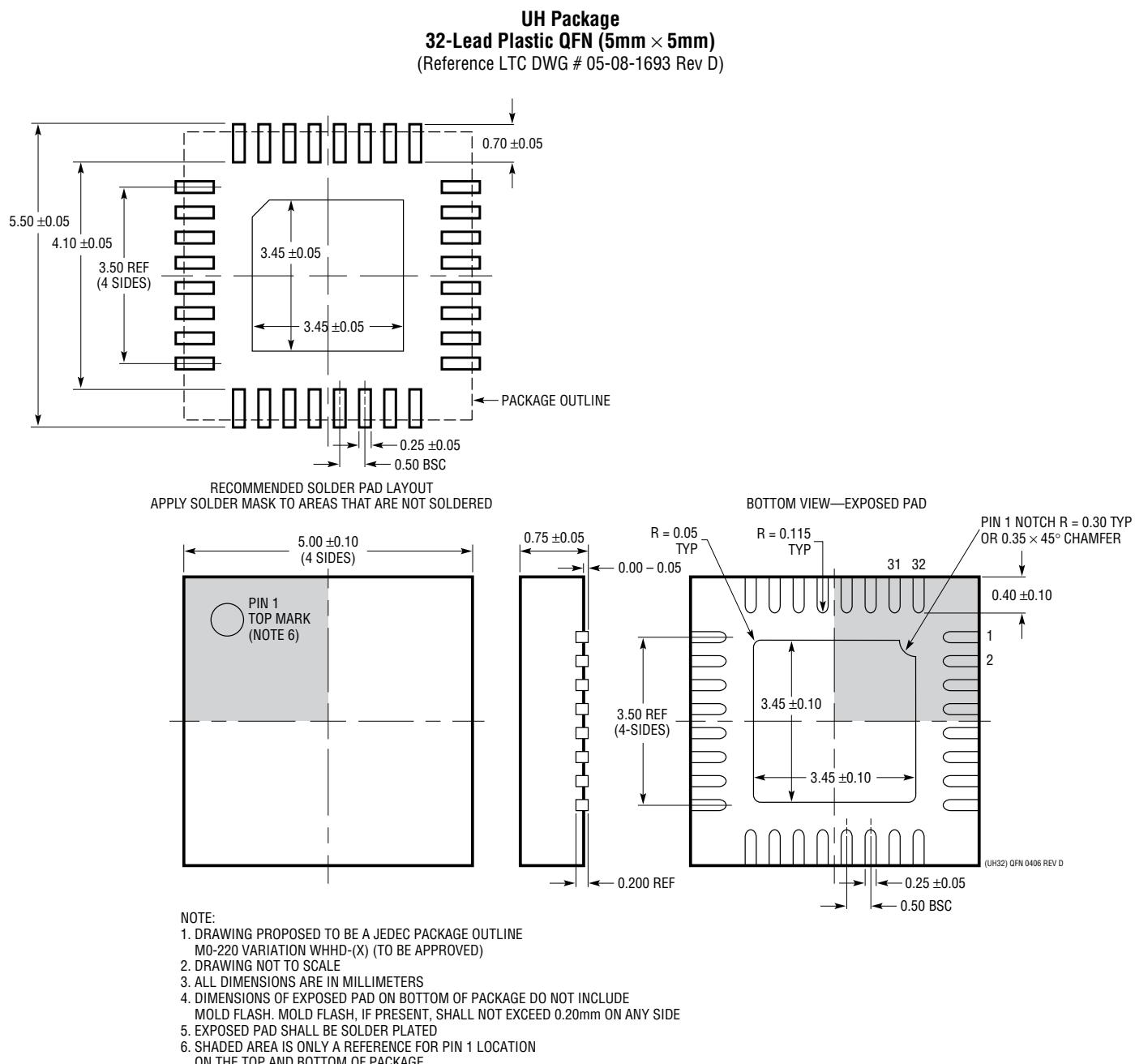
| ADDR | MSB | [6] | [5] | [4] | [3] | [2] | [1] | LSB | R/W | DEFAULT |
|-------------|------------|-----------|----------|----------|----------|----------|----------|------------|------------|----------------|
| 0x00 | IM3QY[7] | IM3QY[6] | IM3QY[5] | IM3QY[4] | IM3QY[3] | IM3QY[2] | IM3QY[1] | IM3QY[0] | R/W | 0x80 |
| 0x01 | IM3QX[7] | IM3QX[6] | IM3QX[5] | IM3QX[4] | IM3QX[3] | IM3QX[2] | IM3QX[1] | IM3QX[0] | R/W | 0x80 |
| 0x02 | IM3IY[7] | IM3IY[6] | IM3IY[5] | IM3IY[4] | IM3IY[3] | IM3IY[2] | IM3IY[1] | IM3IY[0] | R/W | 0x80 |
| 0x03 | IM3IX[7] | IM3IX[6] | IM3IX[5] | IM3IX[4] | IM3IX[3] | IM3IX[2] | IM3IX[1] | IM3IX[0] | R/W | 0x80 |
| 0x04 | IM2QX[7] | IM2QX[6] | IM2QX[5] | IM2QX[4] | IM2QX[3] | IM2QX[2] | IM2QX[1] | IM2QX[0] | R/W | 0x80 |
| 0x05 | IM2IX[7] | IM2IX[6] | IM2IX[5] | IM2IX[4] | IM2IX[3] | IM2IX[2] | IM2IX[1] | IM2IX[0] | R/W | 0x80 |
| 0x06 | HD3QY[7] | HD3QY[6] | HD3QY[5] | HD3QY[4] | HD3QY[3] | HD3QY[2] | HD3QY[1] | HD3QY[0] | R/W | 0x80 |
| 0x07 | HD3QX[7] | HD3QX[6] | HD3QX[5] | HD3QX[4] | HD3QX[3] | HD3QX[2] | HD3QX[1] | HD3QX[0] | R/W | 0x80 |
| 0x08 | HD3IY[7] | HD3IY[6] | HD3IY[5] | HD3IY[4] | HD3IY[3] | HD3IY[2] | HD3IY[1] | HD3IY[0] | R/W | 0x80 |
| 0x09 | HD3IX[7] | HD3IX[6] | HD3IX[5] | HD3IX[4] | HD3IX[3] | HD3IX[2] | HD3IX[1] | HD3IX[0] | R/W | 0x80 |
| 0x0A | HD2QY[7] | HD2QY[6] | HD2QY[5] | HD2QY[4] | HD2QY[3] | HD2QY[2] | HD2QY[1] | HD2QY[0] | R/W | 0x80 |
| 0x0B | HD2QX[7] | HD2QX[6] | HD2QX[5] | HD2QX[4] | HD2QX[3] | HD2QX[2] | HD2QX[1] | HD2QX[0] | R/W | 0x80 |
| 0x0C | HD2IY[7] | HD2IY[6] | HD2IY[5] | HD2IY[4] | HD2IY[3] | HD2IY[2] | HD2IY[1] | HD2IY[0] | R/W | 0x80 |
| 0x0D | HD2IX[7] | HD2IX[6] | HD2IX[5] | HD2IX[4] | HD2IX[3] | HD2IX[2] | HD2IX[1] | HD2IX[0] | R/W | 0x80 |
| 0x0E | DCOI[7] | DCOI[6] | DCOI[5] | DCOI[4] | DCOI[3] | DCOI[2] | DCOI[1] | DCOI[0] | R/W | 0x80 |
| 0x0F | DCOQ[7] | DCOQ[6] | DCOQ[5] | DCOQ[4] | DCOQ[3] | DCOQ[2] | DCOQ[1] | DCOQ[0] | R/W | 0x80 |
| 0x10 | 0* | 0* | 0* | 0* | 0* | IP3IC[2] | IP3IC[1] | IP3IC[0] | R/W | 0x04 |
| 0x11 | GERR[5] | GERR[4] | GERR[3] | GERR[2] | GERR[1] | GERR[0] | IP3CC[1] | IP3CC[0] | R/W | 0x82 |
| 0x12 | LVCM[2] | LVCM[1] | LVCM[0] | CF1[4] | CF1[3] | CF1[2] | CF1[1] | CF1[0] | R/W | 0x48 |
| 0x13 | BAND | LF1[1] | LF1[0] | CF2[4] | CF2[3] | CF2[2] | CF2[1] | CF2[0] | R/W | 0xE3 |
| 0x14 | PHA[8] | PHA[7] | PHA[6] | PHA[5] | PHA[4] | PHA[3] | PHA[2] | PHA[1] | R/W | 0x80 |
| 0x15 | PHA[0] | AMPG[2] | AMPG[1] | AMPG[0] | AMPCC[1] | AMPCC[0] | AMPIC[1] | AMPIC[0] | R/W | 0x6A |
| 0x16 | EDEM | EDC | EADJ | EAMP | SRST | SDO_MODE | 0* | 0* | R/W | 0xF0 |
| 0x17 | CHIPID[1] | CHIPID[0] | 0* | 0* | 0* | 0* | 0* | 1* | R/W | 0x01 |

*Unused, do not change default value.

APPENDIX**Table 10. Serial Port Register Bit Field Summary**

| BITS | FUNCTION | DESCRIPTION | VALID VALUES | DEFAULT |
|-------------|-----------------------------------|--|---------------------|----------------|
| AMPCC[1:0] | IF Amplifier IM3 CC Adjust | Used to optimize the IF amplifier IM3. | 0x00 to 0x03 | 0x02 |
| AMPIC[1:0] | IF Amplifier IM3 IC Adjust | Used to optimize the IF amplifier IM3. | 0x00 to 0x03 | 0x02 |
| AMPG[2:0] | IF Amplifier Gain Adjust | Adjusts the amplifier gain from 8dB to 15dB. | 0x00 to 0x07 | 0x06 |
| BAND | LO Band Select | Selects which LO matching band is used. BAND = 1 for high band. BAND = 0 for low band. | 0, 1 | 1 |
| CF1[5:0] | LO Matching Capacitor CF1 | Controls the CF1 capacitor in the LO matching network. | 0x00 to 0x1F | 0x08 |
| CF2[5:0] | LO Matching Capacitor CF2 | Controls the CF2 capacitor in the LO matching network. | 0x00 to 0x1F | 0x03 |
| CHIPID | Chip Identification Bits | Factory set to default value. | 0x00 to 0x03 | 0x00 |
| DCO1[7:0] | I-Channel DC Offset | Controls the I-channel DC offset over a range from -200mV to 200mV. | 0x00 to 0xFF | 0x80 |
| DCOQ[7:0] | Q-Channel DC Offset | Controls the Q-channel DC offset over a range from -200mV to 200mV. | 0x00 to 0xFF | 0x80 |
| EADJ | Enable Nonlinearity Adjust | Enables the nonlinearity adjustment circuitry if EADJ = 1. | 0, 1 | 1 |
| EAMP | Enable IF Amplifiers | Enables the IF amplifiers if EAMP = 1. | 0, 1 | 1 |
| EDC | Enable DC Offset Adjust | Enables the DC offset adjustment circuitry if EDC = 1. | 0, 1 | 1 |
| EDEM | Enable Demodulator | Enables the demodulator circuitry if EDEM = 1. | 0, 1 | 1 |
| GERR[5:0] | I _Q Gain Error Adjust | Controls the I _Q gain error over a range from -0.5dB to 0.5dB. | 0x00 to 0x3F | 0x20 |
| HD2IX[7:0] | HD2 I-Channel X-Vector | Controls the I-channel HD2 X-vector adjustment if EADJ = 1. | 0x00 to 0xFF | 0x80 |
| HD2IY[7:0] | HD2 I-Channel Y-Vector | Controls the I-channel HD2 Y-vector adjustment if EADJ = 1. | 0x00 to 0xFF | 0x80 |
| HD2QX[7:0] | HD2 Q-Channel X-Vector | Controls the Q-channel HD2 X-vector adjustment if EADJ = 1. | 0x00 to 0xFF | 0x80 |
| HD2QY[7:0] | HD2 Q-Channel Y-Vector | Controls the Q-channel HD2 Y-vector adjustment if EADJ = 1. | 0x00 to 0xFF | 0x80 |
| HD3IX[7:0] | HD3 I-Channel X-Vector | Controls the I-channel HD3 X-vector adjustment if EADJ = 1. | 0x00 to 0xFF | 0x80 |
| HD3IY[7:0] | HD3 I-Channel Y-Vector | Controls the I-channel HD3 Y-vector adjustment if EADJ = 1. | 0x00 to 0xFF | 0x80 |
| HD3QX[7:0] | HD3 Q-Channel X-Vector | Controls the Q-channel HD3 X-vector adjustment if EADJ = 1. | 0x00 to 0xFF | 0x80 |
| HD3QY[7:0] | HD3 Q-Channel Y-Vector | Controls the Q-channel HD3 Y-vector adjustment if EADJ = 1. | 0x00 to 0xFF | 0x80 |
| IM2IX[7:0] | IM2 I-Channel X-Vector | Controls the I-channel IM2 X-vector adjustment if EADJ = 1. | 0x00 to 0xFF | 0x80 |
| IM2QX[7:0] | IM2 Q-Channel X-Vector | Controls the Q-channel IM2 X-vector adjustment if EADJ = 1. | 0x00 to 0xFF | 0x80 |
| IM3IX[7:0] | IM3 I-Channel X-Vector | Controls the I-channel IM3 X-vector adjustment if EADJ = 1. | 0x00 to 0xFF | 0x80 |
| IM3IY[7:0] | IM3 I-Channel Y-Vector | Controls the I-channel IM3 Y-vector adjustment if EADJ = 1. | 0x00 to 0xFF | 0x80 |
| IM3QX[7:0] | IM3 Q-Channel X-Vector | Controls the Q-channel IM3 X-vector adjustment if EADJ = 1. | 0x00 to 0xFF | 0x80 |
| IM3QY[7:0] | IM3 Q-Channel Y-Vector | Controls the Q-channel IM3 Y-vector adjustment if EADJ = 1. | 0x00 to 0xFF | 0x80 |
| IP3CC[1:0] | RF Input IP3 CC Adjust | Used to optimize the RF input IP3. | 0x00 to 0x03 | 0x02 |
| IP3IC[2:0] | RF Input IP3 IC Adjust | Used to optimize the RF input IP3. | 0x00 to 0x07 | 0x04 |
| LF1[1:0] | LO Matching Inductor LF1 | Controls the LF1 inductor in the LO matching network. | 0x00 to 0x03 | 0x03 |
| LVCM[2:0] | LO Bias Adjust | Used to optimize mixer IP3. | 0x00 to 0x07 | 0x02 |
| PHA[8:0] | I _Q Phase Error Adjust | Controls the I _Q phase error over a range from -2.5 Degrees to 2.5 Degrees. | 0x000 to 0x1FF | 0x100 |
| SDO_MODE | SDO Readback Mode | Enables the SDO readback mode if SDO_MODE = 1. | 0, 1 | 0 |
| SRST | Soft Reset | Writing 1 to this bit resets all registers to their default values. | 0, 1 | 0 |

PACKAGE DESCRIPTION



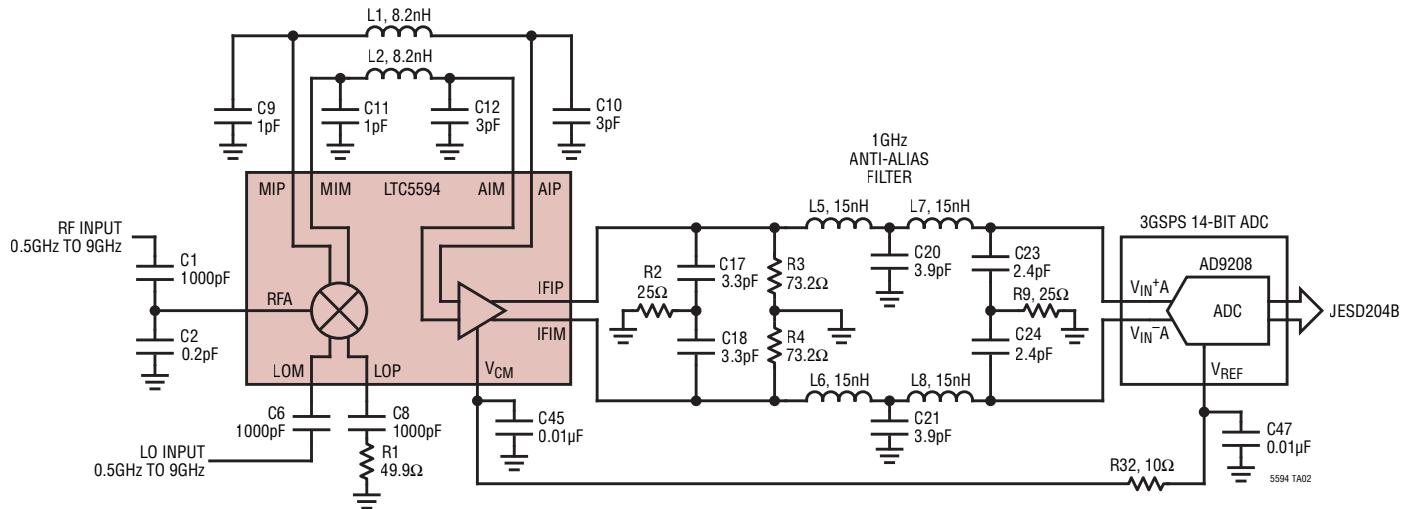
REVISION HISTORY

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|-----|-------|--------------------------------|-------------|
| A | 06/18 | Added $T_J = 25^\circ\text{C}$ | 5, 7 |

LTC5594

TYPICAL APPLICATION

Simplified Schematic of a 0.5GHz to 9.0GHz Receiver, (Only I-Channel Is Shown)



RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|------------------------------------|---|--|
| Infrastructure | | |
| LTC5553 | 3GHz to 20GHz Microwave Mixer with 500MHz to 9GHz IF | Up-or-Down Conversion, 21.5dBm IIP3 at 17GHz, 0dBm LO Drive |
| LTC5552 | 3GHz to 20GHz Microwave Mixer with DC to 6GHz IF | Up-or-Down Conversion, 18.3dBm IIP3 at 17GHz, 0dBm LO Drive |
| LTC5549 | 2GHz to 14GHz Mixer with Integrated LO Doubler | Ultra-Wideband Bidirectional Up-, or Down-Conversion Mixer, 22.8dBm IIP3 at 12GHz, 0dBm LO Drive, 500MHz to 6GHz IF Bandwidth |
| LTC5548 | 2GHz to 14GHz Mixer with IF Frequency Extending to DC | Ultra-Wideband Bidirectional Up-, or Down-Conversion Mixer, 18.7dBm IIP3 at 12GHz, 0dBm LO Drive with On-Chip Frequency Doubler, DC to 6GHz IF Bandwidth |
| LTC5588-1 | 200MHz to 6GHz Quadrature Modulator | 31dBm OIP3, -160dBm/Hz Output Noise Floor, Excellent ACPR Performance |
| LTC6433-15 | <100kHz to 1.4GHz High OIP3 Amplifier | Fixed 15dB Gain, Single-Ended 50Ω Input and Output, 41dBm OIP3 at 240MHz, 3.3dB NF |
| RF PLL/Synthesizer with VCO | | |
| ADF5355 | Microwave Wideband Synthesizer with Integrated VCO | 54MHz to 13.6GHz, -221dBc/Hz Normalized In-Band Phase Noise Floor |
| LTC6948 | Ultralow Noise Fractional-N Synthesizer with Integrated VCO | 370MHz to 6.39GHz PLL, No ΔΣ Modulator Spurs, 18-Bit Fractional Denominator, -226dBc/Hz Normalized In-Band Phase Noise Floor |
| ADCs | | |
| AD9208 | 14-Bit, 3GspS JESD204B Dual ADC | 70dB SFDR, Integrated Input Buffer |
| LTC2185 | 16-Bit, 125Msps 1.8V Dual ADC | 76.8dB SNR, 90dB SFDR, 185mW/Channel Power Consumption |
| LTC2158-14 | 14-Bit, 310Msps 1.8V Dual ADC, 1.25GHz Full-Power Bandwidth | 68.8dB SNR, 88dB SFDR, 362mW/Ch Power Consumption, 1.32V _{P-P} Input Range |