IYAD ALHASAN

2120 El Paseo St. • Houston, Texas 77054

(346)-625-5515 | inalhasan@uh.edu | LinkedIn Profile | Personal Website

PROFESSIONAL EXPERIENCE

- Golden Electronics, Amman, Jordan.
 - ASIC Digital Design & Verification Engineer (Team Lead) July 2021 August 2023:
 - Testing and debugging RTL code of 1G/10G/25G/40G/100G Ethernet's (802.3) PCS sublayer IP core.
 - o Code Coverage analysis and corner cases detection using VCS.
 - o Results reporting automation & flow automation using BASH, Python, TCL.
 - Run and debug errors occurring in RTL signoff flows such as Lint, CDC, RDC, Synthesis and Power intent (UPF) for Ethernet's (802.3) 1G/10G MAC sublayer IP core.
 - FMEDA & DFMEA automation scripts debug (TCL).
- Dimitri's Coffee Factory, Amman, Jordan.
 - IoT Engineer March 2021 June 2021:
 - Build various IoT sensor nodes targeting coffee roasting & brewing processes monitoring using custom designed PCB boards.
 - o PCB design using Altium.
 - o Products deployment in coffee House Branches and data collection for ML training purposes.

EDUCATION

- ➤ Master of Science in Computer & Systems Engineering: 2023 2025.
 - University of Houston, Houston, Texas. GPA: 4.0.
 - Relevant Coursework & Projects:
 - VLSI Design: Designed 2GHz Semi-Dynamic flipflop using Cadence Virtuoso (180nm technology).
 - CMOS Analog ICs: Designed a 2 Stage OPAMP and built a Butterworth filter using Cadence Virtuoso (180nm technology).
 - Digital Signal Processing: Designed a Filter to separate Morse code Hidden in Beethoven music using MATLAB.
 - Introduction to Cybersecurity.
 - RTOS for IoT: Designed a Clock and Calendar app using RTOS features developed in class.
 - Active Research Topic: Implementing an FPGA based hardware accelerator for Fully Homomorphic Encryption. Advisor: Dr. Biresh Joardar.
 - o **Teaching Projects:** FPGA Hardware acceleration guide. Link: <u>FPGA Acceleration Guide.</u>
- ▶ Bachelor of Science in Electrical Engineering: 2016 2021.
 - Jordan University of Science and Technology, Irbid, Jordan. GPA: 3.82.
 - Academic Graduation Project: Designed an LCL filter for Grid-Connected Source Converter and carried out all control & stability analysis using MATLAB & Simulink.

TECHNOLOGIES USED

- Languages: C, C++, TCL, Perl, Python, BASH, TCSH, System Verilog.
- ➤ **Tools:** MATLAB/Simulink, Synopsys Design Compiler, Synopsys Fusion Compiler, Synopsys Spyglass, Synopsys VC Spyglass, Synopsys VCS, Cadence Virtuoso, LT-Spice, Xilinx Vivado, Perforce, Git.
- Communication Protocols/Interfaces: Ethernet Protocol (802.3), AMBA Protocol (APB, AHP, AXI), XAUI.

> Achievements/Awards:

- Voted best in team & promoted to Team Lead (2022, Golden Electronics).
- Awarded a competitive scholarship by the University of Houston.
- **Extra-Curricular Work:** IEEE JUST Member, Science shows content creator at Naqsh, Kahrabji Team academic member, Design of a Prayer Times AI chatbot website, Electronics undergraduate courses teacher.
- > Work Eligibility: Eligible to work in the U.S.