IYAD ALHASAN

2120 El Paseo St. • Houston, Texas 77054

(346)-625-5515 | inalhasan@uh.edu | LinkedIn Profile | Personal Website

PROFESSIONAL EXPERIENCE

➢ Houston Methodist Hospital, Houston, Texas.

- **VRS Specialist • June 2024 - Present:**
  - Design of State-of-the-art Ultrasound Imaging Circuits.

➢ Golden Electronics, Amman, Jordan.

- **ASIC Digital Design & Verification Engineer • July 2021 - August 2023:**
  - Maintaining testbench of 1G/10G/25G/40G/100G Ethernet's (802.3) PCS sublayer IP cores and debugging RTL code.
  - Code Coverage analysis and corner cases detection using VCS.
  - Results reporting automation & flow automation using BASH, Python, TCL.
  - Debugging errors occurring in RTL signoff flows such as Lint, CDC, RDC, Synthesis and Power intent (UPF) for Ethernet's (802.3) 1G/10G MAC sublayer IP core.
  - FMEDA & DFMEA automation scripts debug (TCL).

➢ Dimitri's Coffee Factory, Amman, Jordan.

- **IoT Engineer • March 2021 - June 2021:**
  - Build various IoT sensor nodes targeting coffee roasting & brewing processes monitoring using custom designed PCB boards.
  - PCB design using Altium.
  - Products deployment in coffee House Branches and data collection for ML training purposes.

EDUCATION

➢ Master of Science in Computer Engineering: 2023 – 2025.

- **University of Houston, Houston, Texas. GPA: 4.0/4.0.**
  - **Relevant Coursework & Projects:**
    - **VLSI Design:** Designed 2GHz Semi-Dynamic flipflop using Cadence Virtuoso (180nm technology).
    - **CMOS Analog ICs:** Designed a 2 Stage OPAMP and built a Butterworth filter using Cadence Virtuoso (180nm technology).
    - **Digital Signal Processing:** Designed a Filter to extract Morse code hidden in Beethoven music using MATLAB.
    - **Introduction to Cybersecurity**.
    - **RTOS for IoT**: Designed a Clock and Calendar app using RTOS features developed in class.
    - **Advanced Computer Architecture:** Current Semester.
    - **Principles of Internetworking:** Current Semester.
  - **Active Research Topic:** Implementing FPGA hardware acceleration on CKKS Fully Homomorphic Encryption. **Advisor:** Dr. Biresh Joardar.
  - **Teaching Projects:** FPGA Hardware acceleration guide. Link: FPGA Acceleration Guide.

➢ Bachelor of Science in Electrical Engineering: 2016 – 2021.

- **Jordan University of Science and Technology, Irbid, Jordan. GPA: 3.82/4.0.**
  - **Academic Graduation Project:** Designed an LCL filter for Grid-Connected Source Converter and carried out all control & stability analysis using MATLAB & Simulink.

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TECHNOLOGIES USED

- **Languages:** C, Assembly, C++, TCL, Perl, Python, BASH, TCSH, Verilog, System Verilog, UVM.
- **Tools:** MATLAB, Simulink, Synopsys Design Compiler, Synopsys Fusion Compiler, Synopsys Spyglass, Synopsys VC Spyglass, Synopsys VCS, Cadence Virtuoso, LT-Spice, Xilinx Vivado, Perforce, Git.
- **Communication Protocols/Interfaces:** Ethernet Protocol (802.3), AMBA Protocol (APB, AHB, AXI), XAUI.

MISCELLANEOUS

- **Achievements/Awards:**
  - Voted best in team & promoted to Team Lead (2022, Golden Electronics).
  - Awarded a competitive scholarship by the University of Houston.
- **Extra-Curricular Work:** IEEE JUST Member, Science shows content creator at Naqsh, Kahrabji Team academic member, Design of a Prayer Times AI chatbot website, Electronics undergraduate courses teacher.
- **Skills:**
  - Design of OOP SystemVerilog testbenches.
  - Debugging functional issues using VCS & DVE tools.
  - Debugging CDC/RDC & Lint issues using Synopsys Spyglass/VC-Spyglass & Synopsys Design Compiler tools.
  - FPGA design using Xilinx Vivado.
  - Task automation using BASH/Python/TCL.
  - Deep understanding of Ethernet & AMBA Protocols.
- **Work Eligibility:** Eligible to work in the U.S.