BJT AMPLIFIER DESIGN

A report submitted to the

Department of Electrical and Information Engineering
Faculty of Engineering
University of Ruhuna Sri Lanka

On 20th of September 2023

In completing an assignment for the module
EE4105 Electronic Project

By:
Group 13

ABSTRACT

This report includes all the details of the project which was carried out under the module EE4105 Electronic Project. There we were given to design a CE amplifier with a given bandwidth and gain. So this report provides all the information of the process that we carried out by our group to fulfill the requirements of the project. The information has been detailed under the following topic.

1. Introduction

   This part includes a brief introduction to the design with problem statement, objectives and methodology.

2. Design of the Amplifier

   Here we have included the all the details of the circuit we designed with the necessary calculations and assumptions and then after the components we selected with the reasons for the selection.

3. Implementation of the Circuit

   This chapter contains the schematic and PCB layout that we designed through the Proteus Software and then the images of practically implemented circuit.

4. Results and Discussion

   This topic contains the details of Proteus simulation results, theoretical and experimental results and the discussion we have built through the observations that we got.

Therefore, this report includes all the necessary details of the design of CE amplifier under the specified chapters in detailed with the steps which we carried out throughout the project.

PREFACE

This electronic project explores the frontiers of electronic design, aiming to transcend conventional thinking and address real-world challenges. The team's journey is not just technical but also an exploration of possibilities. This project was conceived not merely as a technical endeavor but as an exploration of possibilities. Within these pages, you will find a detailed account of our project's objects, design, challenges faced, and the solutions that emerged. We would like extend to our gratitude to Dr. Achintha I. Kondarage, Mr. D. S. De Silva, module coordinators of this module.

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1 INTRODUCTION

The common emitter amplifier is a single-stage bipolar junction transistor (BJT) circuit. It takes its input from the base, collects its output from the collector, and shares the emitter connection between both terminals. This amplifier employs Voltage Divider Biasing, a common technique. It uses two resistors as a potential divider across the power supply, and the midpoint of this network provides the necessary base bias voltage for the transistor. This configuration is widely used in bipolar transistor amplifier circuits to establish the transistor's operating point, ensuring proper amplification characteristics. Therefore, the common emitter amplifier, a single-stage BJT circuit, utilizes voltage divider biasing for effective signal amplification.

1.1 PROBLEM STATEMENT

The project task was to implement a Common Emitter BJT amplifier with the following specifications.

- Voltage gain = 320
- Bandwidth of Low Pass Filter = 1.7 kHz

1.2 OBJECTIVES

- **Understand BJT Amplifiers:** Gain an understanding of the construction and operational principles of Bipolar Junction Transistor (BJT) amplifiers.
- **Component Value Calculation:** Determine the appropriate values for components like resistors and capacitors based on provided specifications for amplifier design.
- **Circuit Design and Simulation:** Create schematic diagrams and simulate the common emitter amplifier circuit design using suitable software or tools.
- **PCB Implementation:** Utilize PCB layout techniques to physically implement the amplifier circuit design on a printed circuit board (PCB).
- **3D Visualization:** Use a 3D visualizer to inspect and visualize the PCB layout for spatial understanding and error detection.
- **Theoretical vs. Experimental Comparison:** Analyze and compare the results obtained through theoretical calculations and simulations with the practical experimental results to evaluate the amplifier's performance.

1.3 METHODOLOGY

1. Gathering information about the BJT common emitter amplifier for component value calculations.
2. Selecting transistors based on the calculated values.
3. Determining a block diagram considering amplifier stages and filters.
4. Calculating component values for assigned characteristics.
5. Simulating the design using Proteus software.
6. Troubleshooting and fine-tuning the design.
7. Implementing the circuit on a PCB using Proteus software.
8. Evaluating theoretical and practical performance and reporting findings.
9. Presenting the final design and report.

2 DESIGN OF THE AMPLIFIER

2.1 CONSTRUCTION OF THE DESIGN

The amplifier design is expected to do two main operations.

- Amplifier part: according to our requirements, the input signal needs to amplify by 320 times.
- Filter part: the output signal need to attenuate by 3 dB when the input/output reaches to 1800 Hz.

The diagram shows the circuit design for the project and the stages.

Figure 2.1 Different stages for the circuit

- Input buffer: This is used to match the output impedance of the source and the input impedance of the amplifier.

  Gain ~ 1

- Filter: This is used to attenuate the input signal by 3dB to have bandwidth as 1700Hz

  Gain ~ 1

- Amplifier: The amplifier is used to amplify the input signal up to required amount of gain.

  Gain = 320

- Input buffer: This is used to match the output impedance of the amplifier and the input impedance of the load.

  Gain ~ 1

2.2 TRANSISTOR AND OPAMP SELECTION

2N2222 transistor is used for the implementation. The transistor is used for input butter, output buffer and for the amplifier. [1]

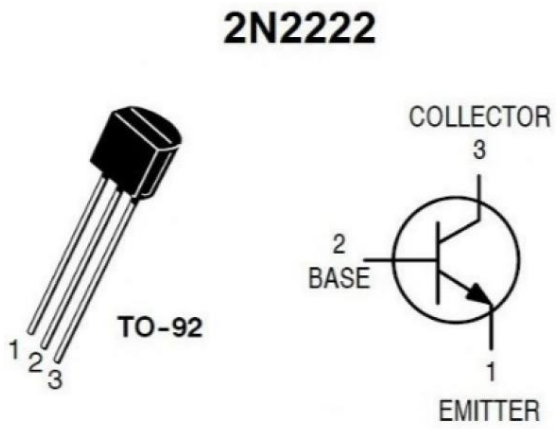


Figure 2.2 2N2222 transistor pin configuration

Transistor properties

- Collector current – 150 mA
- Collector-Emitter voltage – 10V
- Minimum gain – 100
- Maximum gain – 300

For the low pass filter LM741 IC is used. [2]

Figure 2.3 Image of LM741 IC

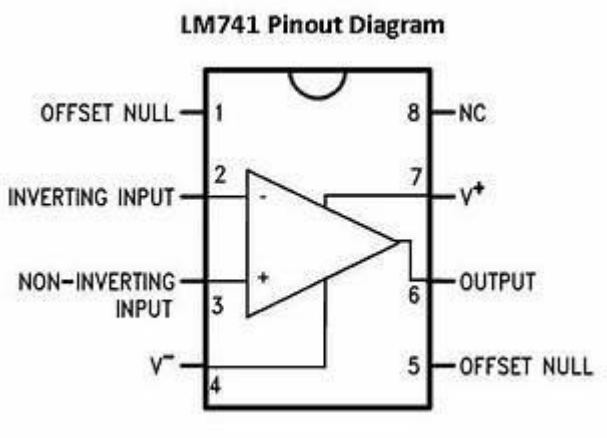


Figure 2.4 Pin diagram for the IC

2.3 CALCULATIONS

The section includes all the calculations related to the design. The calculations are done by isolating all the components to avoid the effects of other parts of the circuit. But the actual values and the calculated values have some differ, the deviations and the solutions are mentioned at the simulation part.

Voltage supply for used in the amplifier is 15V.

2.3.1 INPUT/OUTPUT BUFFERS

As input/output buffers, common collector amplifiers are used. They have fixed gain ≈ 1 and it resolves the impedance mismatch.

Construction of common-collector amplifier is shown below.

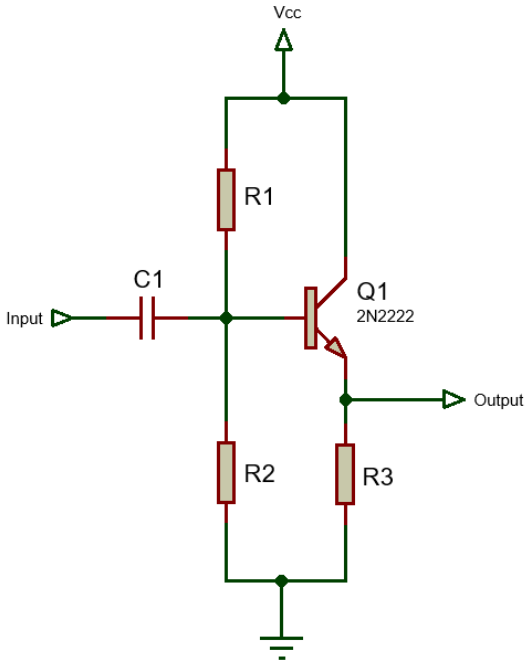


Figure 2.5 Circuit diagram of the input buffer

Calculations:

For a largest possible symmetric output voltage swing

$$V_E = \frac{V_{cc}}{2} = \frac{15}{2} = 7.5V$$

The Q point used for the calculations;

$$V_{CE} = 7.5V$$

$$I_C = 2.5mA$$

Here $I_C \approx I_E$

$$Emitter\ Resistor\ (R_E) = R_3 = \frac{V_E}{I_E}$$

$$R_E = \frac{7.5V}{2.5mA}$$

$$R_E = 3\text{k}\Omega$$

Base Voltage of Q_1 = V_B

$$V_B = V_E + 0.7V = 8.2V$$

R_1 and R_2 values to get the desired V_B,

$$V_B = \frac{R_2 \times V_{CC}}{R_1 + R_2}$$

$$8.2 = \frac{R_2 \times 15}{R_1 + R_2}$$

$$\frac{R_1}{R} = \frac{34}{41}$$

$$R_1 = 82k\Omega$$

$$R_2 = 100k\Omega$$

Input impedance of the buffer,

$$Z_{in} = R_1 \,||\, R_2 \,||\, [\beta r_E + (1+\beta)R_E]$$

Here $r_E \ll R_E$,

$$Z_{in} = R_1 \,||\, R_2 \,||\, \beta R_E$$

$$Z_{in} = 82 \,||\, 100 \,||\, 100 \times 1$$

$$Z_{in} = 31k\Omega$$

To get a lower cutoff frequency around 10Hz,

$$C_1 = \frac{1}{2\pi \times 10 \times 31000} \approx 1\mu F$$

Complete design of input/output buffer

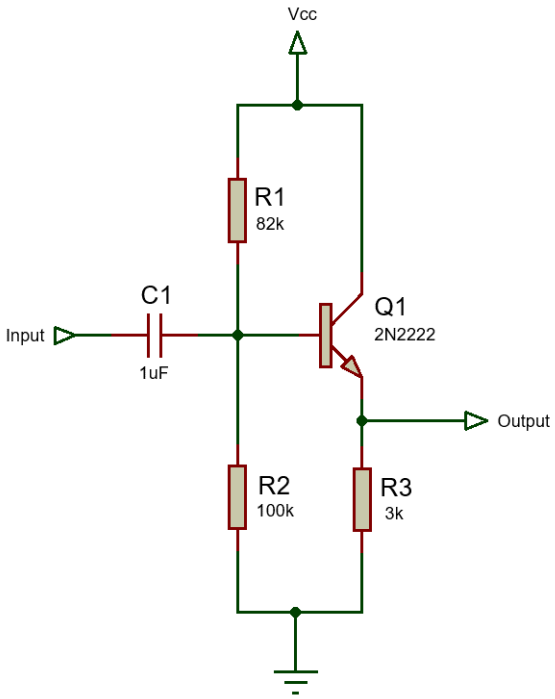


Figure 2.6 Final design of Input/output Buffer

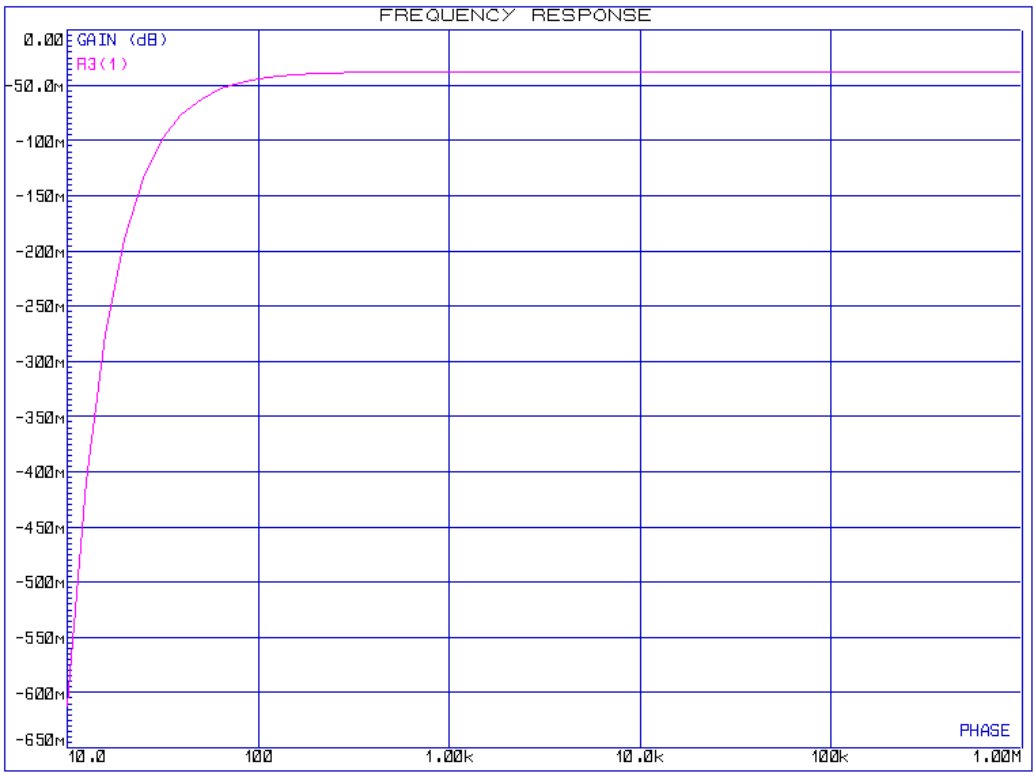


Figure 2.7 Frequency response of the input buffer stage

2.3.2 FILTER

The general configuration of second order Butterworth low pass filter is shown in the figure. Here, the figure 2.8 uses op-amp as the active component.

Here, the gain is needed to set as 1. Therefore, filter component values for unity gain filter design is calculated using the configuration.

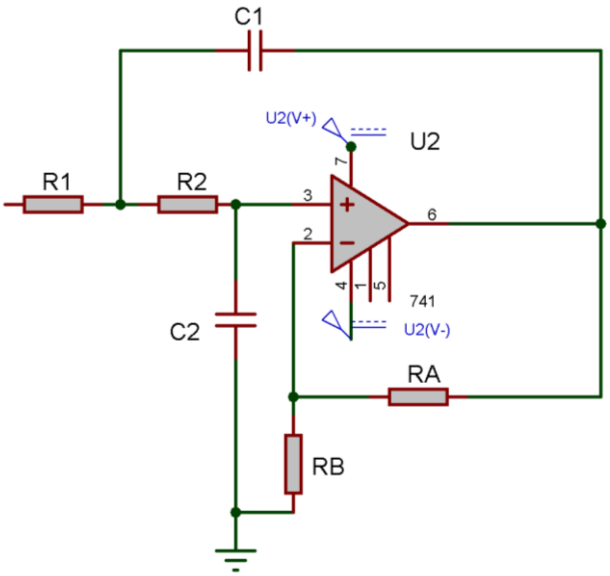


Figure 2.8 Configuration of second order Butterworth low pass filter

Calculations;

The calculations are done according to the attached filter coefficient table in the appendix

The value of capacitance, C is chosen as 33pF

$$K = \frac{10^{-4}}{fC} = \frac{10^{-4}}{1800 \times 33 \times 10^{-12}}$$

$$K = 1.683 \times 10^{3}$$

For unity gain buffer R_B is open and $R_A = 0$

- $R_1 = 1.683 \times 10^3 \times 1.422\ \Omega = 2.393\ k\Omega \approx 2.2\ k\Omega$
- $R_2 = 1.683 \times 10^3 \times 5.399\ \Omega = 9.086\ k\Omega \approx 10\ k\Omega$
- $R_A = Open$
- $R_B = 0$
- $C_1 = 0.33 \times 33 \times 10^{-12} F = 10.89\ pF \approx 10\ pF$
- $C_2 = C = 33\ pF$

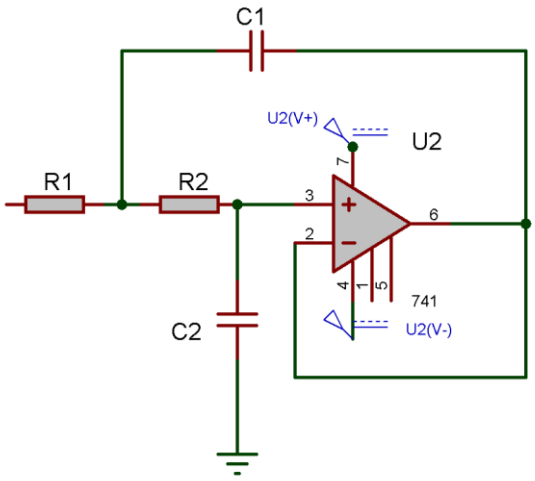


Figure 2.9 Configuration of second order Butterworth low pass filter with order =1

Complete filter design

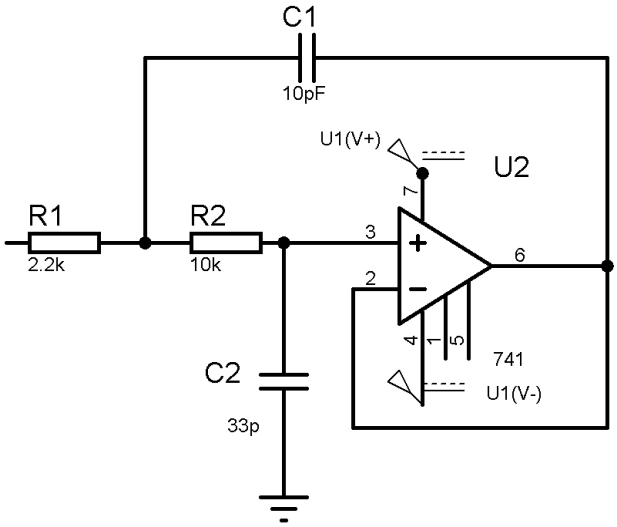
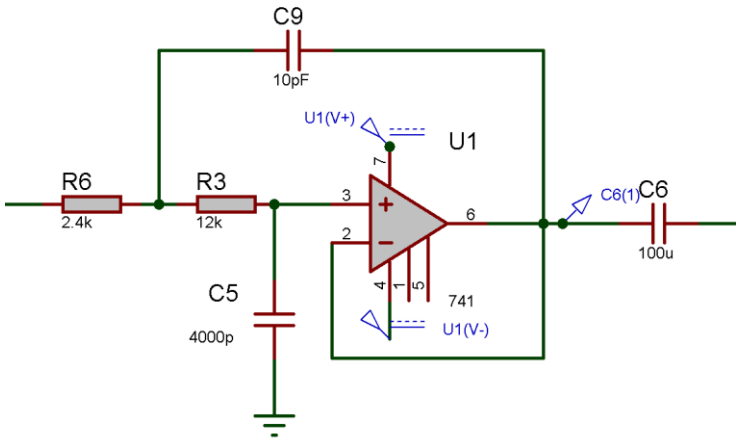


Figure 2.10 Complete filter design

Error resolving

The necessary output was not seen in the frequency response after combining all the stages into one circuit. That occurs, we assume, as a result of incorrect offset, mismatched input and output impedances, feedback or stability problems, noise, and interferences. As a result, rather of using the computed values, the values for the suitable need were added.

The tuned values together with the circuit are shown in the image below.



The frequency response of the low pass Butterworth filter is shown here.

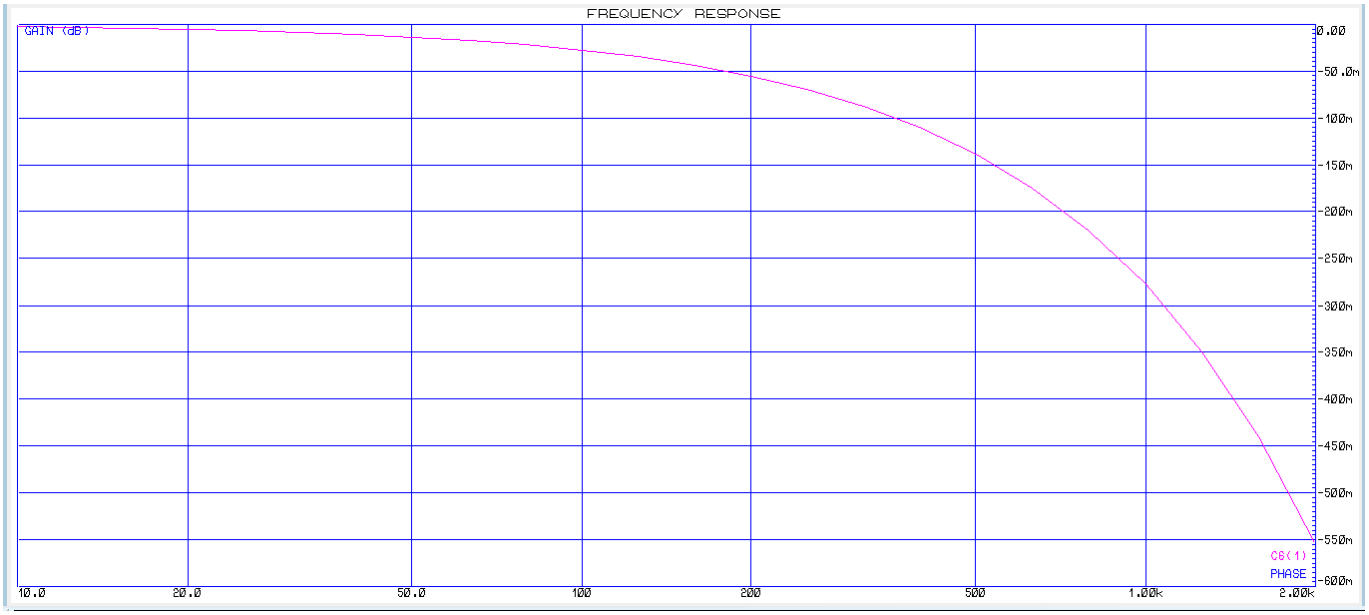


Figure 2.11 Frequency response of the filter stage

2.3.3 AMPLIFIER

To receive the required gain and to receive the required low cut off frequency BJT amplifier configuration was used. Here we used NPN Common Emitter Configuration. Here for the Common Emitter Amplifier voltage gain is medium although the power gain is high. But the phase relationship is 180 degrees between input and output.

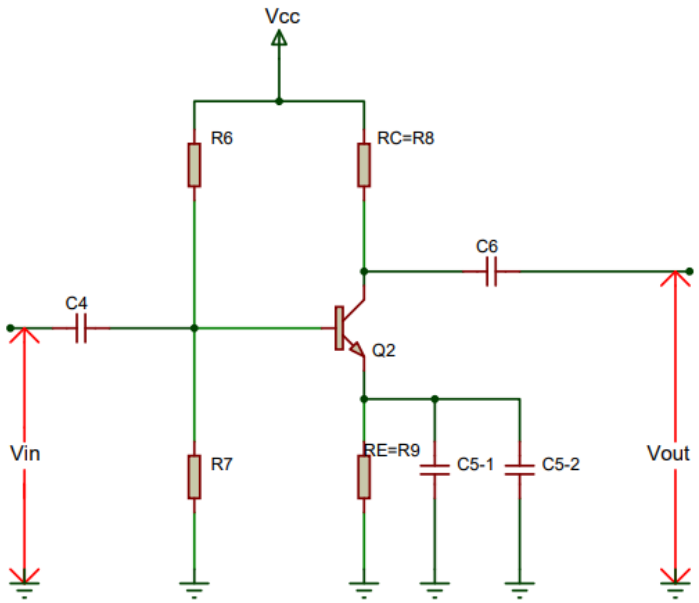


Figure 2.12 Circuit diagram of CE BJT amplifier

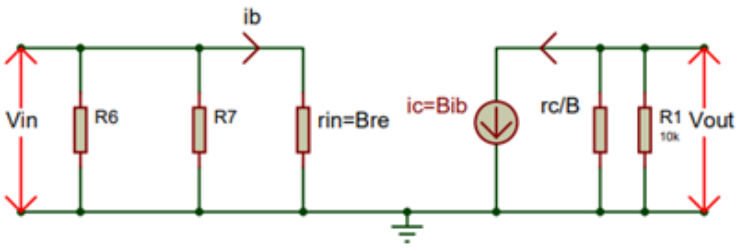


Figure 2.13 AC equivalent of CE BJT amplifier

AC Analysis:

$$i_e = i_c + i_b$$

$$i_c = \beta i_b$$

$$\therefore i_e = \beta i_b + i_b$$

$$\therefore i_b = \frac{i_e}{(\beta + 1)}$$

Input resistance, $r_{in} = \frac{v_{be}}{i_b}$

$$\therefore r_{in} = \frac{v_{be}}{i_e}(\beta + 1)$$

$$r_{in} = r_e(\beta + 1) \sim \beta r_e \text{ where }, r_e = \frac{25mV}{i_E}$$

Assumption: Thermal voltage at room temperature=25mV

$$V_o = -i_c(R_C // r_o)$$

$$V_o = -\beta i_b R_C$$

$$V_o = -\beta \frac{v_{be}}{r_{in}} R_C$$

$$V_o = -\frac{v_{in}}{r_e} R_C$$

$$A_V = \frac{v_o}{v_{in}} = \frac{R_C}{r_e}$$

$$R_C = \beta r_e \text{ - - - - - (1)}$$

DC Analysis:

Using Kirchhoff's Law,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$V_{CC} = I_C(R_C + R_E) + + V_{CE}$$

$$I_C = -\frac{V_{CE}}{(R_C + R_E)} + \frac{V_{CC}}{(R_C + R_E)} \text{ - - - - -(2)}$$

Assuming that $V_{CC} = 15V$, $V_{CE} = 6V$ and $I_C = I_E = 2.5mA$,

$$r_e = \frac{25mV}{2.5mA}$$

$$r_e = 10\Omega$$

From equation (1):

$$R_8 = R_C = 320 \times 10 = 3.2k\Omega$$

Selected resistor value: $R_9 = 3.2k\Omega$

From equation (2):

$$15V = 2.5mA \times 3.2k\Omega + 6 + 2.5mA \times R_E$$

$$R_9 = R_E = 400\Omega$$

Selected resistor value: R_9= 350 Ω

$$V_B = V_E + V_{BE} = 2.5mA \times 400\Omega + 0.7\text{V} = 1.7\text{V}$$

This voltage is supplied to the R_7 resistor.

$$\therefore 1.7V = 15V \times \frac{R_7}{R_6 + R_7}$$

$$\therefore \frac{R_6}{R_7} = \frac{133}{17}$$

Selected resistor values: $R_6 = 1500\ \Omega$ and $R_7 = 240\Omega$.

<u>Calculating Capacitors' Values</u>

$$R_{in_{eq1}} = R_6 // R_7 // \beta r_e$$

$$R_{in_{eq1}} = 1500\Omega // 200\Omega // 320 \times 10\Omega$$

$$R_{in_{eq1}} = 167.25\Omega$$

Let lower cutoff frequency as 100Hz,

$$\therefore C_4 = \frac{1}{2\pi \times 100 \times 167.25}$$

$$C_4 = 95.2\mu F$$

Selected capacitor value: $C_4 = 100\mu F$

$$R_{in_{eq2}} = R_E // r_e$$

$$R_{in_{eq2}} = 400\Omega // 10\Omega$$

$$R_{in_{eq2}} = 9.76\Omega$$

$$\therefore C_5 = \frac{1}{2\pi \times 100 \times 9.76}$$

$$C_5 = 163\mu F$$

Selected capacitor values: $C_{5-1} = 100\mu F$ and $C_{5-2} = 100\mu F$

$$R_{in_{eq3}} = R_C = 3.2k\Omega$$

$$\therefore C_6 = \frac{1}{2\pi \times 100 \times 3200}$$

$$C_6 = 0.5uF$$

Selected capacitor value: C_6= $1uF$

CE Amplifier with Calculated Values

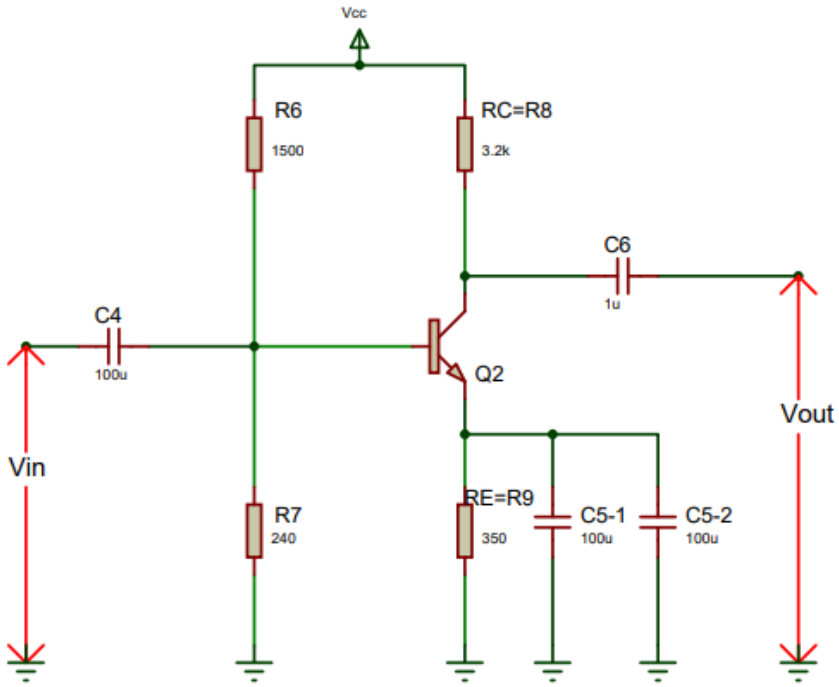


Figure 2.14 Amplifier stage with the calculated values

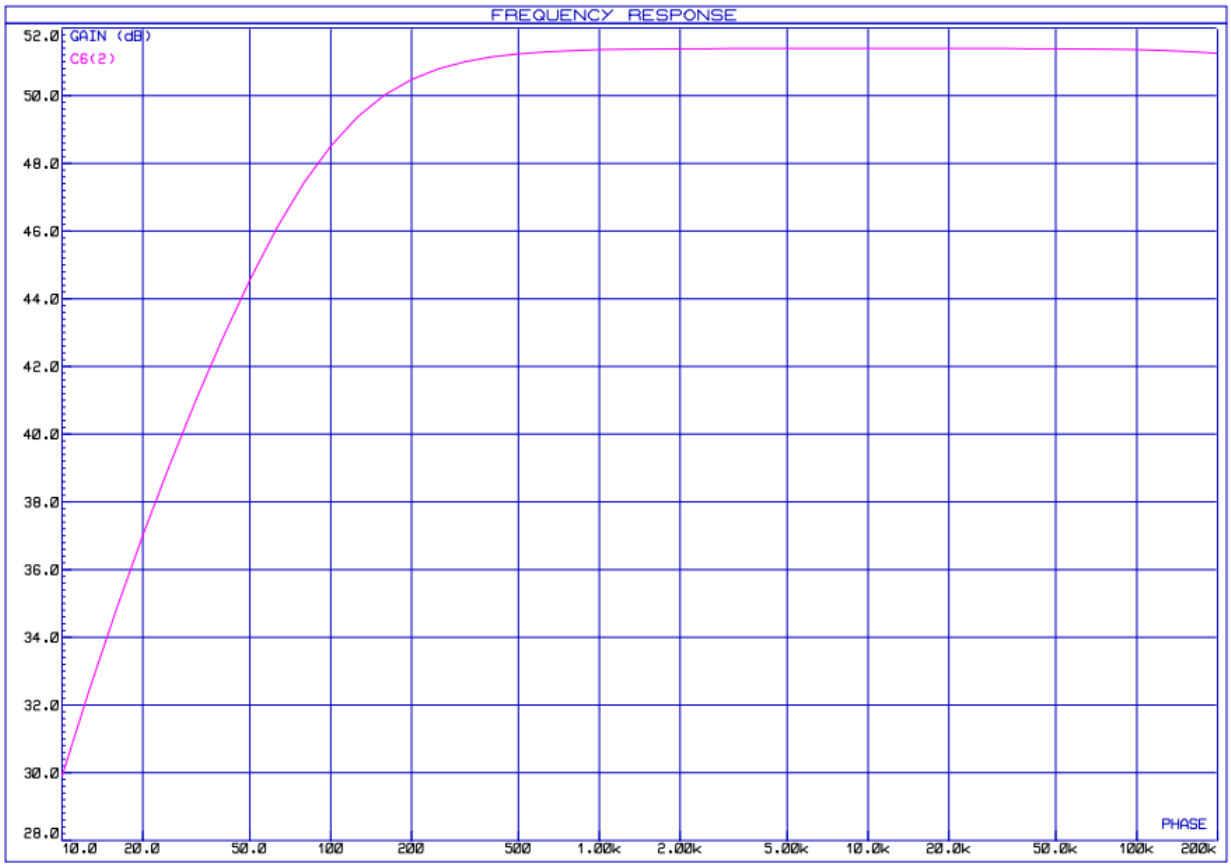


Figure 2.15 Frequency response of amplifier stage

3 IMPLEMENTATION OF THE CIRCUIT

3.1 FINAL SCEMATIC DESIGN OF THE AMPLIFIER

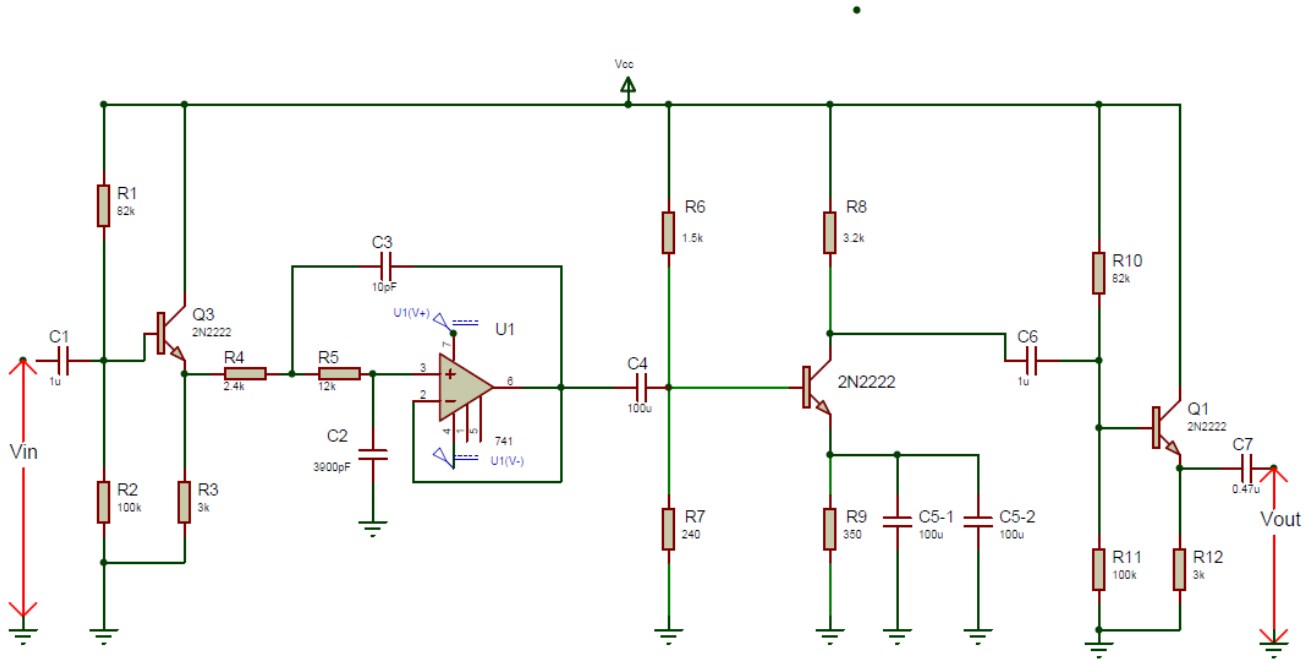


Figure 3.1 Final design of the amplifier

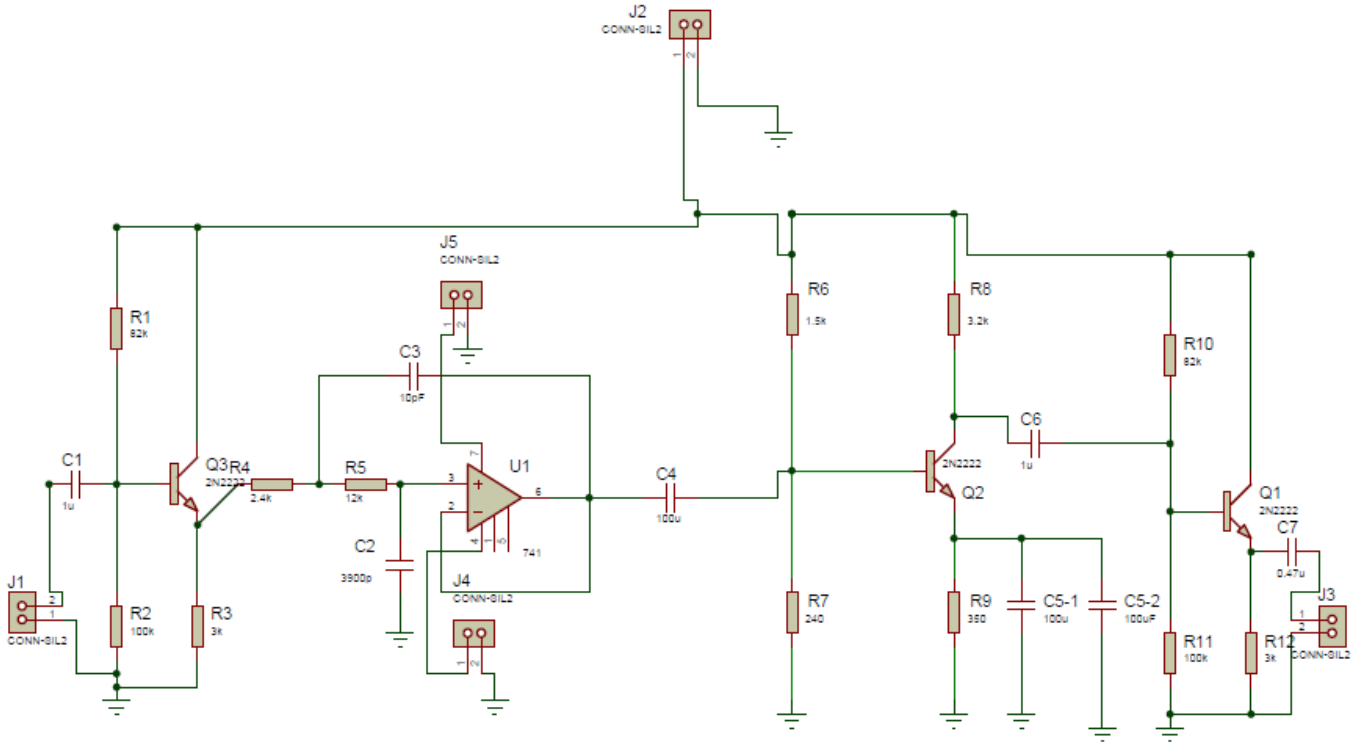


Figure 3.2 Final design after connecting the conn-sil

3.2 PCB LAYOUT OF THE AMPLIFIER

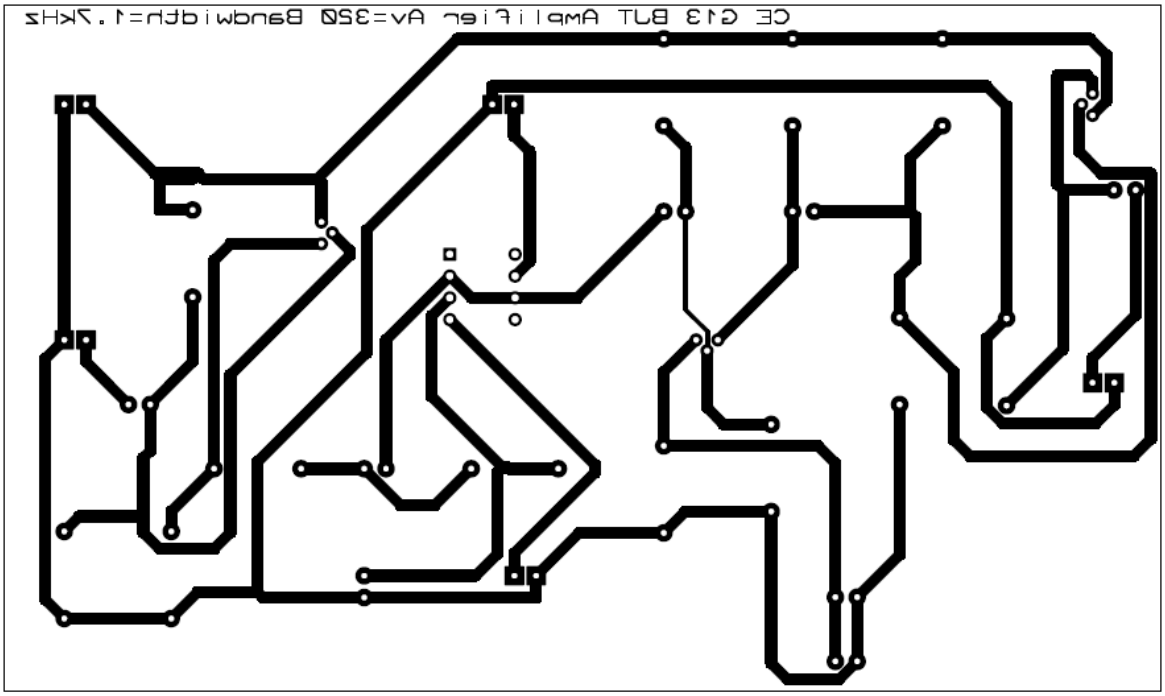


Figure 3.3 PCB layout of the circuit

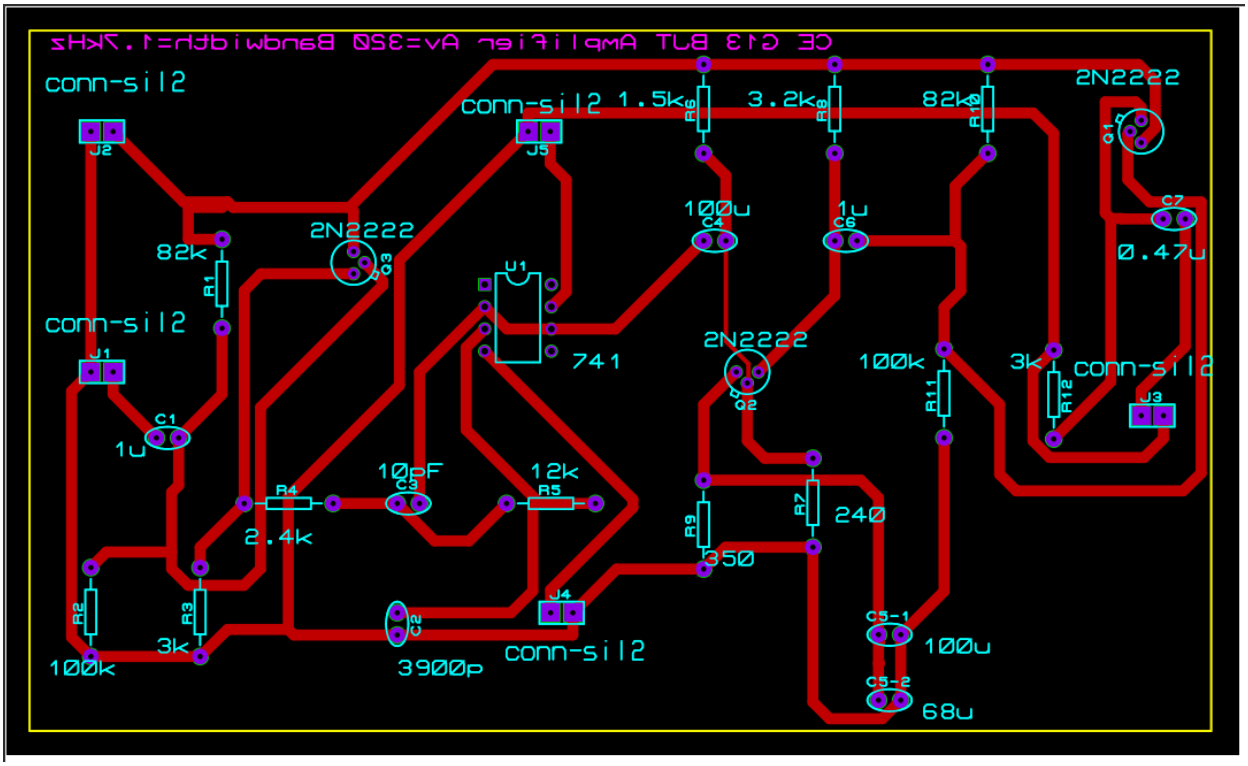


Figure 3.4 PCB design of the circuit

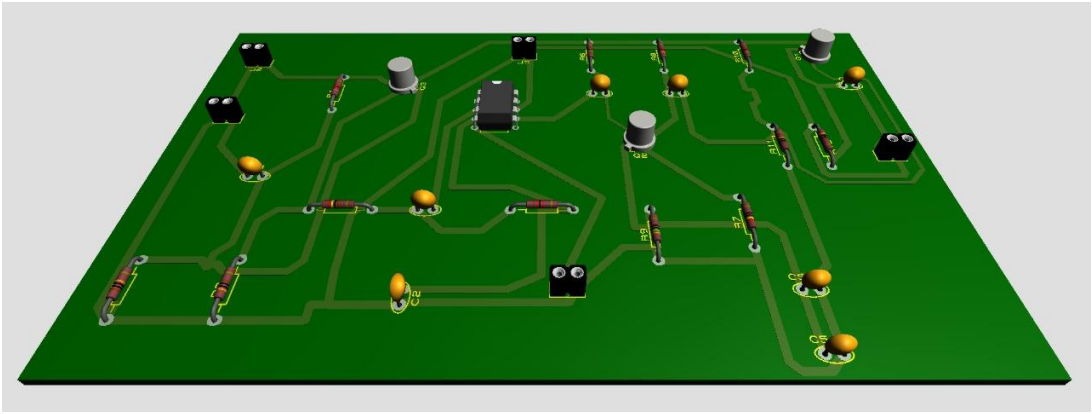


Figure 3.5 3d top view of the PCB

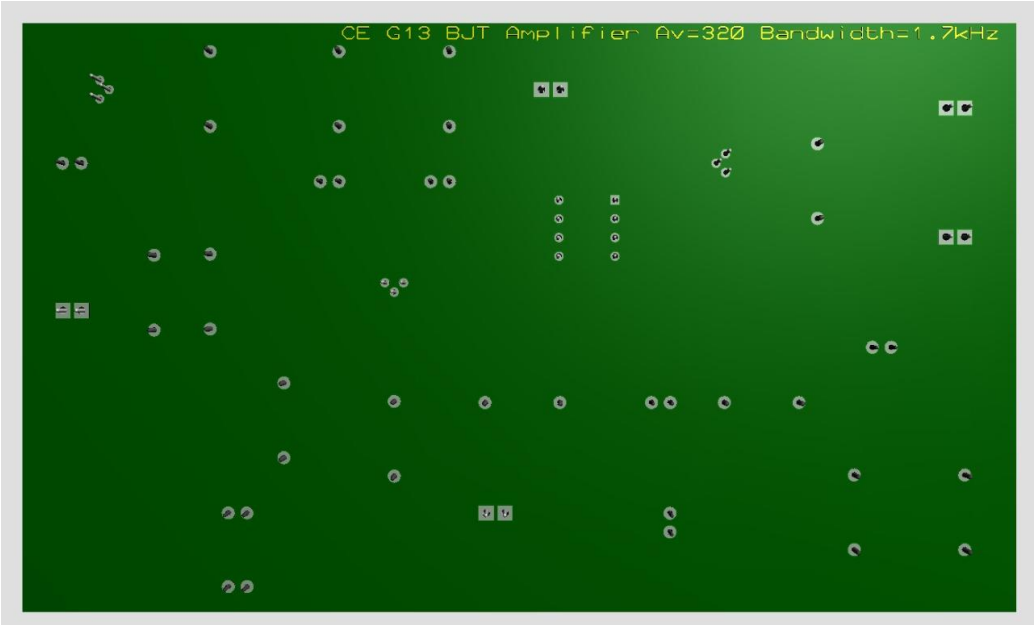


Figure 3.6 3d bottom view of the PCB

3.3 PHYSICAL IMPLEMENTATION

Firstly, the circuit was tested by using breadboards and the other components. Then, the layout for the PCB was printed and the components were soldered according to the PCB layout. As some capacitors and resistors are not available, the circuit was tuned with the suitable available values.

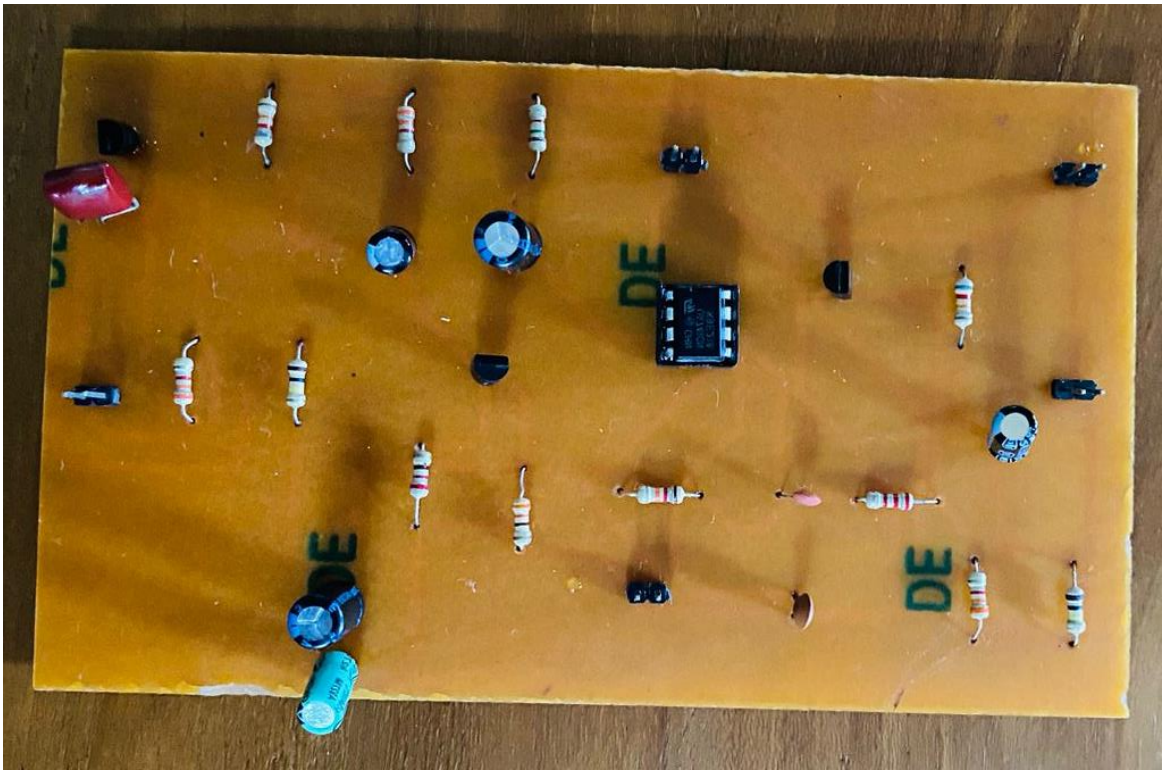


Figure 3.7 Top view of the printed board with soldered components

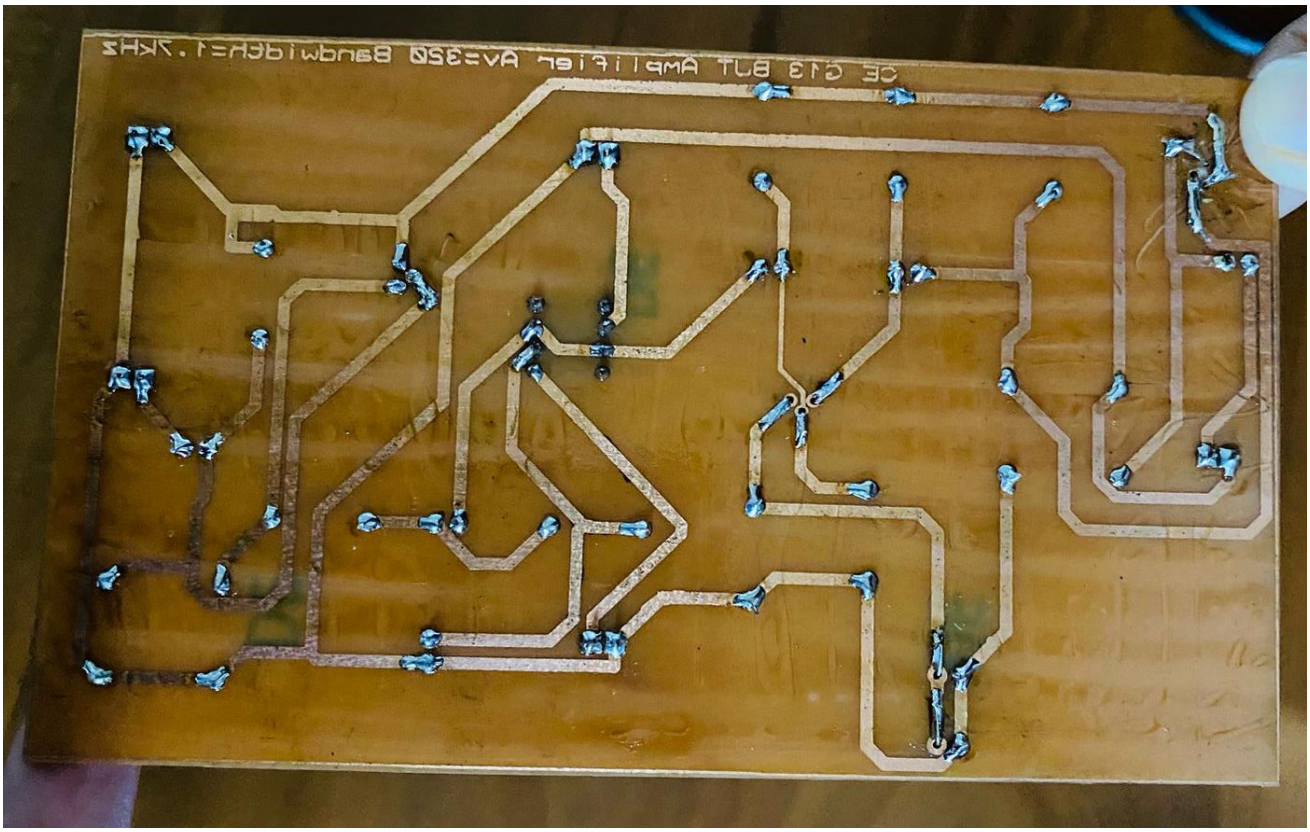


Figure 3.8 Bottom view of the printed board with soldered components

4 RESULTS AND DISCUSSION

4.1 SIMULATION RESULTS

Amplifier output in time domain:

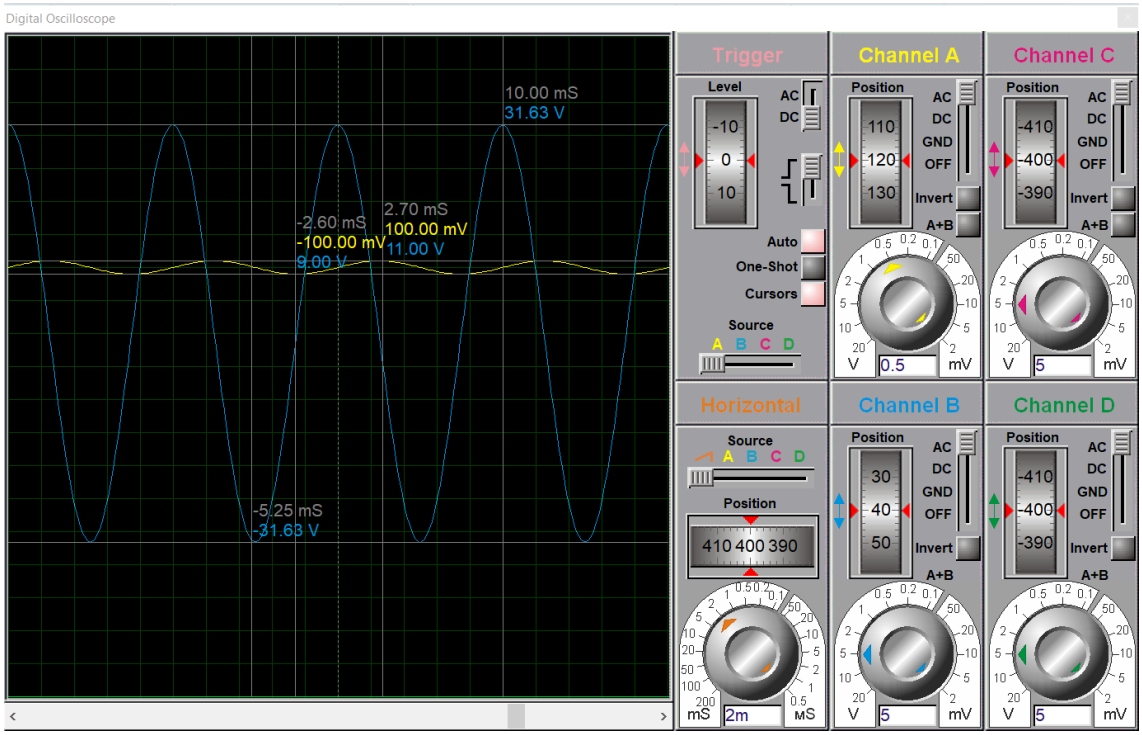


Figure 4.1 Amplifier output in time domain

Observations:

Input signal = 100 mV

Output voltage = 31.63 V

Gain obtained from the simulation,

$$A_V = \frac{V_{out}}{V_{in}} = \frac{31.63\ V}{100\ mV} = 316.3\ \approx 320$$

Amplifier output in frequency domain:

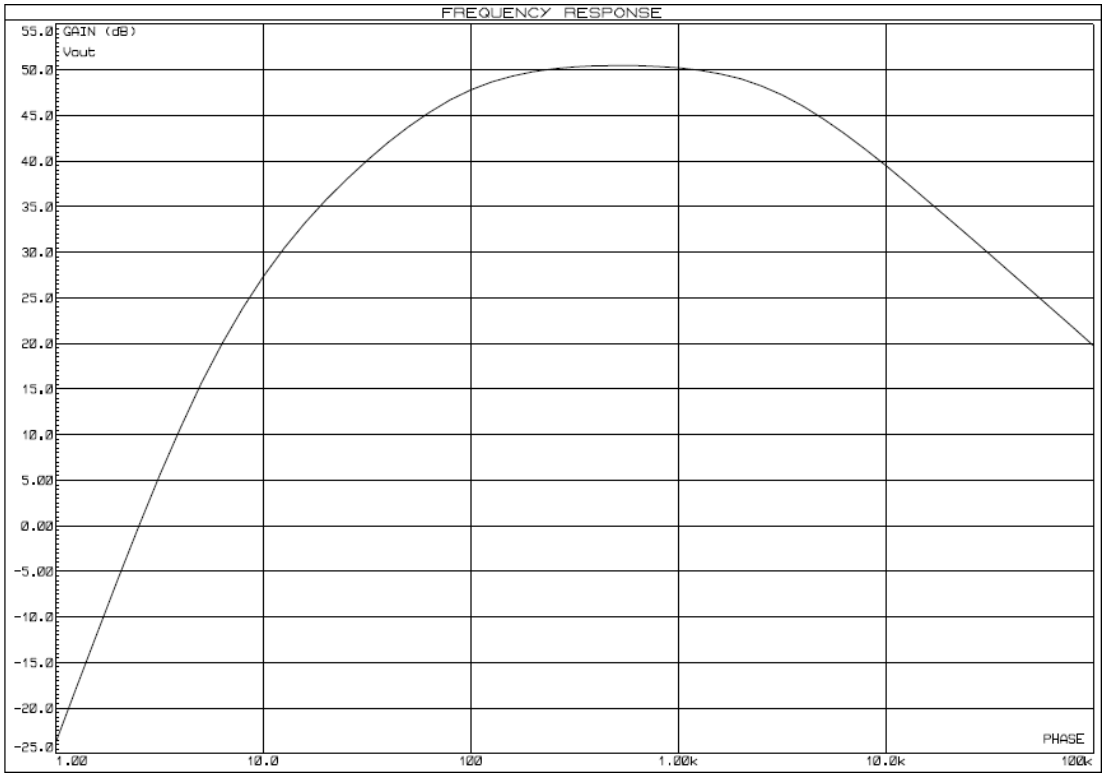


Figure 4.2 Amplifier output in frequency domain

Observations:

- Band pass gain = 50.5dB
- Higher cutoff frequency = 1.8kHz when gain is 49.3dB
- Lower cutoff frequency = 100 Hz when gain is 47.8dB

Therefore,

Bandwidth of the amplifier = $f_H - f_L$ = 1800 – 100 = 1700 Hz

Effect of test equipment in to the simulation

When testing a circuit in practice, a signal generator and an oscilloscope are connected to it. However, these instruments are not ideal, and their non-ideal parameters, such as output impedance and input impedance, can affect the results of the test. These non-ideal parameters can be simulated using circuit simulation tools, and the results of the simulation can be used to predict to some extent what will happen in the actual circuit.

In other words, the non-ideal parameters of a signal generator and oscilloscope can introduce errors into the results of a circuit test. However, by simulating the circuit and taking into account the non-ideal parameters of these instruments, it is possible to get a more accurate prediction of the circuit's behavior in the real world.

Initially, two identical copies of the amplifier design were produced, with one circuit subjected to laboratory equipment parameter settings. Subsequently, simulations were conducted to analyze the frequency response of both circuits when exposed to the same input signal.

While the amplifier design is expected to function correctly in a physical implementation, it is susceptible to errors stemming from various factors like component value inaccuracies, PCB trace resistance, capacitance, inductance, interference, noise, temperature fluctuations, and equipment inaccuracies.

4.2 EXPERIMENTAL RESULTS

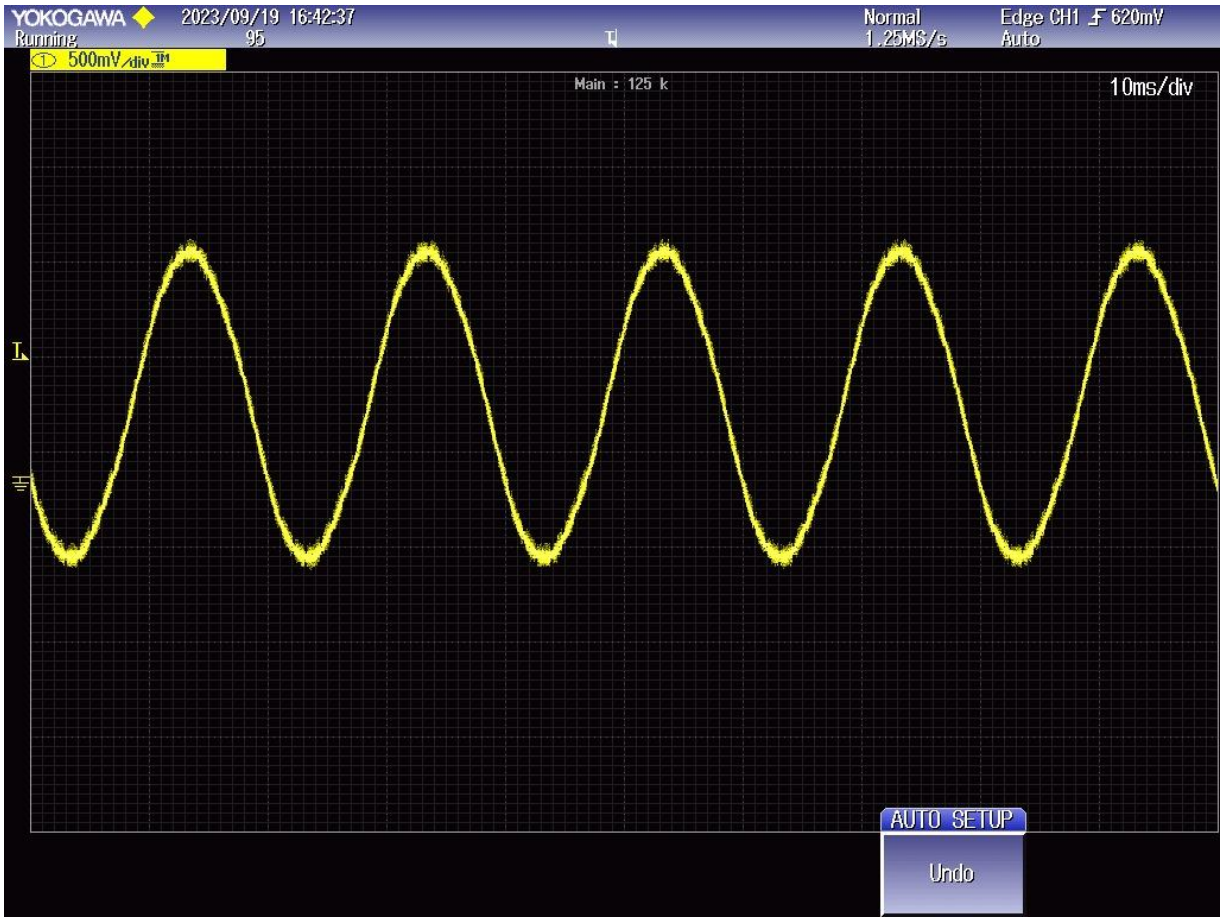


Figure 4.3 Amplifier output signal in time domain

Observations:

Input signal = 50 mV

Output voltage = 620 mV

Gain obtained from the simulation,

$$A_V = \frac{V_{out}}{V_{in}} = \frac{620\ mV}{50\ mV} = 12.4$$

*Due to some errors with the equipment the output varied with time to time. This image contains the one of the output we got.

4.3 DISCUSSION

In our project, we embarked on the task of designing a Bipolar Junction Transistor (BJT) common emitter amplifier with specific performance parameters: a 1.7 kHz bandwidth and an impressive 320 voltage gain. To achieve these objectives, we employed a combination of design techniques and electronic components.

To meet the bandwidth requirement, we utilized 741 operational amplifiers to construct low-pass Butterworth filters with a cutoff frequency set at 1.8 kHz. Additionally, we incorporated input and output buffers into our design to address any impedance mismatches that might arise during signal transmission.

In our theoretical analysis and Proteus simulation, we initially aimed for a gain of 320, which was successfully achieved. However, upon practical implementation, the experimental gain value deviated from the theoretical target. Several factors contributed to this variance. Firstly, the unavailability of precise resistor and capacitor values in the market can introduce discrepancies in the circuit. Moreover, noise introduced by real-world components, differences between the theoretical and practical characteristics of components, and variations in circuit temperature during operation all played roles in the outcome. Additionally, human errors, instrumental errors, and inaccuracies associated with oscilloscope calibration, probe capacitors, PCB trace capacitors, and inductances may have influenced the results.

Despite these challenges, our project was ultimately successful in creating a functional BJT common emitter amplifier that came remarkably close to meeting the desired bandwidth and gain values. This outcome underscores the effectiveness of our design and implementation, highlighting our ability to adapt to real-world conditions and produce a reliable electronic circuit.

5 REFERENCES

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6 APPENDIX

Table 14.2 Second-Order Low-Pass Butterworth VCVS Filter Designs

	CIRCUIT ELEMENT VALUES[a]					
Gain	1	2	4	6	8	10
R_1	1.422	1.126	0.824	0.617	0.521	0.462
R_2	5.399	2.250	1.537	2.051	2.429	2.742
R_3	Open	6.752	3.148	3.203	3.372	3.560
R_4	0	6.752	9.444	16.012	23.602	32.038
C_1	0.33C	C	2C	2C	2C	2C

[a] Resistances in kilohms for a K parameter of 1.

Figure 6.1 Table used for calculation of low pass Butterworth filter