

LandTiger V2.0

LPC17XX Development Board



User Manual
Version V1.1

www.PowerMCU.com, www.PowerAVR.com
Copyright © 2009, PowerMCU; Copyright © 2012, WH

Table of Content

Table of Content.....	2
1 Overview.....	3
2 Circuit and interface description.....	5
2.1 Power supply.....	5
2.2 Clock source.....	6
2.3 Reset Mode.....	7
2.4 Analog Input (ADC).....	7
2.5 Digital Analog Conversion Output (DAC).....	8
2.6 USB-Host.....	8
2.7 USB-Device.....	10
2.8 Databus Interface.....	12
2.8.1 LED Interface.....	12
2.8.2 Conversion Circuit 8bit-16bit.....	13
2.8.3 Display Interface.....	14
2.9 EEPROM.....	16
2.10 DataFlash.....	16
2.11 CAN.....	17
2.12 RS-232.....	18
2.13 RS-485.....	19
2.14 SD card.....	20
2.15 Ethernet.....	22
2.16 Joystick.....	23
2.17 Switches.....	24
2.18 Reset and Booting.....	25
2.19 JTAG Debug Function and JLINK emulator.....	27
2.20 External Connector.....	29
3 LCD HY-32C, 3.2", 320x240, 65K colours.....	31
4 Downloading Application Software.....	34
4.1 In System Programming (ISP) using FlashMagic.....	34
4.2 In System Programming (ISP) using the onboard JLink device.....	35
4.3 In System Programming (ISP) using external JLink devices.....	36
5 Portpin Usage on LandTiger vs mbed.....	38
6 Software compatibility.....	42
6.1 Compatibility with Keil.....	42
6.2 Compatibility with mbed.....	42
6.2.1 Hardware.....	42
6.2.2 Downloading new application software.....	45
6.3 Compatibility with CooCox CoIDE for ARM.....	45
7 JTAG Interface Description.....	46
7.1 JTAG standard connector for ISP and Debugging.....	46
7.2 SWD and SWO/SWV (also called SWV) compatibility.....	50
7.3.1 Serial Wire Output (SWO) compatibility.....	52
7.3.2 Serial Wire Viewer (SWV) compatibility.....	52
7.3.3 Cortex 10 Pin Debug compatibility.....	52
7.3.4 Cortex 20 Pin Debug compatibility.....	53
7.3.5 ARM ETM 'Mictor' Connector (38-pin).....	53
8 References.....	55

1 Overview

The LandTiger V2.0 NXP LPC1768 ARM development board is based on a second-generation ARM Cortex-M3 microcontroller, a high-performance, low-power 32-bit microprocessor designed for embedded system applications, suitable for instrumentation, industrial communications, motor control, lighting control, alarm systems, and other fields. The board supports USB2.0 Device and Host, dual CAN interfaces, RS-485 interface and an on-board USB emulator for JLINK. The development board is supported by a rich set of example software and detailed information to facilitate the users to quickly project development. A short feature overview:

Powerful LPC1768 MCU Cortex-M3 core:

- Clock frequency up to 100MHz.
- Includes support of eight areas of memory protection unit (MPU).
- Built-in Nested Vectored Interrupt Controller (NVIC).
- 512KB on-chip Flash program memory, supports in-system programming (ISP) and In Application Programming (IAP).
- 64KB SRAM for high-performance CPU access through the instruction bus, system bus, data bus access.
- AHB multi-layer matrix with 8-channel general-purpose DMA controller (GPDMA).
- Supports SSP, UART, I2C, I2S, ADC, DAC, Timer, PWM, GPIO, etc., can be used for memory-to-memory transfer.
- Standard JTAG test / debug interface and a serial wire debugging and serial wire tracking port option.
- Simulation trace module supports real-time tracking.
- 4 low-power modes: sleep, deep sleep, power-down, deep power-down.
- Single 3.3V power supply (2.4V - 3.6V).
- Operating temperature: -40° C - 85° C.
- Non-maskable interrupt (NMI) input.
- On-chip integrated power-on reset circuit.
- Built-in systems timer (SysTick), to facilitate operating system migration.

Onboard resources:

- 2 RS232 serial interfaces (using straight-through serial cable), (RS232 Transceiver: SP3232). One serial port supports ISP download of programs.
- 2 CAN bus communication interfaces (CAN Transceiver: SN65VHD230).
- RS485 communication interface (485 Transceiver: SP3485).
- RJ45-10/100M Ethernet network interface (Ethernet PHY: DP83848).
- DAC output interface, on-board speaker and speaker output driver (LM386).
- ADC input interface, on-board adjustable potentiometer input.
- Color LCD display interface (supports 2.8-inch or 3.2-inch color TFT 320X240). Touchscreen supported through SPI interface.
- USB2.0 Interface, USB host and USB Device interface.
- SD/MMC card (SPI) interface.
- I2C Interface, connected to onboard 2Kbit EEPROM (24LC02).
- SPI serial interface connected to onboard 16Mbit Flash (AT45DB161D).
- 2 user keys, 2 function keys (INT0 and Reset button).
- 8 LED lights (Digital outputs).
- Five-way joystick button (Digital Inputs).

- Serial ISP download support (COM0).
- Standard JTAG download, simulation debugging interface.
- Integrated JLINK compatible emulator (USB): support online simulation and debug capabilities, support KEIL, IAR and other mainstream development environments.
- Optional external 5V power supply or USB input to provide 5V power supply.
- Breakout available for all the IOs, user-friendly connection of external application development circuits.

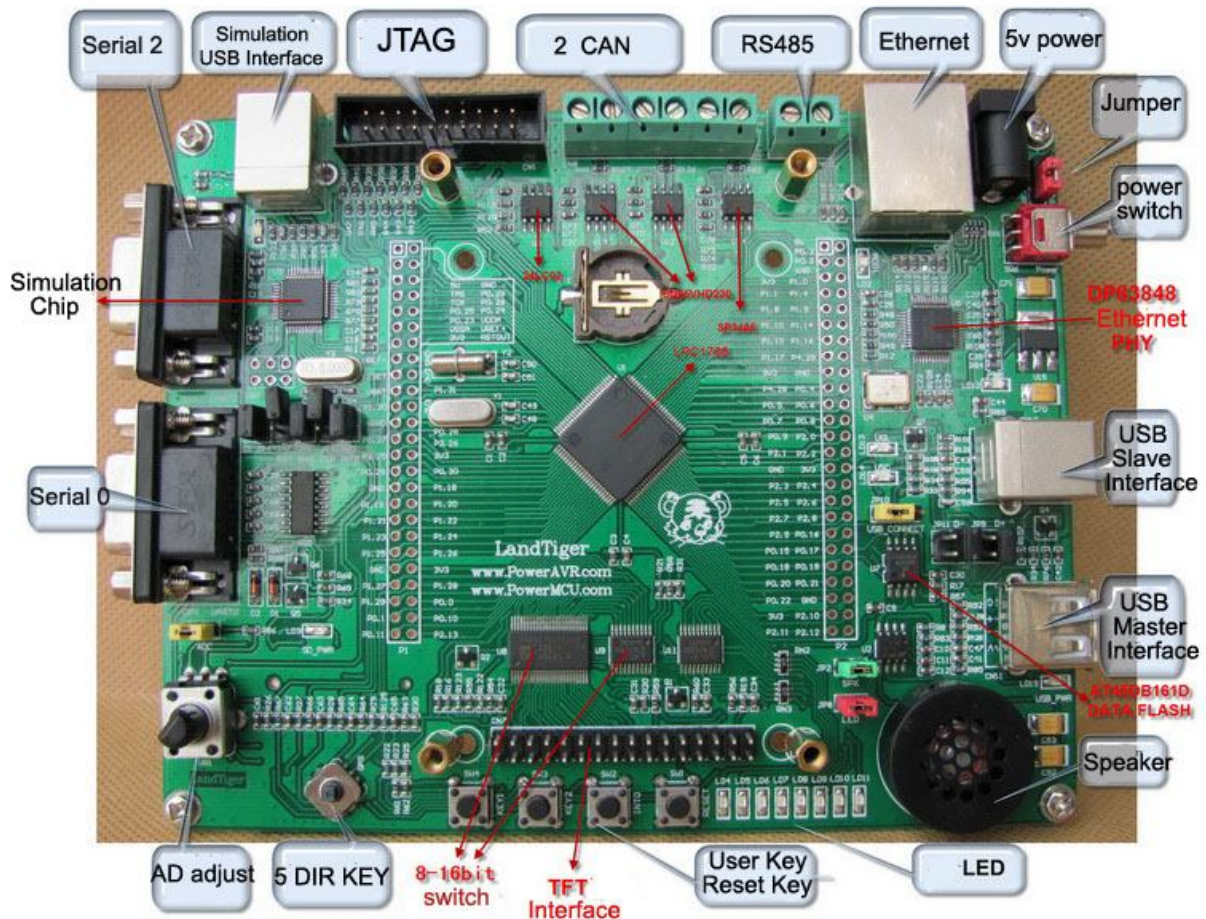


Figure 1 Board Overview (Note: Picture shows version 1.0 of the board)

2 Circuit and interface description

Due to the limited space in this manual, please use the circuit schematic reference for additional details on ICs and specific functions.

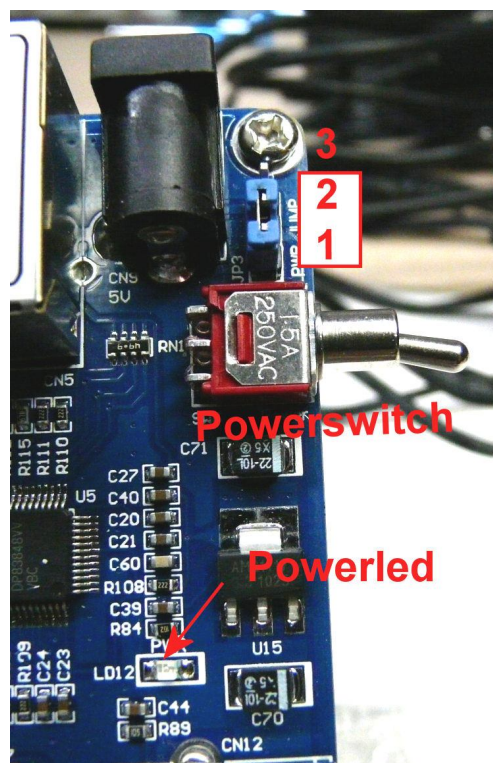
2.1 Power supply

The LandTiger development board may be powered by an external 5V power input or by the USB debug interface 5V power input.

- 5V DC power adapter connected to CN9, power select jumper JP3 plugged into 1-2 selects the external 5V power supply.
- Connecting the PC USB cable to the USB debug port CN4 and power select jumper J3 plugged into 2-3 will choose USB 5V supply. The board will be powered by the PC USB port (maximum current of 500mA limit).

Tabel 1 Jumper settings for powersupply select

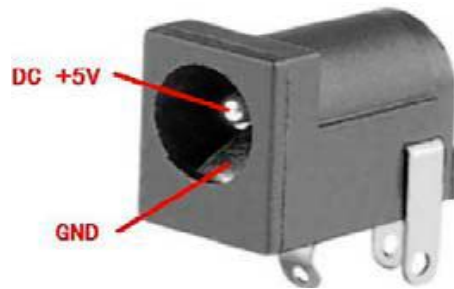
Jumper	Description
JP3	JP3 is used to select the external 5V power supply or USB powersupply. External 5V power supply: Jumper short 1-2 USB-powered: Jumper short 2-3



Figur 2 Powersupply Jumper JP3, connector CN9 and main powerswitch

Main powersupply switch SW6 is provided to switch the board on or off. LED LD11 indicates when the board is powered.

Note1: CN9 powerconnector inner pin is positive, outer ring is negative. The input voltage must not exceed $5V \pm 5\%$. Plug dimensions: 5mm outside, 2.5mm inside.



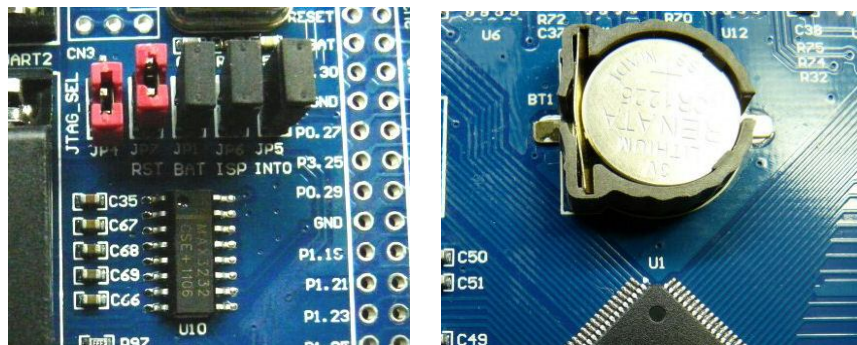
Figur 3 External 5V powersupply connector CN 9

Note2: The USB Device port (CN12) can not be used to power the LandTiger board.

Note3: Insert JP1 jumper to connect the onboard battery to the RTC when the board is disconnected from the external powersupply, when JP1 is open the RTC will only run as long as power is supplied and not maintain time when switched off.

Tabel 2 Jumper settings for RTC powersupply

Jumper	Description
JP1	JP1 is used to connect onboard backup battery to the RTC. Battery backup: Jumper inserted No battery backup: Jumper removed



Figur 4 RTC Battery Jumper JP1 and batteryholder BT1

Note1: The RTC backup battery type is CR1225 (Lithium, 3V).

2.2 Clock source

The development board has four different clock sources: System clock, Realtime Clock (RTC clock), Ethernet clock and Debugger interface clock.

- Y1, 12 MHz crystal, is the main system clock source, the internal RC oscillator of the CPU can not be used.
- Y2, 32.768 kHz crystal, is the clock source for the RTC.
- U4, 50MHZ crystal, is the Ethernet PHY chip DP83848 clock.

- Y3, 8 MHz is the clock for the JLink Debugger interface

Note 1: See section 2.1 on powersupply and onboard battery backup for the RTC.

2.3 Reset Mode

The reset signal in the Land Tiger LPC17XX development board is active low reset. The reset modes include the following:

- Press Reset button Reset (SW1)
- Reset signal is input through the JTAG emulator download.
- Reset signal is input through the ISP COM1 port (DTR control).

2.4 Analog Input (ADC)

Adjustable potentiometer VR1 is connected to analog channel P1.31 (AD0.5). JP12 jumper is used to enable the potmeter input. VR1 setting provides input voltages between 0V and 3V3 to the ADC.

Tabel 3 Jumper setting for Analog Input

Jumper	Description
JP12	JP12 is used to enable the VR1 connection to ADC input (P1.31 AD0.5). VR1 Connected to AD0.5: Jumper short No ADC input: Jumper removed



Figur 5 ADC Potmeter and Jumper JP12

2.5 Digital Analog Conversion Output (DAC)

External speaker circuit is connected to DAC output pin P0.26. The DAC output is enabled by JP2 jumper. The speaker is driven by an onboard audio amplifier U2 (LM386).

Tabel 4 Jumper setting for DAC output

Jumper	Description
JP2	JP2 is used to enable the external speaker. Speaker connected to P0.26: Jumper short No Speaker output: Jumper removed



Figuur 6 Loudspeaker and Jumper J2

2.6 USB-Host

LandTiger LPC17XX development board provides a full-speed USB 2.0 Host port (CN11), through a standard USB-A Type connector. The USB host port may be used to connect USB peripherals, such as: USB disk, USB mouse, USB keyboard and other equipment. Set JP9, JP11 jumpers into 3-4 position for the USB Host interface.

Jumper	Description
JP9	Select USB-D +. USB host: JP9 set to 3-4

Jumper	Description
JP11	Select USB-D -. USB host: JP11 set to 3-4

Connected devices should be provided with 5V power. This power is activated under control of the user program. Note that maximum current is limited.

IO Pin	Description
P1.19	<p>Activate USB Host power. LED LD15 is lit when power is activated.</p> <p>USB power control by P1.19: control signal is active low.</p>

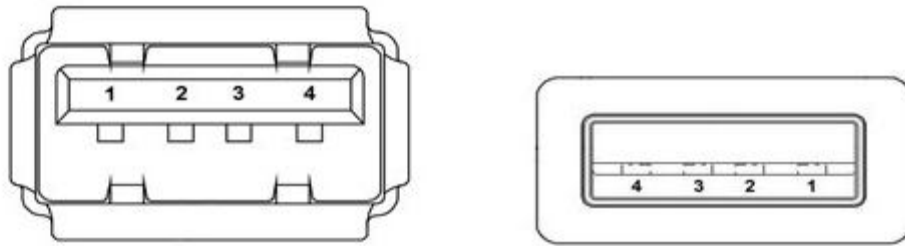
Tabel 5 The LPC1768 reserves a number of pins for the USB Host functions.

IO Pin	Description
P0.29	<p>USB_D+</p> <p>Connected to either the Host or Device connector by JP9 Release P0.29 pin by removing JP9</p>
P0.30	<p>USB D-</p> <p>Connected to either the Host or Device connector by JP11 Release P0.30 pin by removing JP11</p>
P1.22	<p>Sense USB Host power state.</p> <p>USB powersense by P1.22: input signal is active high. Release P1.22 pin by removing R78</p>
P1.19	<p>Activate USB Host power. LED LD15 is lit when power is activated.</p> <p>USB power control by P1.19: control signal is active low. P1.19 may be used a general purpose output and LD15 may be used as general purpose indicator when USB Host functions are disabled.</p>

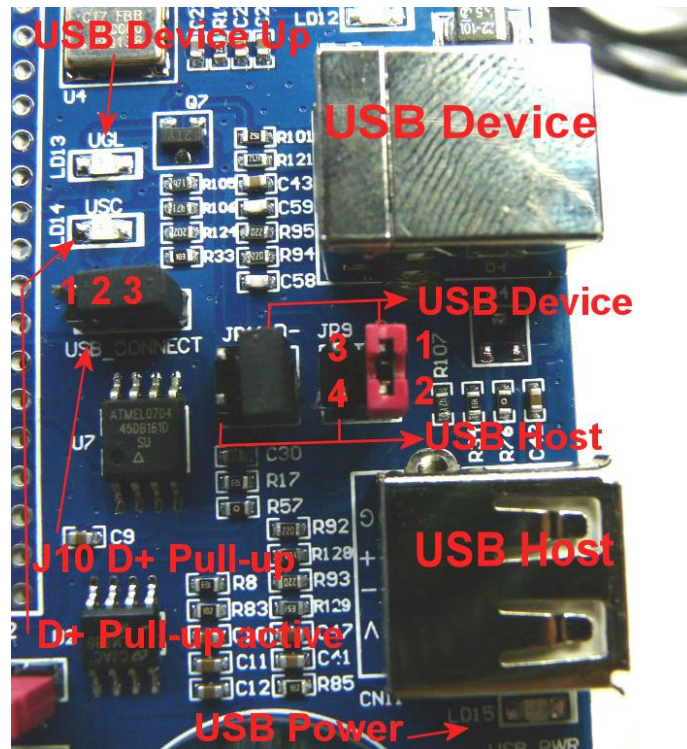
Tabel 6 CN11 USB AB-type pin functions

Pin	Description	Typical wire colour
1	VBUS (5V)	Red
2	D-	White
3	D+	Green
4	GND	Black

Note1: The figure shows a front view of the socket (left) and the plug is facing you.



Figuur 7 USB AB Host Connector CN11 (left) and Plug (right)



Figuur 8 USB Jumpers and LEDs

2.7 USB-Device

The Land Tiger LPC17XX development board provides a full-speed USB 2.0 device port (CN12), through a standard USB-B Type connector. Set JP9, JP11 jumper Plugged into 1-2 position for the USB Device interface.

Jumper	Description
JP9	Select USB-D +. USB device: JP9 set to 1-2
Jumper	Description
JP11	Select USB-D -. USB device: JP11 set to 1-2

The D+ line may have a pull-up activated to signal high-speed mode.

This pull-up may either be permanent or controlled by software.

Jumper	Description
JP10	Select USB-D + signal pull-up resistor mode. LED LD14 is lit when the pull-up is activated. USB pull-up control by P2.9: JP10 set to 1-2 (P2.9 control signal is active low). USB permanent pull-up: JP10 set to 2-3

IO Pin	Description
P2.9	Activate USB Device pull-up. LED LD14 is lit when the pull-up is activated. USB pull-up control by P2.9: JP10 set to 1-2 (P2.9 control signal is active low).

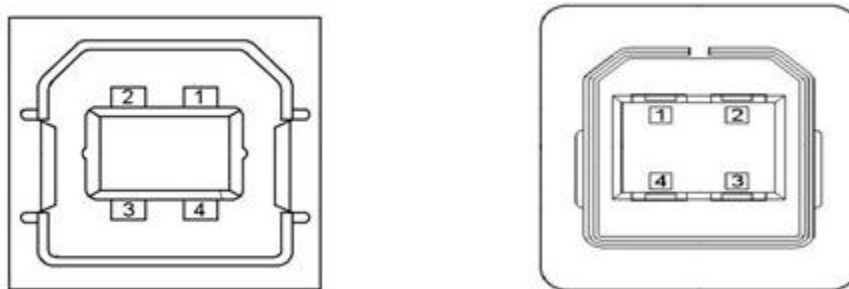
Tabel 7 LPC1768 reserved pins for the USB Device functions.

IO Pin	Description
P0.29	USB_D+ Connected to either the Host or Device connector by JP9 Release P0.29 pin by removing JP9
P0.30	USB D- Connected to either the Host or Device connector by JP11 Release P0.30 pin by removing JP11
P1.30	Sense VBUS from host in USB- Device mode. VBUS is active high. Release P1.30 pin by removing R123.
P1.18	USB Device is up indicator. LED LD13 is lit when USB is activated. (active low) P1.18 may be used a general purpose output and LD13 may be used as general purpose indicator when USB Device functions are disabled.
P2.9	Activate USB Device pull-up. LED LD14 is lit when the pull-up is activated. USB pull-up control by P2.9: JP10 set to 1-2 (P2.9 control signal is active low). P2.9 may be used a general purpose output and LD14 may be used as general purpose indicator when USB Device functions are disabled.

Table 8 CN12 USB B-type pin functions

Pin	Description	Typical wire color
1	VBUS (5V)	Red
2	D-	White
3	D+	Green
4	GND	Black

The figure below shows a front view of the socket (left), the plug (right) is facing you.

**Figure 9 USB B Device Connector CN12 (left) and Plug (right)**

Note1: The USB Device port (CN12) can not be used to power the LandTiger board. Power must be supplied either by the external power connector or by the USB debug port (CN4).

2.8 Databus Interface

The ARM LPC1768 does not have a separate data, address and controlbus. The LandTiger board is designed to emulate a simple processorbus by using some of the regular port pins. Port pins P2.0 ... P2.7 represent an 8 bit databus. The datalines are connected to an 8bit - 16bit conversion circuitry provided by U8 and U9. A number of controllines are also available that provide /RD, /WR, /CS and /RS. The LPC1768 Resetline is also available.

The main use for the bus is to control an LCD display. However, the design is generic and may be used to control other peripheral hardware also.

2.8.1 LED Interface

The 8 data lines P2.0-P2.7 are directly connected to a 74LV244 driver (U11) followed by 8 red LEDs (LD4 ... LD11). The LEDs display the current bitpattern on the databus. The LEDs may be disabled by removing JP8.

Jumper	Description
JP8	Enable databus LEDs. LEDs enabled: JP8 inserted LEDs disabled: JP8 removed

Note1: the datalines are shared with the LCD and the LEDs will show any databus activity to the LCD.

Note2: P2.7 corresponds to LD4 (leftmost), P2.0 corresponds to LD11 (rightmost)



Figur 10 LEDs and Enable Jumper J8

2.8.2 Conversion Circuit 8bit-16bit

The datalines are connected to an 8bit - 16bit conversion circuitry provided by U8 (16bit bidirectional buffer, 74ALVC164245) and U9 (8bit latch, 74LV573). The tables below show the steps needed to use the 8-16 bit conversion circuitry for Read and Write operations. There are 3 specific controllines required for the 8-16 bit conversion unit: LCD_DIR, LCD_EN, LCD_LE.

Tabel 9 Write operation sequence for 16 bit Databus

Steps	Control/datapin	IO Pin
Set P2.0-P2.7 as Output		
Set Buffer Direction to WR	LCD_DIR=1	P0.21
Enable buffer outputs	LCD_EN=0	P019
Latch D00-D07 Transparant	LCD_LE=1	P0.20
Setup D00-D07	Write LSBs	P2.0-P2.7
Latch D00-D07	LCD_LE=0	P0.20
Setup D08-D15	Write MSBs	P2.0-P2.7
Select Device	LCD_CS=0	P0.22
Select Data/Control Reg	LCD_RS=X	P0.23
Write Data (Start)	LCD_WR=0	P0.24
Write Data (End)	LCD_WR=1	P0.24
Deselect Device	LCD_CS=1	P0.22
...		

Tabel 10 Read operation sequence for 16 bit Databus

Steps	Control/datapin	IO Pin
Set P2.0-P2.7 as Input		
Set Buffer Direction to RD	LCD_DIR=0	P0.21
Enable MSB buffer outputs	LCD_EN=0	P019
Select Device	LCD_CS=0	P0.22
Select Data/Control Reg	LCD_RS=X	P0.23
Read Data (Start)	LCD_RD=0	P0.25

Read D08-D15	Read MSBs	P2.0-P2.7
Enable LSB buffer outputs	LCD_EN=1	P019
Read D00-D07	Read LSBs	P2.0-P2.7
Read Data (End)	LCD_RD=1	P0.25
Deselect Device	LCD_CS=1	P0.22
...		

Tabel 11 Databus interface description

Description	IO Pin
DB00	P2.0 (latched)
DB01	P2.1 (latched)
DB02	P2.2 (latched)
DB03	P2.3 (latched)
DB04	P2.4 (latched)
DB05	P2.5 (latched)
DB06	P2.6 (latched)
DB07	P2.7 (latched)
DB08	P2.0 (buffered)
DB09	P2.1 (buffered)
DB10	P2.2 (buffered)
DB11	P2.3 (buffered)
DB12	P2.4 (buffered)
DB13	P2.5 (buffered)
DB14	P2.6 (buffered)
DB15	P2.7 (buffered)
/CS	P0.22
RS	P0.23
/WR	P0.24
/RD	P0.25
RESET	RESET

2.8.3 Display Interface

The CN7 Databus interface of the Land Tiger LPC17XX development board can be connected to a 2.8 or 3.2 inch 320X240 TFT color LCD. The datalines are connected to P2.0 ... P2.7 and by 8bit - 16bit conversion circuit connected to the LCD.

In addition to the 16 bit databus, the LCD interface also supports a touchschreen controller. This interface is provided as an SPI bus.

Depending on the LCD board the LCD backlight may be controlled either as on/off or with variable brightness (PWM control).

The databus/LCD connector pinout is defined in the table below:

Tabel 12 CN7 Databus/Color TFT LCD interface description

Pin	Description	IO Pin	Comment
1	5V	Power supply	See Note2
2	GND	Ground	
3	DB00	P2.0 (latched)	Databus
4	DB01	P2.1 (latched)	
5	DB02	P2.2 (latched)	
6	DB03	P2.3 (latched)	
7	DB04	P2.4 (latched)	
8	DB05	P2.5 (latched)	
9	DB06	P2.6 (latched)	
10	DB07	P2.7 (latched)	
11	DB08	P2.0 (buffered)	
12	DB09	P2.1 (buffered)	
13	DB10	P2.2 (buffered)	
14	DB110	P2.3 (buffered)	
15	DB12	P2.4 (buffered)	
16	DB13	P2.5 (buffered)	
17	DB14	P2.6 (buffered)	
18	DB15	P2.7 (buffered)	
19	/CS	P0.22	Low active
20	RS	P0.23	RS = 1: Instruction Register RS = 0: Data Register
21	/WR	P0.24	Low active WR
22	/RD	P0.25	Low active RD
23	RESET	RESET	Low active
24	NC	NC	Do not connect
25	BLVCC	5V	Backlight VCC
26	BLGND	GND	Backlight GND
27	BLCNT (Brightn. PWM)	NC	Control of the backlight brightness via PWM
28	TP_INT Touchscreen	P2.13	Low level while the touch screen detects pressing
29	/TP_CS Touchscreen	P0.6	Low active
30	TP_SCK Touchscreen	P0.7	Connects to SPI SCK
31	TP_MOSI Touchscreen	P0.9	Connects to SPI MOSI
32	TP_MISO Touchscreen	P0.8	Connects to SPI MISO
33	3V3	3V3	See Note2
34	GND	GND	

Note1: details on the LCD operation may be found in Chapter 3.

Note2: The 5V-3V3 converter on the HY32-C LCD board is interfering with mainboard 3V3 powersupply !!!!! The 0-Ohm resistor R58 should be removed from the mainboard.

2.9 EEPROM

LandTiger LPC17XX development board includes a 24LC02 (2 kbit / 256kByte) EEPROM (U6) connected to the LPC1768 I2C_0 port (fast mode supported, upto 1 Mbit/s).

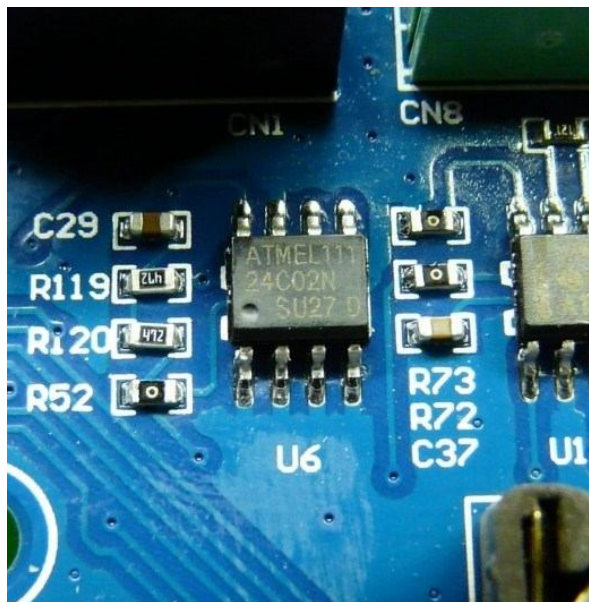
IO Pin	Description
P0.27	EEPROM SDA
P0.28	EEPROM SCL

Note1: The I2C Slaveaddress of the EEPROM is hardcoded at 0xA0 (8 bit address)

Note2: The I2C0 SDA and SCL lines have R121 and R122 pull-up Rs installed (4K7 to 3V3). This may interfere with Pull-Up Rs on an external I2C bus.

Note3: The Write Protect of the EEPROM is disabled (pull to GND).

Note4: The I2C EEPROM may be disabled by removing R53 in the SDA line. That will release P0.27 pin, however the pull-up R is still activated. P0.28 may be used without risk of conflict, however the pull-up R also remains activated.



Figuur 11 I2C EEPROM 24C02 (U6)

2.10 DataFlash

LandTiger LPC17XX development board includes an AT45DB16D (16 Mbit / 2MByte) DataFlash (U7) connected to the LPC1768 SPI_0 port.

IO Pin	Description
P0.18	DataFlash MOSI
P0.17	DataFlash MISO

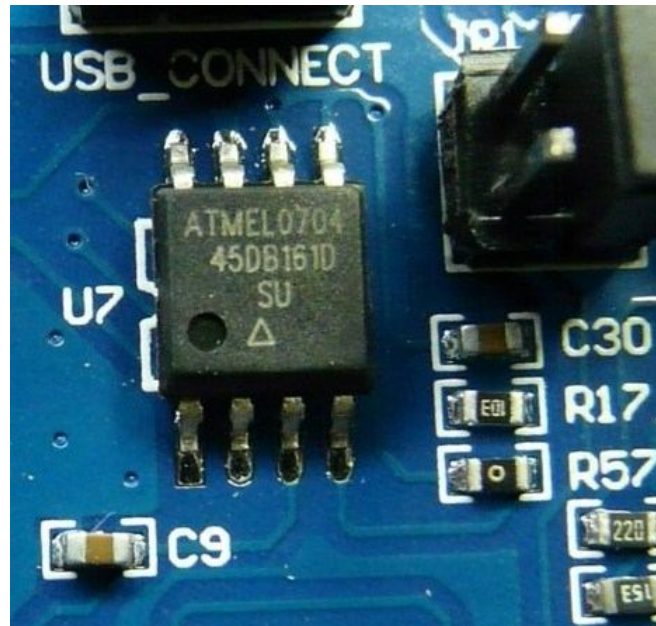
P0.16	DataFlash /CS (active low)
P0.15	DataFlash SCK

Note1: The Slaveaddress of the FLASH ...

Note2: The SPI_CS has a pull-up R installed of 10K to 3V3.

Note3: The /WriteProtect of the DataFlash is disabled (pull-up to 3V3).

Note4: The Flash may be disabled by removing R59 in /CS line. That will release P0.16 pin. P0.15, P0.17, P0.18 may be used without risk of conflict.



Figuur 12 SPI Flash 45DB16D (U7)

2.11 CAN

The LandTiger LPC17XX development board supports 2 CAN2.0 A/B bus communication interfaces. CAN_1 uses UART XX, CAN_1 uses UART XX. The CAN Transceivers are U12 and U13 (SN65HVD230).

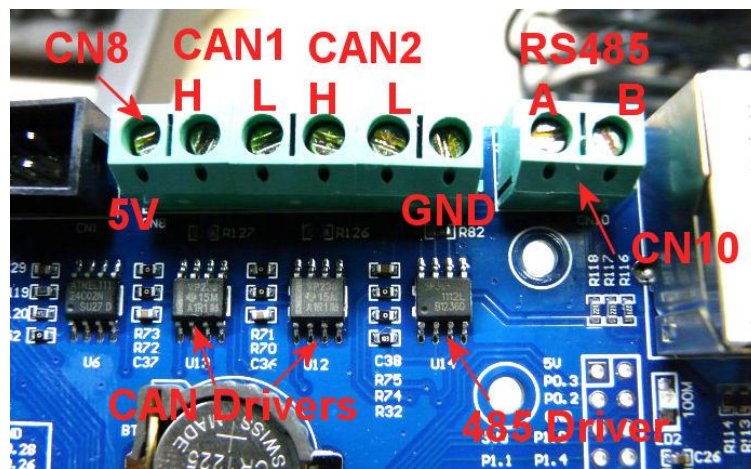
The CAN bus screw terminal accepts 5.08mm pitch leads.

Tabel 13 CAN interface description CN8

Pin	Description	IO Pin
1	5V	
2	CAN_1 H	P0.0/P0.1
3	CAN_1 L	P0.0/P0.1
4	CAN_2 H	P0.4/P0.5
5	CAN_2 L	P0.4/P0.5
6	GND	

IO Pin	Description	Comment
P0.0	CAN1_RX	CANRX1/TXD3
P0.1	CAN1_TX	CANTX1/RXD3

P0.4	CAN2_RX	CANRX2
P0.5	CAN2_TX	CANTX2



Figur 13 CAN1 and CAN2 connector CN8; RS485 Connector CN10

Note1: The CAN1 and CAN2 inputs/outputs are terminated by R129 and R128 (120 ohm). This means the LandTiger should be located on either end of the CAN bus rather than somewhere in the middle.

Note2: The CAN1 may be disabled by removing R74 in CAN1_RX line. That will release P0.0 pin. P0.1 may be used without risk of conflict.

Note3: The CAN2 may be disabled by removing R72 in CAN2_RX line. That will release P0.4 pin. P0.5 may be used without risk of conflict.

2.12 RS-232

The Land Tiger LPC17XX development board supports two bi-directional RS-232 Communication interfaces COM1, COM2 connected to LPC1768 UART0 and UART2. The RS232 Transceivers is U10 (SP3232).

The COM1 RS-232 interface may also be used for automatic ISP programming (serial download program). The port provides two control signals for RESET and ISP activation. The circuitry is compatible with the ISP standard as defined by NXP. Note: JP6, JP7 jumpers must be installed to use serial programming procedures.

Tabel 14 COM1 interface description

Pin	Description	IO Pin
1		NC
2	TXD	UART0_TX (P0.2)
3	RXD	UART0_RX (P0.3)
4	DTR	DTR (Control RESET)
5	GND	GND
6		NC
7	RTS	RTS (Control ISP, P2.10)
8		NC

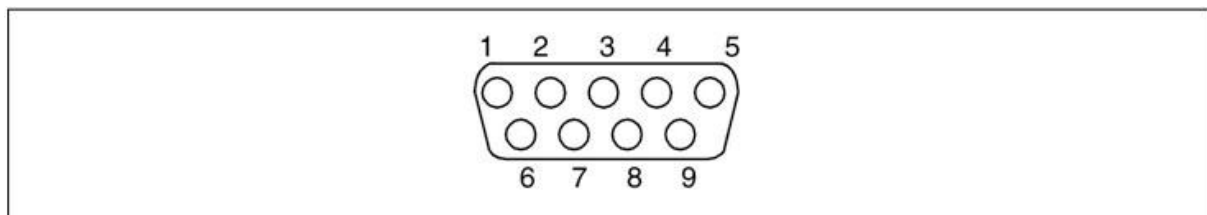
9		NC
Shield	Shield	GND

Tabel 15 COM2 interface description

Pin	Description	IO Pin
1		NC
2	TXD	UART2_TX (P0.10)
3	RXD	UART2_RX (P0.11)
4	DTR	NC
5	GND	GND
6		NC
7	RTS	NC
8		NC
9		NC
Shield	Shield	GND

Jumper	Description
JP6	Enable ISP Select. Enable ISP Select: JP6 inserted Disable ISP Select: JP6 removed

Jumper	Description
JP7	Enable ISP Reset. Enable ISP Reset: JP7 inserted Disable ISP Reset: JP7 removed

**Figuur 14 RS232 connector COM1, COM2 (female, front view)**

Note1: The COM1/UART0 may be disabled by removing R70 in UART0_RX line. That will release P0.3 pin. P0.2 may be used without risk of conflict.

Note2: The COM2/UART1 may be disabled by removing R71 in UART1_RX line. That will release P0.11 pin. P0.10 may be used without risk of conflict.

2.13 RS-485

The LandTiger LPC17XX development board supports a bi-directional RS-485 communication interface via CN10 to UART3. The 485 Transceiver is U14 (SP3485).

Tabel 16 RS485 interface description CN10

Pin	Description	IO Pin
1	485A	UART3_TX (P4.28)
2	485B	UART3_RX (P4.29)

IO Pin	Description	Comment
P4.28	485_TX	
P4.29	485_RX	
P2.8	485_DIR	TX/RX Direction (RX is active low, TX is active high)

Note1: The 485A and 485B inputs/outputs are terminated by R84 (120 ohm). This means the LandTiger should be located on either end of the RS485 bus rather than somewhere in the middle.

Note2: The 485A and 485B inputs/outputs do not have pull-up/pull-down resistors to provide a defined bias idle voltage. These resistors may have to be added externally.

Note3: The 485 interface may be disabled by removing R77 in 485_RX line, that will release P4.29 pin. Also remove R76 in 485_DIR line to release P2.8. P4.29 may be used without risk of conflict.



Figur 15 CAN1 and CAN2 connector CN8; RS485 Connector CN10

2.14 SD card

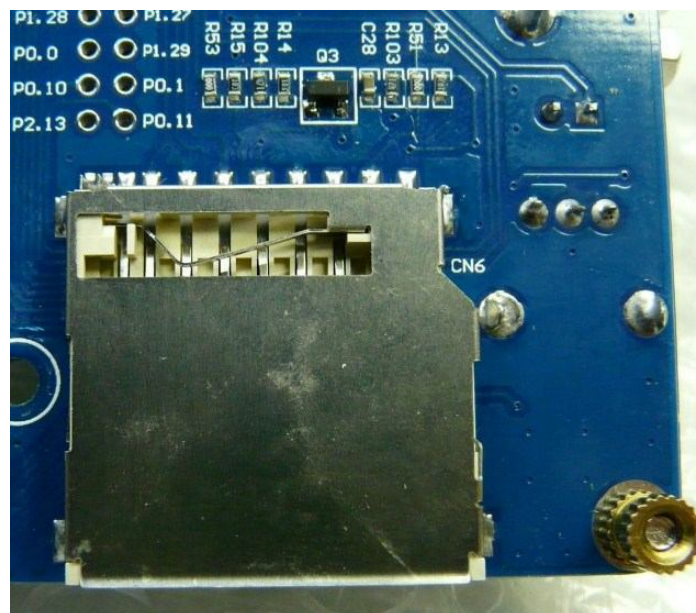
The Land Tiger LPC17XX development board supports an SD card interface (CN6). The SD card is accessed through the LPC1768's SSP0 port. A card detection signal is available. The power supply to the SD card is under control of the LPC17XX.

Tabel 17 SD Card connector CN9

SD Pin	Description	IO Pin
1	/SDcard_CS	P1.21 (SSEL0) Active Low
2	SDcard_DIN	P1.24 (MOSI0)
3	Vss/GND	Vss/GND
4	+3V3	+3V3 (P3.26 controlled)
5	SDcard_CLK	P1.20 (SCK0)
6	Vss/GND	Vss/GND
7	SDcard_DOUT	P1.23 (MISO0)
8	NC	NC
9	NC	NC
10	/SDcard_detect	P3.25, Active Low
11	GND	GND
12	NC	NC

Tabel 18 SD Card controlsignals

IO Pin	Description
P1.21	/SDcard_CS, Active Low
P3.26	SD Power, Active Low LD3 is lit when power in on
P3.25	/SDcard_detect, Active Low

**Figuur 16 SD card socket (Power on LED LD3 is located on frontside of board)**

Note1: The SD card interface may not be fully disabled by removing 0-Ohm resistors. The best option is to prevent a card from being inserted. Removing R52 in SD_CS line will release P1.21 pin. Remove R54 in SD_CD line to release P3.25. P3.26 and LD3 may be used without risk of conflict.

2.15 Ethernet

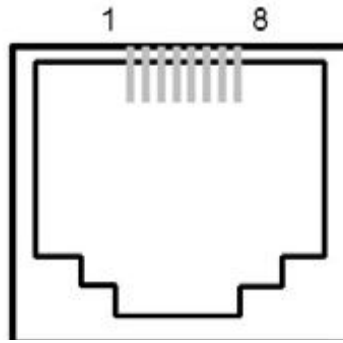
The LandTiger LPC17XX development board has onboard support for 10/100 Mbit/s Ethernet communication. The LPC1768 chip supports the RMII interface and links to the DP83848 (U5) Ethernet PHY chip. This device interfaces out via the RJ45 connector (CN5) which has internal magnetics and network filters. The RJ45 connector has integrated LEDs to indicate link connectivity and collisions. A separate LED indicates 10/100 Mbit/s link speed (LD2).



Figur 17 Ethernet PHY and RJ45 connector

Tabel 19 Ethernet controlsignals

IO Pin	Description
P1.4	ENET_TX_EN
P1.0	ENET_TX_D0
P1.1	ENET_TX_D1
P1.9	ENET_RX_D0
P1.10	ENET_RX_D1
P1.14	ENET_RX_ER
P1.8	ENET_CRS
P1.16	ENET_MDC
P1.17	ENET_MDIO
P1.15	ENET_REF_CLK



Figuur 18 RJ45 connector CN5 (frontview)

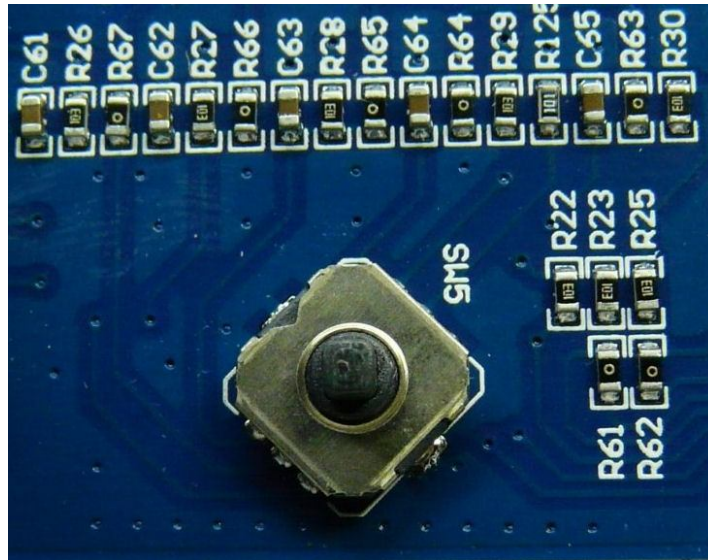
Tabel 20 RJ45 interface description

Pin	Description
1	TxData+
2	TxData-
3	RxData+
4	Shield
5	Shield
6	RxData-
7	Shield
8	Shield
Shield	Shield

Note1: The Ethernet interface may be not be fully disabled by removing 0-Ohm resistors. Removing R49, R50 and R51 will release P1.15, P1.16 and P1.17.

2.16 Joystick

The LandTiger LPC17XX board features a 5 way digital joystick (SW5). The joystick may be used for example to select options in a menu shown on the LCD. Each direction (up, down, left, right) and the Select function are connected to a dedicated digital inputpin on the LPC17XX. Multiple keys can be pressed at the same time (e.g. up and right). Inputpins are active low when a key is pressed. The inputpins are hardware debounced.



Figuur 19 Joystick 5-Way Switch

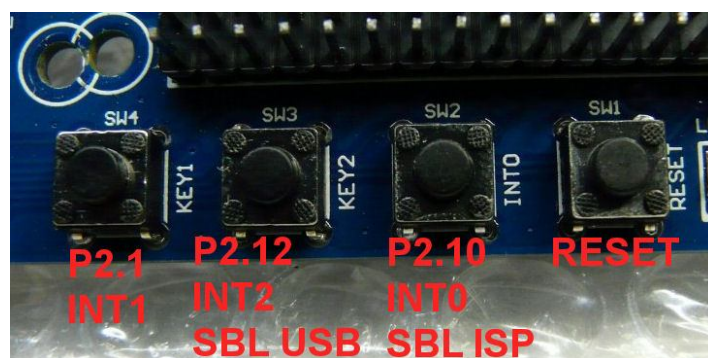
Tabel 21 Joystick 5-way switchsignals

IO Pin	Description
P1.25	Select (Active Low)
P1.26	Down (Active Low)
P1.27	Left (Active Low)
P1.28	Right (Active Low)
P1.29	Up (Active Low)

Note1: The Joystick interface may be fully disabled by removing 0-Ohm resistors. Removing R65, R66, R67, R68 and R69 will release P1.29, P1.28, P1.27, P1.26 and P1.25.

2.17 Switches

The LandTiger LPC17XX board features 4 switches: Key1 (SW4), Key2 (SW3), INT0 (SW2), RESET (SW1). These switches have several functions. See table below.



Figuur 20 Switches and Alternate functions

Tabel 22 Switch Description

Key type	Description	Comment
Key1	Connected to INT1 (P2.11), Active Low, Pull-Up R of 10K installed.	SW4
Key2	Connected to INT2 (P2.12), Active Low, Pull-Up R of 10K installed.	SW3, Secondary function to enter the USB ISP mode.
INT0	Connected to INT0 (P2.10) when JP5 is inserted. Active Low, Pull-Up R of 10K installed.	SW2, Secondary function to enter the COM1 ISP mode.
Reset	Manual Reset	SW1

Note1: Key1 may be disabled by removing R64, this will release P2.11.

Note2: Key2 may be disabled by removing R63, this will release P2.12.

2.18 Reset and Booting

The LandTiger LPC17XX development board has several options for Reset and booting.

Tabel 23 Reset and Boot options

Reset type	Description	Comment
Power On	The board will reset when power is applied. The LPC17XX will boot by starting the user program stored in internal Flash (512 KBytes).	
Manual Reset	The board will reset whenever the user presses the Reset key. (SW1) and then behaves just as after Power-On reset.	
Manual Reset and enter ISP mode	The device will enter the ISP programming mode when INT0 (SW2) is pressed and held before applying a Reset. The device is then ready to accept and store new user-code in the internal Flash.	SW2 is only connected to INT0 (P2.10) when JP5 is inserted. New program download through COM1 (UART0). On completion of download, Reset again to activate the new code.
External Reset	The board will reset whenever DTR is activated on COM1 and then behaves just as after Power-On reset.	DTR is only connected to Reset when JP7 is inserted.
External	The board will reset and enter	DTR is only connected to

Reset and enter ISP mode	the ISP programming mode whenever DTR is activated (Reset) and RTS is activated (ISP) on COM1. The board then behaves just as like manually entering the ISP mode and it is ready to accept and store new user-code in the internal Flash.	Reset when JP7 is inserted. RTS is only connected to INT0 (P2.10) when JP6 is inserted. New program download through COM1 (UART0). On completion of download, Reset again to activate the new code.
External Reset and enter ISP mode	The device may be Reset and brought in ISP mode through the JTAG port.	New program download through JTAG.
Manual Reset and enter ISP mode	The device will enter the USB Secondary bootloader programming mode when Key2 (SW3) is pressed and held before applying a Reset. The device is then ready to accept and store new user-code through the USB device port.	Key2 is connected to INT2 (P2.12). The USB Host will detect the LPC17XX as a mass storage device holding one binary file (the current program). Delete that file and download a new one through USB. Reset again to activate the new code. Note: a special USB bootloader must be stored in Flash first. See NXP documentation.

Tabel 24 Reset and Boot Jumper settings

Jumper	Description	Comment
JP5	INT0 (P2.10) connected to Key2	Insert Jumper to enable manual entering ISP mode
JP7	Reset activated by DTR	Insert Jumper to enable external Reset
JP6	INT0 (P2.10) activated by RTS	Insert Jumper to enable external entering ISP mode

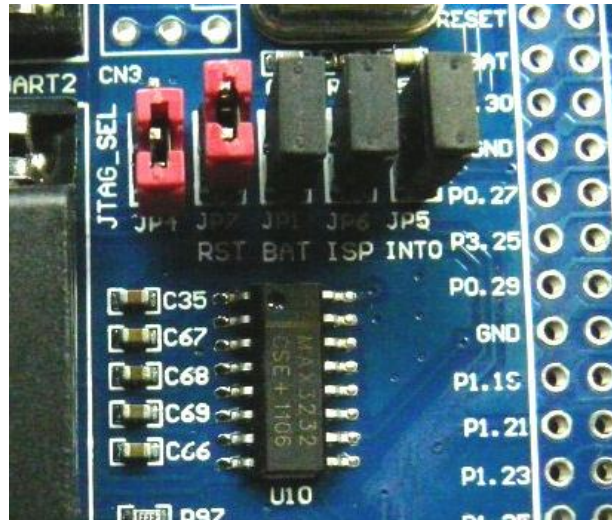


Figure 21 Jumper settings to enable serial port COM1 ISP
Jumper JP6 ISP mode enable by RTS
Jumper JP7 Reset enable by DTR
(Note: Jumper JP5 manual ISP mode enabled by pressing Key2)

Note1: The serial bootloader is a standard feature of NXP processors. Free PC software like FlashMagic may be used to download a compiled application program. FlashMagic is able to control Reset and INTO to initiate the ISP without need for the user to press any buttons on the board itself. The appropriate jumpers JP6, JP7 must be installed.

Note2: SW2/INT0 may be used as normal IO pin during program execution. The special function to enter ISP is only used during reset.

Note3: SW3/Key2/INT2 may be used as normal IO pin during program execution. The special function to enter USB bootloader is only used during reset.

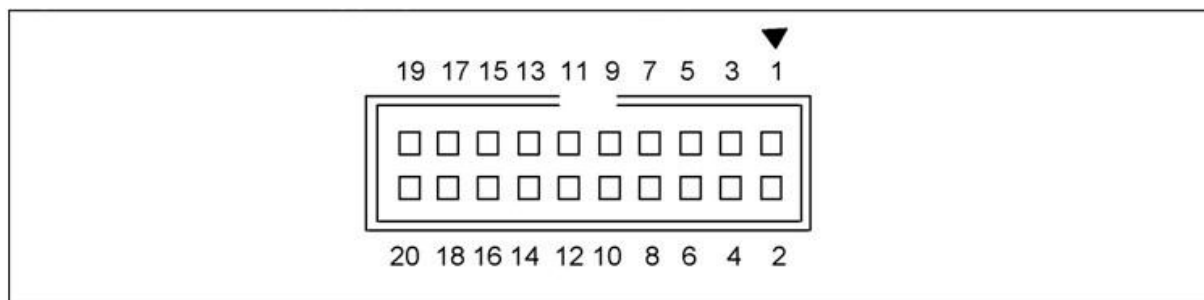
2.19 JTAG Debug Function and JLINK emulator

LandTiger LPC17XX development board has onboard support for JTAG debugging, downloads and other features. The debugging port (CN4) provides access to the on-board JLINK emulator (U3). JLINK is a JTAG emulator designed for ARM cores. It connects via USB (CN4) to a PC running Microsoft Windows 2000, Windows XP, Windows 2003, Windows Vista or Windows 7. JLink has a built-in 20-pin JTAG connector (CN1), which is compatible with the standard 20-pin connector defined by ARM.

The JTAG/SWD interface and JLINK emulator supports KEIL, IAR and other mainstream development environments.

The JTAG/SWD interface (CN1) may also be connected to any external general purpose JTAG/SWD debugging device. In this case the on-board JLINK emulator must be disabled by inserting JP4.

LED LD1 shows the current status of the JLINK debugger interface.



Figur 22 JTAG Connector CN1 for External JTAG device

Tabel 25 JTAG Connector CN1

Pin	Description	Comment
1	VRef	3.3V power
2	VSupply	3.3V power
3	TRST/	
4	GND	
5	TDI	
6	GND	
7	TMS/SWDIO	
8	GND	
9	TCK/SWDCLK	
10	GND	
11	RTCK	
12	GND	
13	TDO/SWO	
14	GND	
15	SRST/	
16	GND	
17	DBGREQ	NC
18	GND	
19	DBGACK	NC
20	GND	

Tabel 26 SWD CN3 Connector

Pin	Description	Comment
1	Power	3.3V power
2	GND	
3	SWDIO	
4	GND	
5	SWDCLK	
6	GND	

Tabel 27 JTAG Mode Settings

Jumper	Description	Comment
JP4	JTAG_SEL	Insert Jumper to enable external JTAG device. Remove Jumper to enable onboard JLINK emulator

Tabel 28 JLINK Interface Status

LED LD1	Description	Comment
Flash 10Hz	Un-Initialized	
Flash 1 Hz	Error	
Solid on	Initialized/Ready	
Short Flash	Communication	

Note1: The board may be powered by the USB JLINK debugging port CN4. Set Jumper JP3 to position 2-3.

2.20 External Connector

The LandTiger LPC17XX development board has soldering connectors to provide access to all processor I/O pins, powersupply and GND.

**Figur 23 External Connector (front)**

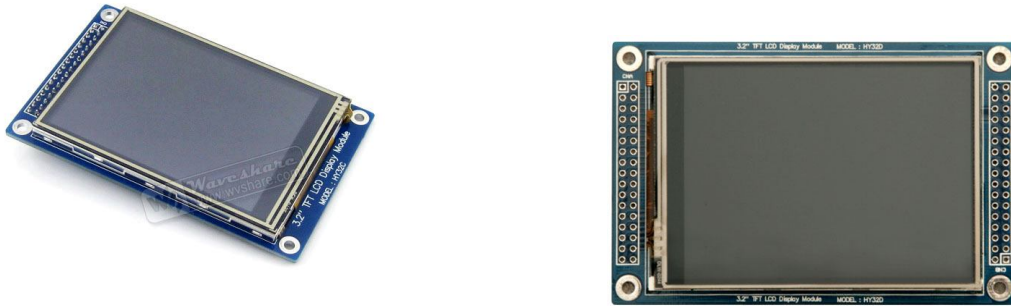


Figuur 24 External Connector (rear)

The pin description is printed on the silkscreen (both front and rearside of PCB). A detailed list of all pins and how they are used on the LandTiger is given in the Appendix.

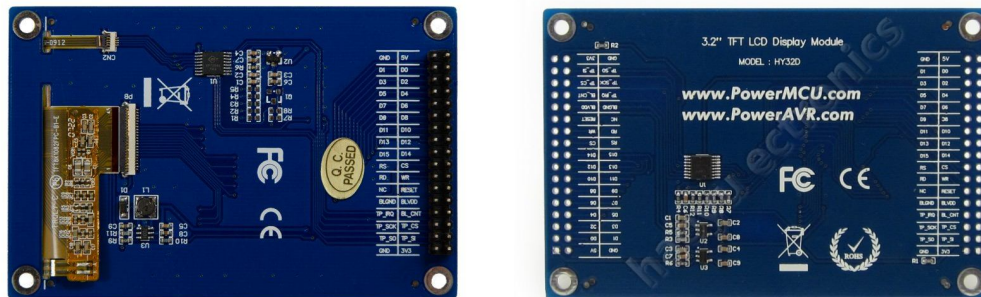
3 Color LCD, 3.2", 320x240, 65K colours

LandTiger is compatible with several types of Color LCDs. There are currently two types of 3.2" displays available. Both displays are functionally identical, but have different LCD panels and some differences in the electrical design. The displays are identified as HY32C and HY32D.



Figur 25 HY32C (left) and HY32D (right) seen from frontside

Notice that LCD HY32C has only one row of connectors and HY32D has two connectors with identical pinout. Physical dimensions and mounting holes are also identical.



Figur 26 HY32C (left) and HY32D (right) seen from rearside

Tabel 29 Characteristics of the LCDs

Characteristic	Type
LCD Controller	SSD1289 (Chip on Glass)
Touch Screen Controller	XPT2046
LCD Type	TFT
LCD Interface	16-bit parallel
Touch Screen Interface	SPI
Backlight	LED
Colors	65536
Resolution	320 * 240 DOTS
Backpanel illumination	LED
Backlight voltage generator	RT9293 (HY32C only)

The main difference in the electrical design is that the HY32C has a different LCD panel which also needs a voltage up converter to drive the backpanel LEDs. The converter device is the RT9293.

Note1: The schematic of HY32C is not available.

Note2: The schematic of HY32D is available as part of the LandTiger documentation.

Tabel 30 Pinout Description of LCDs

Pin	Name	Description	Comment
1	5V	5V power supply	When powered from 5V supply: Pin 1 & Pin 2 as power input, Pin 33 & Pin 34 provide 3.3V output.
2	GND	Ground	GND
3	D0	Data Lines	D0-D15
4	D1		
5	D2		
6	D3		
7	D4		
8	D5		
9	D6		
10	D7		
11	D8		
12	D9		
13	D10		
14	D11		
15	D12		
16	D13		
17	D14		
18	D15		
19	/CS	LCD chip select	Low active
20	RS	Instruction / Data register selection	RS = 1: Instruction Register RS = 0: The Data Register
21	/WR	Write	WR = 0, RD = 1
22	/RD	Read	WR = 1, RD = 0
23	/RESET	Reset the controller chip	Low active
24	NC	Do not connect	Do not connect
25	BLVCC	5 V or 3.3V	Backlight VCC
26	BLGND	Ground	Backlight GND
27	BLCNT	Backlight brightness adjustment	Control of the backlight brightness via PWM
28	TP_IRQ	Interrupt Touch screen	Low level while the touch screen detects pressing
29	/TP_CS	Touch screen chip select	Low active
30	TP_SCK	Touch screen SPI clock	Connects to SPI SCK
31	TP_SI	Touch screen input data	Connects to SPI MOSI
32	TP_SO	Touch screen output data	Connects to SPI MISO
33	3.3V	3.3V power supply	When powered from 3.3V supply: Pin 33 & Pin 34 as power input, Pin 1 & Pin 2 keep NC.

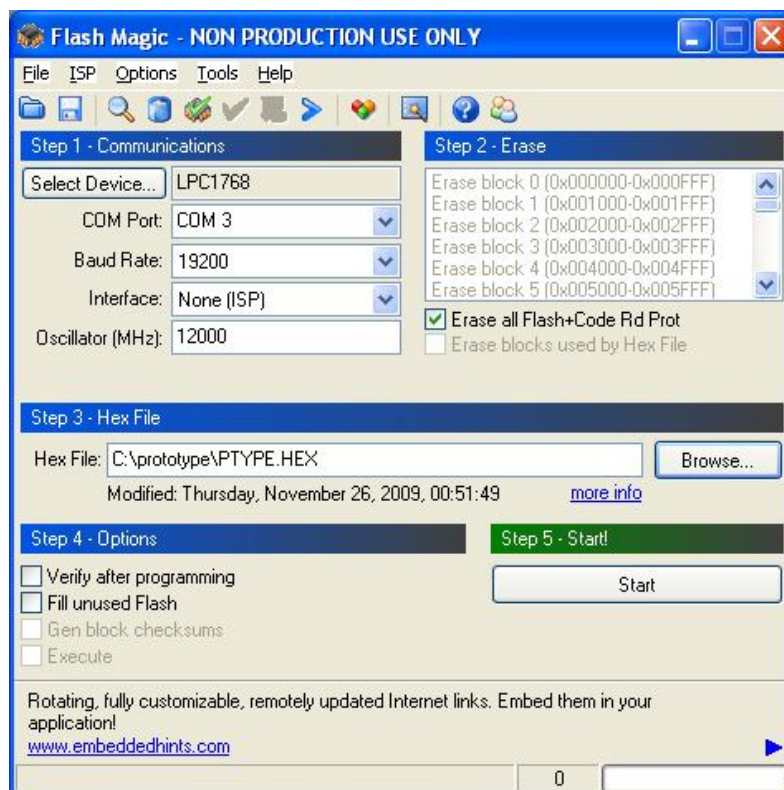
34	GND	Ground	
----	-----	--------	--

Note1: The 5V-3V3 converter on the HY32C LCD board is interfering with LandTiger mainboard 3V3 powersupply !!!!! The 0-Ohm resistor R58 should be removed from the LandTiger mainboard.

4 Downloading Application Software

4.1 In System Programming (ISP) using FlashMagic

Flashing a new program in the LandTiger LPC17xx may be done by entering the ISP bootloader mode and downloading the new code through UART 0. A free PC software application named FlashMagic may be used for this purpose (www.flashmagictool.com). All you need is a serial cable (fully wired) between the PC and LandTiger COM0. Set JP6 and JP7 to enable ISP mode via COM0. Select the LPC1768 device and the correct PC Com port in FlashMagic, select the desired .hex file and press 'Start'. Then press the Reset button on the LandTiger to execute the new program.



Figuur 27 Flashmagic

Some compilers (e.g. mbed cloud compiler) produce a .bin file. FlashMagic needs a .hex file. Convert the compiler .bin file with a modern bin2hex utility and use the /4 option for either 24 or 32 bit addressing range, not the standard 16 bit range. Example:

```
bin2hex /4 test.bin test.hex
```

An alternative bin2hex tool is part of the GNU toolsuite:

```
arm-none-eabi-objcopy -I binary -O ihex test.bin test.hex
```

Download the Bin2Hex from <http://www.hex2bin.com/bin2hex>, or if your running a 64-bit system use this instead <http://www.ht-lab.com/freeutils/bin2hex/bin2hex.zip>)

Download the GNU tools from <https://sourcery.mentor.com/sgpp/lite/arm/portal/release1802>

Download the Keil bin2hex utility <http://www.keil.com/download/docs/113.asp>

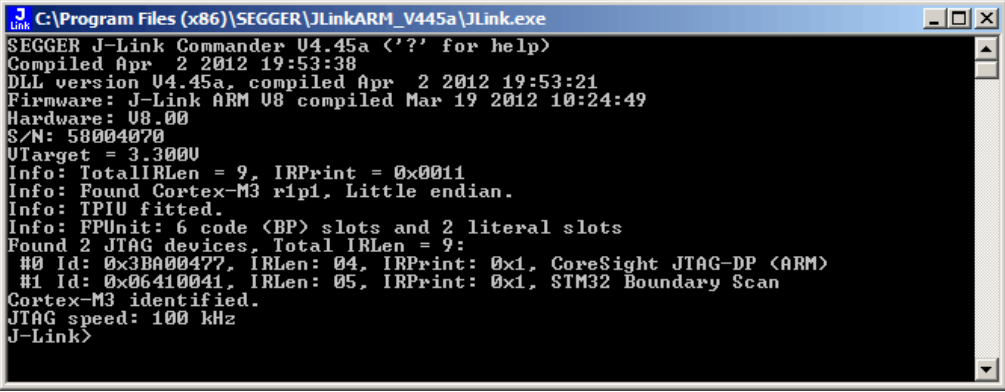
Download FlashMagic from www.flashmagictool.com

4.2 In System Programming (ISP) using the onboard JLink device

LandTiger LPC17XX development board has onboard support for JTAG debugging, downloads and other features. The debugging port (CN4) provides access to the on-board JLINK emulator (U3). JLINK is a JTAG emulator designed for ARM cores. It connects via USB (CN4) to a PC running Microsoft Windows 2000, Windows XP, Windows 2003, Windows Vista or Windows 7. The JTAG/SWD interface and JLINK emulator supports KEIL, IAR and other mainstream development environments.

A PC application program such as JFlash will accept compiled .bin files and flash the target processor. See www.segger.com for supported features.

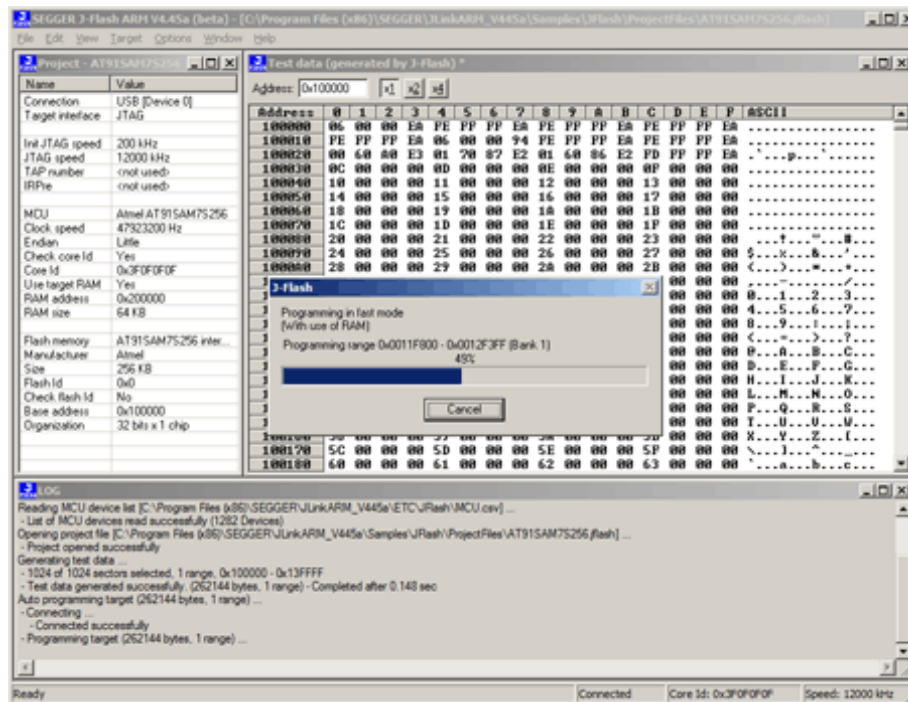
Download JFlash software from www.segger.com. Install the software and run the JLink commander application. J-Link commander (JLink.exe) is a command line based utility that can be used for verifying proper functionality of J-Link as well as for simple analysis of the target system. It supports some simple commands, such as memory dump, halt, step, go etc. to verify the target connection.



```
J C:\Program Files (x86)\SEGGER\JLinkARM_V445a\JLink.exe
SEGGER J-Link Commander U4.45a ('?' for help)
Compiled Apr  2 2012 19:53:38
DLL version U4.45a, compiled Apr  2 2012 19:53:21
Firmware: J-Link ARM U8 compiled Mar 19 2012 10:24:49
Hardware: U8.00
S/N: 58004070
UTarget = 3.300V
Info: TotalIRLen = 9, IRPrint = 0x0011
Info: Found Cortex-M3 r1p1, Little endian.
Info: TPIU fitted.
Info: FPUnit: 6 code <BP> slots and 2 literal slots
Found 2 JTAG devices, Total IRLen = 9:
#0 Id: 0x3BA00477, IRLen: 04, IRPrint: 0x1, CoreSight JTAG-DP <ARM>
#1 Id: 0x06410041, IRLen: 05, IRPrint: 0x1, STM32 Boundary Scan
Cortex-M3 identified.
JTAG speed: 100 kHz
J-Link>
```

Figuur 28 JLink Commader (Jlink.exe)

J-Flash is PC software running on Windows (Windows 2000 and later) systems, which enables you to program the internal and external flash of your microcontroller via J-Link.



Figuur 29 JFlash

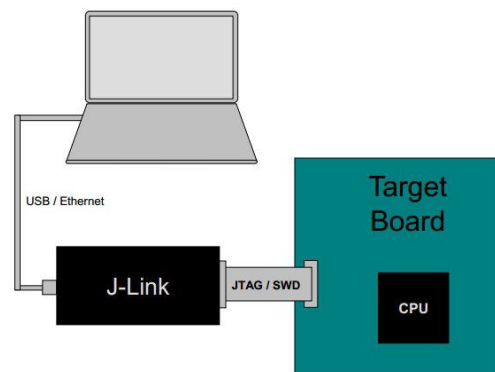
In JFlash you first need to select the proper device (LPC1768) from the device database, then select the .bin file and flash that into the target processor. Detailed instructions are given in the JLink and JFlash manuals. See www.segger.com.

Note 1: Many well known IDEs (eg Keil, IAR, CoCoX and GNU GDB) support JLink flashing and debugging without the need for the standalone JFlash application.

4.3 In System Programming (ISP) using external JLink devices

The JTAG/SWD interface (CN1) may also be connected to any external general purpose JTAG/SWD debugging device. In this case the on-board JLINK emulator must be disabled by inserting JP4.

External JLINK devices may be used for programming and debugging the ARM LPC1768 on LandTiger. The JLINK device is connected to a USB port on your PC and connects to the targetboard using a JTAG connector (CN1).



Figuur 30 JLINK Setup



Figuur 31 JLINK Flash and Debug device

A PC application program such as JFlash will accept compiled .bin files and flash the target processor. See www.segger.com for a range of available devices and supported features. Follow the explanations given above on using JLink Commander and JFlash.

Note1: Many well known IDEs (eg Keil, IAR, CooCox and GNU GDB) support JLink flashing and debugging without the need for the standalone JFlash application.



Figuur 32 Converter for different JTAG and SWD connectors.

Note2: The standard connector on JLINK is the 20 pin JTAG connector. Converter boards and cables may be needed sometimes to connect JLINK to the some of the other JTAG/SWD plugs that are in use.

5 Portpin Usage on LandTiger vs mbed

Tabel 31 Port 0 description

IO Pin	Description	Usage LandTiger	Comment LandTiger	Usage mbed	Comment mbed
P0.0	P0.0/RD1/TXD3/SDA1	CAN1_RX	CAN1	P9	SDA1/TXD3
P0.1	P0.1/TD1/RXD3/SCL1	CAN1_TX	CAN1	P10	SCL1/RXD3
P0.2	P0.2/TXD0/AD0.7	UART0_TX	COM1	TXD0	I/F MagicChip
P0.3	P0.3/RXD0/AD0.6	UART0_RX	COM1	RXD0	I/F MagicChip
P0.4	P0.4/I2SRX_CLK/RD2/CAP2.0	CAN2_RX	CAN2	P30	CAN_RD2
P0.5	P0.5/I2SRX_WS/TD2/CAP2.1	CAN2_TX	CAN2	P29	CAN_TD2
P0.6	P0.6/I2SRX_SDA/SSEL1/MAT2.0	TP_CS	Touchscreen	P8	SSEL1
P0.7	P0.7/I2STX_CLK/SCK1/MAT2.1	SCK1	Touchscreen	P7	SCK1
P0.8	P0.8/I2STX_WS/MISO1/MAT2.2	MISO1	Touchscreen	P6	MISO1
P0.9	P0.9/I2STX_SDA/MOSI1/MAT2.3	MOSI1	Touchscreen	P5	MOSI1
P0.10	P0.10/TXD2/SDA2/MAT3.0	UART2_TX	COM2	P28	SDA2/TXD2
P0.11	P0.11/RXD2/SCL2/MAT3.1	UART2_RX	COM2	P27	SCL2/RXD2
P0.12	NA				
P0.13	NA				
P0.14	NA				
P0.15	P0.15/TXD1/SCK0/SCK	SCK	SPI_Flash	P13	SCK0/TXD1
P0.16	P0.16/RXD1/SSEL0/SSEL	DF_CS	SPI_Flash	P14	SSEL0/RXD1
P0.17	P0.17/CTS1/MISO0/MISO	MISO	SPI_Flash	P12	MISO0
P0.18	P0.18/DCD1/MOSI0/MOSI	MOSI	SPI_Flash	P11	MOSI0
P0.19	P0.19/DSR1/SDA1	LCD_EN	LCD_8_16	NC	
P0.20	P0.20/DTR1/SCL1	LCD_LE	LCD_8_16	NC	
P0.21	P0.21/RI1/RD1	LCD_DIR	LCD_8_16	NC	
P0.22	P0.22/RTS1/TD1	LCD_CS	LCD	NC	
P0.23	P0.23/AD0.0/I2SRX_CLK/CAP3.0	LCD_RS	LCD	P15	AD0.0

P0.24	P0.24/AD0.1/I2SRX_WS/CAP3.1	LCD_WR	LCD	P16	AD0.1
P0.25	P0.25/AD0.2/I2SRX_SDA/TXD3	LCD_RD	LCD	P17	AD0.2
P0.26	P0.26/AD0.3/AOUT/RXD3	AOUT	Speaker	P18	AD0.3/AOUT
P0.27	P0.27/SDA0/USB_SDA	SDA	EEPROM	NC	
P0.28	P0.28/SCL0/USB_SCL	SCL	EEPROM	NC	
P0.29	P0.29/USB_D+	USB_D+	USB Host/Device	P31	USB_D+
P0.30	P0.30/USB_D-	USB_D-	USB Host/Device	P32	USB_D-
P0.31	NA				

Tabel 32 Port 1 description

IO Pin	Description	Usage LandTiger	Comment LandTiger	Usage mbed	Comment mbed
P1.0	P1.0/ENET_TXD0	ENET_TXD0	Ethernet	EN_TXD0	Ethernet
P1.1	P1.1/ENET_TXD1	ENET_TXD1	Ethernet	EN_TXD1	Ethernet
P1.2	NA				
P1.3	NA				
P1.4	P1.4/ENET_TX_EN	ENET_TX_EN	Ethernet	EN_TX_EN	Ethernet
P1.5	NA				
P1.6	NA				
P1.7	NA				
P1.8	P1.8/ENET_CRCS	ENET_CRCS	Ethernet	EN_CRCS	Ethernet
P1.9	P1.9/ENET_RXD0	ENET_RXD0	Ethernet	EN_RXD0	Ethernet
P1.10	P1.10/ENET_RXD1	ENET_RXD1	Ethernet	EN_RXD1	Ethernet
P1.11	NA				
P1.12	NA				
P1.13	NA				
P1.14	P1.14/ENET_RX_ER	ENET_RX_ER	Ethernet	EN_RX_ER	Ethernet
P1.15	P1.15/ENET_REF_CLK	ENET_REF_CLK	Ethernet	EN_RX_CK	Ethernet
P1.16	P1.16/ENET_MDC	ENET_MDC	Ethernet	EN_MDC	Ethernet

P1.17	P1.17/ENET_MDIO	ENET_MDIO	Ethernet	EN_MDIO	Ethernet
P1.18	P1.18/USB_UP_LED/PWM1.1/CAP1.0	USB_UP_LED	USB Host/Device	LED1	
P1.19	P1.19/MC0A/USB_PPWR/CAP1.1	USB_PPWR	USB Host/Device	NC	
P1.20	P1.20/MCFB0/PWM1.2/SCK0	SCK0	SD_Card	LED2	
P1.21	P1.21/MCABORT/PWM1.3/SSEL0	SD_CS	SD_Card	LED3	
P1.22	P1.22/MC0B/USB_PWRD/MAT1.0	USB_PWRD	USB Host/Device	NC	
P1.23	P1.23/MCFB1/PWM1.4/MISO0	MISO0	SD_Card	LED4	
P1.24	P1.24/MCFB2/PWM1.5/MOSI0	MOSI0	SD_Card	NC	
P1.25	P1.25/MC1A/MAT1.1	JOY_SEL	Joystick	LED_LNK	Ethernet
P1.26	P1.26/MC1B/PWM1.6/CAP0.0	JOY_DOWN	Joystick	LED_SPD	Ethernet
P1.27	P1.27/CLKOUT/USB_OVRCCR/CAP0.1	JOY_LEFT	Joystick	EN_OS_EN	Ethernet
P1.28	P1.28/MC2A1.0/MAT0.0	JOY_RIGHT	Joystick	EN_RST	Ethernet
P1.29	P1.29/MC2B/PCAP1.1/MAT0.1	JOY_UP	Joystick	NC	
P1.30	P1.30/VBUS/AD0.4	VBUS	USB Host/Device	P19	AD0.4
P1.31	P1.31/SCK1/AD0.5	ADC_IN	Potmeter	P20	AD0.5

Tabel 33 Port 2 description

IO Pin	Description	Usage LandTiger	Comment LandTiger	Usage mbed	Comment mbed
P2.0	P2.0/PWM1.1/TXD1	DB00	LCD_Bus	P26	PWM1.1/TXD1
P2.1	P2.1/PWM1.2/RXD1	DB01	LCD_Bus	P25	PWM1.2/RXD1
P2.2	P2.2/PWM1.3/CTS1/TRACEDATA3	DB02	LCD_Bus	P24	PWM1.3
P2.3	P2.3/PWM1.4/DCD1/TRACEDATA2	DB03	LCD_Bus	P23	PWM1.4
P2.4	P2.4/PWM1.5/DSR1/TRACEDATA1	DB04	LCD_Bus	P22	PWM1.5
P2.5	P2.5/PWM1.6/DTR1/TRACEDATA0	DB05	LCD_Bus	P21	PWM1.6
P2.6	P2.6/PCAP1.0/RI1/TRACECLK	DB06	LCD_Bus	NC	
P2.7	P2.7/RD2/RTS1	DB07	LCD_Bus	NC	
P2.8	P2.8/TD2/TXD2	485_DIR	RS485	NC	
P2.9	P2.9/USB_CONNECT/RXD2	USB_CONNECT	USB Host/Device	USB_CON	
P2.10	P2.10/EINT0/NMI	ISP	SW2,JP5/RTS,JP6	TGT_SBL_ISP	

P2.11	P2.11/EINT1/I2STX_CLK	KEY1	SW4	NC	
P2.12	P2.12/EINT2/I2STX_WS	KEY2	SW3	NC	
P2.13	P2.13/EINT3/I2STX_SDA	TP_INT	Touchscreen	EINT3	JTAG_IRQ on mbed

Tabel 34 Port 3 description

IO Pin	Description	Usage LandTiger	Comment LandTiger	Usage mbed	Comment mbed
P3.25	P3.25/MAT0.0/PWM1.2	SD_CD	SD_Card	NC	
P3.26	P3.26/STCLK/MAT0.1/PWM1.3	SD_PWR	SD_Card	NC	

Tabel 35 Port 4 description

IO Pin	Description	Usage LandTiger	Comment LandTiger	Usage mbed	Comment mbed
P4.28	P4.28/RX_MCLK/MAT2.0/TXD3	485_TX	RS485	NC	
P4.29	P4.29/TX_MCLK/MAT2.1/RXD3	485_RX	RS485	NC	

6 Software compatibility

6.1 Compatibility with Keil

See <http://blog.tkjelectronics.dk/2011/09/review-poweravr-nxp-lpc1768-board/>

The board has basically the same features and connections as the Keil MCB1700. This made it possible to use the examples located in the Keil examples folder, for that specific board. It just required some minor changes:

1. The LCD files should be replaced by the one from a WayEngineer example (GLCD_SPI_LPC1700.c etc.)
2. The LED initializing and controlling part should be changed, as the LEDs are not connected in the same way
3. If Analog inputs are used in the example this has to be fixed too, as in the Keil examples, the used Analog inputs are on one of the same pins as the LCD data bus.
4. Unfortunately as all of the examples are using the Keil uVision compiler, you have to download a use the evaluation period to test some of the examples (as they exceed the Lite version limit).

It would have been good if they had made a couple of demonstrations for the free GNU GCC compiler.

The WayEngineer website has many application examples (download the ZIP-file). Not all of the demonstrations may compile with the latest Keil uVision, Most of the times this just required the removal of the chip/system files, as these had to be loaded from the compiler directory instead.

Regarding the Keil uVision everything was reported to works great. The On-board programmer and debugger integrate nicely with the Keil environment – so it is very easy to program and debug your application.

Some problems were noticed getting Keil to recognize and program the board, without giving some kind of error. This was fixed by the following steps in each project:

1. Go to “Option for Target ‘...’” or press Alt+F7
2. Go to ‘Utilities’
3. Set programmer to “Cortex-M/R J-Link/J-Trace”
4. Click ‘Settings’ and then click ‘Add’
5. Find “LPC17xx IAP 512KB Flash”
6. Click ‘Add’ to confirm the selection
7. Finally tick ‘Program’, ‘Verify’ and “Reset and run”
8. And check “Erase full chip”

6.2 Compatibility with mbed

6.2.1 Hardware

LEDs
Pins
COM0

PWM

Ethernet

mbed microcontroller boards have a built-in interface to provide functionality such as drag-n-drop download, reset, serial-over-usb, and access to the mbed local file system. These functions provide means to control the interface using semihost calls it supports. The mbed Ethernet library for example sets the MAC address by calling a weak function extern "C" void mbed_mac_address(char * mac) to copy in a 6 Byte (12 character) MAC address. This function performs a semihosting request to the mbed interface to get the serial number, which contains a MAC address unique to every mbed device. If you are using the eth library on your own board (i.e. not an mbed board like the LandTiger), you should implement your own extern "C" void mbed_mac_address(char * mac) function to overwrite the existing one and avoid a call to the interface (which doesn't exist).

```
extern "C" void mbed_mac_address(char * mac) {

//MAC address may for example be cloned from scrapped modem box

    mac[0] = 0x00;
    mac[1] = 0x01;
    mac[2] = 0x02;
    mac[3] = 0x03;
    mac[4] = 0x04;
    mac[5] = 0x05;
};
```

Note1: the mbed has the ability to power down the PHY by disabling its oscillator (P1.27). The mbed is also able to reset the PHY through P1.28. Both features are not supported on the LandTiger. The PHY is always enabled and the reset occurs with the reset the LandTiger board.

Probably best to avoid using P1.27 and P1.28 in your software to prevent interference with the Ethernet library.

Note2: mbed uses the PHY LED_LINK and LED_SPEED outputs as digital inputs on P1.25 and P1.26. This allows mbed software to test the status and perhaps activate some other LED. The LandTiger PHY has LEDs connected directly to its Link, Speed and Traffic outputs. The processor pins P1.25 and P1.26 may be used for other purposes.

USB Device: Set jumpers JP9,JP11 to 1-2, Set jumper JP10 to 1-2 (Enable USB_CONNECT P2_9), VBUS P1_30 not used, USB_UP_LED P1_18 not used.

USB Host: Set jumpers JP9,JP11 to 3-4, Enable USB_PPWR (P1_19 low), USB_PWRD P1_19 not used,

The mbed interface functions that are define in 'mbed_interface.h' and which should be overridden by user provide code are:

```
/* Function: mbed_interface_connected
 * Determine whether the mbed interface is connected,
 * based on whether debug is enabled
 *
```

```
* Variables:
* returns - 1 if interface is connected, else 0

int mbed_interface_connected(void);

/* Function: mbed_interface_reset
* Instruct the mbed interface to reset, as if the
  reset button had been pressed
*
* Variables:
* returns - 1 if successful, else 0 (e.g. interface not present)
*/
int mbed_interface_reset(void);

/* Function: mbed_interface_disconnect
* This will disconnect the debug aspect of the interface,
  so semihosting will be disabled.
* The interface will still support the USB serial aspect
*
* Variables:
* returns - 0 if successful, else -1 (e.g. interface not present)
*/
int mbed_interface_disconnect(void);

/* Function: mbed_interface_powerdown
* This will disconnect the debug aspect of the interface, and if the
  USB cable is not connected, also power down the interface. If the
  USB cable is connected, the interface will remain powered up and
  visible to the host
*
* Variables:
* returns - 0 if successful, else -1 (e.g. interface not present)
*/
int mbed_interface_powerdown(void);

/* Function: mbed_interface_uid
* This returns a string containing the 32-character UID of the mbed
  interface
*
* This is a weak function that can be overwritten if required
*
* Variables:
* uid - A 33-byte array to write the null terminated 32-byte string
* returns - 0 if successful, else -1 (e.g. interface not present)
*/
int mbed_interface_uid(char *uid);

/* Function: mbed_mac_address
* This returns a unique 6-byte MAC address, based on
  the interface UID
*
* If the interface is not present, it returns a default
  fixed MAC address (00:02:F7:F0:00:00)
*
* This is a weak function that can be overwritten if you want to
  provide your own mechanism to provide a MAC address.
```

```

*
* Variables:
* mac - A 6-byte array to write the MAC address
*/
void mbed_mac_address(char *mac);

/* Function: mbed_die
* Cause the mbed to flash the BLOD LED sequence
*/
void mbed_die(void);

```

6.2.2 Downloading new application software

The mbed cloud compiler produces a .bin file. Convert the compiler .bin file with a modern bin2hex utility to prepare the software for Flashmagic. JLINK will accept the .bin files directly and flash the processor.

6.3 Compatibility with CoCoX CoIDE for ARM

CoCoX CoIDE for ARM is a free Eclipse based IDE for ARM Cores, using the GNU Compiler (GCC). It supports ARM7/9 targets as well as Cortex-M0/M3/M4 targets. More information about CoIDE and the installation process can be found here

<http://www.coocox.org>.

Please note that when using CoIDE for the first time, some additional setup is required to enable GCC in CoIDE.

For more information, please refer to http://www.coocox.org/CoIDE/Compiler_Settings.html

In the following, a short step-by-step tutorial how to get up and running with CoIDE and J-Link in general is given. For this tutorial, the sample project generator that is integrated into CoIDE was used. Used components:

IDE	CoIDE V1.4.0
Emulator	J-Link
J-Link SW Version	V4.40c
Evalboard	STM32F103ZE-EVAL (STM32F103ZG)
Additional SW	GCC Toolchain

Start CoIDE and click New Project button from the status bar.

Enter a Project Name and click Finish

Zie screendumps

Zie http://www.segger.com/cms/IDE_Integration_coocox.html

Copy ook de screenshots !!!

7 JTAG Interface Description

The JTAG technology was defined by IEEE Std.-1149.1 standard and it exists for over a decade. JTAG is used mostly for Connection testing and In System Programming (ISP).

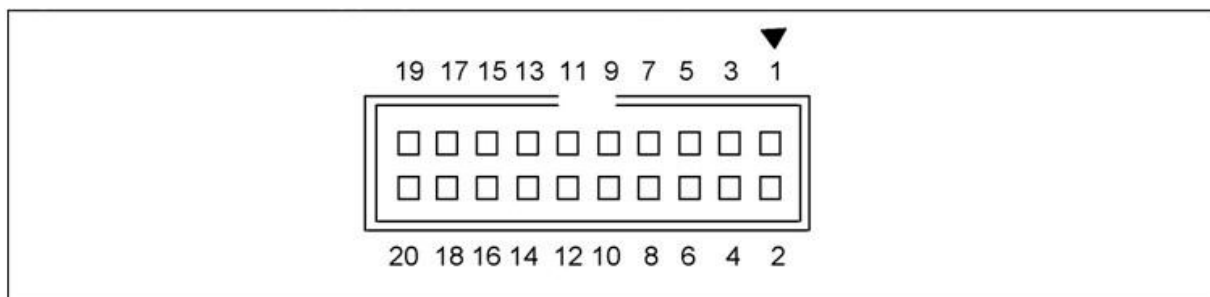
The JTAG interface is 4/5-pin interface added to a chip, the interface is designed such that multiple chips having a JTAG interface have their JTAG lines daisy-chained together, and a test probe need only connect to a single “JTAG port” to have access to all chips on a circuit board. The basic connector pins are:

Tabel 36 Basic JTAG Signals

Pin	Signal	Description	Comment
1	TDI	Test Data In	
2	TDO	Test Data Out	
3	TCK	Test Clock	
4	TMS	Test Mode Select	
5	TRST	Test Reset	optional.

7.1 JTAG standard connector for ISP and Debugging

Many modern programmable devices, such as FPGAs and CPLDs, are designed not only to be JTAG compliant, but also support additional JTAG functionality to allow them to be programmed after they have been attached to the circuit. Other devices, such as some flash memories, can be programmed indirectly through their connection to devices in the JTAG chain. The ability to use JTAG to program devices ‘in system’ avoids the need to buy expensive programmers and socketed devices. There is also the advantage of being able to easily update the image held on the device. The standard 20 pin 2.54mm (0.1”) JTAG connector was defined by ARM. J-Link has a built-in 20-pin JTAG connector, which is compatible with this standard.



Figuur 33 JTAG Standard 20 Pin Connector

Tabel 37 Standard JTAG interface 20 pin connector signals

Pin	Signal	Type	Description
1	VTref	Input	This is the target reference voltage.

			It is used to check if the target has power, to create the logic-level reference for the input comparators and to control the output logic levels to the target. It is normally fed from Vdd of the target board and must not have a series resistor.
2	Vsupply	NC	This pin is not connected in J-Link. It is reserved for compatibility with other equipment. Connect to Vdd or leave open in target system.
3	nTRST	Output	JTAG Reset. Output from J-Link to the Reset signal of the target JTAG port. Typically connected to nTRST of the target CPU. This pin is normally pulled HIGH on the target to avoid unintentional resets when there is no connection.
5	TDI	Output	JTAG data input of target CPU. It is recommended that this pin is pulled to a defined state on the target board. Typically connected to TDI of target CPU.
7	TMS	Output	JTAG mode set input of target CPU. This pin should be pulled up on the target. Typically connected to TMS of target CPU.
9	TCK	Output	JTAG clock signal to target CPU. It is recommended that this pin is pulled to a defined state of the target board. Typically connected to TCK of target CPU.
11	RTCK	Input	Return test clock signal from the target. Some targets must synchronize the JTAG inputs to internal clocks. To assist in meeting this requirement, you can use a returned, and retimed, TCK to dynamically control the TCK rate. J-Link supports adaptive clocking, which waits for TCK changes to be echoed correctly before making further changes. Connect to RTCK if available, otherwise to GND.
13	TDO	Input	JTAG data output from target CPU. Typically connected to TDO of target CPU.
15	RESET	I/O	Target CPU reset signal.

			Typically connected to the RESET pin of the target CPU, which is typically called "nRST", "nRESET" or "RESET".
17	DBGRRQ	NC	This pin is not connected in J-Link. It is reserved for compatibility with other equipment to be used as a debug request signal to the target system. Typically connected to DBGRRQ if available, otherwise left open.
19	5V-Target supply	Output	This pin can be used to supply power to the target hardware.

Note1: All pins marked NC are not connected inside J-Link. Any signal can be applied here; J-Link will simply ignore such a signal.

Note2: Pins 4, 6, 8, 10, 12, 14, 16, 18, 20 are GND pins connected to GND in J-Link. They should also be connected to GND in the target system.

Note3: Pin 2 is not connected inside J-Link. A lot of targets have pin 1 and pin 2 connected. Some targets use pin 2 instead of pin 1 to supply VCC. These targets will not work with J-Link, unless Pin 1 and Pin 2 are connected on the target's JTAG connector.

Note4: Pin 3 (TRST) should be connected to target CPUs TRST pin (sometimes called NTRST). J-Link will also work if this pin is not connected, but you may experience some limitations when debugging. TRST should be separate from the CPU Reset (pin 15)

Note5: Pin 11 (RTCK) should be connected to RTCK if available, otherwise to GND.

Note6: Pin 19 (5V-Target supply) of the connector can be used to supply power to the target hardware. Supply voltage is 5V, max. current is 300mA. The output current is monitored and protected against overload and short-circuit.

There are also other JTAG connectors in use. This includes:

- 20 pin JTAG version with 2mm pin pitch and the same pinout as standard JTAG
- 14 pin JTAG version with 2.54mm pin pitch
- 10 pin JTAG version with 2.54mm (0.1") pin pitch
- 10 pin JTAG version with 2.00mm pin pitch.
- 9 pin JTAG version with 1.27mm (0.05") pin pitch
- 19 pin JTAG version with 1.27mm (0.05") pin pitch
- 6 pin 2.54mm pin pitch socket - SWD Interface for Cortex Core
- 4 pin 2.54mm pin pitch socket - SWD Interface-Cortex Core

Tabel 38 JTAG interface 14 pin connector signals

Pin	Signal	Type	Description
1	VTref	Input	This is the target reference voltage. It is used to check if the target has

			power, to create the logic-level reference for the input comparators and to control the output logic levels to the target. It is normally fed from Vdd of the target board and must not have a series resistor.
2	GND		
3	nTRST	I/O	Target CPU reset signal. Typically connected to the RESET pin of the target CPU, which is typically called "nRST", "nRESET" or "RESET".
4	GND		
5	TDI	Output	JTAG data input of target CPU. It is recommended that this pin is pulled to a defined state on the target board. Typically connected to TDI of target CPU.
6	GND		
7	TMS	Output	JTAG mode set input of target CPU. This pin should be pulled up on the target. Typically connected to TMS of target CPU.
8	GND		
9	TCK	Output	JTAG clock signal to target CPU. It is recommended that this pin is pulled to a defined state of the target board. Typically connected to TCK of target CPU.
10	GND		
11	TDO	Input	JTAG data output from target CPU. Typically connected to TDO of target CPU.
12	nSRST		
13	Vsupply	NC	This pin is not connected in J-Link. It is reserved for compatibility with other equipment. Connect to Vdd or leave open in target system.
14	GND		

Tabel 39 JTAG interface 10 pin connector signals

Pin	Signal	Type	Description
1	VTref	Input	This is the target reference voltage. It is used to check if the target has power, to create the logic-level reference for the input comparators and to control the output logic levels to the target. It is normally fed from

			Vdd of the target board and must not have a series resistor.
2	Vsupply	NC	This pin is not connected in J-Link. It is reserved for compatibility with other equipment. Connect to Vdd or leave open in target system.
3	RESET	I/O	Target CPU reset signal. Typically connected to the RESET pin of the target CPU, which is typically called "nRST", "nRESET" or "RESET".
4	RESET	I/O	Target CPU reset signal. Typically connected to the RESET pin of the target CPU, which is typically called "nRST", "nRESET" or "RESET".
5	TDI	Output	JTAG data input of target CPU. It is recommended that this pin is pulled to a defined state on the target board. Typically connected to TDI of target CPU.
6	NC/TDO	NC/Input	JTAG data output from target CPU. Typically connected to TDO of target CPU.
7	TMS	Output	JTAG mode set input of target CPU. This pin should be pulled up on the target. Typically connected to TMS of target CPU.
8	GND		
9	TCK	Output	JTAG clock signal to target CPU. It is recommended that this pin is pulled to a defined state of the target board. Typically connected to TCK of target CPU.
10	GND		

7.2 SWD and SWO/SWV (also called SWV) compatibility

The J-Link and J-Trace support ARM's Serial Wire Debug (SWD). The SWD replaces the standard JTAG port with a clock (SWDCLK) and a single bi-directional data pin (SWDIO), providing all the normal JTAG debug and test functionality. SWDIO and SWCLK are overlaid on the TMS and TCK pins. In order to communicate with a SWD device, J-Link sends out data on SWDIO, synchronous to the SWCLK. With every rising edge of SWCLK, one bit of data is transmitted or received on the SWDIO. The data read from SWDIO can then be retrieved from the input buffer.

Tabel 40 SWD pinout on 20 pin connector

Pin	Signal	Type	Description
1	VTref	Input	This is the target reference voltage. It is used to check if the target has power, to create the logic-level reference for the input comparators and to control the output logic levels to the target. It is normally fed from Vdd of the target board and must not have a series resistor.
2	Vsupply	NC	This pin is not connected in J-Link. It is reserved for compatibility with other equipment. Connect to Vdd or leave open in target system.
3	Not used	NC	This pin is not used by J-Link. If the device may also be accessed via JTAG, this pin may be connected to nTRST, otherwise leave open.
5	Not used	NC	This pin is not used by J-Link. If the device may also be accessed via JTAG, this pin may be connected to TDI, otherwise leave open.
7	SWDIO	I/O	Single bi-directional data pin.
9	SWCLK	Output	Clock signal to target CPU. It is recommended that this pin is pulled to a defined state of the target board. Typically connected to TCK of target CPU.
11	Not used	NC	This pin is not used by J-Link. This pin is not used by J-Link when operating in SWD mode. If the device may also be accessed via JTAG, this pin may be connected to RTCK, otherwise leave open.
13	SWO	Output	Serial Wire Output trace port. (Optional, not required for SWD communication.)
15	RESET	I/O	Target CPU reset signal. Typically connected to the RESET pin of the target CPU, which is typically called "nRST", "nRESET" or "RESET".
17	Not used	NC	This pin is not connected in J-Link.
19	5V-Supply	Output	This pin is used to supply power to some eval boards. Not all JLinks supply power on this pin, only the KS (Kickstart) versions. Typically left open on target hardware.

Note1: Pins 4, 6, 8, 10, 12, 14, 16, 18, 20 are GND pins connected to GND in J-Link. They should also be connected to GND in the target system.

7.3.1 Serial Wire Output (SWO) compatibility

J-Link can be used with devices that support Serial Wire Output (SWO). Serial Wire Output (SWO) support means support for a single pin output signal from the core. It is currently tested with Cortex-M3 only.

The supported SWO speeds depend on the connected emulator. They can be retrieved from the emulator. Currently, the following are supported:

Emulator	Speed, formula	Resulting max. speed
J-Link V6	6MHz/n, n >= 12	500kHz
J-Link V7	6MHz/n, n >= 1	6MHz

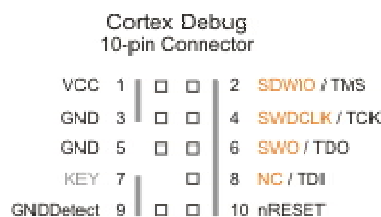
7.3.2 Serial Wire Viewer (SWV) compatibility

The Instrumentation Trace Macrocell (ITM) and Serial Wire Output (SWO) can be used to form a Serial Wire Viewer (SWV). The Serial Wire Viewer provides a low cost method of obtaining information from inside the MCU. The SWO can output trace data in two output formats, but only one output mechanism is valid at any one time. The two defined encodings are UART and Manchester. The current J-Link implementation supports only UART encoding. Serial Wire Viewer uses the SWO pin to transmit different packets for different types of information. The three sources in the Cortex-M3 core which can output information via this pin are:

- Instrumentation Trace Macrocell (ITM) for application-driven trace source that supports printf-style debugging. It supports 32 different channels, which allow it to be used for other purposes such as real-time kernel information as well.
- Data Watchpoint and Trace (DWT) for real-time variable monitoring and PC-sampling, which can in turn be used to periodically output the PC or various CPU-internal counters, which can be used to obtain profiling information from the target.
- Timestamping. Timestamps are emitted relative to packets.

7.3.3 Cortex 10 Pin Debug compatibility

The Cortex Debug Connector provides support for Serial Wire and JTAG interface modes in a very small, low cost 10-pin (0.05") connector. This new style connector provides access to all SWD, SWV, and JTAG signals available on a Cortex-Mx device.



A 10-pin header ([Samtec FTSH-105-01](#)) is specified with dimensions: 0.25" x 0.188" (6.35mm x 4.78mm).

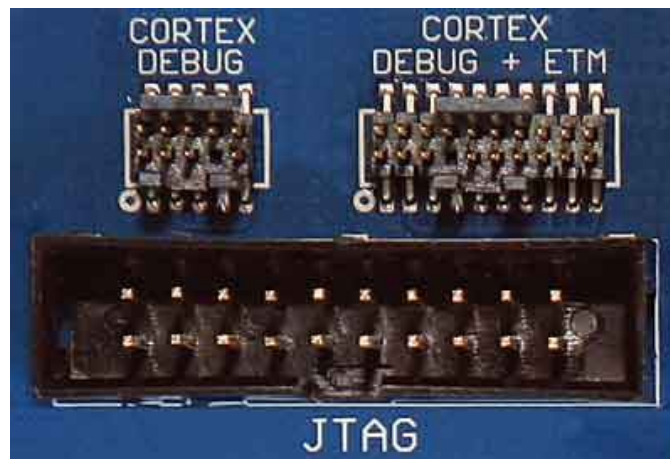
7.3.4 Cortex 20 Pin Debug compatibility

The Cortex Debug+ETM Connector is a new small 20-pin (0.05") connector that provides access to SWD, SWV, JTAG, and ETM (4-bit) signals available on a Cortex-M3 device.

A 20-pin header ([Samtec FTSH-110-01](#)) is specified with dimensions: 0.50" x 0.188" (12.70mm x 4.78mm).

**Cortex-M3 / ETM Debug Interface
20-pin Connector**

Vtref	1	□ □	2	SDWIO / TMS
GND	3	□ □	4	SWDCLK / TCK
GND	5	□ □	6	SWO/EXTb/TRACECTL / TDO
KEY	7	□	8	NC/EXTb / TDI
GNDDetect	9	□ □	10	nRESET
GND/TgtPwr+Cap	11	□ □	12	TRACECLK
GND/TgtPwr+Cap	13	□ □	14	TRACEDATA[0]
GND	15	□ □	16	TRACEDATA[1]
GND	17	□ □	18	TRACEDATA[2]
GND	19	□ □	20	TRACEDATA[3]



Figuur 34 Standard and smaller new connectors

7.3.5 ARM ETM 'Mictor' Connector (38-pin)

The Mictor (Matched Impedance ConnecTOR) has been the standard way to connect a trace probe to an ARM target. It supports up to 32-bit ETM trace and is really intended for use with very high-speed ARM processors such as Cortex-R4 and Cortex-A9. As Cortex-M3 ETM only supports 4-bit trace, the best connector solution to support debug and ETM is the 20-pin Cortex Debug+ETM connector.



8 References

PowerMCU: www.PowerMCU.com

LandTiger Schematic: LandTiger V2.0 Schematic.pdf

HY32D Schematic: HY32D_SCH.pdf

HY32C Schematic <http://propix.com.pl/pl/p/LCD-3.2-TFT-SSD1289-HY-32C/194>

ARM: www.arm.com

NXP: www.nxp.com

LPC1768 Datasheets and Documentation: www.nxp.com

Keil Compilers and IDE: www.keil.com

JLINK: www.segger.com.

GNU tools: <https://sourcery.mentor.com/sgpp/lite/arm/portal/release1802>

Flashmagic: <http://www.flashmagictool.com/>

Mbed: www.mbed.org

Bin2Hex: <http://www.hex2bin.com/bin2hex>
(or if your running a 64-bit system use this instead
<http://www.ht-lab.com/freetils/bin2hex/bin2hex.zip>)

CooCox IDE: <http://www.coocox.org>