LAB:14

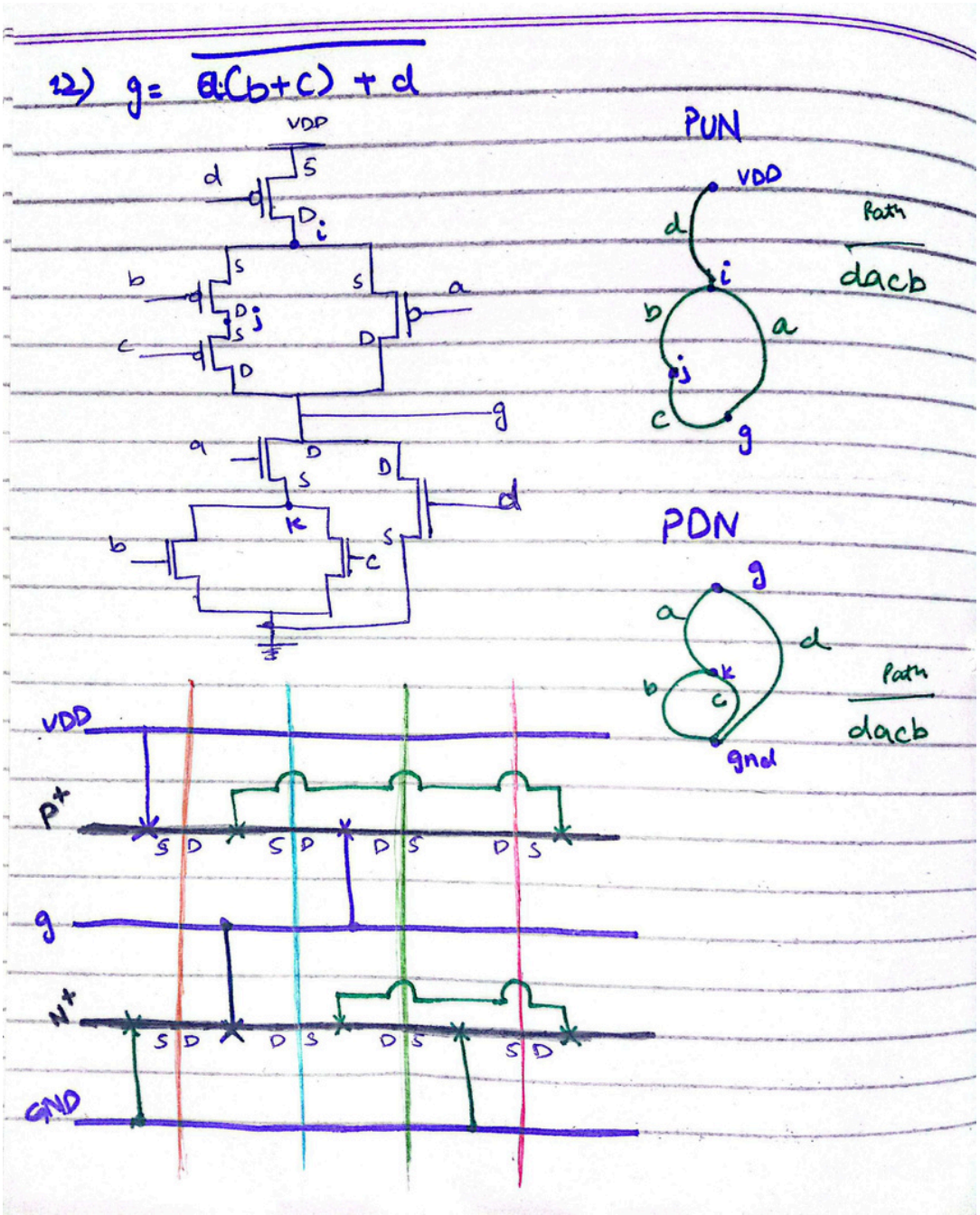
From the Boolean functions given below (Choose one, Sr# = Group#), present the Truth table and design schematics of static CMOS gates. Draw the logic graph and find common Euler Paths for pull-up and pull-down network. Sketch the corresponding stick diagram. Follow the complete design flow pattern as covered in Lab # 13.

NOTES:

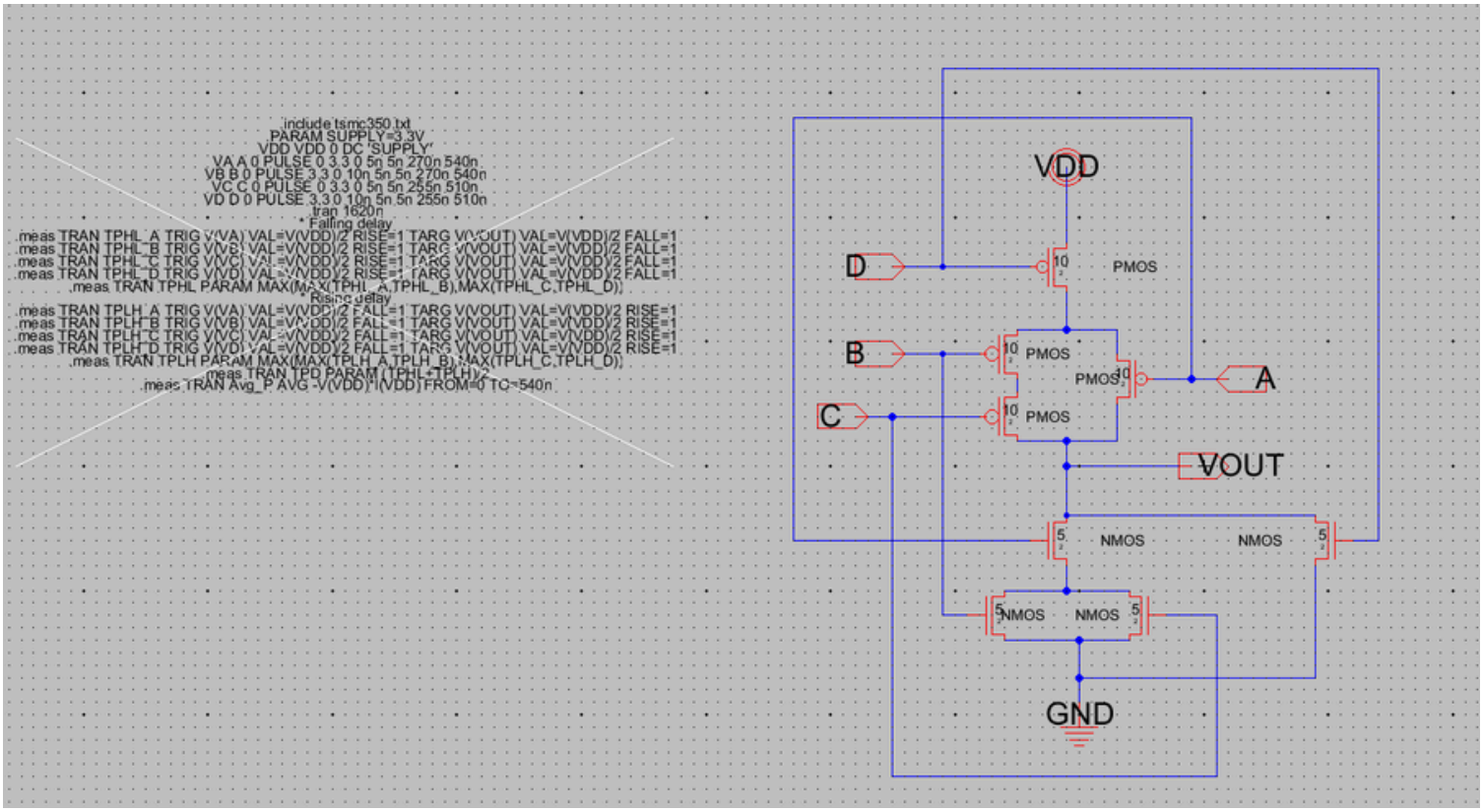
A. Draw static CMOS logic circuits that implement the given functions. For an N input gate, there should be 2N number of transistors in the circuits.

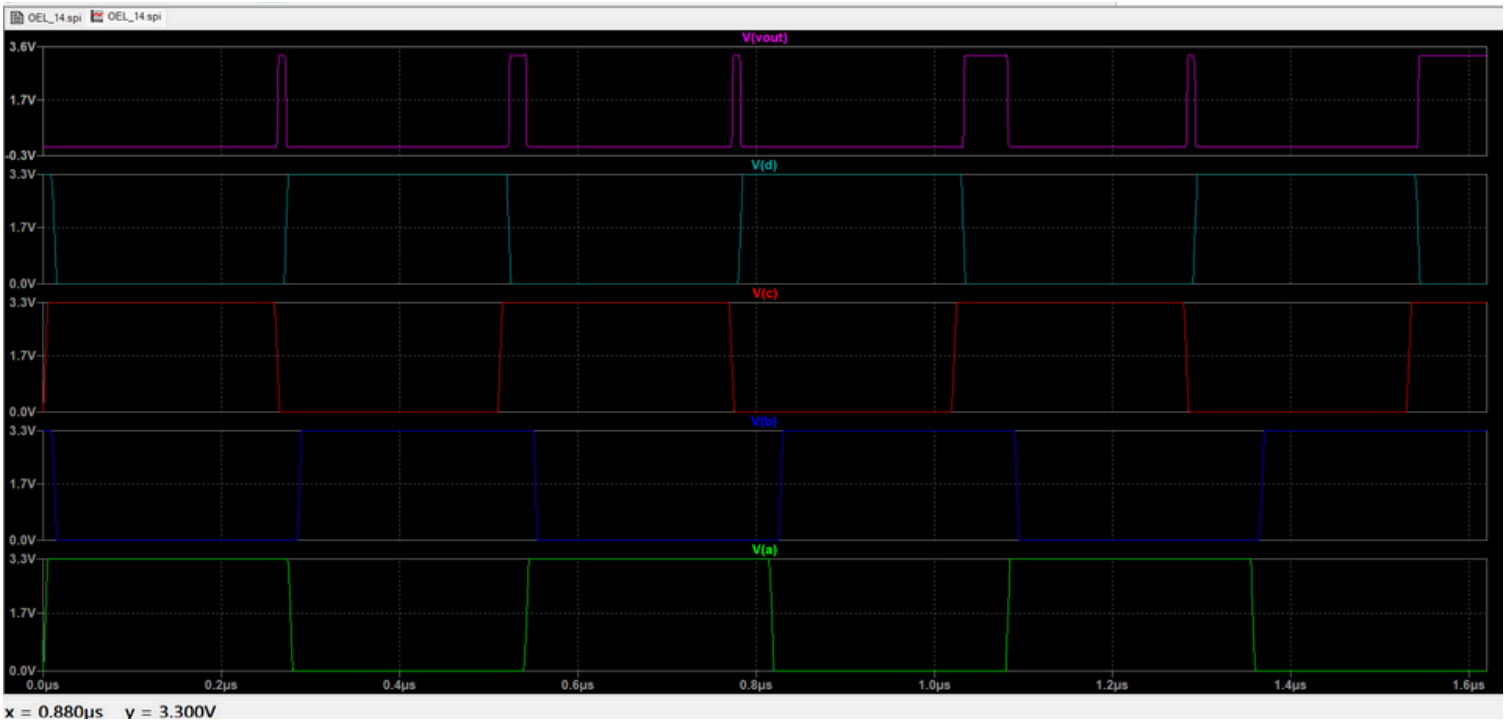
B. Draw Euler graphs for the circuits drawn in part A. Thus, derive Euler paths to determine the right input order and draw stick diagrams accordingly.
Note: (Use multiple color markers for stick diagrams. For consistency, following color markers are recommended for all problems: **N+ active: green, P+ active: Brown, Poly: Red, Metal: Blue, VIA/ Contacts: Black,** N-Well: Yellow)

12. $g = \overline{a \cdot (b+c)+d}$

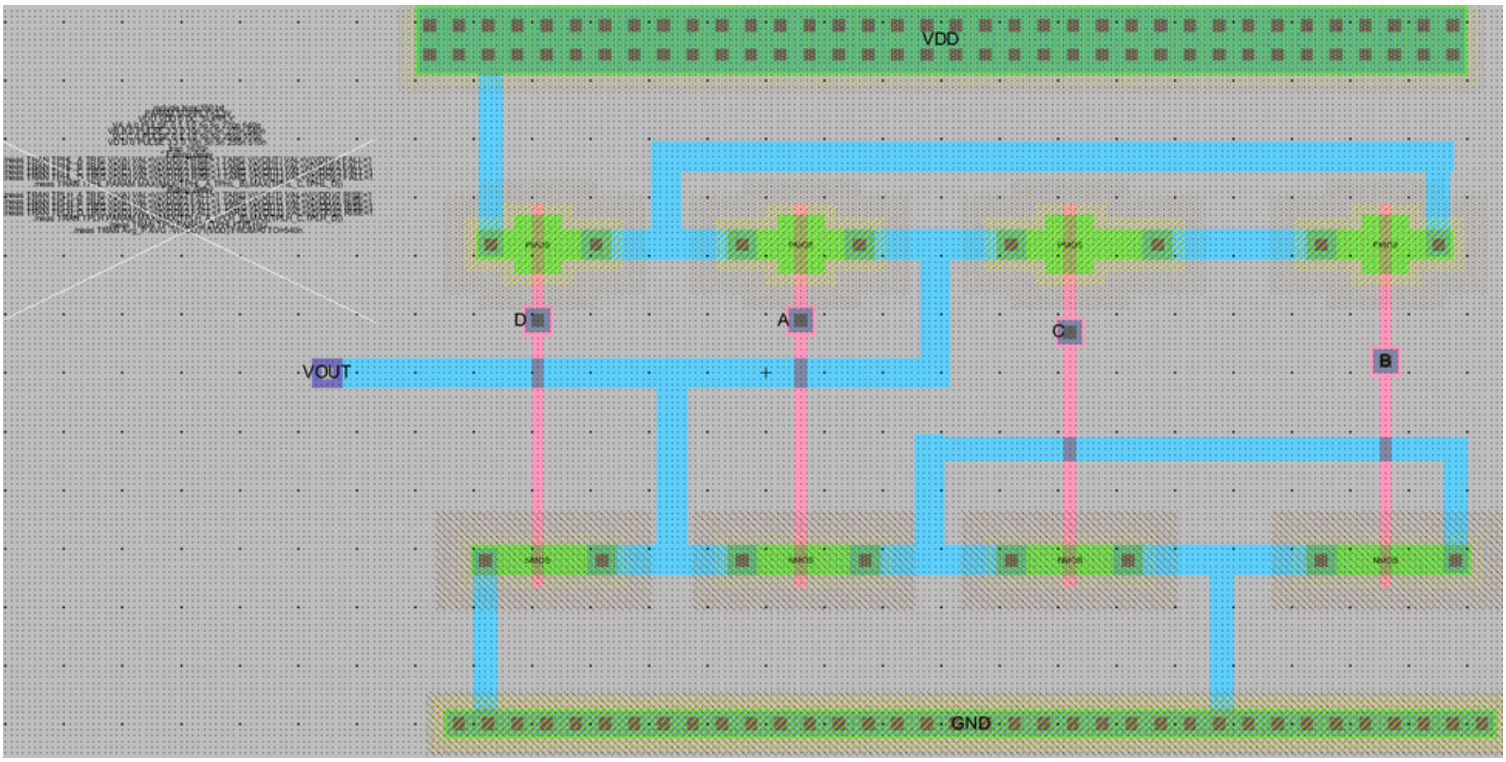


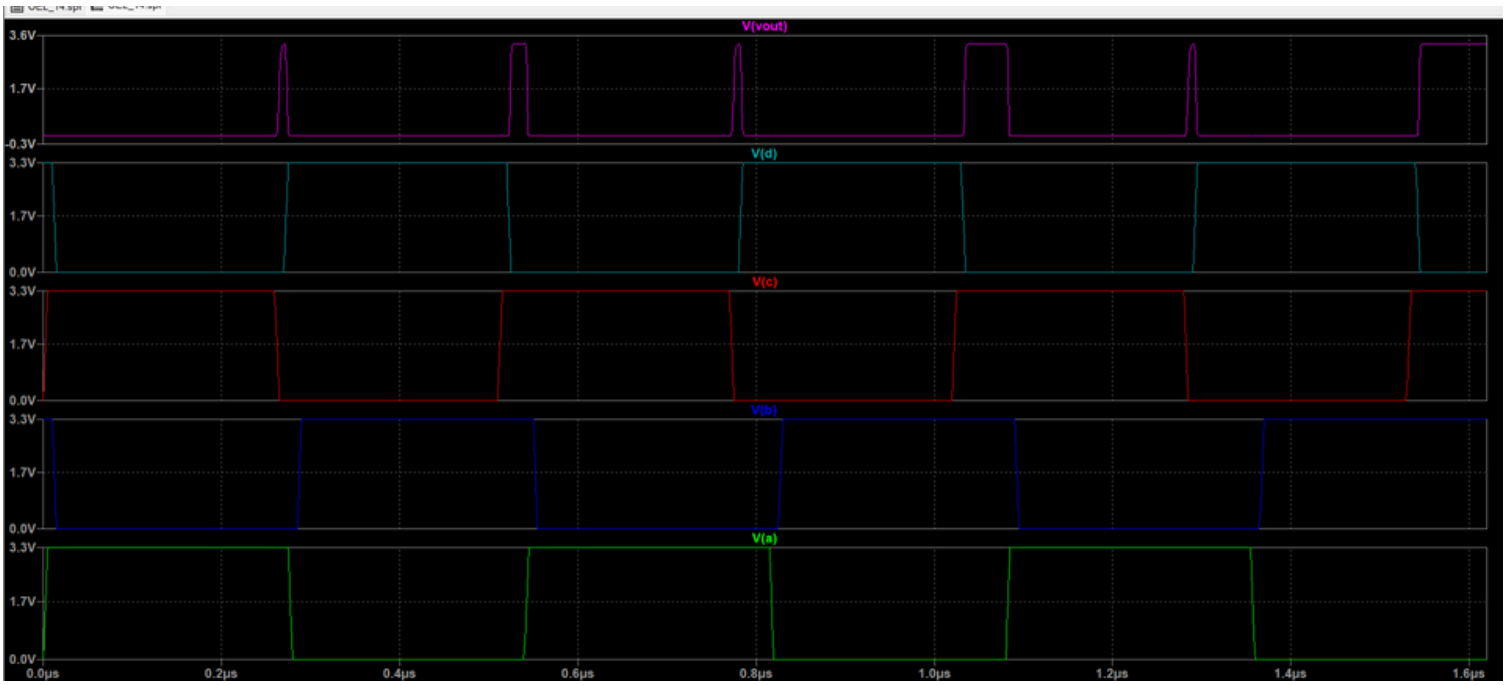
SCHEMATIC:


.include tsmc350.txt
.PARAM SUPPLY=3.3V
VDD VDD 0 DC 'SUPPLY'
VA A 0 PULSE 0 3.3 0 5n 5n 270n 540n
VB B 0 PULSE 3.3 0 10n 5n 5n 270n 540n
VC C 0 PULSE 0 3.3 0 5n 5n 255n 510n
VD D 0 PULSE 3.3 0 10n 5n 5n 255n 510n
.tran 1620n
* Falling delay
.meas TRAN TPHL_A TRIG V(VA) VAL=V(VDD)/2 RISE=1 TARG V(VOUT) VAL=V(VDD)/2 FALL=1
.meas TRAN TPHL_B TRIG V(VB) VAL=V(VDD)/2 RISE=1 TARG V(VOUT) VAL=V(VDD)/2 FALL=1
.meas TRAN TPHL_C TRIG V(VC) VAL=V(VDD)/2 RISE=1 TARG V(VOUT) VAL=V(VDD)/2 FALL=1
.meas TRAN TPHL_D TRIG V(VD) VAL=V(VDD)/2 RISE=1 TARG V(VOUT) VAL=V(VDD)/2 FALL=1
.meas TRAN TPHL PARAM MAX(MAX(TPHL_A,TPHL_B),MAX(TPHL_C,TPHL_D))
* Rising delay
.meas TRAN TPLH_A TRIG V(VA) VAL=V(VDD)/2 FALL=1 TARG V(VOUT) VAL=V(VDD)/2 RISE=1
.meas TRAN TPLH_B TRIG V(VB) VAL=V(VDD)/2 FALL=1 TARG V(VOUT) VAL=V(VDD)/2 RISE=1
.meas TRAN TPLH_C TRIG V(VC) VAL=V(VDD)/2 FALL=1 TARG V(VOUT) VAL=V(VDD)/2 RISE=1
.meas TRAN TPLH_D TRIG V(VD) VAL=V(VDD)/2 FALL=1 TARG V(VOUT) VAL=V(VDD)/2 RISE=1
.meas TRAN TPLH PARAM MAX(MAX(TPLH_A,TPLH_B),MAX(TPLH_C,TPLH_D))
.meas TRAN TPD PARAM '(TPHL+TPLH)/2'
.meas TRAN Avg_P AVG -V(VDD)*I(VDD) FROM=0 TO=540n
VDD
D
B
C
A
VOUT
GND
PMOS
NMOS


OEL_14.spi
V(vout)
3.6V
1.7V
-0.3V
V(d)
3.3V
1.7V
0.0V
V(c)
V(b)
V(a)
0.0µs
0.2µs
0.4µs
0.6µs
0.8µs
1.0µs
1.2µs
1.4µs
1.6µs
x = 0.880µs y = 3.300V

LAYOUT:





Design Rule Check (DRC)

```
Checking cell 'OEL_14{lay}'
        No errors/warnings found
0 errors and 0 warnings found (took 0.199 secs)
```

Layout vs schematic analysis (NCC)

```
  exports match, topologies match, sizes match in 0.086 seconds.
Summary for all cells: exports match, topologies match, sizes match
NCC command completed in: 0.102 seconds.
```

Sr#	Without Sizing		With Sizing	
	t_{pLH}	t_{pHL}	t_{pLH}	t_{pHL}
1.	tplh=2.51386136178e-07	tphl=2.6949056936e-07		
2.			tplh=2.52242137734e-07	tphl=2.71039164452e-07