create a file sample.txt, copy the content from https://en.wikipedia.org/wiki/Verilog In the above file write a python script to do the following

1. count total number of lines and words, print the value
2. count how many times verilog word (with exact matching word) repeated. print the value
3. count how many times verilog word (no need of exact matching word) repeated. print the value
4. Count how many times verilog is starting word in the line
5. Replace verilog with VHDL (with exact matching word) and save the content to sample_vhdl.txt
6. Remove empty line and update sample_ver.txt