

Design a circuit which generates the Fibonacci sequence starting with 1 and 1 as the first two numbers. The Fibonacci sequence is a sequence of numbers where each number is the sum of the two previous numbers. More formally this can be expressed as: $F_0 = 1$ $F_1 = 1$ $F_n = F_{n-1} + F_{n-2}$ for $n > 1$. Following the definition of the Fibonacci sequence above we can see that the sequence is 1, 1, 2, 3, 5, 8, 13, etc. The sequence should be produced when the active low signal (resetn) becomes active. In other words, the sequence should restart from 1 followed by another 1 (the Fibonacci sequence's initial condition) as soon as resetn becomes active.

Input and Output Signals

- clk - Clock signal
- resetn - Synchronous reset-low signal
- out - Current Fibonacci number

Output signals during reset

- out - 1 when resetn is active (the first 1 of the Fibonacci sequence)