In this question, design a Mealy Finite State Machine (FSM) that has five states, S0-S4. Upon resetn logic low, the FSM resets and current state becomes S0. The inputs din and cen are registered inside the module, therefore, their registers also reset to zero. When resetn = 1, the FSM starts its operation. doutx must produce one whenever the current cycle din as well as the previous cycle din have the same values. Similarly, douty must output one whenever the current cycle din is the same now as it was for the past two cycles. Input cen (the registered version of it, inside the module) is used to gate the output. That is, in a particular cycle, if cen = 0, then outputs doutx and douty are both zero. Try to solve this question using a textbook Mealy FSM approach. Sketch the state diagrams with the five possible state and the allowed transitions between them.

Input and Output Signals

- clk - Clock signal
- resetn - Synchronous, active low, reset signal
- cen - Chip enable
- din - 1-bit input a
- doutx - 1-bit output x
- douty - 1-bit output y

Output signals during reset

- doutx - 0
- douty – 0

Example:

In the example, initially, resetn = 0 & din = 0. In the next cycle, resetn is unpressed, din = 0 and cen = 0. Output doutx is asserted as din was 0 for the current and previous cycle. When din switches to one, doutx is deasserted. doutx and douty are asserted again after a few cycles with din = 1. Note that cen = 1 for most of the time, that is, the outputs are not gated.