Build a circuit that pulses dout one cycle after the rising edge of din. A pulse is defined as writing a single-cycle. When resetn is asserted, the value of din should be treated as 0.

*Even if din maintains a value of 1 for mulitple cycles after its rising edge, dout's pulse should only last for exactly one cycle.

*If din has multiple rising edges, dout will have multiple pulses.

*If resetn goes low in the same cycle as the input's rising edge, the resetn specification takes priority. This means the output is 0, instead of a pulse.

Input and Output Signals

clk - Clock signal

resetn - Synchronous reset-low signal

din - Input signal

dout - Output signal

Output signals during reset

dout - 0 when resetn is active