TEAM 22

JASWANTH PALLAPPA
HEMANJALI GERIDIPUDI
NITHISHA BUPATHI RAJU
DHUSHYANTH

TEST PLAN FOR MEMORY CONTROLLER

The memory controller is capable of serving a 12-core 4.8 GHz processor with a single 16GB PC5-38400 DIMM. It exploits a closed page policy and exhibits FCFS IN-ORDER scheduling. The controller is able to a handle a queue of 16 outstanding requests.

Here, to verify the functionality of the simulation I have considered four test cases.

CASE 1:

This test is done to verify the closed page nature of the Memory Controller.

Here, I have given two inputs with access to the same row, but different columns. If it is an open page policy, the simulated result does not include the pre-charge command when there is a page hit (Access to the same row). However, if it is a closed page policy, irrespective of the access pattern to the next row, the DRAM Memory Controller will always issue a pre-charge command.

TEST INPUTS:

0	1	000000000	0
1	8	000000028	1

EXPECTED OUTPUT:

2	0	ACT0	0	0	0	
4	0	ACT1	0	0	0	
82	0	RD0		0	0	0
84	0	RD1		0	0	0
180	0	PRE		0	0	
258	0	ACT0	0	0	0	
260	0	ACT1	0	0	0	
338	0	WR0		0	0	A
340	0	WR1		0	0	A
432	0	PRE		0	0	

CASE 2: TEST FOR t_{RRD_L}

The test case to verify the Row-to-Row column delay Long. This is done specially to verify that the row access with in the same bank group behaves differently from the row access to the different bank group.

TEST INPUTS:

0	10	000202E27	0
1	8	000222636	1
2	7	0000D6E2A	1

3	6	000120E22	2
4	5	000294A38	1

EXPECTED OUTPUT:

2	0	ACT0	4	3	8	
4	0	ACT1	4	3	8	
82	0	RD0		4	3	29
84	0	RD1		4	3	29
180	0	PRE		4	3	
258	0	ACT0	4	1	8	
260	0	ACT1	4	1	8	
338	0	WR0		4	1	22D
340	0	WR1		4	1	22D
432	0	PRE		4	1	
510	0	ACT0	4	3	3	
512	0	ACT1	4	3	3	
590	0	WR0		4	3	16A
592	0	WR1		4	3	16A
684	0	PRE		4	3	
762	0	ACT0	4	3	4	
764	0	ACT1	4	3	4	
842	0	RD0		4	3	208
844	0	RD1		4	3	208
940	0	PRE		4	3	
1018	0	ACT0	4	2	A	
1020	0	ACT1	4	2	A	
1098	0	WR0		4	2	14E
1100	0	WR1		4	2	14E
1192	0	PRE		4	2	

TEST CASE 3: Over all test

This test is to verify that the simulation is correctly mapping the address bits and accessing the queue properly and showcasing the outputs at the right CPU Clock cycle.

TEAM 22

JASWANTH PALLAPPA **NITHISHA BUPATHI RAJU**
HEMANJALI GERIDIPUDI **DHUSHYANTH**

TEST INPUTS:

0	1	0000B6BBC	0
1	8	000120735	1
2	2	0001BAAAF	1
3	9	000120E22	2
4	10	000190932	1
5	5	0001E35A9	0

EXPECTED OUTPUT:

2	0	ACT0	7	2	2	
4	0	ACT1	7	2	2	
82	0	RD0		7	2	36F
84	0	RD1		7	2	36F
180	0	PRE		7	2	
258	0	ACT0	6	1	4	
260	0	ACT1	6	1	4	
338	0	WR0		6	1	20D
340	0	WR1		6	1	20D
432	0	PRE		6	1	
510	0	ACT0	5	2	6	
512	0	ACT1	5	2	6	
590	0	WR0		5	2	3AB
592	0	WR1		5	2	3AB
684	0	PRE		5	2	
762	0	ACT0	4	3	4	
764	0	ACT1	4	3	4	
842	0	RD0		4	3	208
844	0	RD1		4	3	208
940	0	PRE		4	3	
1018	0	ACT0	2	2	6	
1020	0	ACT1	2	2	6	
1098	0	WR0		2	2	10C

1100	0	WR1		2	2	10C
1192	0	PRE		2	2	
1270	0	ACT0	3	1	7	
1272	0	ACT1	3	1	7	
1350	0	RD0		3	1	23A
1352	0	RD1		3	1	23A
1448	0	PRE		3	1	

CASE 4:

This test is run to verify if the memory controller can handle an empty queue. Here, some memory requests are given initially and the memory controller is made stall by not providing any inputs for a huge time lapse. This will exhaust the queue and make it empty. After which, another request is sent to test if the memory controller can stall for some time and again process the requests after some time.

TEST INPUTS:

0	1	0000B6BBC	0
1	8	000120735	1
2	2	0001BAAAF	1
3	9	000120E22	2
4	10	000190932	1
5000	5	0001E35A9	0

EXPECTED RESULTS:

2	0	ACT0	7	2	2	
4	0	ACT1	7	2	2	
82	0	RD0		7	2	36F
84	0	RD1		7	2	36F
180	0	PRE		7	2	
258	0	ACT0	6	1	4	
260	0	ACT1	6	1	4	
338	0	WR0		6	1	20D
340	0	WR1		6	1	20D
432	0	PRE		6	1	
510	0	ACT0	5	2	6	

512	0	ACT1	5	2	6	
590	0	WR0		5	2	3AB
592	0	WR1		5	2	3AB
684	0	PRE		5	2	
762	0	ACT0	4	3	4	
764	0	ACT1	4	3	4	
842	0	RD0		4	3	208
844	0	RD1		4	3	208
940	0	PRE		4	3	
1018	0	ACT0	2	2	6	
1020	0	ACT1	2	2	6	
1098	0	WR0		2	2	10C
1100	0	WR1		2	2	10C
1192	0	PRE		2	2	
5002	0	ACT0	3	1	7	
5004	0	ACT1	3	1	7	
5082	0	RD0		3	1	23A
5084	0	RD1		3	1	23A
5180	0	PRE		3	1	