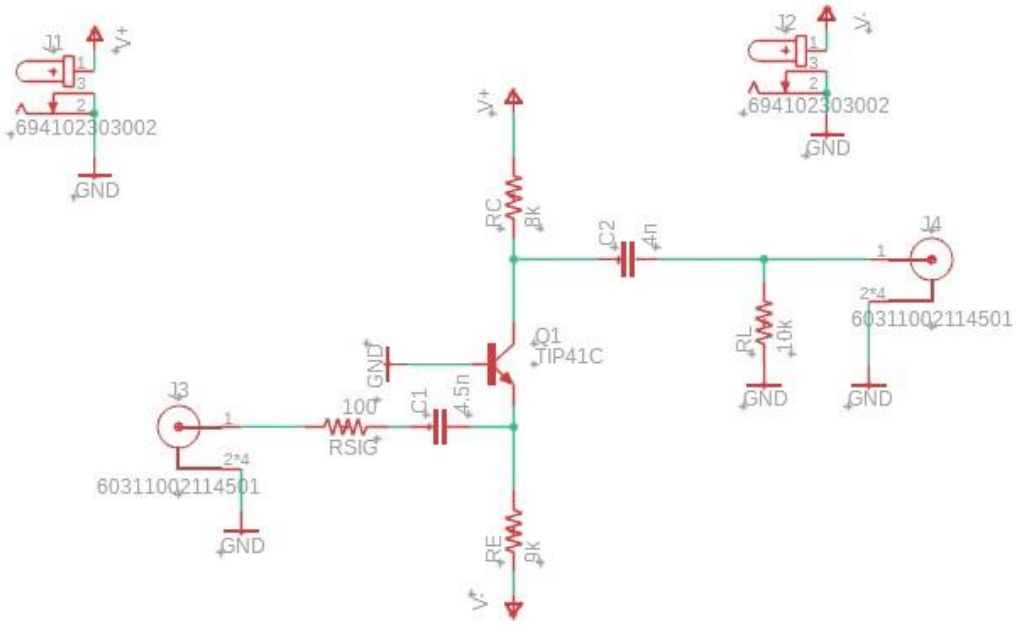
NATIONAL TECHNICAL UNIVERSITY OF ATHENS
SCHOOL OF ELECTRICAL AND COMPUTER ENGINEERING

MICROELECTRONICS AND PACKAGING TECHNIQUES
ACADEMIC YEAR 2023-2024

FINAL LAB PROJECT

1. **Circuit Description:** We have a common-base (CB) circuit using a BJT transistor. Our circuit has the following form:



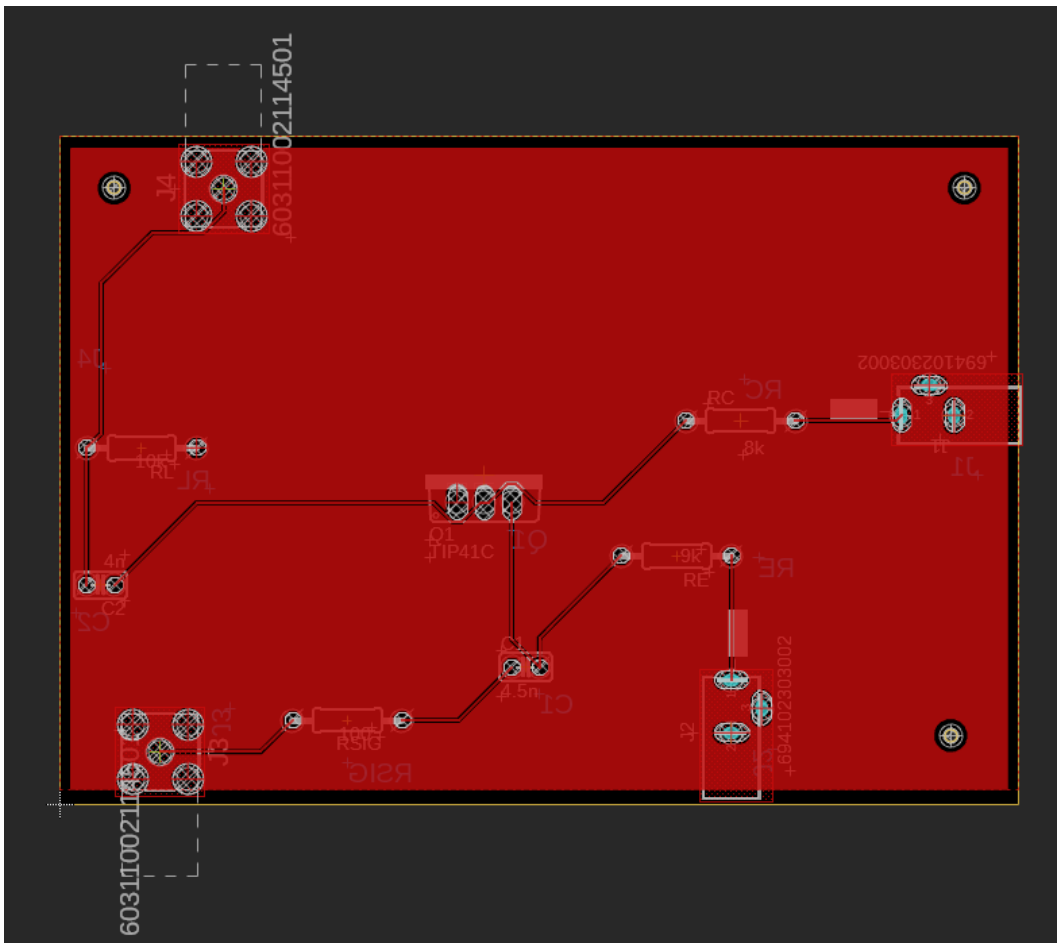
The expected gain is calculated by the formula:

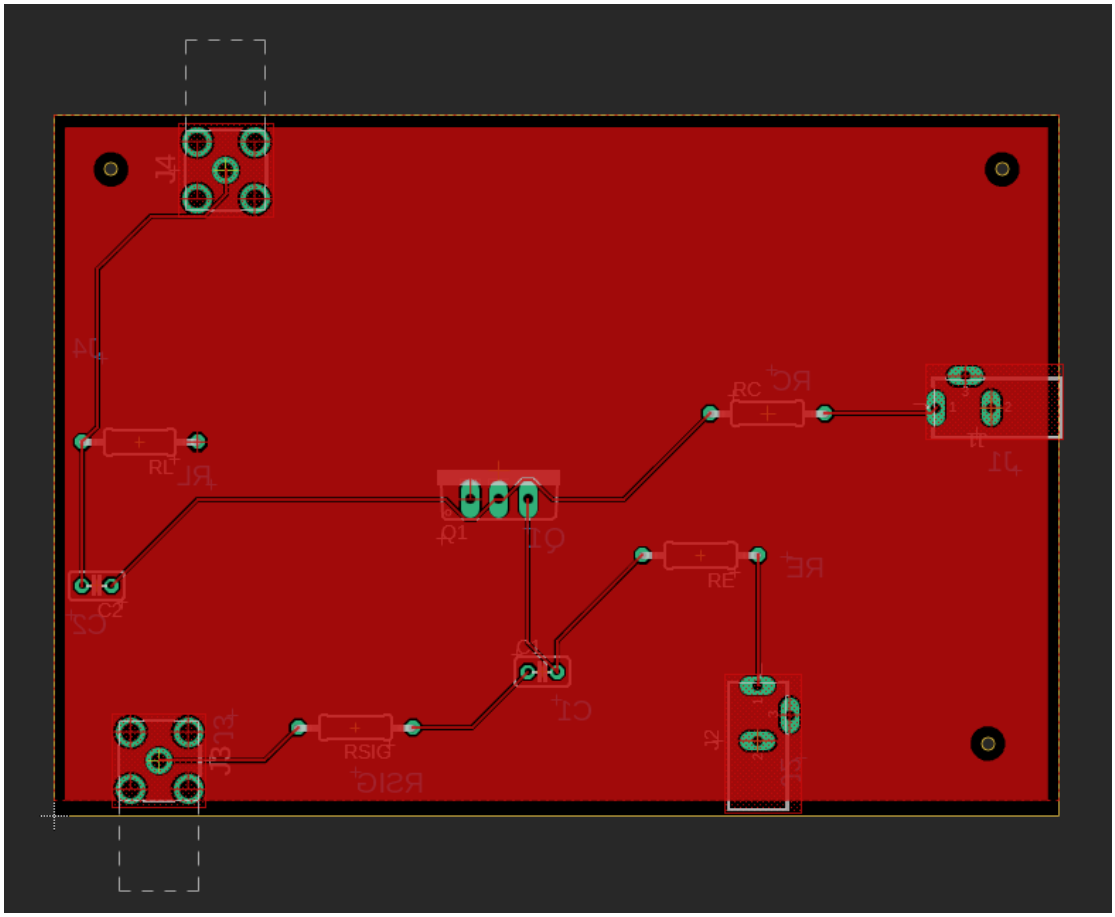
$$Gv = (Rin/(Rin + Rsig)) * gm(RC \parallel RL))$$

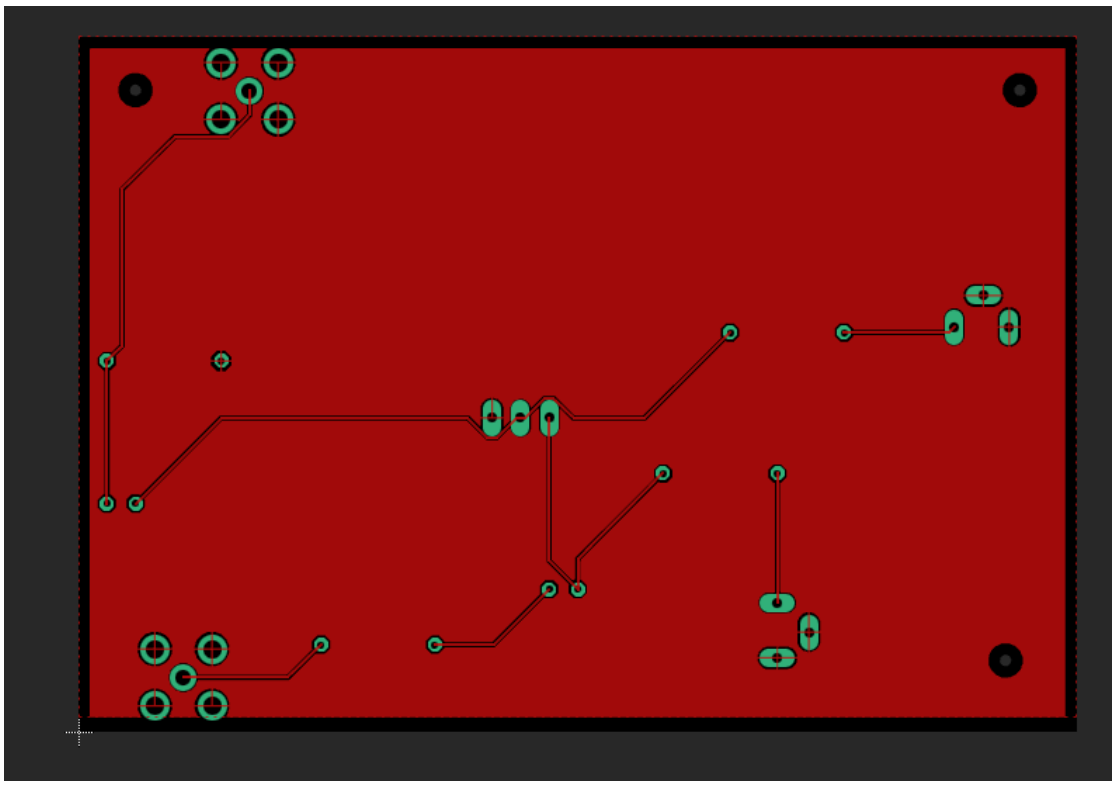
where $Rin = re \parallel RE$

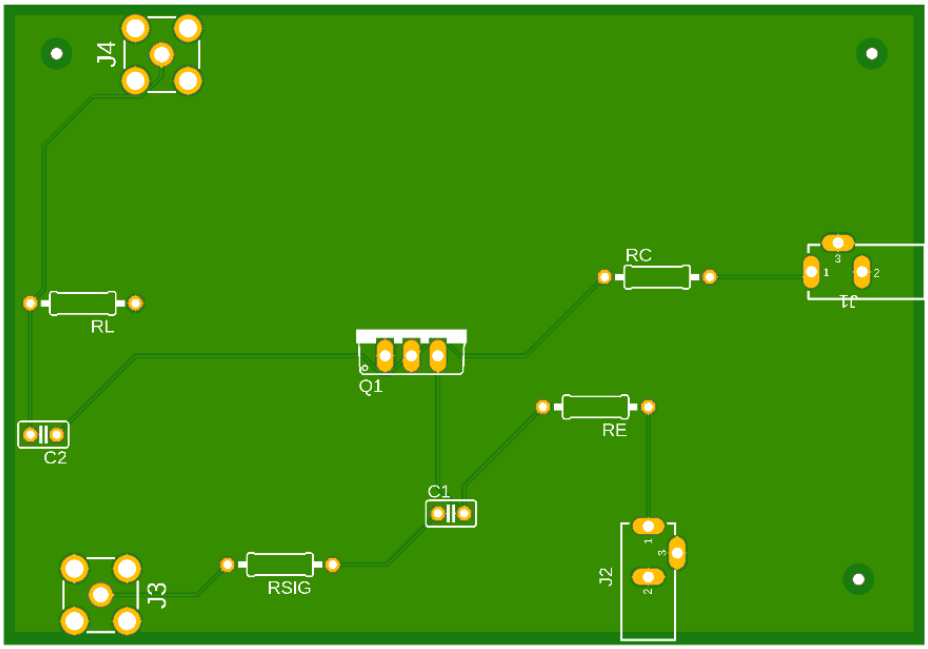
We selected circuit components from the Fusion library that are available in 3D format for a complete circuit presentation.

2. Electronic Design and PCB Images:



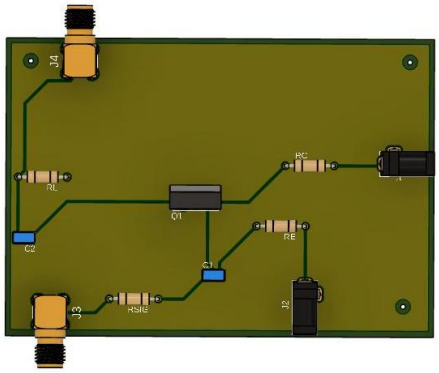

RL
RC
RE
RSIG
Q1
C1
C2

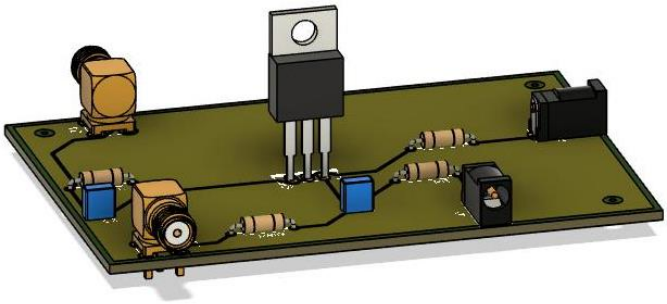




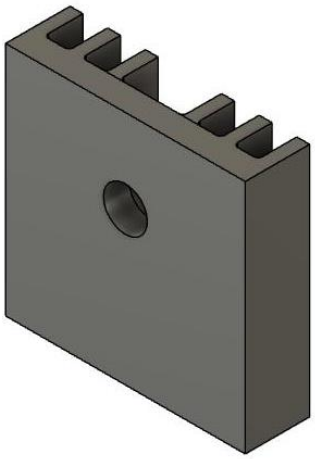
3. 3D PCB Image with the Heat Sink, Image of the Heat Sink with Dimensions, and Justification of the Heat Sink Design Approach Based on the Component Specifications:

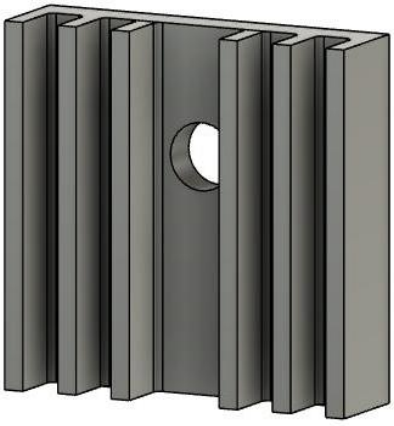
PCB:



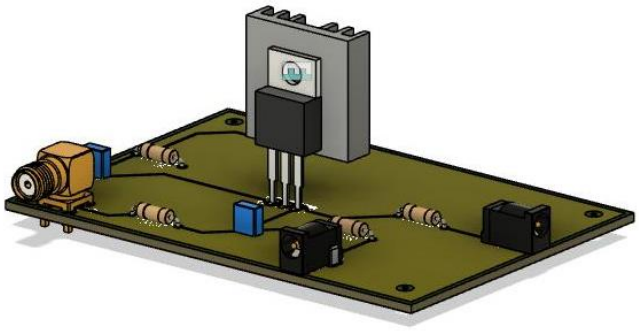


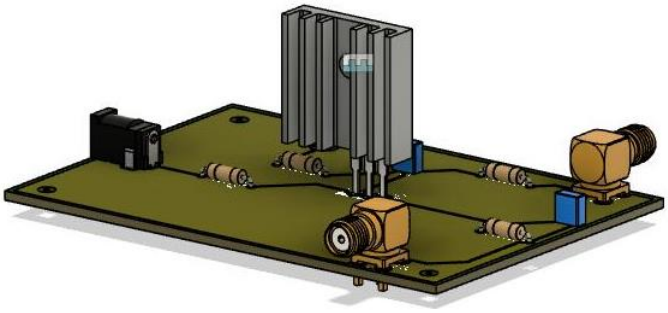
Heat Sink:





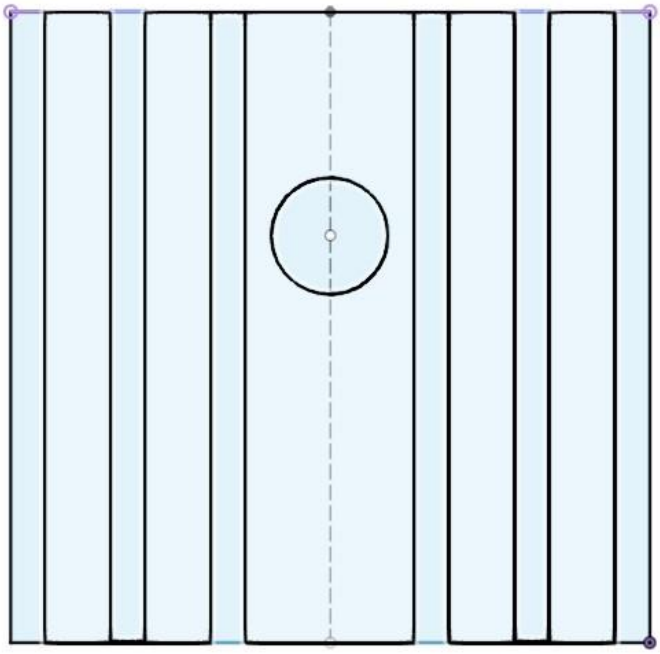
Both Together:





Heat Sink Dimensions:

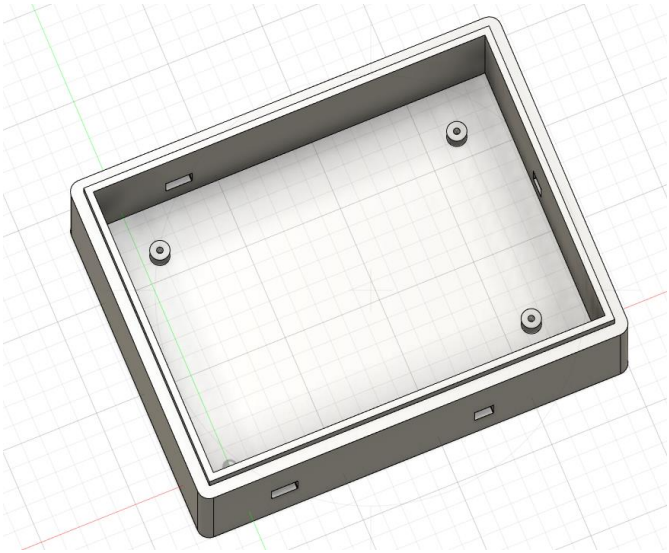
- Height: 22 mm, taller than the original since the width was increased, and thus the height was slightly increased as well.
- 3 fins on each side, compared to 2 on the original, to improve performance for our BJT.
- Width of each fin: 1.2 mm, the same as the original.
- Distance between fins: 2.3 mm, the same as the original.
- Radius of circle: 2.04 mm, the same as the original.
- Total width of the heat sink: $1.2*6+2.3*4+5.9=22.31.2 * 6 + 2.3 * 4 + 5.9 = 22.31.2*6+2.3*4+5.9=22.3$ mm.
- Length of the heat sink: 6.24 mm.
- Length of the fins from the base of the heat sink: 6 mm.



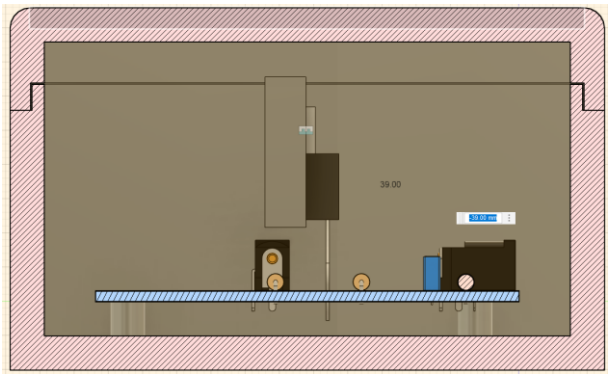
We designed the heat sink this way to maximize surface area, adding more slots on the left and right compared to the one presented to us, resulting in more efficient operation. Specifically, the heat sink transfers heat from the BJT transistor to the lower-temperature air that comes into contact with it.

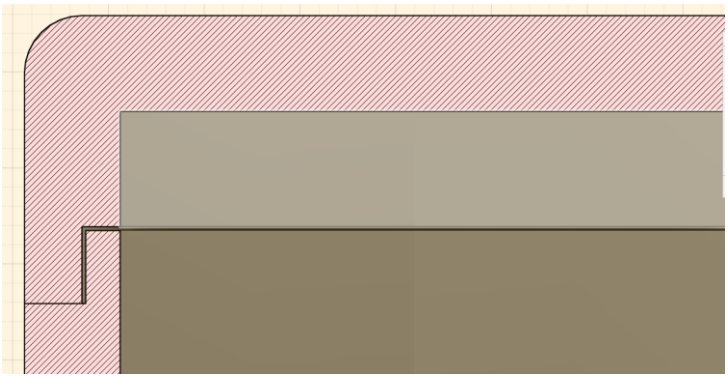
As for the PCB design, we ensured to leave enough space behind the BJT for easy placement of the heat sink on top of it.

4. Images Presenting the Enclosure and Its Characteristics:

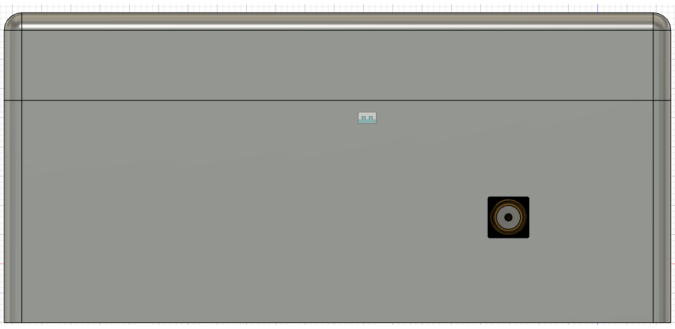


We created 3 holes at the base of the enclosure for mounting the PCB with screws.

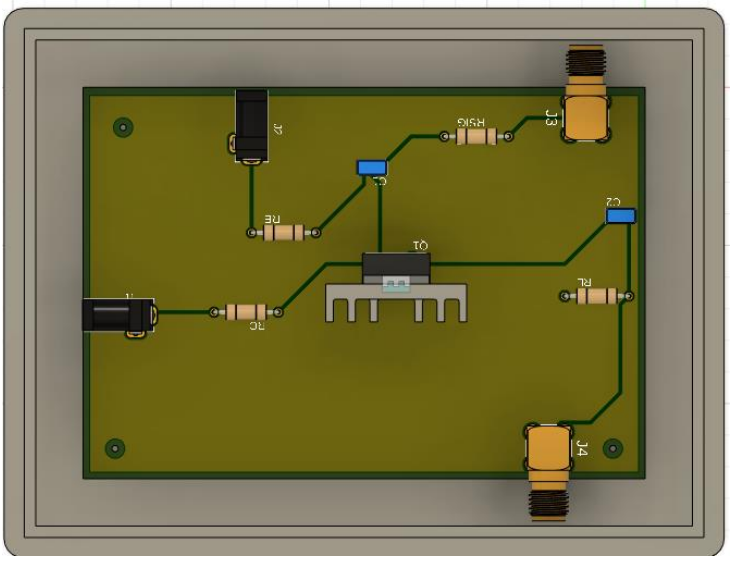


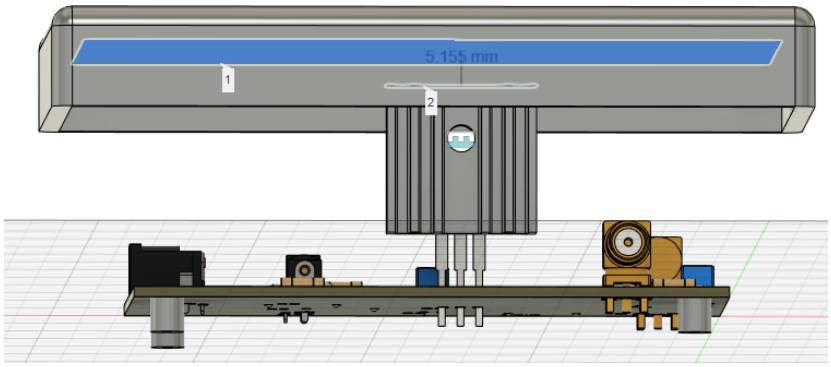


A section analysis shows that the walls of the base do not penetrate the walls of the cover, ensuring the cover of the enclosure can close without any issues.



We also see 4 holes for each jack connection in our circuit.





There are holes in the cover directly above the heat sink, allowing contact with the outside air. Additionally, our student ID numbers are engraved.

Overall Image:

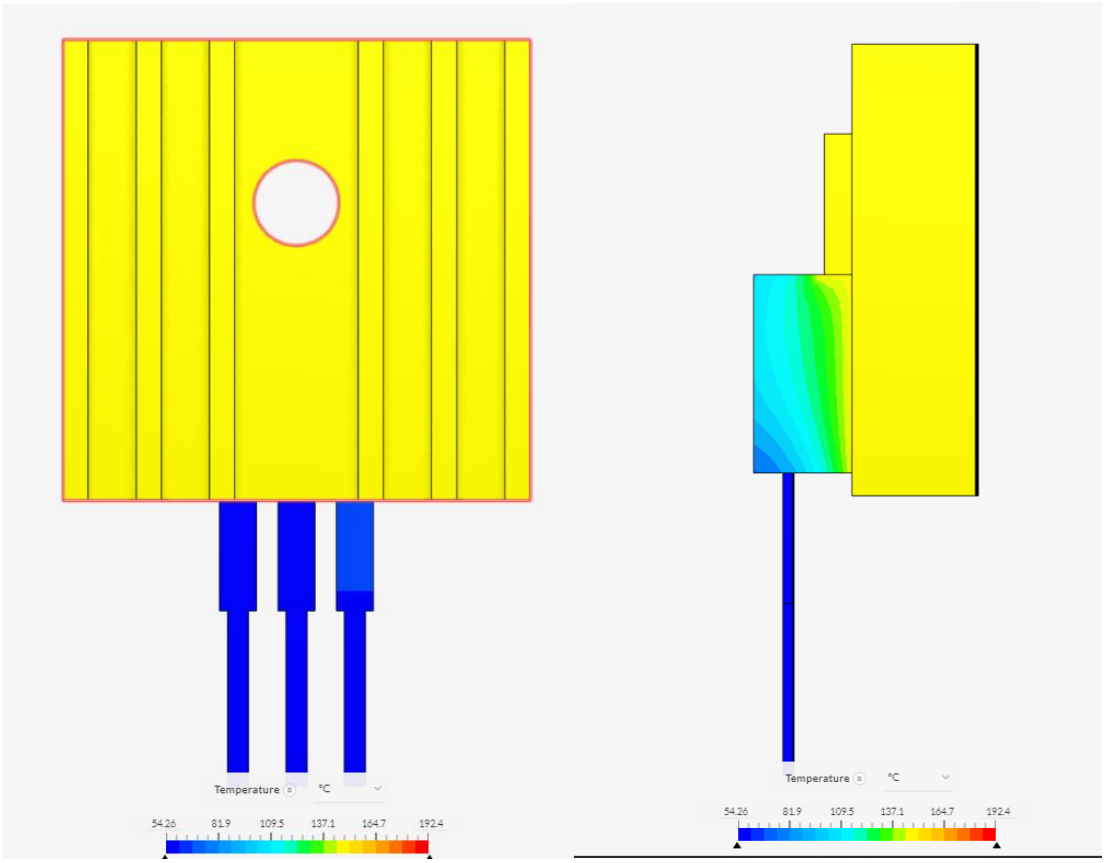
The height of the enclosure (from cover to the inner surface of the base) is 48 mm.

5. **Description of the Thermal Analysis of the PCB Under Free and Forced Convection, with Corresponding Images and Comments on the Effectiveness of the Heat Sink, Whether It Meets Its Purpose (Within Standard Operating Conditions of the Critical Component), and Comparison Between Free and Forced Convection:**

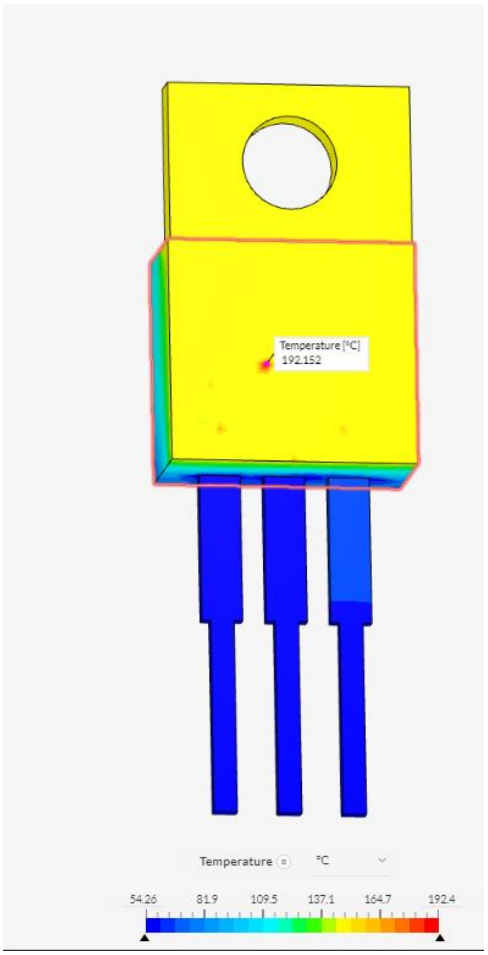
By applying the appropriate materials to the BJT and assuming a duty cycle of 90% while drawing a maximum current of 7.05 A at 1.3 V, the thermal power absorbed by the transistor is calculated as:
$Qth=0.9*7.05*1.3=8.2485$ W

Next, we divide by the surface area of the transistor in contact with the heat sink (102.98 mm^2). This gives the heat flux value:
Heat flux value=0.0801126432 W/mm^2

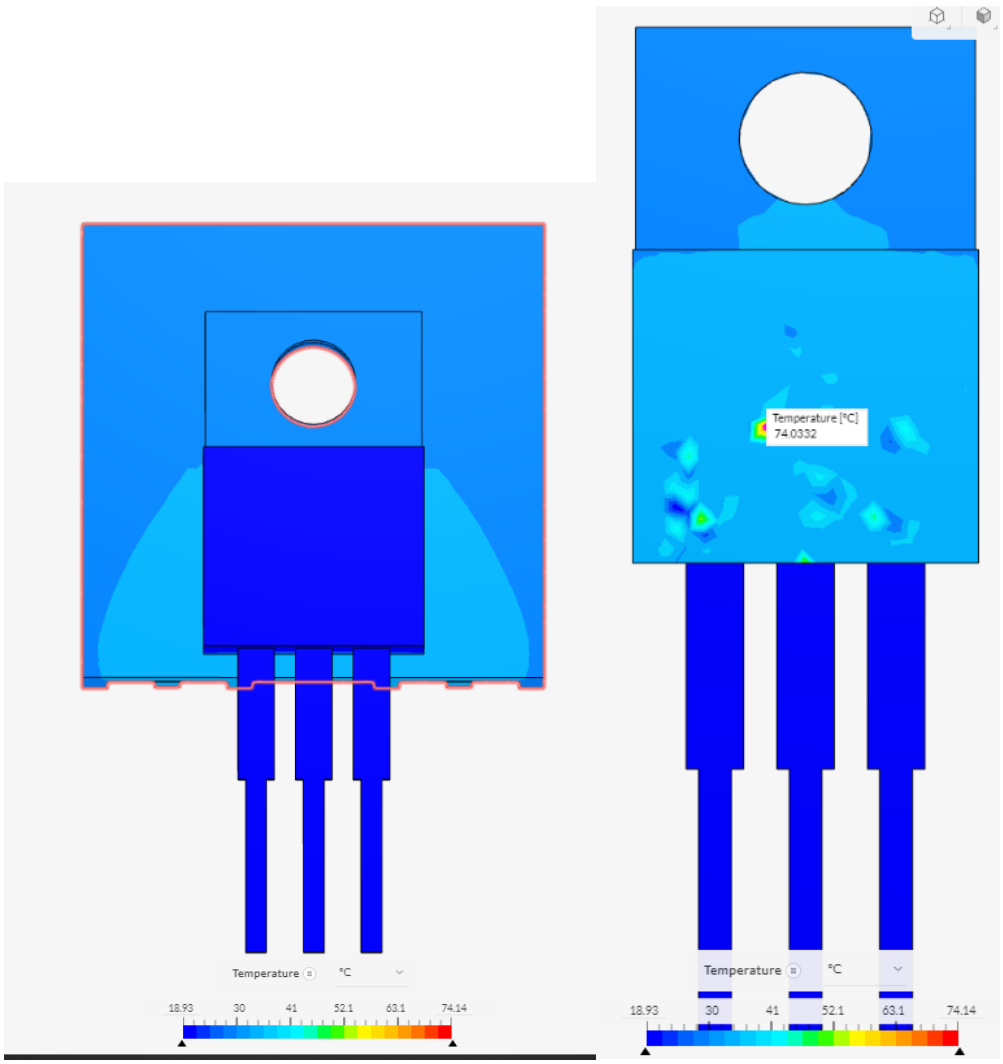
Thus, the result of our simulation for free convection is as follows:



In general, there doesn't seem to be any problem, as our transistor operates up to 150°C. Therefore, our heat sink is functioning adequately. However, by removing the heat sink, we notice some areas exceed this temperature.



For this reason, we also examined the case of forced convection. In this scenario, the temperatures are significantly lower, with a maximum temperature of 74°C.



Overall, as seen in our report, we did not observe significant deviations from the lab presentations by the instructors, as we followed the steps applied in the labs to the letter.