**Project Thistle Specification**

- RISC architecture, load/store

- 8-bit System on solder-less breadboard

- Uses 74LS TTL series or compatible logic

- Variable clock speed: 0.1Hz → 10Hz, either astable or monostable

- 256 Bytes of RAM – Hand programmable

- 2 general purpose 8-bit registers and one 8-bit null register

- An I/O register connected to 4 seven segment displays and a DIP switch, supports 2's complement

- An 8-bit ALU, supports 2's complement

**Instruction Set:**

**- LD** : 0000 + xxReg + Address **Registers:** A → 00

**- ST** :0001 + xxReg + Address B → 01

**- ADD** : 0010 + xxxx IO → 10

**- SUB** : 0011 + xxxx NR → 11

**- MOV** : 0100 + R1R2

**- IN** : 0101 + xxReg

**- CLR** : 0110 + xxReg

**- HLT** : 0111 + xxxx

**- JC** : 1000 + xxxx + Address

**- JNC** : 1001 + xxxx + Address

**- JMP** : 1010 + xxxx + Address

**- JR** : 1011 + xxReg

**- TWC** : 1100 + xxxx

**- NOP** : 1101 + xxxx

**Syntax:**

**Registers:** A,B,NR,IO

**Addresses:** 0 → 255

**- LD** Reg, Addr. → Stores value from address into selected register

**- ST** Reg, Addr. → Stores value from selected register into address

**- ADD →** Adds contents of A and B, puts result in A

**- SUB**  → Subs B from A, puts result in A

**- MOV** Reg1,Reg2 → Moves contents of register 1 to register 2

**- IN** Reg → Halts system until user writes to I/O register

**- CLR** Reg → Clears selected register

**- HLT** → Halts system

**- JC** Addr. → Jumps to address if the carry bit is set

**- JNC** Addr. → Jumps to address if the carry bit is not set

**- JMP**  Addr. → Jumps to address

**- JR** Reg → Jumps to address in selected register

**- TWC →** Toggles the 2's complement of the output display, default binary

**- NOP →**Null operation

**Block Diagram:**

