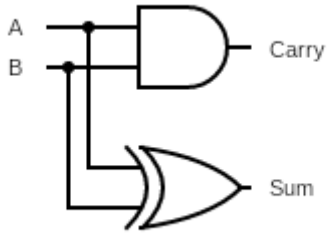
COA Assignment-1 Report

Group no. : 64
Names of group members :

1. 19CS10035 – Jatoth Charan sai
2. 19CS10063- Tirupati Suguna Bhaskar

1)

a) Half Adder



Half Adder Truth Table

Input: A, B

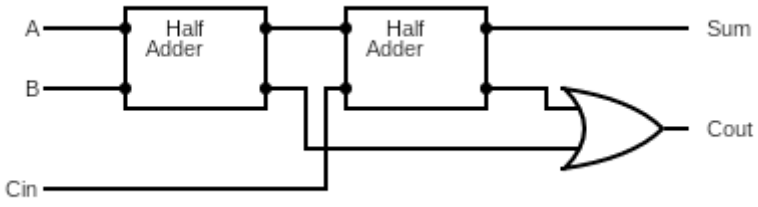
Output: Sum, Carry

A	B	Sum	Carry
1	1	0	1
1	0	1	0
0	1	1	0
0	0	0	0

b) Full Adder

Full Adder Truth Table

Input: a, b, c_0



Output: Sum , Cout

A	B	Cin	Sum	cout
1	1	1	1	1
1	0	1	0	1
0	1	1	0	1
0	0	1	1	0
1	1	0	0	1
1	0	0	1	0
0	1	0	1	0
0	0	0	0	0

c) Ripple Carry Adders

Longest delays:

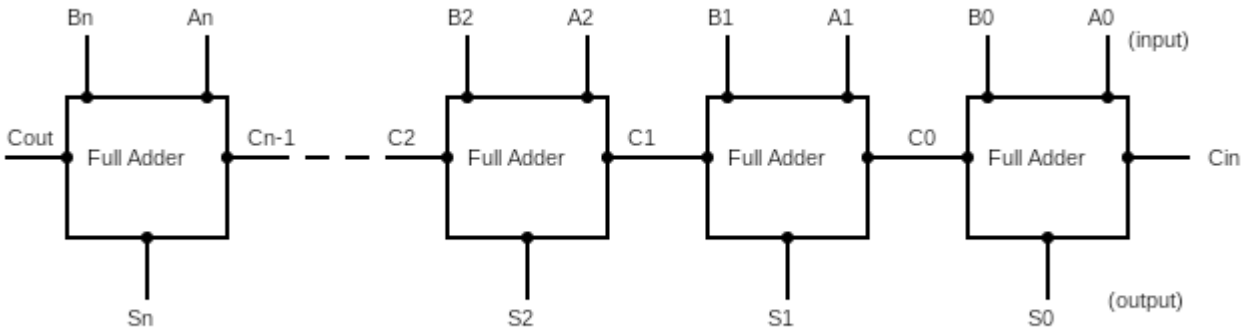
1. 4BitRCA : 5.565ns
2. 8BitRCA : 9.949ns
3. 16BitRCA : 18.717nsa
4. 32BitRCA : 36.253ns
5. 64BitRCA : 71.325ns

- By the above results it is sure that delay is directly proportional to the number of input bits and ripple's in the circuit.

d)

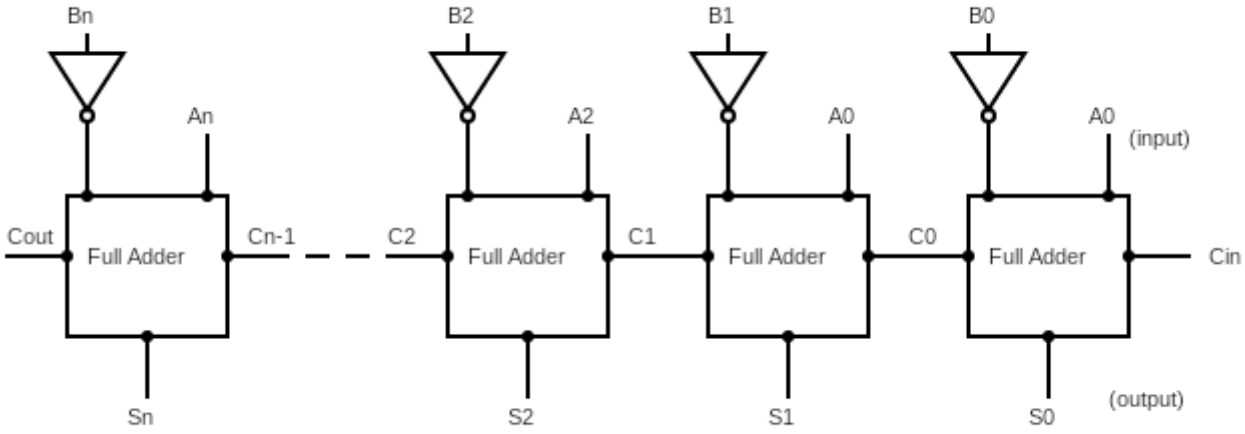
The above circuits Ripple carry adders are formed by cascading of full adders

By cascading n full adders we get n bit RCA



Which can also be used as subtracter by negating the every B bit and giving input

A-B = A+(-B) → A + (~B) as shown in below figure



2)

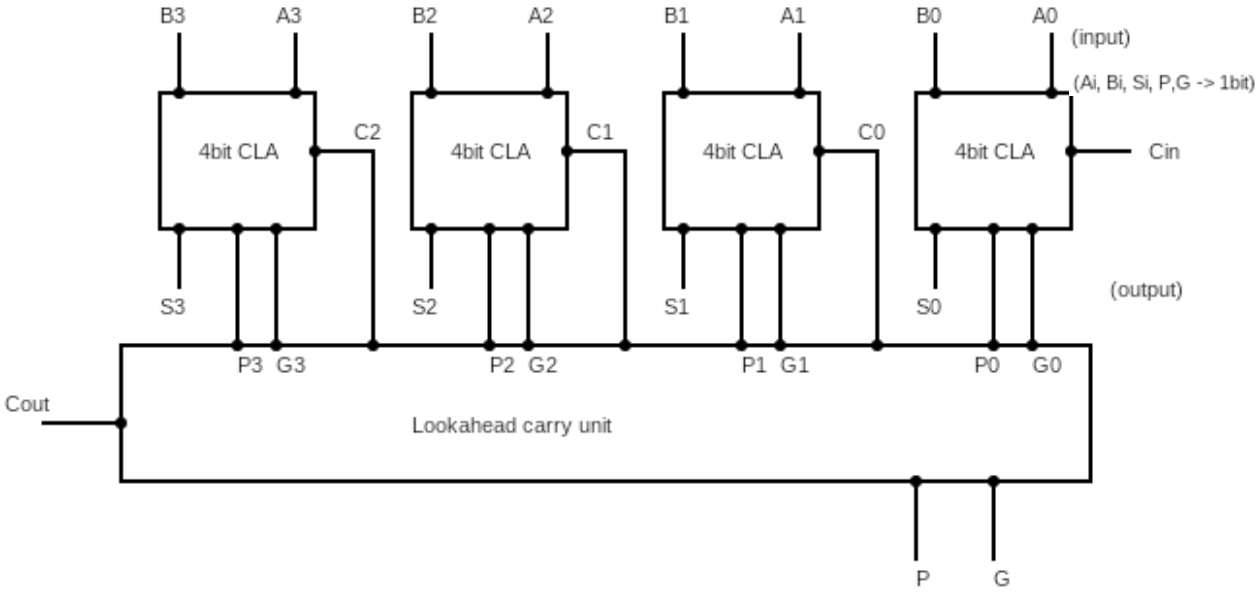
a) Carry Look Ahead Adder

Generate and Propagate Signals :

- G[i] = a[i] & b[i]
- P[i] = a[i] | b[i]

Input: a,b (n bits, a[i] indicate i^{th} bit of a)

Carry Bits: C[n]



1. C[0] = G[0] | (P[0]&Cin)

2. C[1] = G[1] | ((P[1]&G[0]) | (P[1]&P[0]&Cin))

3. C[2] = G[2] | ((P[2]&G[1]) | (P[2]&P[1]&G[0]) | (P[2]&P[1]&P[0]&Cin))

4. C[3] = G[3] | ((P[3]&G[2]) | (P[3]&P[2]&G[1]) | (P[3]&P[2]&P[1]&G[0]) | (P[3]&P[2]&P[1]&P[0]&Cin))

b) 4Bit RCA vs 4Bit CLA

Delay:

4Bit RCA: 5.565ns (Levels of Logic = 20)

(1.117ns logic, 4.448ns route) (20.1% logic, 79.9% route)

4Bit CLA: 2.423ns (Levels of Logic = 5)

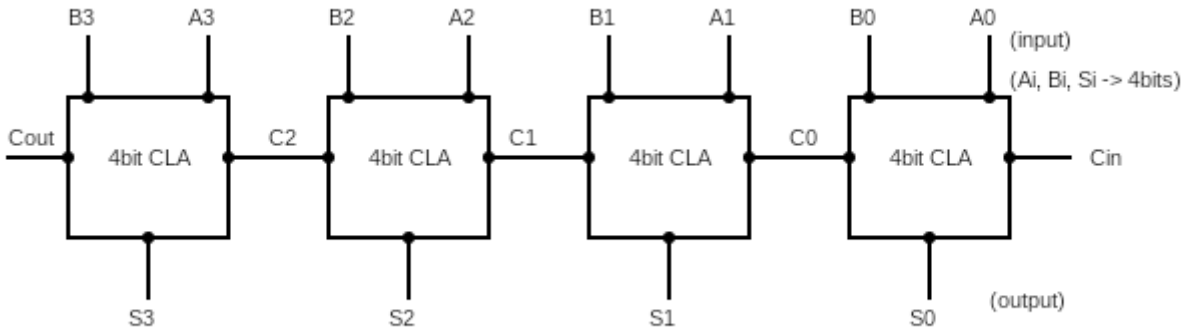
(0.373ns logic, 2.050ns route) (15.4% logic, 84.6% route)

→(Taken from synthesis reports generated by the Xilinx tool)←

- **CLA** is faster than **RCA**, as it has less levels of logic and no ripple carry delay
- Both are tested for correctness using same set of test cases, both resulted correct and same. (Test benches are include in Testing Folder)

c) 16Bit CLA (with Carry Lookahead unit) vs 16Bit CLA Ripple (without Carry lookahead unit)

16Bit CLA Ripple (without Carry Lookahead unit)



Delay:

16Bit CLA (with Carry Lookahead unit): 5.439ns

(Levels of Logic = 10) (0.745ns logic, 4.694ns route)

(13.7% logic, 86.3% route)

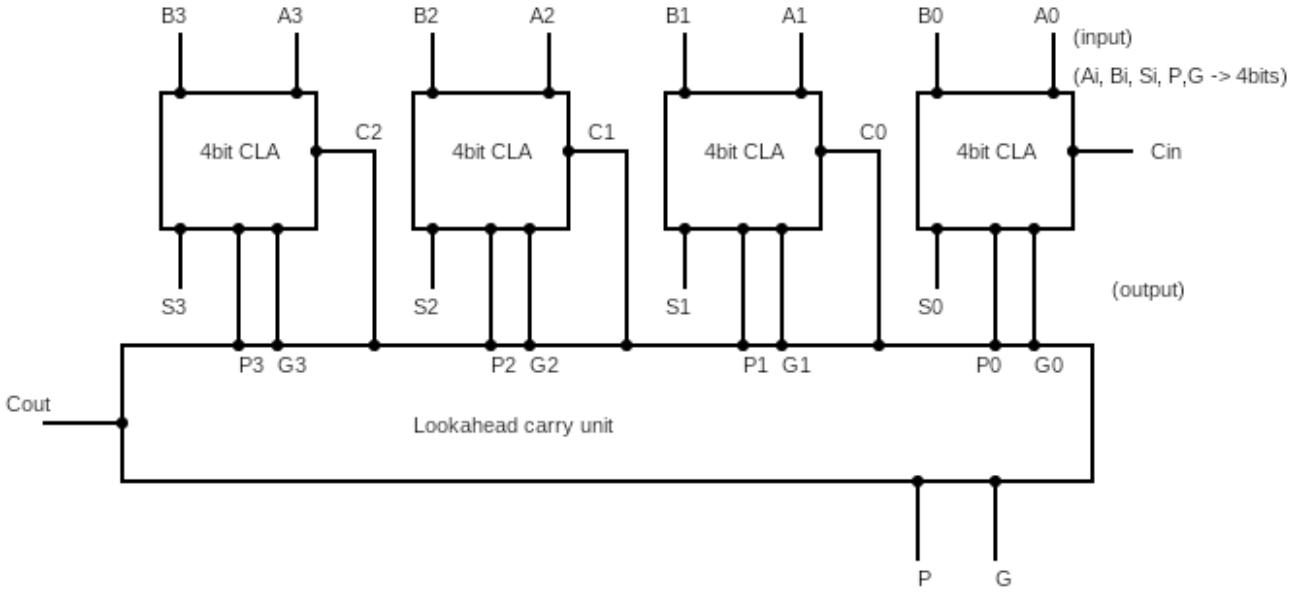
16Bit CLA Ripple (without Carry Lookahead unit): 5.882ns

(Levels of Logic = 13) (0.869ns logic, 5.013ns route)

(14.8% logic, 85.2% route)

CLA with Carry Lookahead unit is faster, as it has less levels of logic and no ripple carry between **4Bit CLA blocks** used in cascading

16Bit CLA vs 16Bit RCA



Delay:

16Bit CLA (with Carry Lookahead unit): 5.439ns

(Levels of Logic = 10) (0.745ns logic, 4.694ns route)

(13.7% logic, 86.3% route)

16Bit RCA: 18.717ns (Levels of Logic = 70)

(4.093ns logic, 14.624ns route) (21.9% logic, 78.1% route)

- **CLA** is faster than **RCA**, as it has less levels of logic and no ripple carry delay
- Both are tested for correctness using same set of test cases, both resulted correct and same. (Test benches are include in Testing Folder)

- No of Slice LUT's used
  - 16BitCLARipple : 36 out of 63400
  - 16BitCLA : 40 out of 63400
  - 16BitRCA : 80 out of 63400

Note:

Verilog file names:

HalfAdder.v → half adder circuit

FullAdder.v → Full adder circuit

CLA_adder.v → CLA 4bit adder circuit

CLA_4test.v → CLA 4bit test bench

CLA_16.v → CLA 16bit adder circuit

CLA_16test.v → CLA 16bit test bench

CLA_16C.v → CLA 16bit Ripple circuit

CLA_16Ctest.v → CLA 16bit ripple test bench

FullAdder_4.v → 4bit full adder circuit

FullAdder_8.v → 8bit full adder circuit

FullAdder_16.v → 16bit full adder circuit

FullAdder_32.v → 32bit full adder circuit

FullAdder_64.v → 64bit full adder circuit

FullAdder_64.v → 64bit full adder test bench.

RCA_4test.v → 4 bit full ripple carry adder test bench