

# Project – mini\_cpu

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디지털 논리회로

전기공학부

201920xx 한O윤 (팀장)

201920xx 전O태 (팀원)

교류학과

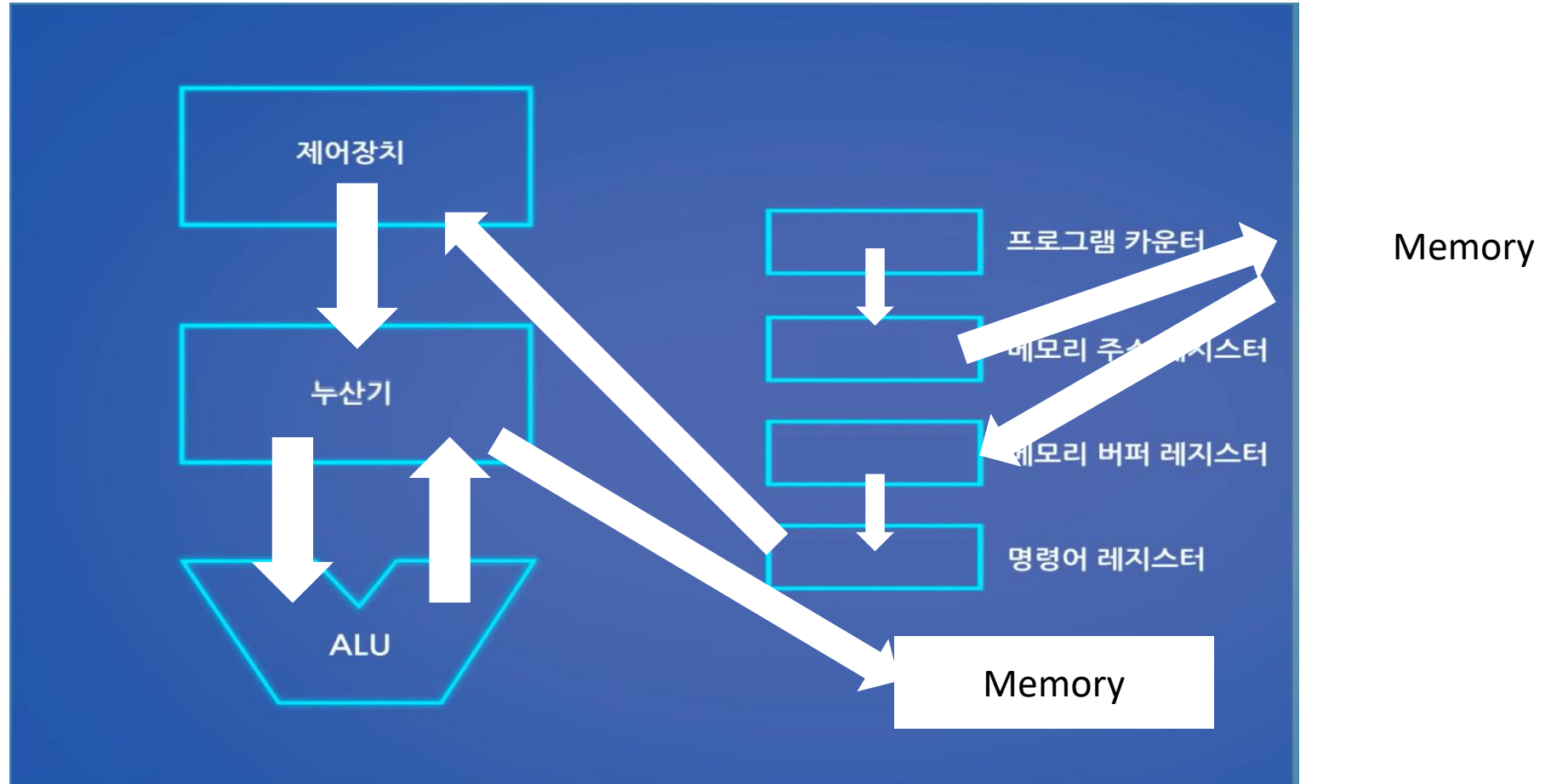
2024xxxx 한O현 (팀원)

# 프로젝트 목표

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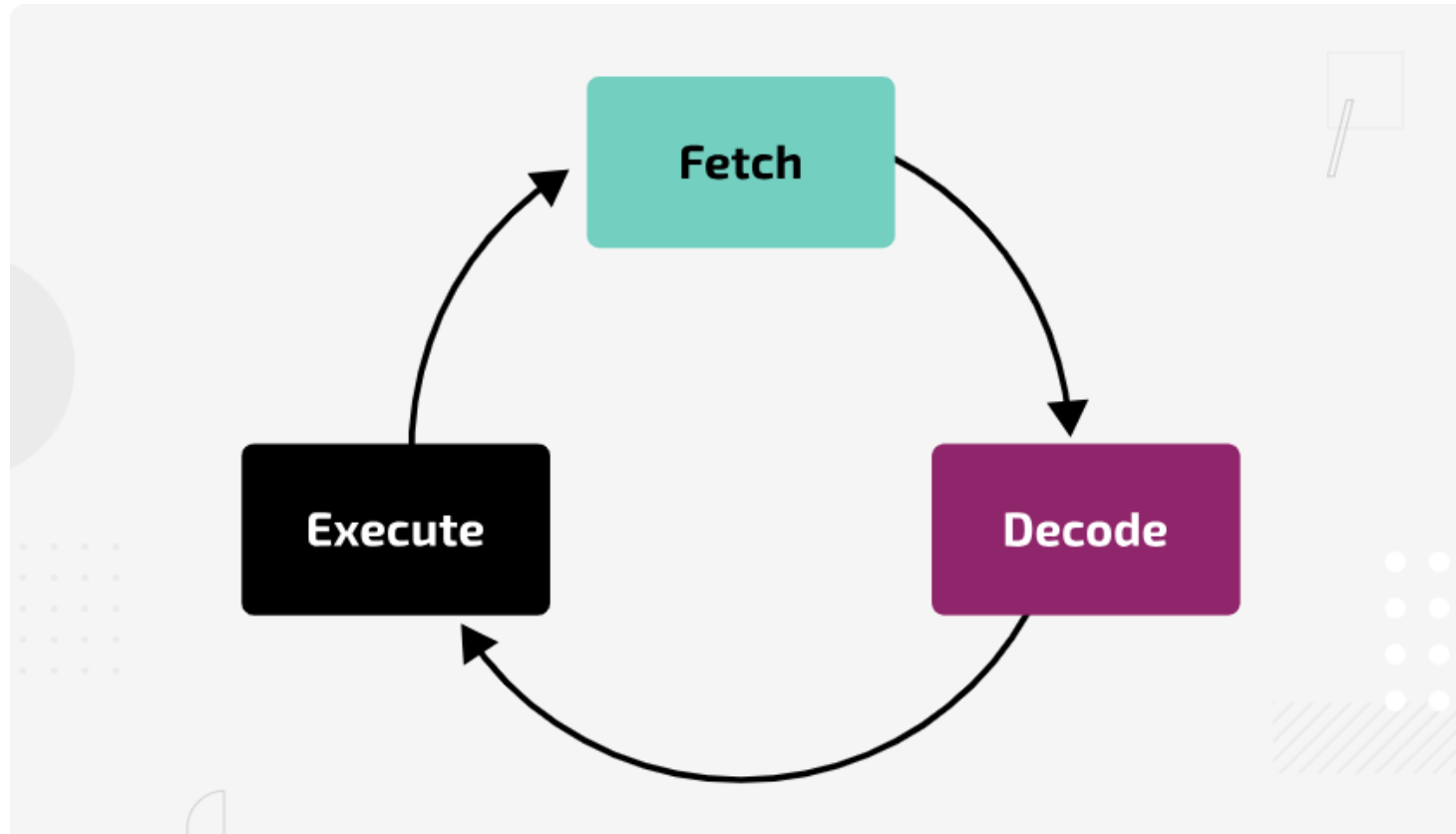
1. HDL(Hardware Description Language) 언어에 대한 이해를 높인다.
2. CPU의 동작 원리를 학습한다.
3. Verilog를 사용하여 간단한 ALU 동작을 구현하는 mini CPU를 설계한다.
4. Place&Route 과정을 통해 결과를 분석한다.

# CPU 동작 원리

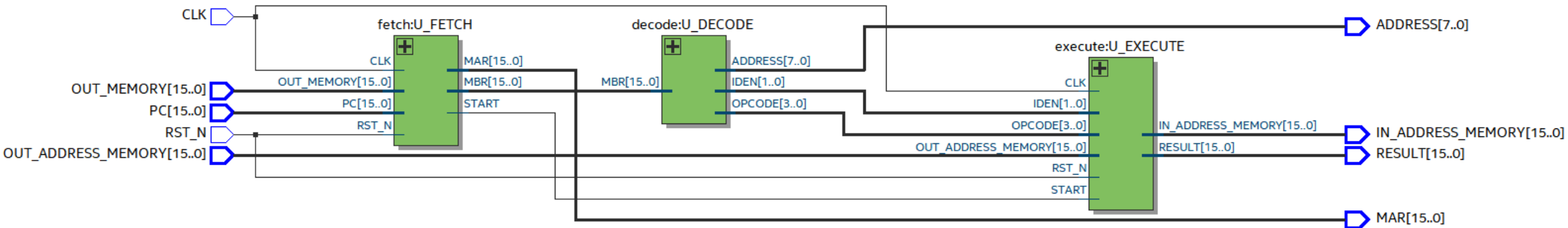


# CPU 동작 원리

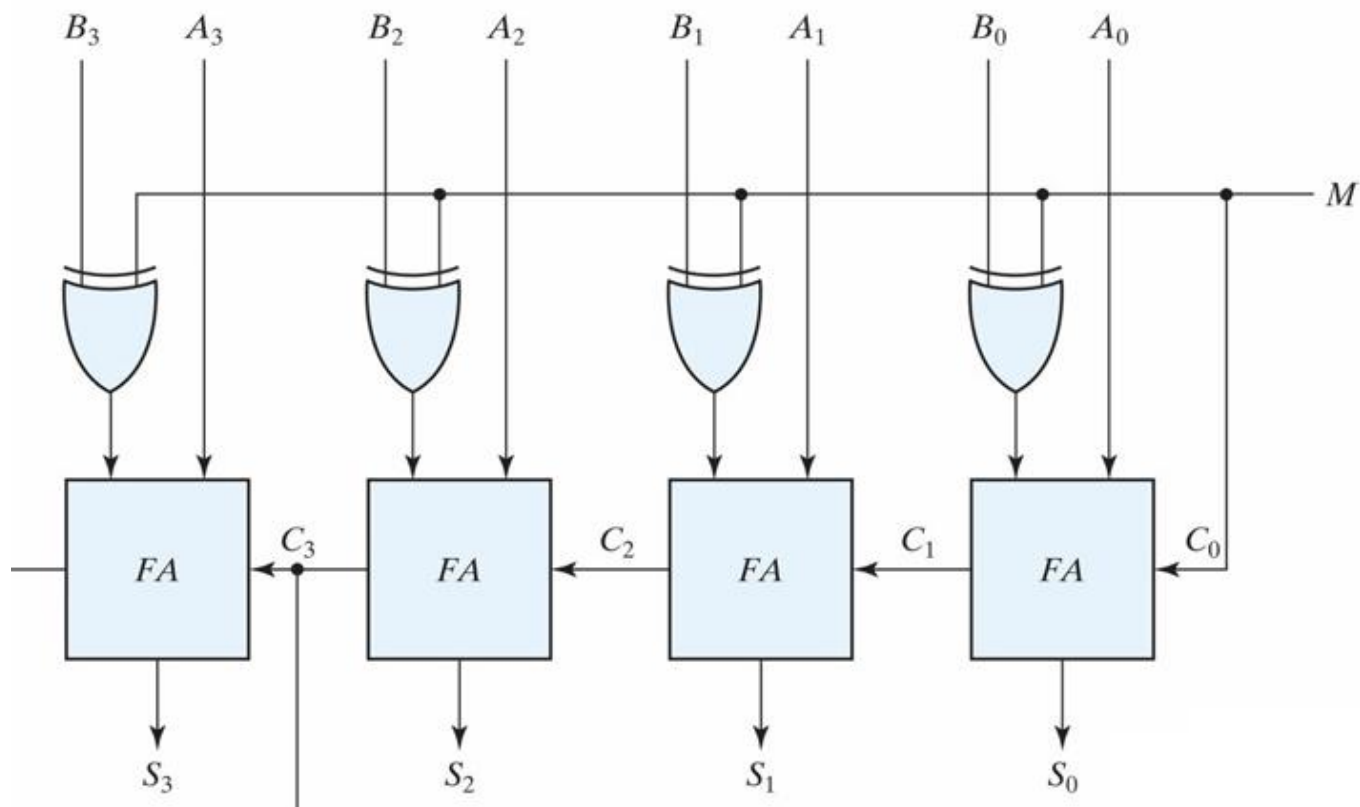
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# CPU RTL 회로도

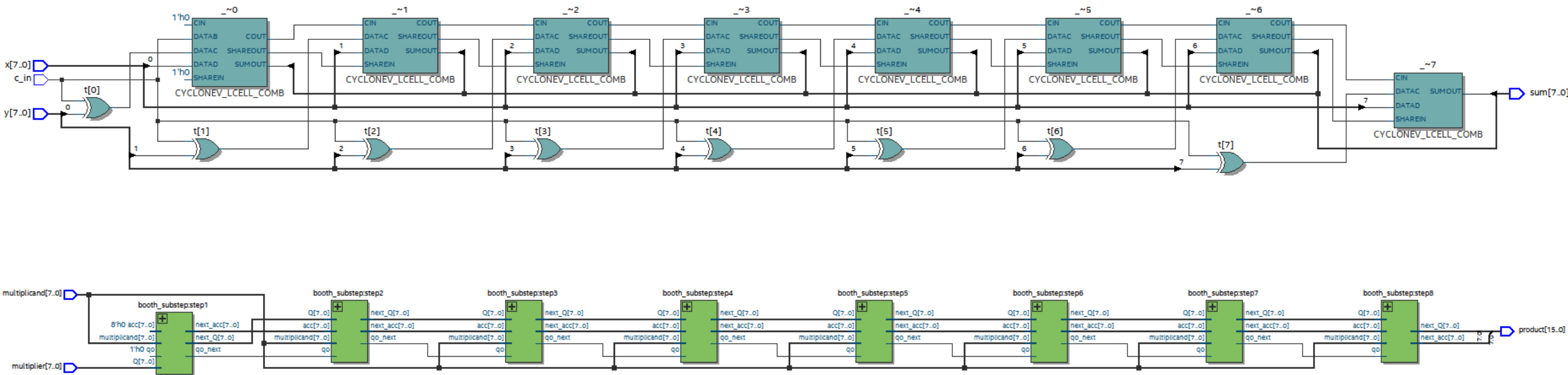


# ADD\_SUB



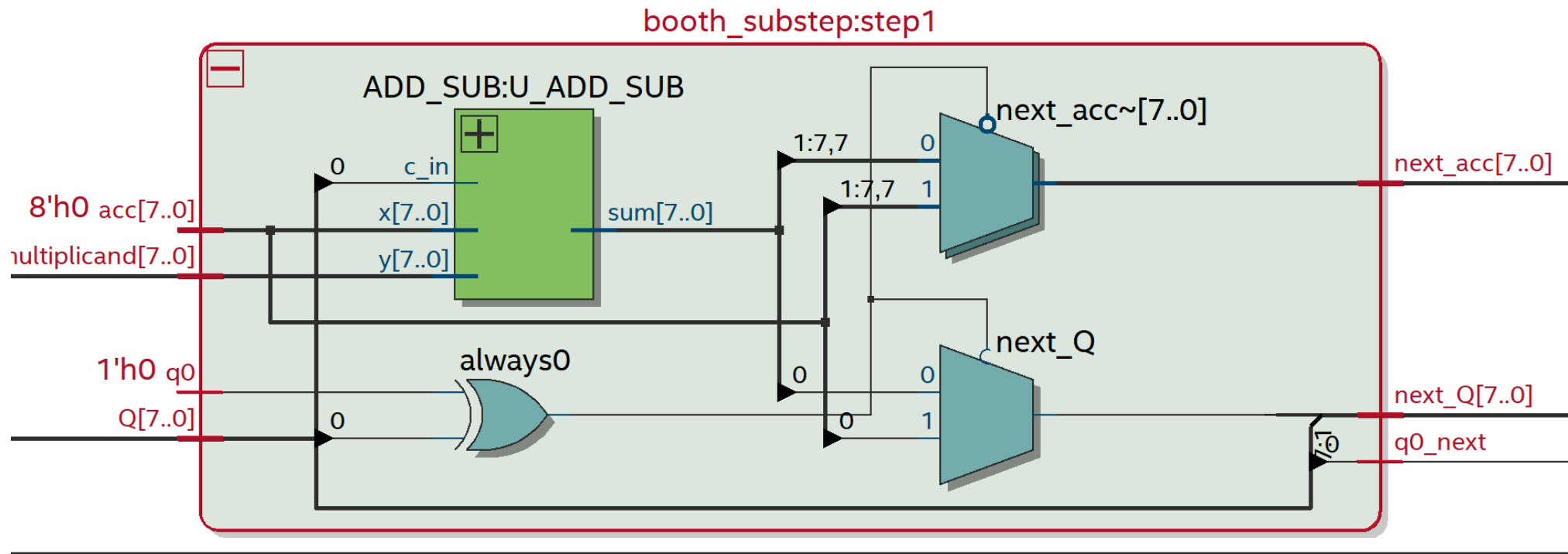
$$\begin{array}{rrrrrrrrrr}
 & & & & 0 & 0 & 1 & 1 & 0 & 6x \\
 & & & & 0 & 1 & 1 & 1 & 0 & 14 \\
 & & & & \hline
 & & & & +1 & 0 & 0 & -1 & 0 \\
 & & & & \hline
 & & & & 0 & 0 & 0 & 0 & 0 & \\
 1 & 1 & 1 & 1 & 1 & 0 & 1 & 0 & & (-6) \\
 & & 0 & 0 & 0 & 0 & 0 & & & \\
 & 0 & 0 & 0 & 0 & 0 & & & & \\
 0 & 0 & 1 & 1 & 0 & & & & & \\
 \hline
 0 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 0 & 84
 \end{array}$$

# ADD\_SUB/Booth\_MUL

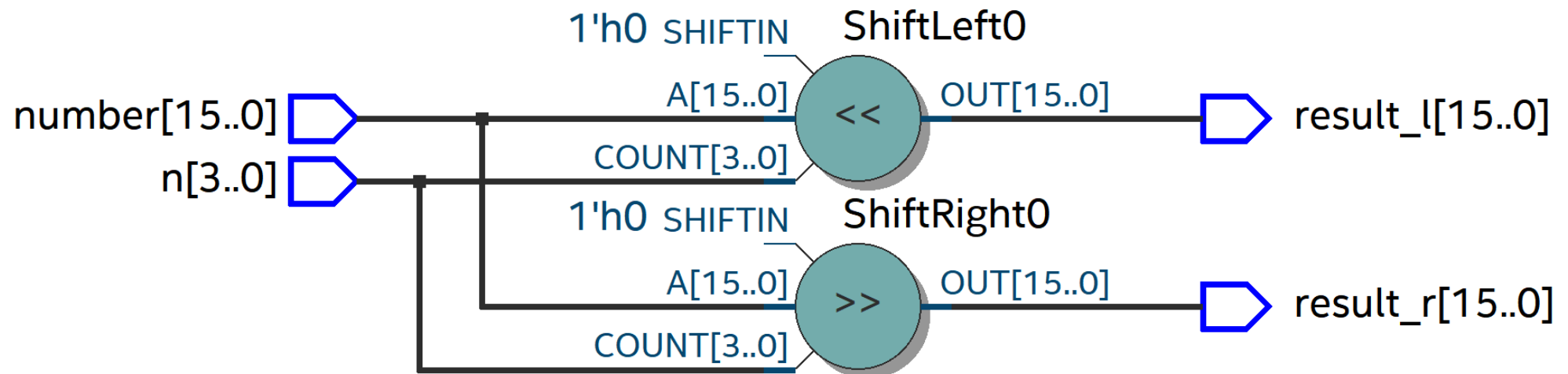




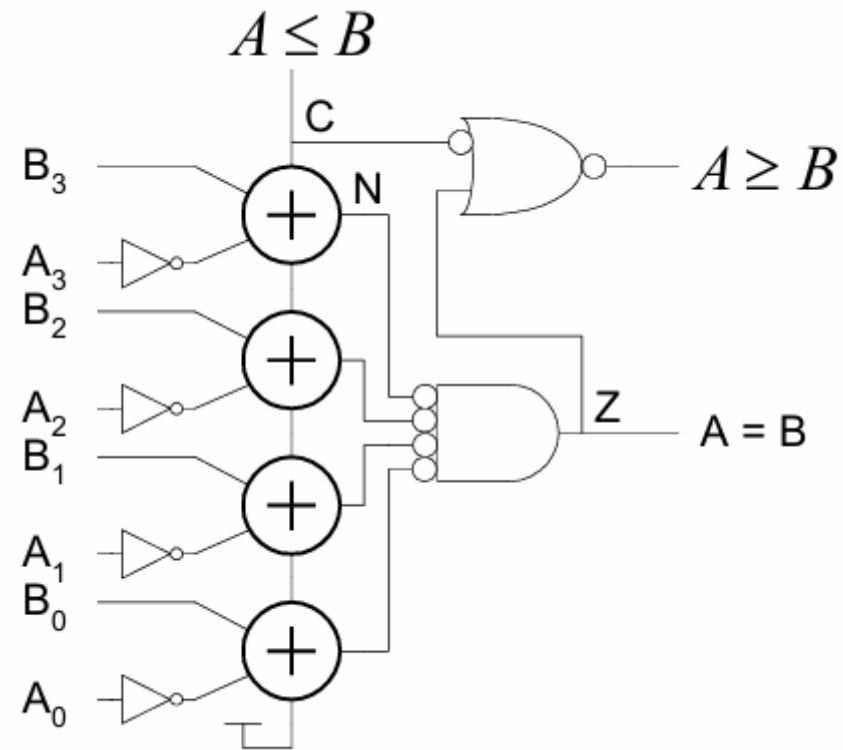
# Booth\_Sub



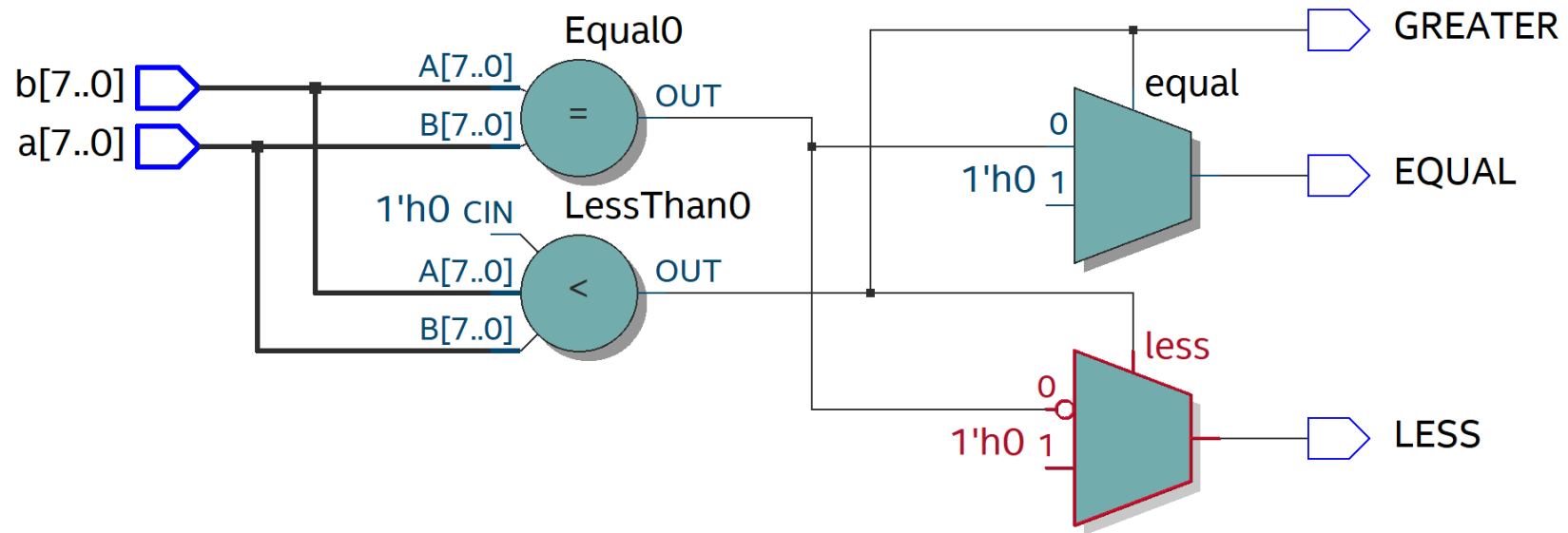
# Barrel\_Shifter



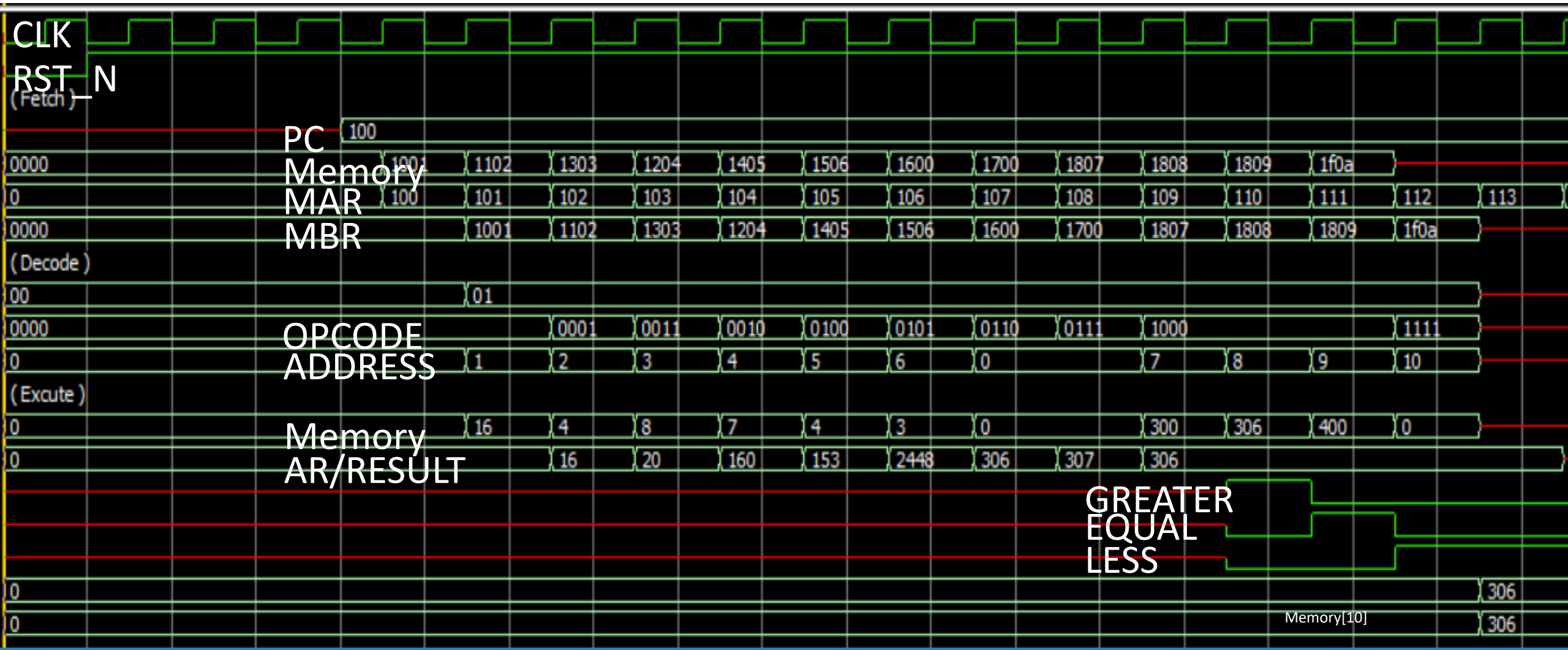
# Comparator



# Comparator



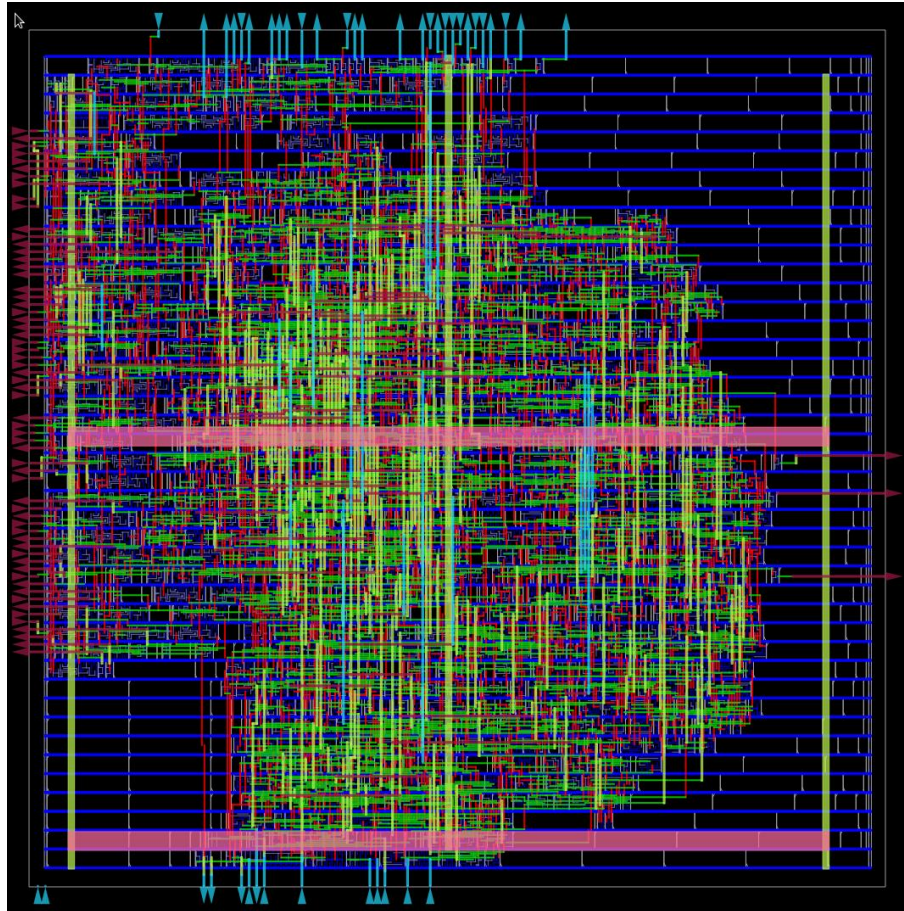
# 전체 Simulation



# Result & Assembly

```
// instruction
mem[100] = 16'b0001_ mov.b  mem[1],ar // ar = 16
mem[101] = 16'b0001_ add.b  mem[2],ar // ar = 16 + 4 = 20
mem[102] = 16'b0001_ mul.w  mem[3],ar // ar = 20 * 8 = 160
mem[103] = 16'b0001_ sub.w  mem[4],ar // ar = 160 - 7 = 153
mem[104] = 16'b0001_ shl.w  mem[5],ar // ar = 153 << 4 = 153 * 16 = 2448
mem[105] = 16'b0001_ shr.w  mem[6],ar // ar = 153 >> 3 = 153 / 8 = 306
mem[106] = 16'b0001_ inc.w  ar      // ar = 306 + 1 = 307
mem[107] = 16'b0001_ dec.w  ar      // ar = 307 - 1 = 306
mem[108] = 16'b0001_ cmp.w  mem[7],ar // great = 1
mem[109] = 16'b0001_ cmp.w  mem[8],ar // equal = 1
mem[110] = 16'b0001_ cmp.w  mem[9],ar // less = 1
mem[111] = 16'b0001_ mov.w  ar,mem[10] // mem[10] = 306
```

# Place & Route



```
=====
finish report_tns
```

```
-----
tns 0.00
```

```
=====
finish report_wns
```

```
-----
wns 0.00
```

```
=====
finish report_worst_slack
```

```
-----
worst slack INF
```

# Place & Route

```
=====
finish report_power
-----
```

Group	Internal Power	Switching Power	Leakage Power	Total Power (Watts)	
Sequential	3.09e-04	2.65e-04	7.43e-06	5.82e-04	3.4%
Combinational	8.69e-03	7.87e-03	4.32e-05	1.66e-02	96.6%
Clock	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.0%
Macro	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.0%
Pad	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.0%
Total	9.00e-03	8.13e-03	5.06e-05	1.72e-02	100.0%
■	52.4%	47.3%	0.3%		

```
=====
finish report_design_area
-----
```

Design area 2250 u^2 61% utilization.

[WARNING GUI-0076] QStandardPaths: XDG\_RUNTIME\_DIR not set, defaulting to '/tmp/runtime-root'

Elapsed time: 0:03.37[h:]min:sec. CPU time: user 1.98 sys 0.33 (68%). Peak memory: 195156KB.



# 역할 분담

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- 📖 한O윤 : 전반적인 CPU 설계 및 마무리, P & R 결과 분석.
- 📖 전O태 : 자료 조사 및 ALU 기초 설계, 테스트 벤치 실행, P & R 결과 분석.
- 📖 한O현 : 자료 조사 및 보고서 초안 작성.

# 참고문헌

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bRd 3D. "CPU는 어떻게 작동할까?" YouTube, 2021, <https://www.youtube.com/watch?v=Fg00LN30Ezg&t=777s>  
<https://github.com/The-OpenROAD-Project>