

Multiphysics-Informed ML-Assisted Chip Floorplanning for Heterogeneous Integration

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Abstract—The floorplan of chiplets in heterogeneously integrated systems-in-package (SiPs) must consider multiphysics (electrical, thermal, and mechanical) performance and meet positional constraints during optimization. This article sets forth an efficient framework for chiplet floorplanning subject to positional and multiphysics-performance-based constraints. Traditional multiphysics simulations, often impractical in optimization due to high computational cost, are replaced by a high-fidelity and efficient conditional image generative model via image-based machine learning (ML). This model is accurate and capable of performing real-time prediction of multiphysics performance throughout 3-D SiPs. Utilizing the image-based ML model for fast performance assessment, we further accelerate the physical design by developing a novel and highly parallelizable dynamic rank-revealing (RR) algorithm for solving the underlying constrained optimization problem. We leverage this algorithm to optimize the position of the chiplets subject to multiphysics performance directly without floorplan representation or convexification techniques while meeting a multitude of constraints. The same ML model and constraints are also integrated into a state-of-the-art corner block list (CBL) floorplan representation under a simulated annealing (SA) optimization framework. The accuracy and efficiency of the proposed optimization method are demonstrated in the floorplanning of chiplets on an interposer subject to thermal constraints, and by comparisons against ML-assisted SA-CBL for performing the same task.

Index Terms—Electrical performance, floorplanning, machine learning (ML), multiphysics, optimization, physical design, placement, system-in-package (SiP), thermal integrity.

I. INTRODUCTION

HETEROGENEOUS integration (HI) [1], [2] via advanced packaging is the assembly and packaging of individual components or chiplets, such as CPUs, GPUs,

can be separately manufactured using nodes and even different semiconductor materials (Si-Ge, InP, and SiC) onto a single substrate. This technology has tremendous potential to overcome the limitations of monolithic integration technology and effectively slow-down of Moore's law.

The physical design of a heterogeneous system-in-package (SiP) involves optimizing the shape of chiplets in the package, as each chiplet can be fabricated by different technology nodes and is subject to distinct physical requirements. Physical design is critical to the final system performance. In addition, the physical layout does not have design rule violations. Moreover, an effective physical design must consider multiphysics performance (electrical, thermal, and mechanical performance). Current package structure is 3-D, which increases the complexity of verifying physical constraints. In early work on chiplet floorplanning [3], [4], [5], [6], such a capability was well developed in prevailing physical design.

One must rely on fast predictive models to facilitate multiphysics performance to facilitate physical design iterations. However, the multiphysics performance of a 3-D SiP remains a challenge even with today's most efficient simulation tools. The underlying optimization problem is difficult as it is not only nonconvex and nonlinear but also a high-dimensional design space with a large number of constraints [7]. The nonconvexity arises from