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Linear programming-based multi-objective floorplanning optimization for system-on-chip

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Abstract

In the area of very large-scale integrated circuit design, optimizing floorplans for area, wirelength, and temperature poses a daunting challenge. This study introduces an innovative floorplanning approach that amalgamates the rectangular packing method with linear programming techniques to ensure optimal module placement in the core area. Leveraging linear programming, this model optimizes three vital layout floorplanning objectives namely area, wirelength, and temperature through an analytical cost function termed linear programming-based multi-objective floorplanning. To enhance the optimization process, adaptive weights are employed for each constraint, effectively preventing congestion and hotspots. To validate the efficacy of the proposed automated floorplanning approach, extensive simulations and synthesis were conducted on benchmark circuits sourced from the Microelectronic Centre of North Carolina and Gigascale Systems Research Center. Comparative analysis with existing solutions demonstrates a significant improvement of 13%, 12% in area, and wirelength, respectively. These outcomes underscore the superior performance and practicality of the proposed floorplanning methodology, showcasing its potential for widespread application in chip design.

Keywords Floorplanning (Fp) · Linear programming (LP) · Multi-objective optimization · Microelectronic Centre of North Carolina (MCNC) · Gigascale Systems Research Center (GSRC) benchmark · Cadence

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1 Introduction

Moore's law predicted the exponential increase in the density of diverse characteristic chip transistors has revolutionized manufacturing, where the area limitation on large chips is no longer complex. This in turn has burdened digital design, verification, validation, and implementation demanding effective Floorplanning (Fp) warranting area optimization and has become an active research area [1]. Particularly, the system's complexity escalated with additional advancements in the designing and manufacturing of microelectronic systems [1, 2]. The heightened design complexity was eased using the state-of-the-art (SoTA) high-level synthesis tools by mere code alteration associated with functional parameters dealing with large applications. Instead, the analysis and simulation tools overlook the complexity of the circuit, emphasizing the quick realization of simple and potential designs to address the design issues. In addition, manufacturing minuscule and compact feature sizes with larger chip dimensions allows a circuit to accommodate millions of transistors. However, the limitation on the circuit size and its external connections end in an unmanageable design.

Therefore, chip design requires the organization of components into modules that minimize the wastage of free space [1] by preserving its functionality. Although the direct realization of a large circuit consumes more space which is resolved by its decomposition into small sub-circuits that minimize the system area with complexity. Also, module splitting labeled as cut size (the number of net numbers cut off by the partition) is expected to be minimal and plays an important role in partitioning to resolve intricate combinatorial optimization issues. Moreover, wirelength minimization poses a serious challenge in physical design automation and results in hotspots when manufacturing large integration chips. Hence, it is crucial to focus on designs that are optimized in terms of partitioning and Fp [3]. Moreover, enhancements in space planning have a direct impact on circuit performance and clock frequency.

Likewise, routing remains another Fp issue related to the increase in metal layers, their thickness, newer design rules, and complexity [4]. Also, the increased congestion related to lower technology nodes burdens the designer in analyzing the possibility of routing adhering to timing constraints [5] prescribed by design rule check (DRC). Consequently area reduction with lower node technology, routing congestion increases on-chip variations. In such scenarios, it is desired to route the best topology with metal layers [3, 6]. Additionally, leakage current dominates VLSI design and demands power gating techniques to mitigate them. Specifically, resource management in ASICs is influenced by node shrinkage and other timing (setup, hold) requirements [7–14] that necessitate several evaluation methods. To fix these timing violations many commercial electronic design automation tools are available in the market, but no effort has been made to study the impact of power consumption on each technique. Also, the increasing demand for low-power applications requires the realization of new power reduction techniques [15, 16]. Finally, temperature plays a major role in making a trade-off between higher performance and lower power consumption.

As the heat dissipation in small areas increases, both the transition and skin temperature [17–19] results in a high barrier and degrades its reliability. This outlines the greater need for formal dynamic power and temperature analysis for predictive thermal management algorithms.

The above discussion outlines the numerous Fp constraints in ensuring effective area optimization with improved performance. Thus, this work delivers a novel LP-based multi-objective Fp (LPMOFP) for physical design automation aimed at system-on-chip (SoC) based on MCNC [20] and GSRC [21] Benchmark circuits. The paper is ordered as follows: Sect. 2 deals chronologically order the recent developments in the intended area with its shortcomings. Implementation of LPMOFP with various linear constraints to address Fp issues is discussed in Sect. 3, while Sect. 4 deals with its formulation meeting design requirements. The performance of LPMOFP is analyzed along with its complexity analyses in Sect. 5. Finally, the presented model is briefly summarized in Sect. 6 with an overview of future work.

2 Related works

Fp's major contribution is the optimal placement of modules in the limited core area which remains the important primal step in the physical design. Any issues or violations encountered in the latter stage insist the designer recommence from Fp sticking to guidelines. The highly prioritized modules in Fp are generally classified into hard (with fixed width (w) and height (h)) and soft (shapes are permitted to vary within the aspect ratio) modules. Also, the initial arrangement of modules in the circuit core area does not offer a unity aspect ratio which is one of the requirements in Fp. A few such contributions meeting the above Fp constraints are systematically listed hereunder with their pros and cons.

Several Fp strategies engaging nature-inspired optimization, namely evolutionary algorithms (EAs) [22], genetic algorithms (GAs) [23], evolution strategies (ES), [22], and evolutionary programming (EP), have performed well rather, their efficiency deteriorated with their search criteria getting trapped in the local minima. The sensitivity of these nature-inspired models to parameters such as crossover rate, mutation rate, and population size poses another obstacle. Finding optimal values for these parameters requires meticulous exploration, adding complexity to the optimization process. Consequently, a novel sequence pair coding with parallel particle swarm optimization (PPSO) is introduced in [1] for area optimization. Accordingly, to explore search space this algorithm utilizes a new greedy operation to find optimal solutions. The scheme trapped into local optimum when dealing with large-dimensional space and converged slowly. Similarly, another nature-inspired firefly optimization algorithm [24] is proposed for optimizing multiple objectives simultaneously. Herein, the model uses B^*tree-based representations for encoding and an improved movement strategy that incorporates crossover and mutation operators; however, its global search nature resulted in premature convergence. To avoid this slow convergence rate, another nature-inspired swarm intelligence-based metaheuristic algorithm named enhanced firefly optimization is introduced in [25]

to address floorplanning concerns and is termed MFP in this work, wherein the model mainly concentrates on minimizing the temperature across the layout, area, and wirelength in a fixed-outline constraint scenario utilizing a novel encoding scheme based on sequence pair representation and attains a competitive solution to these objectives by incorporating crossover and mutation operators that reduce the convergence rate.

Alternately, an adaptive hybrid memetic algorithm (AHMA) is proposed in [26] to solve the Fp problem, wherein GA and modified simulated annealing (SA) are used for global and local search, respectively, while balancing these two by death probability technique. However, their reliance on the static cost function failed to balance between multiple objectives simultaneously owing to the overly sophisticated crossover. As an improvement to [26], a new algorithm to solve the VLSI floorplanning problem for non-slicing VLSI floorplans for reducing area and wirelength, utilizing dual-population AHMA is proposed in [27], wherein B^*-tree representation is used to encode the floorplan with GA and SA as search algorithms and also introduced a dynamic and self-adjusting objective function to improve the performance. Similarly, the Fp in [28] combined GA with the C4.5 decision tree (DT) for optimizing area and wirelength. The algorithm makes use of binary tree representation for coding and a modified cost function to account for power dissipation in addition to other design parameters. Also, a hybrid optimization strategy using GA and SA for search criteria demanded numerous iterations for determining global optimal values and escalated the computational cost with delayed convergence.

Likewise, for VLSI floorplanning applications, mathematical programming stands as a cornerstone due to its capacity to offer a structured and rigorously defined approach to address the intricate challenges of chip layout optimization. Mathematical programming methods, such as linear and integer programming [29] and dynamic programming [30–32], allow for the formulation of floorplanning problems with well-defined objective functions and constraints, ensuring a systematic and theoretically grounded path to optimal or near-optimal solutions. These methods, though computationally intensive in certain cases, offer the advantage of providing guarantees in terms of optimality and feasibility. Moreover, they are adept at handling complex multi-objective problems and exhibit a certain degree of stability, rendering them particularly valuable in scenarios where precise adherence to design constraints and performance specifications is paramount. In contrast to nature-inspired evolutionary algorithms, mathematical programming in VLSI floorplanning provides an invaluable foundation of mathematical rigor, precision, and reliability for achieving optimal chip layouts.

Evolutionary algorithms in Fp were replaced with mixed modules [18] to render a thermal-aware fixed schematic for 3D IC energy consumption. The scheme assigned diverse energy modules to several layers for analytically capturing the Sub 3D thermal mask distributed across the diverse areas. Additionally, temperature across each layer was analyzed before refining the Through-Silicon Vias (TSV) positions. The modules' biased placement in a particular area ended in inefficient Fp. Recently, [6] employed a corner stitch data structure blended with an evolutionary algorithm for refining modules' placement. The Fp performed mobile expansion of module

ranges based on the design hierarchy before module placements to avoid local routing congestion. This Fp accounted for data flow limitations by constraining the modules to be placed in close locations. Experimental analysis revealed its superiority over the prevailing module position Fps while the method encountered placement issues when dealing with corners, corner input, and output pin routing congestion (Hotspot) which is highly essential in determining its efficacy. Fp [33] strategized network routing using diverse topologies meeting the timing and DRC requirements. The best network topology was identified from the available list based on different criteria to automatically route the specific metal layers. Also, it resolved the network time violations by offering different layout solutions.

Another routing-based Fp [34] evaluated RC delay to capture the pin-to-pin open length and short-length variations of each topology for selecting the optimal one based on numerous router constraints. The optimal routing topology was identified by evaluating the slack based on its polarity and the best timing. Also, timing issues influence Fp in minimizing core area which is witnessed in [35] that engaged Clock and Concurrent Data (CCD) [35] for module placement by considering CTS, and the routing phase for automatic placement and routing (APR) for area reduction. Therefore, revealing the scope for improvement in Fp design, if the timing constraints are considered in formulating the optimal cost function. Similarly, dynamic and static power reduction is another major factor influencing low-power IC design. This is addressed by modeling dynamic and static power equations of the diverse components to reduce their consumption. Dynamic power depends on switching and short-circuit power, while static accounts for the leakage and current flows through the transistor under no activity conditions. Addressing the same, [36] delivered an effective power consumption reduction technique using the C2MOS logic that dynamically evaluated the phase control using piped systems, although advanced the scheme caters only to the NAND, and NOR layout designs, thus, motivating the usage of low-power design techniques, namely clock gating, multi-voltage, level shifters, dynamic voltage and frequency scaling (DVFS), adaptive voltage and frequency scaling (AVFS), and customized low-power library cells. To counter these scenarios, a higher level of abstraction, learning, and awareness is desired that considers the performance of the core resources warranting efficient management.

Furthermore, timing issues setup, and hold time impact Fp and plays a major role in the system's performance. Therefore, [37] assessed the impact of individual optimization schemes across different flow stages in 100 industrial designs. Also, the ratio of Δ power/Δ setup time after global legalization and routing was measured by including the power added directly by setup time optimization. Also, indirect power consumption across the locations and global routing disturbance-induced power was significantly reduced by an average of 7.3%. The power-driven approach [15] further reduced the hold time power dissipation by an average of 7.2%. Moreover, the temperature is another major parameter influencing Fp that needs to be considered when modeling the optimization function. Dynamic temperature investigations of multi-input and multi-output multiprocessor systems under diverse rigorous conditions were done [38] to identify temperature convergence at a stationary point. These models offered Fp that managed the system temperature without affecting

their performance. These discussions clearly illustrate that to render an optimal Fp numerous multidimensional circuit parameters along with their constraints are to be considered in their objective function. Accordingly, an optimization model is presented in this manuscript deploying LP that ensures uniformity in addressing the numerous parameters participating in the optimization. Moreover, LP helps determine the best solution from a wider range of linear parameters or its requirements by exploiting its connectivity. Overall, this work aims to optimize the three design parameters in Fp and accordingly, the following research objectives are investigated in detail.

- Realization of individual cost functions related to area, wirelength, and temperature
- Formulation of unique constraint-based multi-objective optimization models for optimal Fp using linear programming
- Dynamic update of weighting factors concerned with multi-objectives
- Validation of the realized LPMOFP on MCNC and GSRC benchmark circuits.

3 Proposed methodology

Ongoing research in Fp has more widely concentrated on addressing either of the constraints. Accordingly, several contributions deployed bio-inspired algorithms that partially resolved the Fp issues by considering fewer constraints. Also, the recursive evaluation of fitness value does not guarantee the quality of the attained optimal solution and is time-consuming. Moreover, the local search converges at a premature stage by getting trapped in the local minimum, especially with complex problems and when dealing with higher-dimensional space. Hence, considering the aforesaid problems herein, an LP-based optimal Fp scheme is suggested that considers the numerous design constraints by considering the outer boundary and placement coordinates of the modules from the MCNC benchmark circuits. The scarcity in area-optimized automatic Fp methods has resulted in this work wherein, the optimization model is initially developed in Python. Subsequently, based on the attained optimal netlist, the chip is designed using Cadence EDA physical design tools. The representatives of the area, wirelength, and temperature along with their constraints are mathematically formulated using a linear programming [39] minimization model to realize the optimal Fp. Therefore, an LP model aiming at minimization of the cost function is developed and deployed for rendering optimal Fp, wherein the constant weights, present in the model are normalized and the unknowns are interpolated. Finally, Cadence Genus, Innovus, Tempus, and Voltus tools for synthesis, place and route, timing, and power calculation are utilized for model verification [4, 6, 7, 12, 33, 35, 37, 40].

The first initiative of using LP in Fp [41] failed miserably owing to the critical number of design restrictions. Therefore, this Fp considers the same along with LP boundary conditions in modeling the optimal area dimensions defined in Eqs. (1 and 2). These conditions were formulated based on the presumed reference width 'W_{ref}'

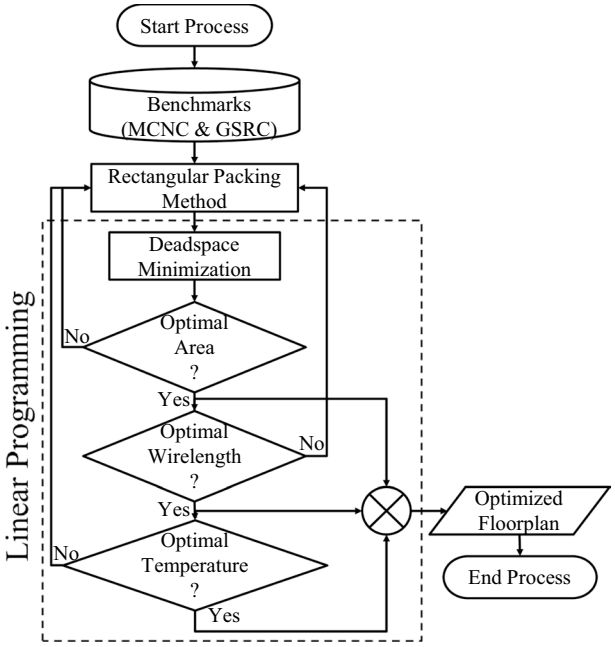

Fig. 1 Flow diagram of the proposed LP-based Fp

and height $'H_{\text{ref}}'$ available in benchmark circuits to yield the optimized width $'W_{\text{opt}}'$ and height $'H_{\text{opt}}'$.

$$W_{\text{opt}} = W_{\text{ref}} - X \tag{1}$$

$$H_{\text{opt}} = H_{\text{ref}} - Y \tag{2}$$

where A_{ref} defined as $W_{\text{ref}} * H_{\text{ref}}$ represents the reference layout area, X, and Y correspond to the change in width and height of reference dimensions and A_{opt} defined as $W_{\text{opt}} * H_{\text{opt}}$ represents the optimized layout circuit area. Figure 1 shows the outline of the intended LPMOFP by considering the constraints of deadspace, wirelength, and temperature.

Using the size of the circuit modules and the reference area from the benchmark circuits, Fig. 1 provides a high-level overview of the developed goal. Initially, the area of each Fp module is calculated in the LP formulation by multiplying its width w_i by its height h_i to represent the bounded area of the benchmark circuit. Later, the rectangular packing method (RPM) [42, 43] places the residual regions in a sequential, side-by-side manner, without any overlap, and rotates the module, if necessary, by 90°. Subsequently, area, wirelength (wl), and temperature associated with final die area reduction are optimized for preventing congestion and hotspots. Thereby, individual cost functions associated with these variables are defined and blended to eventually define the global optimality condition of the LPMOFP. Finally, the LP cost function is iterated by combining the three individually optimized costs

of area, temperature, and wirelength. The area goal, in particular, requires careful placement of all modules inside the core, a task that proves difficult for both manual and automatic Fps owing to the massive number of possible configurations.

To address this, the RPM is used that ensure random placements of circuit modules. RPM is mainly engaged to accommodate a greater number of modules inside the available core area. Also, the modeled cost function minimizes the deadspace in the first stage by bringing module placement together when dealing with benchmark circuits. This setup reduces the computational dimensions of the cost function associated with the area, which is then combined with the other objectives (wirelength, temperature) in the second phase for optimizing Fp iteratively until the objective is met else the procedure is repeated from RPM until the optimal is reached.

3.1 Deadspace

To begin with, area optimization generally requires the optimal placement of module cells during the design phase. This supplements the subsequent stages in the overall design cycle. Based on the constraints associated with module placement in the core area, a core utilization model along with the distance between them is presented in Eqs. (3) and (4).

$$\text{core utilization} = \frac{\text{Area of Modules} + \text{Area of wirelength}}{\text{Total Area of the chip}} \tag{3}$$

$$\text{Distance Between Modules} = \frac{\text{Number of Pins} * \text{Pitch}}{\text{Available Layers/Total Layers}} \tag{4}$$

By considering the entities associated with the modules, namelyw_i − ith module width; h_i− ith module height; a_i − area of the ith module; W, H− total width and height; A_{ref} − total layout reference area, the aspect ratio is defined in Eq. (5).

$$\text{Aspect Ratio} = H/W \tag{5}$$

$$\sum_{i=1}^{n} a_i = \text{Sum of all modules area}$$

Likewise, deadspace defining the left-out space upon placing all the modules in the core area is given in Eq. (6).

$$\text{Total Deadspace}\left(D_{\text{total}}\%\right) = \frac{\text{Total Floorplan Area} - \text{Sum of all modules area} - \text{Wirelength}}{\text{Total Floorplan Area}} \text{X100}$$

$$D_{\text{total}}\% = \frac{A_{ref} - \sum_{i=1}^{n} a_i - WL}{A_{ref}} X100 \tag{6}$$

Also, the wirelength (WL) is given in Eq. (7).

$$WL = \sum_{i=1}^{n} wl_i \tag{7}$$

$$wl_i - \text{wirelength of } ith \text{ module}$$

Half perimeter wirelength (HPWL) represents the sum of the difference between the maximum and minimum distances along the x, y directions of the layout is presented in Eq. (8).

$$\text{Half perimeter wirelength} = \min_{x_i, x_j, y_i, y_j} \left(\left| x_i - x_j \right| + \left| y_i - y_j \right| \right) \tag{8}$$

3.2 Temperature

Finally, the third design parameter temperature is determined and optimized to avoid the hotspots across the modules in a circuit, by evenly distributing the temperature and addressing its interdependencies with area, and wirelength. In general, the temperature of the floorplan depends on the power consumed by each block and its impact on adjacent blocks. Accordingly, the temperature is defined in general form as in Eq. (9)

$$T = R \times P \tag{9}$$

With T being a matrix with order $1 \times n$, with each element representing the temperature of the individual module based on R and P. Likewise, R is the thermal resistance exerted between the modules and is of the order $n \times n$. Similarly, P is power consumed by the individual blocks in the order same as T. Finally, to have an optimal temperature that is evenly distributed across the layout without affecting the area and wirelength optimization, the temperature is estimated utilizing Eq. (10) adopted from [32]

$$\mathrm{T_c} = \frac{1}{\mathrm{n}} \sum_{\mathrm{i=1}}^{\mathrm{n}} \frac{\mathrm{T_{max}} - \mathrm{T_i}}{\mathrm{T_{max}} - \mathrm{T_{Avg}}} \tag{10}$$

The above-discussed mathematical models representing the diverse Fp constraints are covered in the formulated LPMOFP and are discussed in the below sections.

4 Linear programming-based multi-objective floorplanning (LPMOFP)

From a technical point of view, there are four additional requirements for an LP Problem:

1. It assumes that the objective function and its associated constraints are well-defined and stable during the investigation.

2. Secondly, there is proportionality in the objective and constraints.
3. The third technical assumption refers to the addition of individual activities.
4. Finally, the divisibility assumption renders solutions that exist as integers as they can be divisible and assume any decimal value.

Based on the above assumptions, the LP Problem [44] is formulated. The LP optimization (maximizes or minimizes) represents a linear function subject to a finite collection of linear constraints as represented in Eq. (10).

$$CF(LP) = \min \sum_{i=1}^{n} C_i Y_i \; s.t. \sum_{i=1}^{n} a_i \leq A_{ref}; \sum_{i=1}^{n} wl_i \leq wl_c; \sum_{i=1}^{n} T_i \leq T_c; a_i, wl_i, T_i \geq 0 \quad (11)$$

C_i – Constant weights $\alpha, \beta,$ and γ, Y_i – Parameters deadspace, wirelength, and temperature;

A_{ref} – Reference Area; wl_c – chip wire lengthand T_c – chip temperature

Accordingly, all parameters that are to be optimized along with their adaptive weights are considered in the formulated cost function and presented in Eq. (12).

$$CF(LP) = y = \alpha * \text{area} + \beta * \text{wirelength} + \gamma * \text{Temperature} \quad (12)$$

Notations $\alpha, \beta, and \gamma$ represent constant weights ranging from 0 to 1 associated with the aforesaid parameters. The optimization function encompassing the diverse modules with their related weights is presented in matrix form in Eq. (13).

$$CF \Rightarrow y = M * P \quad (13)$$

where M is the matrix of order $n \times 3$ and Parameter $P = \alpha, \beta,$ andγ of order 3×1

Using the principle of least squares, the weight updates in P are predicted as $\widehat{P}$ defined in Eqs. (14)

$$\widehat{P} = (\widehat{\alpha}, \widehat{\beta}, \widehat{\gamma})^T \quad (14)$$

To determine $\widehat{\mathrm{P}}$, the suggested model engaged the linear cost function S(P) based on the principle of least squares and is presented in Eq. (15)

$$\mathrm{S(P)} = \|\mathrm{y} - \mathrm{MP}\|^2 = (\mathrm{y} - \mathrm{MP})^{\mathrm{T}}(\mathrm{y} - \mathrm{MP}) \quad (15)$$

$$S(P) = y^T y - y^T MP - P^T M^T y + P^T M^T MP$$

$$S(P) = y^T y - 2P^T M^T y + P^T M^T MP$$

S(P) measures the discrepancy between the desired floorplan layout (y) and the predicted (MP) that needs to be minimized. M denotes the design matrix encapsulating the relationships between the design parameters and floorplan layout. These design parameters include variables related to module placement, wirelength, and other Fp aspects. Herein, $S(P)$ is a real, convex, and differentiable function so

that the minima will always exist. Also, the optimal weights are attained/predicted when $S(P)$ is at minimum (i.e., at $\frac{\partial S(P)}{\partial P} = 0$).

$$\frac{\partial S(P)}{\partial P} = \frac{\partial (y^T y - y^T MP - P^T M^T y + P^T M^T MP)}{\partial P} = -2M^T y + 2M^T MP$$

Hence

$$2M^T MP - 2M^T y = 0$$

Multiply $(M^T M)^{-1}$ on both sides

$$(M^T M)^{-1} M^T MP = (M^T M)^{-1} M^T y$$

$$\widehat{P} = (M^T M)^{-1} M^T y$$

$$\frac{\partial^2 S(P)}{\partial P^2} = 2M^T M$$

$$\widehat{P} minimizes\, S(P)$$

$$\widehat{P} = (M^T M)^{-1} M^T y \tag{16}$$

where $\widehat{P}$ is an ordinary least square estimator of P and is represented in Eq. (16).

$$\widehat{P} = \begin{bmatrix} \widehat{\alpha} \\ \widehat{\beta} \\ \widehat{\gamma} \end{bmatrix} = (M^T M)^{-1} M^T y \tag{17}$$

where M is the matrix of order $n \times 3$

Finally, $\widehat{\alpha}, \widehat{\beta}, \text{and}\, \widehat{\gamma}$ gives the estimated values using Eq. (16) corresponding to the true value of $\alpha, \beta, \text{and}\, \gamma$. The estimated parameter values of $\widehat{\alpha}, \widehat{\beta}, \text{and} \widehat{\gamma}$ in $\widehat{P}$ are represented in Table 1.

The adaptive weights finalized in Table 1 signify the domination of the parameter $\widehat{\alpha}$ concerned with area in comparison with the weighting parameters $\widehat{\beta}, \text{and} \widehat{\gamma}$ tied with temperature and wirelength. This prioritization in the modeled LPMOFP simultaneously ensures overall Fp optimization with compaction. Also, it is evidenced that the predicted weights from Table 1 helped address the interdependencies between the three floorplan constraints, namely area, wirelength, and temperature are interrelated, and optimizing one impacts the other. For instance, temperature optimization is influenced by both area and wirelength optimizations since densely packed components and longer interconnections generate more heat. To address the interdependencies between these aspects, the proposed LPMOFP works in an iterative manner prioritizing the design parameter to be optimized via the weights $\alpha, \beta, \text{and}\, \gamma$, which are adaptively determined in each iteration by the least square process presented in Eq. (16). Optimization begins by giving the area constraint the

Table 1 Obtained parameter values of $\widehat{\alpha}, \widehat{\beta}$, and $\widehat{\gamma}$

Benchmark circuits	$\widehat{\alpha}$	$\widehat{\beta}$	$\widehat{\gamma}$
apte	0.5	0.3	0.2
xerox	0.4	0.4	0.2
hp	0.5	0.4	0.1
ami33	0.5	0.4	0.1
ami49	0.5	0.3	0.2
n10	0.4	0.4	0.2
n30	0.4	0.4	0.2
n50	0.5	0.4	0.1
n100	0.4	0.4	0.2
n200	0.5	0.3	0.2
n300	0.4	0.3	0.3

highest priority to obtain a space-efficient layout that is adaptively modified across each iteration to achieve the compact Fp. Moreover, the regressive optimization LP model presented in Eq. (11) simultaneously accounts for the temperature and wirelength variations that are weighed by the factors $\widehat{\alpha}, \widehat{\beta}$, and $\widehat{\gamma}$ adaptively as evident in Table 1.

Subsequently, the optimized layout plots obtained for the MCNC benchmark circuits using the modeled cost function are depicted in Fig. 2, wherein the unused area (white space) after placing the modules represents the deadspace.

It is evidenced from Fig. 2a–e that the area occupied by the MCNC benchmark circuits after compaction decreases gradually when compared with initial die areas. This is attributed to the usage of adaptive weights in optimizing the area by prioritizing it over wirelength and temperature by the LPMOFP to reach the optimal. Furthermore, the number of modules in the circuit increases as the aspect ratio approaches unity. As a result, the usage of LPMOFP assists in incorporating as many as number of modules which is one of the required qualities of any model in real time. Moreover, the algorithm tries to minimize the deadspace in the compacted layout by optimizing wirelength with reduced hotspots between them, and the optimal values attained after this compaction are tabulated in Table 3 for MCNC circuits.

A similar analysis is applied to GSRC benchmark circuits, revealing the gradual reduction of deadspace through LP optimization. The modules for the circuits are presented in Fig. 3.

Likewise, a similar pattern is evidenced in the area, and dead space in the GSRC benchmark circuits, as shown in Fig. 3a–f, owing to the prioritization of area and wirelength over temperature using the adaptive weights. From the above analysis, it is evident that the proposed Fp scheme renders consistent optimization in both these diverse circuits signifying its superiority over its predecessors. Accordingly, a detailed performance analysis of the proposed Fp algorithm is elaborated in Sect. 6.

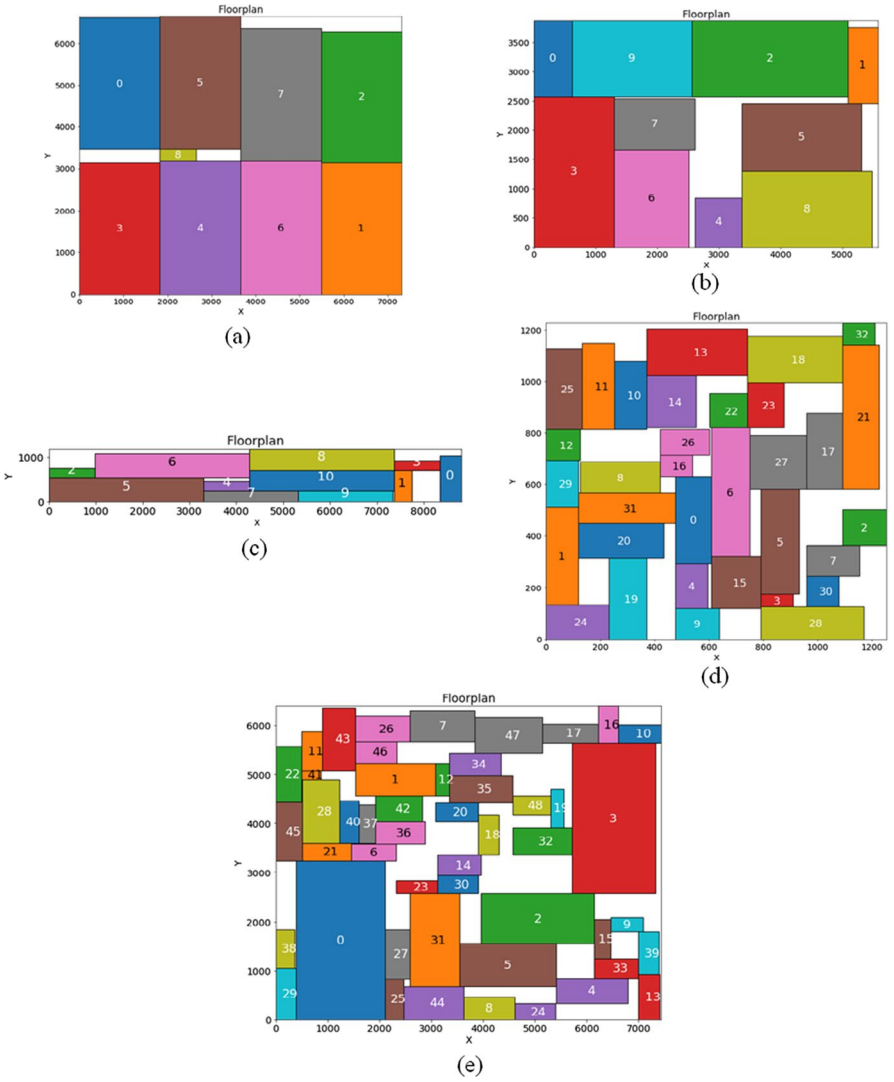

Fig. 2 **a** Apte **b** xerox **c** hp **d** ami33 and **e** ami49 circuit obtained by proposed LP model

5 Performance analysis

The introduced LP-based optimization algorithm is developed in Python on a Windows 10 platform with 2.10 GHz AMD Ryzen5 3550 H and supported by Radeon Vega Mobile Gfx processor having 8 GB RAM. Performance validation of the improved placement coordinates was performed in Python followed by simulation using the Cadence PnR tools on a Red Hat Enterprise Linux platform equipped with a quadra core Xeon (*R*) Processor E5-2609 running at a frequency of 2.40 GHz. The proposed LPMOFP is compared against state-of-the-art algorithms

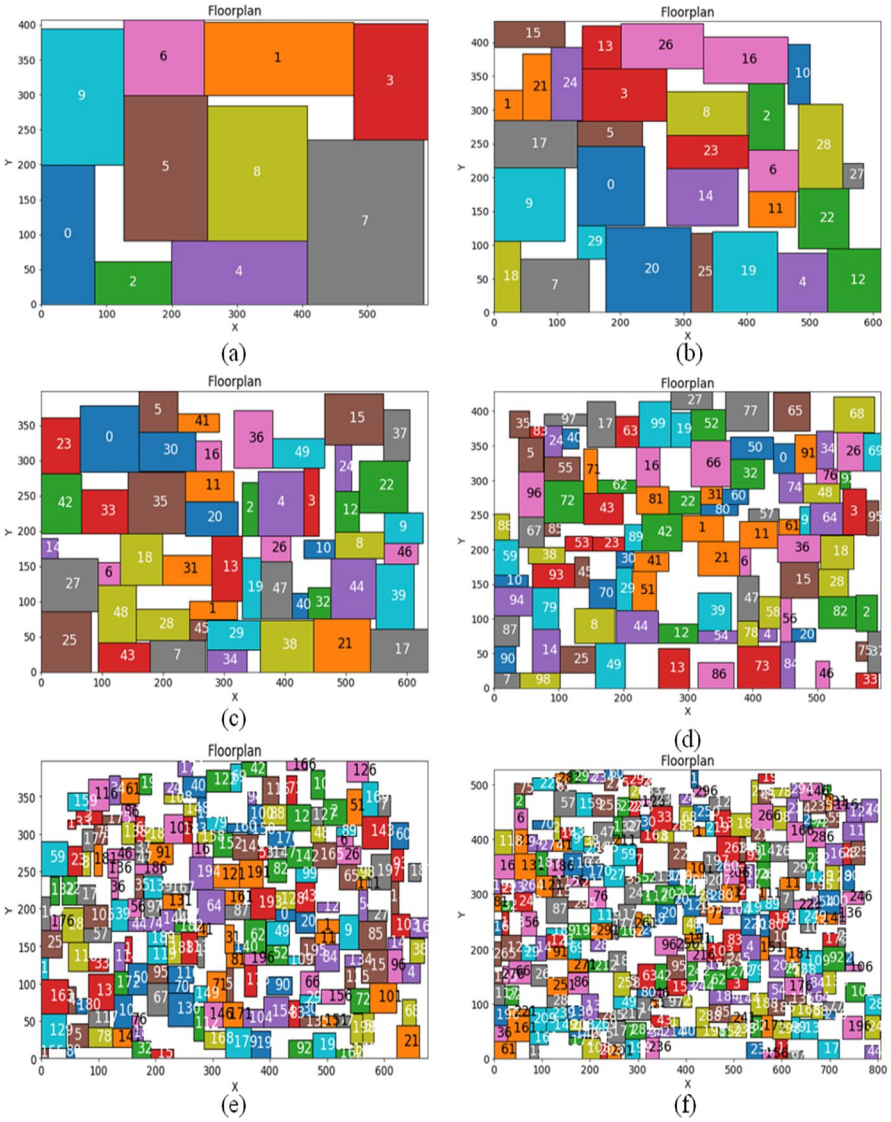

Fig. 3 **a** n10 **b** n30 **c** n50 **d** n100 **e** n200 and **f** n300 circuit with 10, 30, 50, 100, 200, and 300 modules respectively

in terms of deadspace, wirelength, and temperature through an evaluation against two distinct benchmarks, namely MCNC and GSRC, with results reported in Yet Another Language (YAL) format in Table 2.

Table 2 shows that the number of modules and terminals in these circuits may vary widely, making it difficult for Fp designers to choose an appropriate wirelength and deadspace. Another difficulty is that the aspect ratios of the MCNC and GSRC benchmark circuits are not 1:1.

Table 2 MCNC, GSRC benchmark circuit standards

Benchmarks	Circuit	Module	Terminal	Net	Pin	$W_{ref} \times H_{ref}$	Die-Area (mm^2)
MCNC	apte	9	73	97	287	10,500×10,500	110,250,000
	xerox	10	2	203	698	5831×6412	37,388,372
	hp	11	45	83	309	4928×4200	20,697,600
	ami33	33	42	123	522	2058×1463	3,010,854
	ami49	49	22	408	953	7672×7840	60,148,480
GSRC	n10	10	69	118	248	800×800	640,000
	n30	30	212	349	723	800×800	640,000
	n50	50	209	485	1050	800×800	640,000
	n100	100	334	885	1873	800×800	640,000
	n200	200	564	1585	3599	800×800	640,000
	n300	300	569	1893	4358	800×800	640,000

5.1 Result analysis

The proposed Fp algorithm is relatively compared under different scenarios, namely deadspace, wirelength, and temperature. The closeness of simulated deadspace values with the standard value demonstrates the scheme's effectiveness. For relative comparison, the five different area-occupied circuits, namely apte, xerox, hp, ami33, and ami49, used by Nature-Inspired Power Optimization (NIPO) [45], adaptive hybrid memetic algorithm (AHMA) [26], novel Fp automation framework (NFAF) [46], fast thermal analysis method (FTAM) [47], variable-order ant system (VOAS) [48], MOFO-FP (MFP) techniques [25], C4.5 decision tree (C4.5 DT) [28] are considered and stated in Table 3.

Due to the sequential optimization nature of LP in managing multiple targets with a greater convergence rate, Table 3 shows that the suggested Fp dominates in all the circuit dimensions (deadspace, wirelength, temperature). As shown in Table 3, the above parameters were minimized by an increased maximum of 1.53%, 24.43%, and 3.14% as compared to the most current C4.5 DT [28]. Furthermore, the RPM-LP combination enables effective module placement by keeping a 1:1 aspect ratio, which reduces deadspace.

The above analysis is extended to GSRC Benchmark Circuits and relatively compared with the trending Fp schemes, namely simulated annealing–voltage island-aware floorplanning (SA–VIF) [50], skewed binary tree (SKB-Tree) [51], thermal-aware voltage island generation (TAVIG) [13], C4.5 decision tree (C4.5 DT) [28], and LP is showcased in Table 4.

The measured values stated in Table 4 for all the Fp constraints are reduced owing to LP optimization. Also, the GSRC benchmark circuit layout has a 1:1 aspect ratio. The proposed model dominates its peers due to the continuous tracking of optimal values at different states iteratively in n100, n200, and n300 circuits while the minimization degrades if the number of modules is more than 100. Also, the achieved wirelength minimization reduces congestion between

Table 3 Comparison results for MCNC benchmark circuits with LP optimization for area (sq. mm), wirelength (mm), temperature (°C), and deadspace (%)

Optimized parameters	MCNC benchmark circuits	NIPO [45]	AHMA [26]	NFAF [46]	FTAM [47]	VOAS [48]	MFP [25]	C4.5 DT [28]	EMA [49]	LP
Area	apte	56.21	54.48	52.9	50.2	48.7	46.71	46.57	47.56	46.57
	xerox	30.45	26.21	25.16	23.42	21.9	19.65	19.36	20.2	19.36
	hp	20.37	16.26	14.05	11.12	10.85	8.88	8.83	9.45	8.83
	ami33	4.13	3.71	3.20	2.89	2.21	1.16	1.16	1.25	1.15
	ami49	48.26	44.15	42.72	40.5	38.4	35.64	35.47	38.23	35.46
Wirelength	apte	420.63	408.66	410.71	406.03	412.23	402.78	445	448.9	358.14
	xerox	419.73	399.66	403.88	399.14	409.09	394.04	403	402.8	304.54
	hp	167.2	152.95	156.26	152.76	160.75	148.1	166	130.7	147.64
	ami33	63.14	51.44	53.83	51.24	55.54	48.41	55.7	55.69	47.89
	ami49	728.26	711.49	715.67	710.01	719.32	707.91	891	956.2	694.74
Temperature	apte	77.34	75.16	72.75	70.23	74.16	66.78	56.7	58.36	55.12
	xerox	85.94	83.08	89.46	85.3	92.85	79.98	47.1	55.49	46.74
	hp	90.3	86.23	82.13	79.86	84.08	72.16	50.2	65.71	49.54
	ami33	115.46	109.52	105.87	100.56	107.09	95.41	73.7	100.1	71.38
	ami49	76.05	71.35	68.16	66.67	70.88	60.87	52.1	61.65	51.65
Deadspace	apte	–	–	–	–	–	–	–	1.56	0.02
	xerox	–	–	–	–	–	–	–	2.6	0.05
	hp	–	–	–	–	–	–	–	4.0	0.02
	ami33	–	–	–	–	–	–	–	2.5	0.30
	ami49	–	–	–	–	–	–	–	2.6	0.04

(–): Indicates not reported

Table 4 Comparison results for GSRC-Benchmark circuits with LP optimization for area (sq. mm), wirelength (mm), temperature (°C), and deadspace (%)

Optimized parameters	GSRC benchmark circuits	SA-VIF [50]	SKB-Tree [51]	TAVIG [13]	C4.5 DT [28]	DPAHMA [27]	LP
Area	n10	235.438	232.990	–	221.794	–	221.772
	n30	224.896	217.769	–	208.750	–	208.698
	n50	212.528	202.201	–	198.703	–	198.681
	n100	201.928	185.907	205.332	186.900	191.837	186.736
	n200	202.950	184.236	291.973	203.160	189.961	183.995
	n300	–	284.723	346.895	285386	299.854	283.982
Wirelength	n10	20,186	16.098	–	11.684	–	11.154
	n30	56.742	37.721	–	33.086	–	32.692
	n50	105.469	76.783	–	66.128	–	65589
	n100	165.641	121.116	–	102.646	197.10	101.491
	n200	345.094	272.936	–	294.146	350.39	289.536
	n300	–	410.570	–	454.330	523.07	448.496
Temperature	n10	–	–	–	52.75	–	51.24
	n30	–	–	–	69.03	–	64.91
	n50	–	–	–	84.83	–	81.68
	n100	–	–	133.1	126.55	–	111.98
	n200	–	–	128.5	118.51	–	106.39
	n300	–	–	137	128.63	–	123.82
Deadspace	n10	–	–	–	–	–	0.04
	n30	–	–	–	–	–	0.05
	n50	–	–	–	–	–	0.05
	n100	–	–	–	–	2.63	3.87
	n200	–	–	–	–	4.43	4.51
	n300	–	–	–	–	6.46	3.80

(–): Indicates not reported

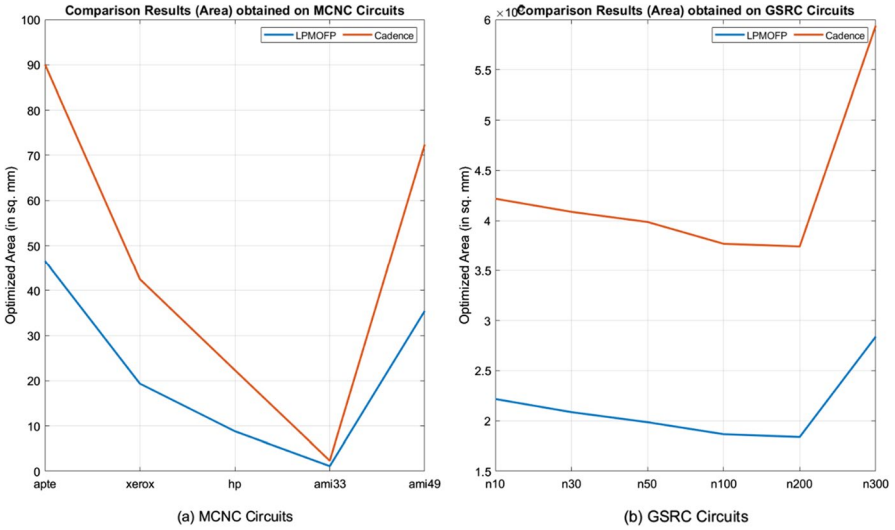

Fig. 4 Comparison of LP area optimization with cadence tools on MCNC and GSRC benchmark circuits

the modules thereby downing the circuit temperature to a maximum of 11.5% in comparison with its competitors.

Furthermore, to showcase the real-time applicability of the LPMOFP, its area optimization results are compared with CADENCE Tools.

From Fig. 4a and b, it is evident that the area optimization using Cadence tools falls behind the proposed model, the improvement in LPMOFP is owing to the utilization of adaptive weights in solving the cost function. Herein LPMOFP, packaging aspects are not taken into consideration, whereas software tools allow some area for packaging aspects.

5.1.1 Complexity analysis

This segment is predominantly intended to illustrate LP optimization in terms of not only obtaining minimal values but also highlighting LP's optimization in a short time and less space. The time complexity of Fp is determined by the location of each module within the circuit. Each module has a width of 'w' and a height of 'h'. Each module that is placed within the circuit is taken into account for the apte circuit. As a result, the time complexity of the apte circuit with 'n' modules is $O(n)$.

The time complexity of an ordinary least square estimator of P is shown as the product of the order of all the matrices in $O(M^T M)^{-1}{}_{n\times n}$, $O(M^T)_{n\times n}$ and $O(y)_{n\times 1}$. Then the complexity analysis of the matrices is the product of the order of the matrices and is represented in Eq. (17).

$$O(n \times n \times n \times 1)$$

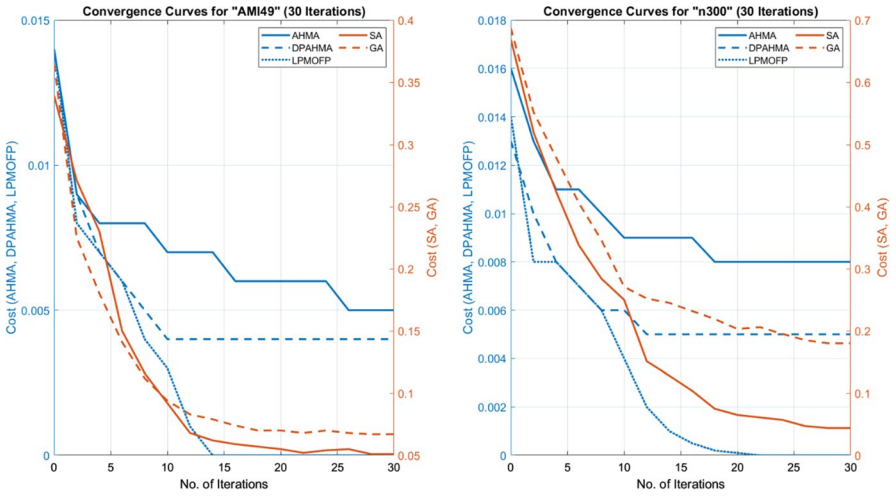

Fig. 5 Convergence curves for ami49 and n300 of MCNC and GSRC benchmark circuits

$$O(n^3) \tag{17}$$

From the preceding discussion, it is clear that the proposal's complexity is reasonable enough to be extended to Fp design.

5.1.2 CPU runtime

In general, the efficacy of any optimization-based Fp depends on the convergence rate for achieving optimal solutions. Accordingly, in this work to evidence, the efficient performance of LPMOFP and its reliability in terms of computational complexity, the convergence curves of the LPMOFP, AHMA [27], DPAHMA [27], SA [52], and GA [52] are showcased for AMI 49 and n300 of MCNC and GSRC benchmark circuits respectively.

From Fig. 5 it is evident that the convergence speed of LPMOFP is high when compared to memetic algorithm variants, SA and GA. The determination of adaptive weights using least squares approximation assisted in attaining this property. Moreover, the LPMOFP is a simple mathematical optimization that always finds exact solutions to linear objectives and constraints [53]. Also, through analysis, it is observed that SA and GA take a long time to converge if the number of modules in the circuit increases.

Moreover, the final complexity arrived in Eq. (17) indicates the speed of convergence and running time of LPMOFP. Accordingly, the CPU runtimes for MCNC and GSRC benchmark circuits are presented in Table 5.

From Table 5, it is apparent that the CPU runtime for attaining a compact Fp depends on the number of modules. However, from convergence curves, it is evidenced that the proposed LPMOFP converges after 15 iterations n300 circuit, this highlights the efficiency of the model. This is attributed to the overall LPMOFP

Table 5 CPU Runtime analysis on the MCNC and GSRC benchmark circuits using LPMOFP

Benchmark	MCNC					GSRC					
Circuits	Apte	Xerox	Hp	Ami33	Ami49	n10	n30	n50	n100	n200	n300
CPU runtime (sec)	13.28	13.30	15.28	34.24	61.79	13.07	30.10	73.95	180.69	712.02	2141.77

framework that prioritized optimization of a particular design parameter based on adaptive weights estimated using the least squares approach.

6 Conclusion

This study delivers an innovative floorplanning approach utilizing a linear programming for multi-objective optimization considering area, wirelength, and temperature as constraints within the objective function. The incorporated linear programming adaptively tuned weights to each constraints that effectively optimize floorplanning design. This approach employs a sequential placement strategy, reducing design complexity by tuning individual design parameters. Performance validation of this approach demonstrates its effectiveness in optimizing area, wirelength, and temperature. By combining the introduced cost function with the rectangular packing method, a substantial reduction of 12.52% in wirelength, 19.44% in area, and 27.42% in temperature was achieved when evaluated on the Microelectronic Centre of North Carolina benchmark, all while maintaining a unity aspect ratio. Circuit simulations were conducted using the Microelectronic Centre of North Carolina benchmark and Gigascale Systems Research Centre Benchmark circuits. Comparative analysis in terms of area, wirelength, and temperature highlights the superior performance of the proposed linear programming-based multi-objective floorplanning over existing approaches. The adaptability of this approach to various benchmarks is facilitated by its consideration of multiple design constraints tuned using an optimization function. Moreover, this multi-objective optimization framework can be extended to include power and crosstalk to improve the practical applicability of the Linear programming-based multi-objective floorplanning. Furthermore, the packaging method used in this work places the modules at random for the first time and the placement is further enhanced by Linear programming-based multi-objective floorplanning. Also, the adopted module placement strategy needs further layout exploration to achieve better optimization or compaction thereby, instigating its extension to deal with large benchmark circuits like AMI49_X and IBM-PLACE.

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Data availability Publicly available benchmark circuits from MCNC [20] and GSRC [21] were utilized for the simulations of the presented methodology.

Declarations

Conflict of interest The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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