

Michelson & Mach-Zehnder Interferometers Design, characterization and fabrication.

Author: Javad Babaki

Electrical and Computer Engineering Department, University of North Carolina at Charlotte, USA.

Email: Jbabaki@uncc.edu

Abstract: As a Silicon photonics project here, the proposal aims to design, simulate, and fabricate a Photonic Integrated Circuit (PIC) comprising a range of photonic components, from fundamental elements to advanced functionalities as part of a complementary research effort. The initial phase involves evaluating the impact of various parameters on individual photonic components such as couplers and MZI Interferometer using Lumerical software, employing both Mode solution and FDTD modules. After gathering and analyzing the data for each component, we proceed to design the overall PIC layout. Following the design phase, we will fabricate the PIC using an E-beam lithography system. The resulting device will be analyzed through computational tools such as MATLAB to assess the influence of fabrication imperfections and external environmental parameters. Additionally, we aim to propose a new compact modeling approach for the advanced components integrated into our library, which could serve as a reference for future developments in photonic device design.

Keywords- PIC, MZI, MI, Y-splitter, Grating Coupler

1. Introduction

Silicon photonics research and commercialization have surged in recent years, driven by significant advancements in both photonic component performance and integration complexity[1]. This technology now supports a broad range of applications, from high-speed data and telecommunications to specialized sensors like LIDAR, gyroscopes, biosensors, and spectrometers[2].

The primary advantage of silicon-based photonics lies in their low-loss, compact waveguides, which offer exceptional consistency due to the mature and precise manufacturing processes within the silicon CMOS ecosystem. Additionally, modern CMOS packaging techniques—originally developed for consumer electronics and IT industries are now being adapted for silicon photonic integrated circuits (PICs). This shift has drastically reduced production costs while improving scalability.

A prime example of this rapid development is the evolution of datacom transceivers, which have progressed through multiple generations of technology. Silicon photonics has moved swiftly from initial product launches to large-scale commercial adoption, with shipments now reaching millions of units annually. With data transfer rates rising from 100 Gbps to the terabit-per-second range, integrating electronics has become critical to minimizing system-wide power consumption and reducing capacitance at both the modulator and photodetector levels[3]. Over the past decade, power efficiency has improved significantly, with energy per bit decreasing from thousands of picojoules to less than one picojoule.

A key element in this ecosystem, the semiconductor laser, is also evolving. Traditionally, these lasers have been separated from the rest of the photonic system, but future designs will integrate them directly into the PIC. This integration will enable a transition from single-laser architectures to arrays featuring potentially thousands of lasers per PIC, leveraging wavelength division multiplexing (WDM) to facilitate petabit-scale data connections[1].

At the same time, the placement of PICs within computing systems is changing. Previously confined to pluggable transceivers at the edge of circuit boards, silicon photonics are now shifting toward co-packaged optics, which combine electronics and photonics within the same housing. The next step in this evolution includes three-dimensional integration, where photonic and electrical integrated circuits (EICs) are stacked together, promising even greater efficiency and performance gains.

The Michelson Interferometer is a fundamental optical instrument used for precision measurements, exploiting the interference of light waves. Developed by Albert A. Michelson in the late 19th century, it operates by splitting a coherent light source into two paths using a beam splitter. These two beams reflect off mirrors and recombine, creating an interference pattern that depends on the optical path difference (OPD). Variations in OPD can be used to measure distances, refractive index changes, or even fundamental physical constants.

Here, the major steps for designing a PIC are proposed. Firstly, a summary about the theory of photonics elements for making a Michelson Interferometer is described. The following section will relate to the simulation and modeling of these elements and their characterization. Components used in silicon photonics (SiPh) such as Y-splitter, Mach-Zehnder interferometer, waveguides, adiabatic directional coupler, grating coupler, Michelson interferometers are evaluated in this section. Third section belongs to the fabrication process carried out by E-Beam lithography. Next section, we will analysis the experiments data and simulated results to understand the efficiency of components in real world as well as the probable side effects of different limitations of the instruments in micro fabrication process. Finally, a brief conclusion is presented as well.

2. Theory

Photonic integrated circuits (PICs) rely on key optical components such as Y-splitters, grating couplers, Mach-Zehnder interferometers (MZIs), and Michelson interferometers (MIs) to manipulate and control light propagation. Y-splitters divide optical power into two waveguides, crucial for signal routing and power distribution. Grating couplers facilitate efficient coupling between optical fibers and on-chip waveguides by leveraging diffraction effects, optimizing mode matching for minimal insertion loss. MZIs exploit interference between two optical paths to achieve high-precision modulation, filtering, and sensing applications, while MIs function similarly but utilize reflection-based interference, enhancing their utility in precise optical delay lines and metrology.

The performance of these components is governed by wave optics, mode propagation, and interference principles. Y-splitters and grating couplers rely on evanescent field coupling and diffraction, respectively, to ensure efficient power transfer. MZIs and MIs operate based on phase differences between propagating beams, where constructive or destructive interference modulates the output intensity. The design and optimization of these structures involve considerations of wavelength dependence, fabrication tolerances, and integration with active elements for advanced photonic functionalities. These components collectively enable key functionalities in optical communication, sensing, and quantum photonics, forming the backbone of modern PIC architectures.

2.1 Key Components of an Interferometer

2.1.1 Y-Splitter

A Y-splitter is a fundamental passive photonic component used to divide an incoming optical signal into two separate waveguides. It forms a crucial part of the interferometer by ensuring equal power distribution between the two arms. The output intensities of the branches depend on the wavelength and structural parameters of the splitter. For an ideal symmetric Y-splitter, the transmitted power in each arm is given by:

$$P_{out,1} = P_{out,2} = P_{in}/2 \quad (\text{Eq.1})$$

where P_{in} is the input optical power, and $P_{out,1}$ and $P_{out,2}$ are the output powers of the two arms. This ratio is also changed by making an imbalanced one where there will not be a 50%-50% splitting anymore.

3.2 Waveguides

Waveguides as a major part of any PIC confine and direct light within the interferometer. They replace free-space beams in integrated photonic Michelson Interferometers, ensuring minimal loss and improved stability. These are typically made of silicon due to their high refractive index contrast, enabling strong light confinement. Where Si material as the core material with the refractive index equals to 3.4 is coated by surrounding materials like SiO_2 which has the refractive index equals to 1.4. A Si waveguide is fabricated via stacked layers of Silicon and silicon oxide on silicon substrates. Different shapes of core are used in different applications where the rectangular WG is more used for on chip applications. There are typically several types of silicon waveguide as depicted in fig. 1 where the str psi waveguide is used in this project.

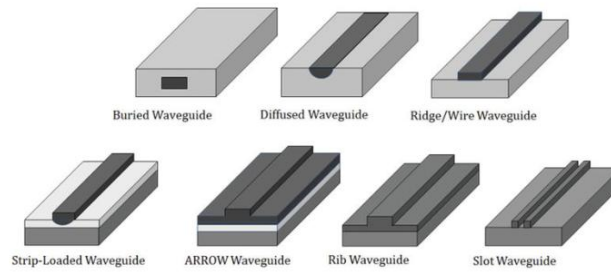


Fig. 1. Various schematics of optical WG[4].

The phase shift in a waveguide of length L is given by:

$$\Delta\varphi = \frac{2\pi L n_{eff}}{\lambda} \quad (\text{Eq. 2})$$

where n_{eff} is the effective refractive index of the waveguide, and λ is the wavelength of the propagating light.

3.3 Mirrors

A Michelson interferometer also consists of two static and movable ones that scatter the light. In microscopy application, the sample is located between the splitter and the static mirror where another movable mirror creates a destructive and instructive interference. These two mirrors are simulated via two y-splitters and a waveguide connecting two outputs of the y-splitter together.

An adiabatic directional coupler is also used in the setup for being evaluated as another main part of PIC.

3.4 Governing Equations for the Michelson and Mach-Zehnder Interferometers

3.4.1 Michelson Interferometer

Interference occurs when two waves combine coherently. The intensity at the output of a Michelson Interferometer follows:

$$I = I_0 [1 + \cos(\frac{2\pi n_{eff} \Delta L}{\lambda})] \quad (\text{Eq. 3})$$

Where I_0 , $\Delta L = L_1 - L_2$ are the maximum intensity, and the optical path difference between the two arm, respectively.

For phase modulation applications, the interference signal can be rewritten in terms of phase difference $\Delta\phi$:

$$I = I_0 [1 + \cos(\Delta\phi)] \quad (\text{Eq. 4})$$

For the Michelson Interferometer, since light passes through each arm twice, the effective optical path difference is doubled, modifying the FSR formula as:

$$\text{FSR}_{MI} = \lambda^2 / 4n_g L \quad (\text{Eq. 5})$$

But for an MZI, the optical paths remain independent, so the standard FSR equation applies:

$$\text{FSR}_{MZI} = \lambda^2 / 2n_g L \quad (\text{Eq. 6})$$

Where n_g represents as group index.

4. Modelling and Simulation

4.1 Mode solution

As an initial step, we simulate the silicon waveguide to determine its supported optical modes and extract the corresponding frequencies for transverse electric (TE) and transverse magnetic (TM) modes. This process allows us to analyze the waveguide's modal characteristics, including effective refractive indices and dispersion properties, which are essential for accurate integration

into subsequent modules. Once identified, these modes and their frequencies are stored in a file like .ldf file, ensuring consistency and reusability in later simulations, such as coupling analysis and interferometric design.

4.2 2.5 FDTD simulation

After defining the geometry of wg with width and height equals to is equals to 500 nm and 220 nm, respectively, the modes of the wg are obtained via FDE solver which two modes TE₀ and TM₀ are depicted in Fig. 2.

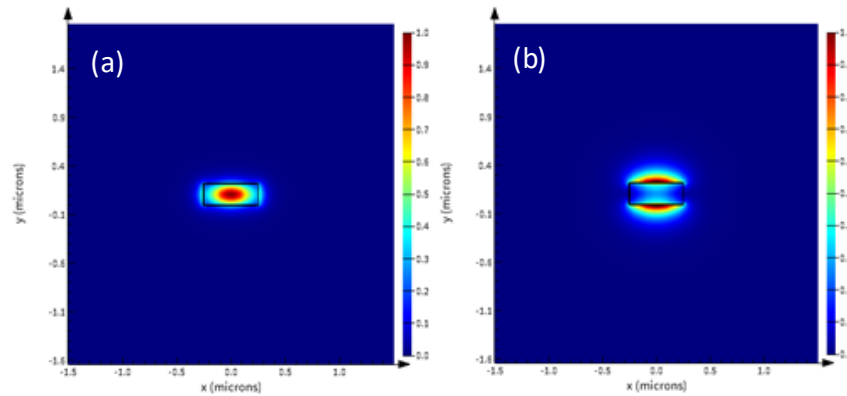


Fig. 2 Electric Intensity in Si WG, (a) of TE mode and (b) of TM mode.

Two important parameters such as effective index and group index are obtained via frequency sweep simulation. The effective index, group index, and dispersion are obtained analytically via fitting procedure and by Matlab with polynomial equation as:

$$n_{eff}(\lambda) = n_1 - n_2(\lambda - \lambda_0) - n_3(\lambda - \lambda_0)^2 \quad (\text{Eq. 7})$$

Where n_1 , $n_1 - n_2$, $\lambda - 2 \cdot \lambda_0$, n_3/c equal to n_{eff} , n_g , and D , respectively. These values are obtained by fitting as: $2.44325 - 1.1316(\lambda - 1.55) - 0.0396678(\lambda - 1.55)^2$

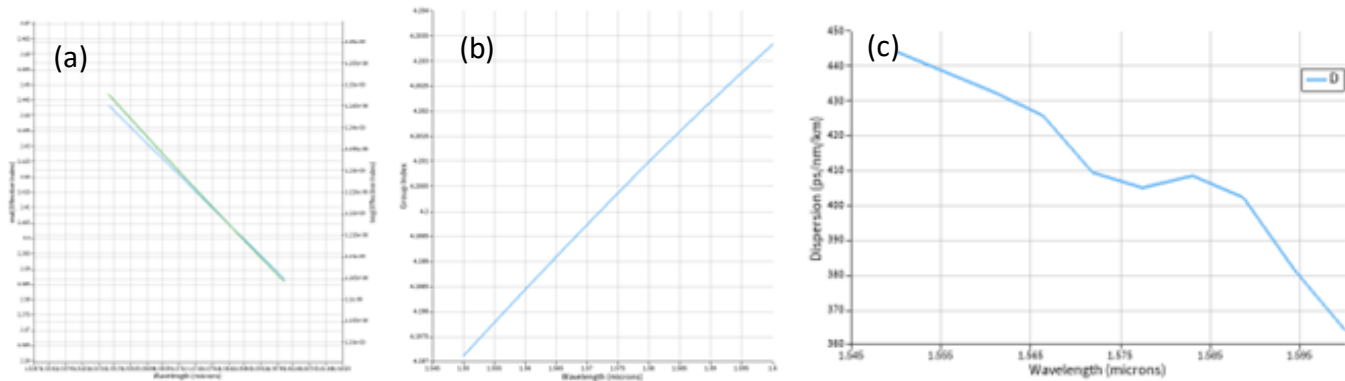


Fig.3. (a) effective index, (b) group index, and (c) dispersion of silicon WG.

After getting this data we save the data to be used later in other modules. Next step relates to 2.5 FDTD simulation where we simulate a y branch splitter. The following shows the simulation results:

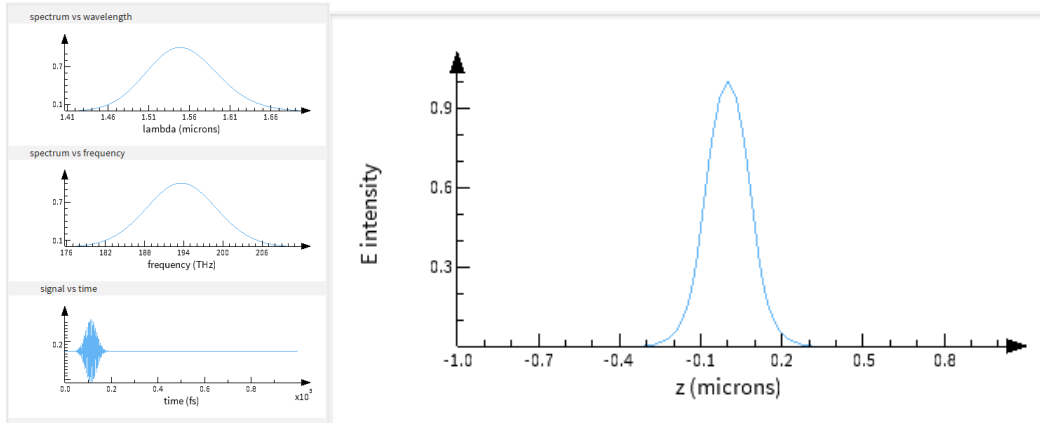


Fig. 4. (left side) laser source definition, (right side) the slab mode profile.

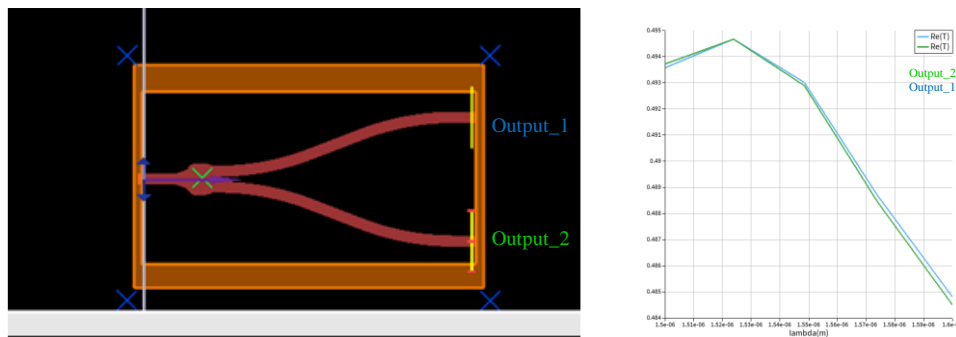


Fig. 5. (left side) schematic of FDTD simulation, (right side) transmission profile of two outputs of y-splitter

4.3 Interconnect module

4.3.1 Grating Coupler

Connection between a fiber to the circuit is performed via edge coupler or by using grating couplers causes. This element has loss. So, we simulated the insertion loss in GC as depicted in fig. 6.

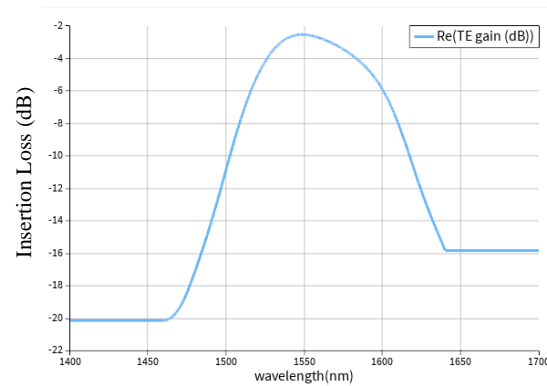


Fig.6 Insertion loss in grating coupler.

4.3.2 Y-branch splitter Design:

Fig. 7 shows the difference between the insertion loss in an ideal branch and the real one with s-parameters data. As it can be seen here, in real elements there is wavelength dependent loss in element.

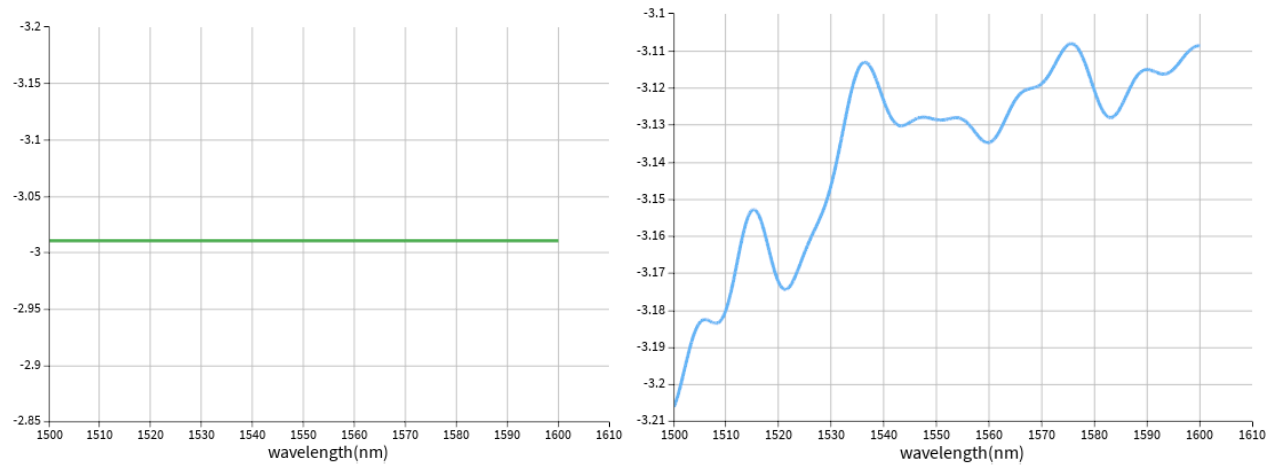


Fig. 7. (left side) Ideal y-branch insertion loss(dB), (right side) a splitter via s-parameters.

4.3.3 MZI Design:

Here, we simulate MZI in interconnect module of Lumerical as the schematic shown in fig. 8. First, we simulate MZI without GCs for both Imbalanced MZI and balanced one (Fig. 8).

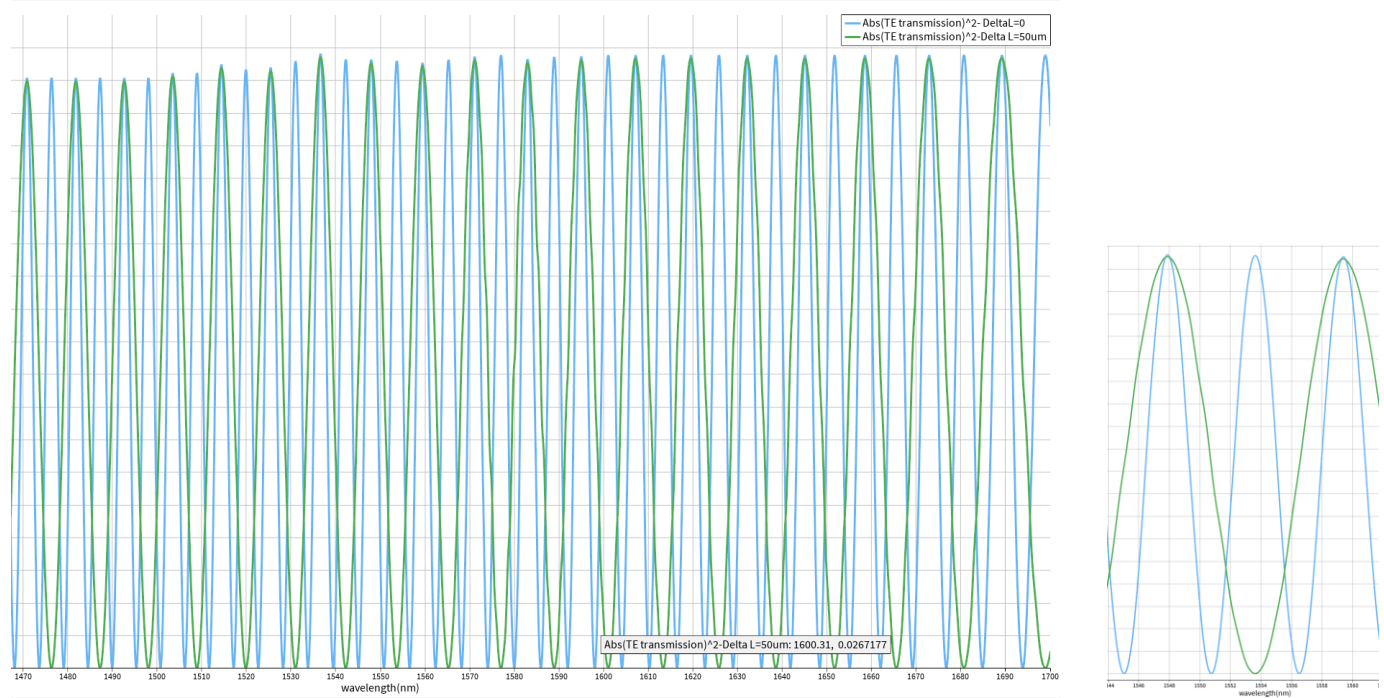


Fig. 8. The MZI transmission for $\Delta L=0$ and $\Delta L=50\mu\text{m}$ MZI with π phase shift, (left image) zoomed in at 1550 nm.

Next, the grating couplers are connected to the circuit with parameters where fig.9 shows the transmission comparison between two MZIs with same arm length and with 50 μm difference between two arms. For balanced ones, they are set to 200 μm .

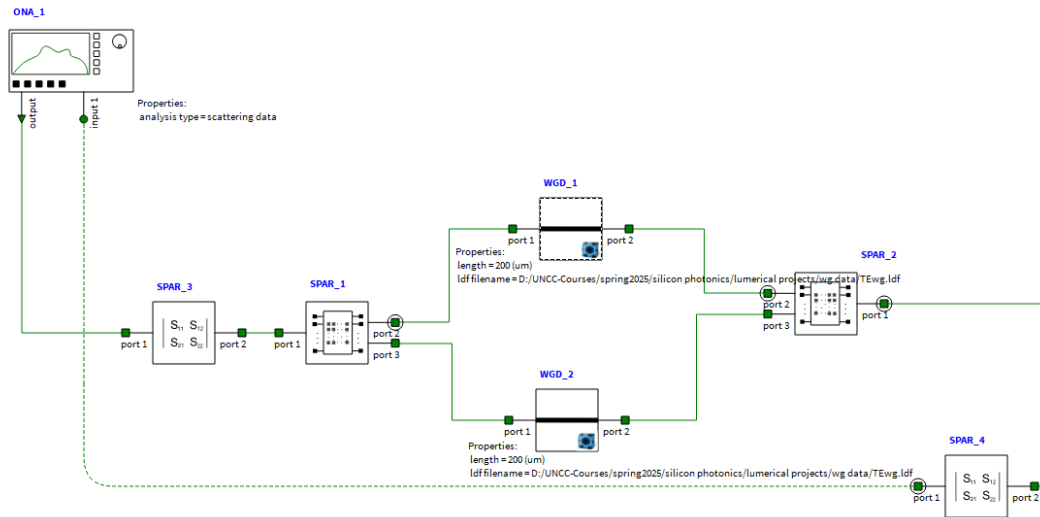
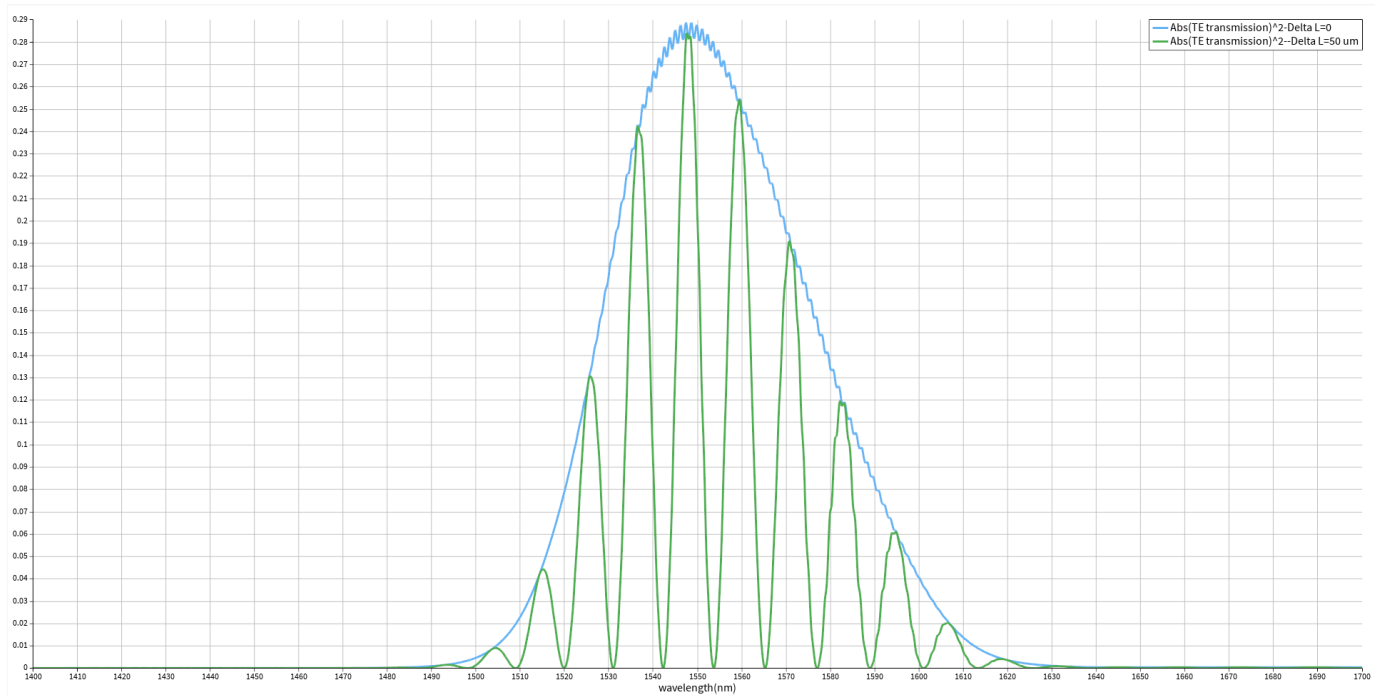


Fig. 9. Schematic of MZI, Interconnect Module.

Fig. 10. Transmission of MZI with $\Delta L=0$ and $\Delta L=50$ um.

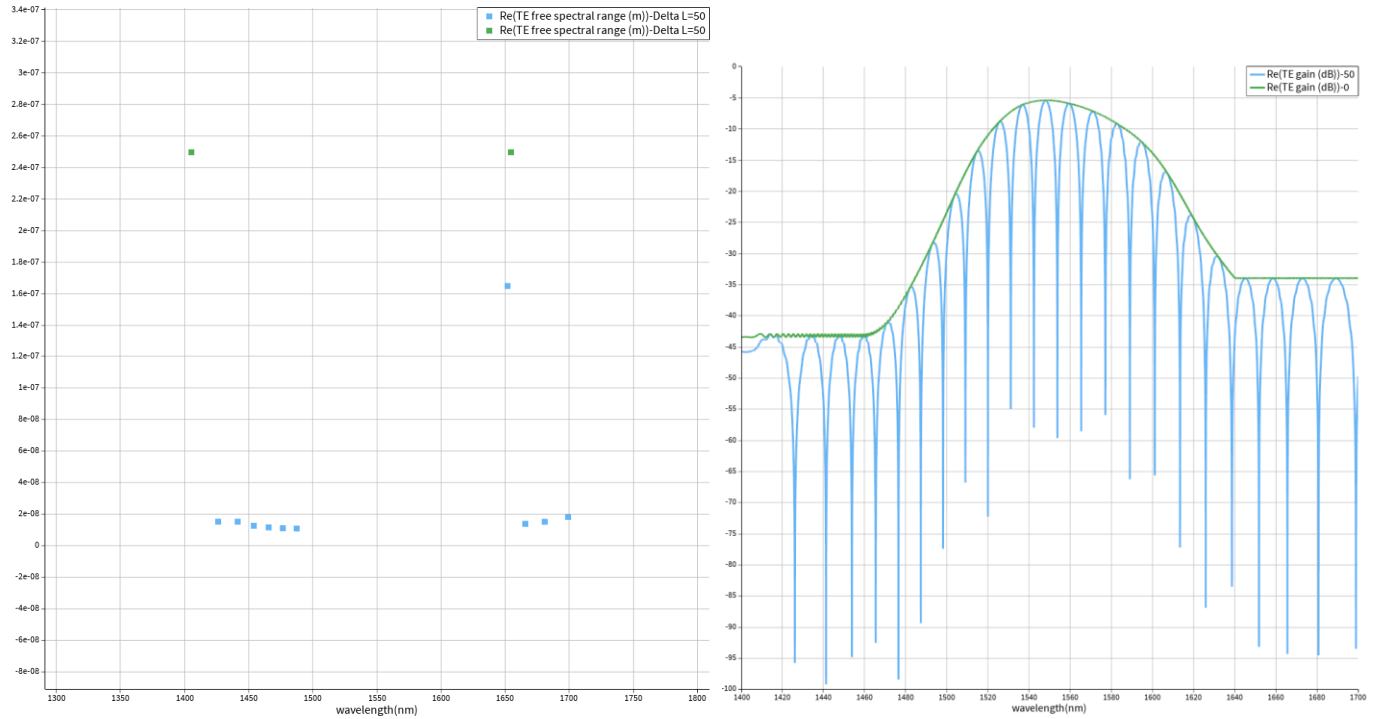


Fig. 11. (left side) FSR of MZIs with $\Delta L=0$ and $\Delta L=50 \mu\text{m}$, and (Right side) gain profiles of MZIs.

4.3.4 MI Design:

In this section, we simulate a MI that can be seen in fig. 12.

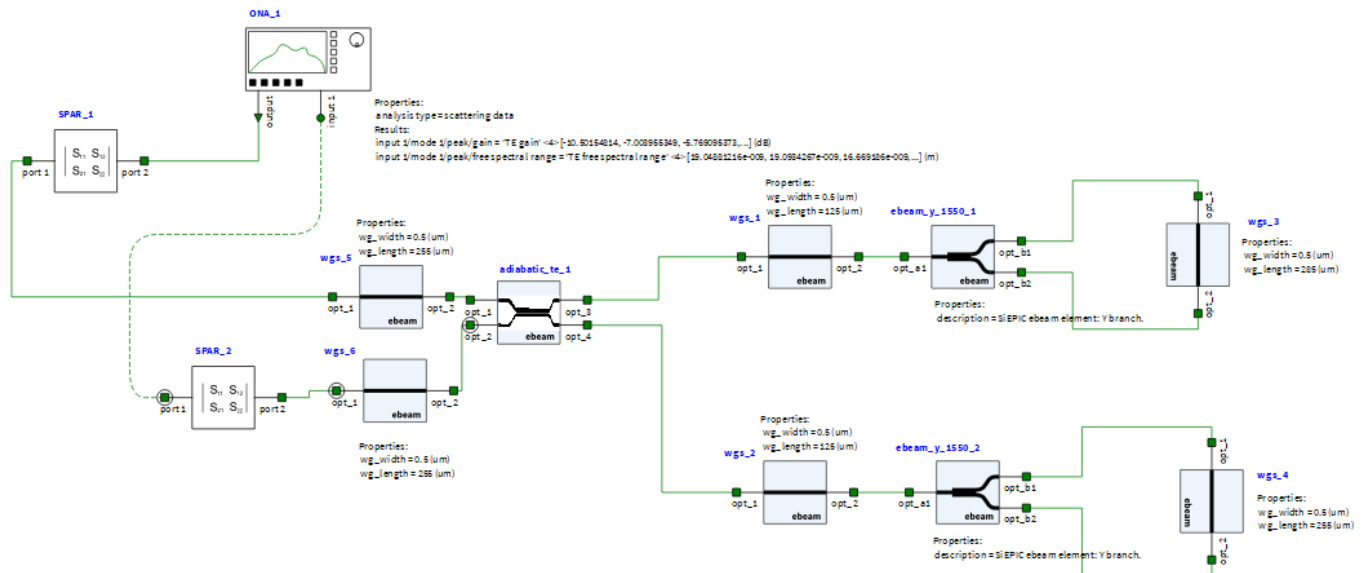


Fig. 12. Interconnect schematic of MI

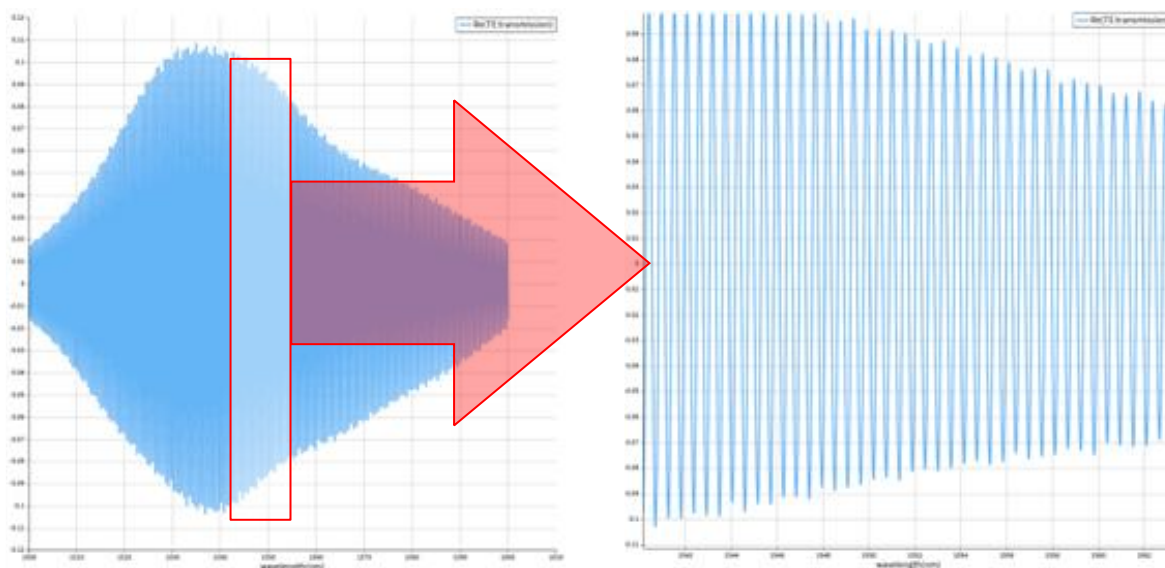
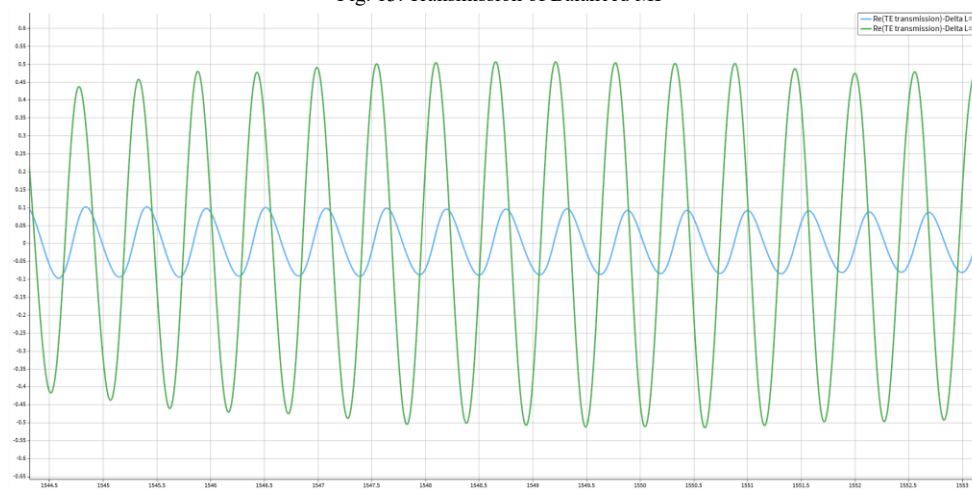


Fig. 13. Transmission of Balanced MI

Fig. 14. Transmission comparison between Imbalanced MI ($\Delta L = 20 \mu\text{m}$) and Balanced MI ($\Delta L = 0$).

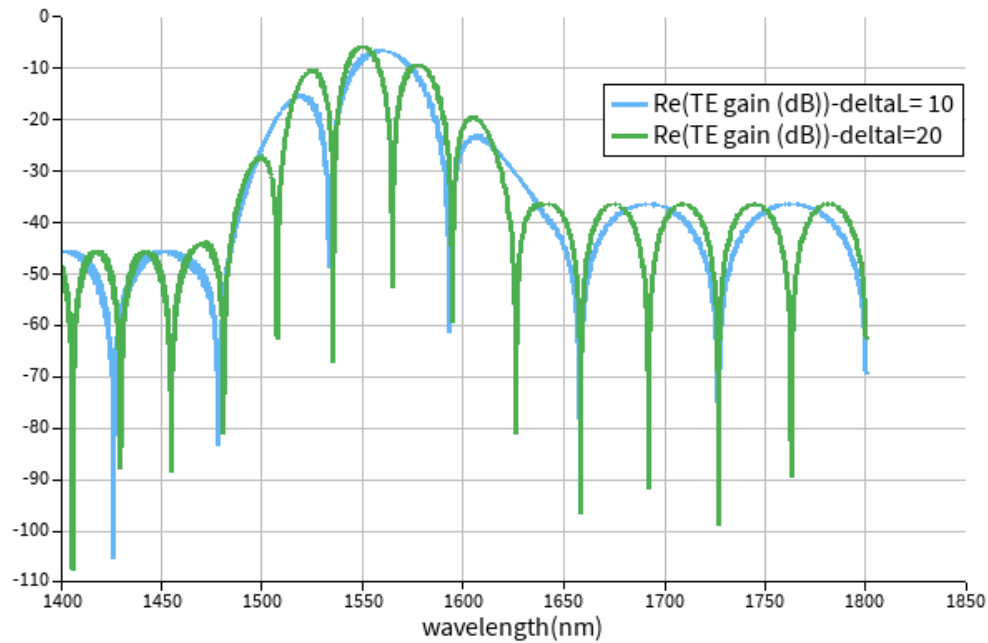


Fig .15. the gain (dB) for $\Delta L=10$ and $\Delta L=20$

5. Fabrication

Klayout is used for designing the layout for fabrication. Fig. 13 shows the proposed layout. There are 5 Parametric cells including imbalanced and Balanced MZI, imbalanced and Balanced MI, and Y splitter. In imbalanced MI, the only length of WG_1 is changed from 255 μm to 275 μm as L is equals to 20 μm .

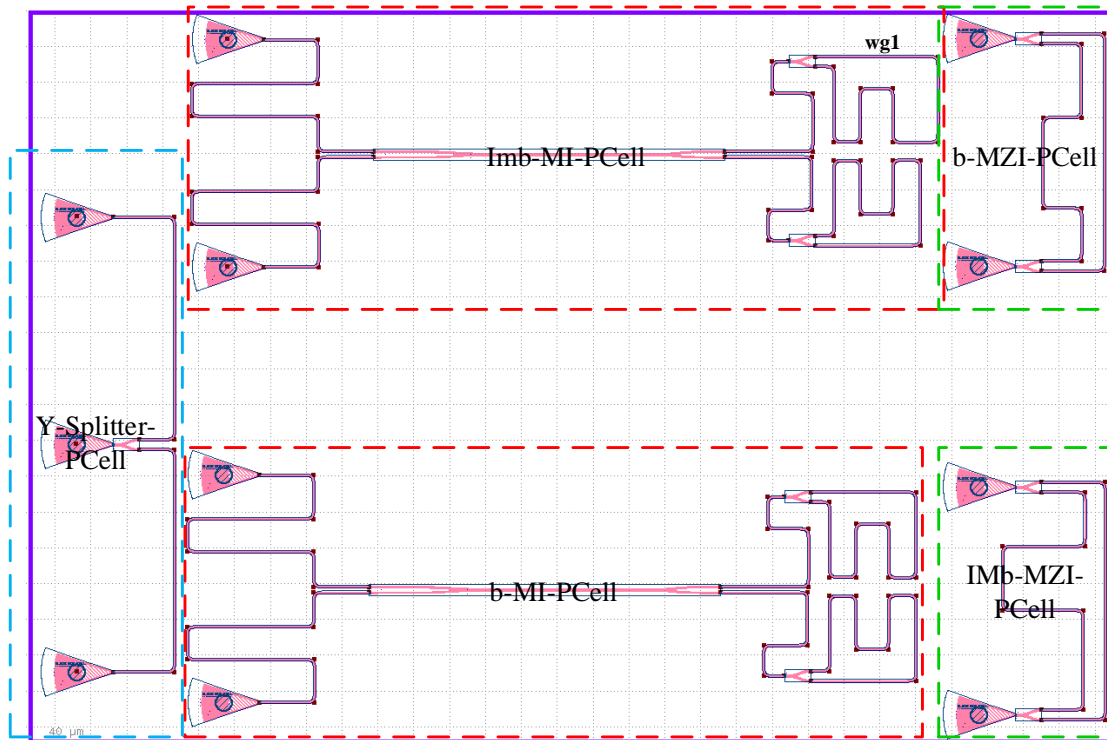


Fig. 16. Layout schematic

5.1 Washington Nanofabrication Facility (WNF) silicon photonics process:

The devices were fabricated using 100 keV Electron Beam Lithography [Bojko 2011]. The fabrication used silicon-on-insulator wafer with 220 nm thick silicon on 3 μm thick silicon dioxide. The substrates were 25 mm squares diced from 150 mm wafers. After a solvent rinse and hot-plate dehydration bake, hydrogen silsesquioxane resist (HSQ, Dow-Corning XP-1541-006) was spin-coated at 4000 rpm, then hotplate baked at 80 $^{\circ}\text{C}$ for 4 minutes. Electron beam lithography was performed using a JEOL JBX-6300FS system operated at 100 keV energy, 8 nA beam current, and 500 μm exposure field size. The machine grid used for shape placement was 1 nm, while the beam stepping grid, the spacing between dwell points during the shape writing, was 6 nm. An exposure dose of 2800 $\mu\text{C}/\text{cm}^2$ was used. The resist was developed by immersion in 25% tetramethylammonium hydroxide for 4 minutes, followed by a flowing deionized water rinse for 60 s, an isopropanol rinse for 10 s, and then blown dry with nitrogen. The silicon was removed from unexposed areas using inductively coupled plasma etching in an Oxford Plasmalab System 100, with a chlorine gas flow of 20 sccm, pressure of 12 mT, ICP power of 800 W, bias power of 40 W, and a platen temperature of 20 $^{\circ}\text{C}$, resulting in a bias voltage of 185 V. During etching, chips were mounted on a 100 mm silicon carrier wafer using perfluoropolyether vacuum oil.

5.2 Applied Nanotools, Inc. NanoSOI process:

The photonic devices were fabricated using the NanoSOI MPW fabrication process by Applied Nanotools Inc. (<http://www.appliednt.com/nanosoi>; Edmonton, Canada) which is based on direct-write 100 keV electron beam lithography technology. Silicon-on-insulator wafers of 200 mm diameter, 220 nm device thickness and 2 μm buffer oxide thickness are used as the base material for the fabrication. The wafer was pre-diced into square substrates with dimensions of 25x25 mm, and lines were scribed into the substrate backsides to facilitate easy separation into smaller chips once fabrication was complete. After an initial wafer clean using piranha solution (3:1 $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$) for 15 minutes and water/IPA rinse, hydrogen silsesquioxane (HSQ) resist was spin-coated onto the substrate and heated to evaporate the solvent. The photonic devices were patterned using a Raith EBPG 5000+ electron beam instrument using a raster step size of 5 nm. The exposure dosage of the design was corrected for proximity effects that result from the backscatter of electrons from exposure of nearby features. Shape writing order was optimized for efficient patterning and minimal beam drift. After the e-beam exposure and subsequent development with a tetramethylammonium sulfate (TMAH) solution, the devices were inspected optically for residues and/or defects. The chips were then mounted on a 4" handle wafer and underwent an anisotropic ICP-RIE etch process using chlorine after qualification of the etch rate. The resist was removed from the surface of the devices using a 10:1 buffer oxide wet etch, and the devices were inspected using a scanning electron microscope (SEM) to verify patterning and etch quality. A 2.2 μm oxide cladding was deposited using a plasma-enhanced chemical vapour deposition (PECVD) process based on tetraethyl orthosilicate (TEOS) at 300 $^{\circ}\text{C}$. Reflectometry measurements were performed throughout the process to verify the device layer, buffer oxide and cladding thicknesses before delivery.

6 Experimental Data

To characterize the devices, a custom-built automated test setup [Chrostowski] with automated control software written in Python was used (<http://siepic.ubc.ca/probestation>). An Agilent 81600B tunable laser was used as the input source and Agilent 81635A optical power sensors as the output detectors. The wavelength was swept from 1500 to 1600 nm in 10 pm steps. A polarization maintaining (PM) fibre was used to maintain the polarization state of the light, to couple the TE polarization into the grating couplers [Wang 2014]. A 90 $^{\circ}$ rotation was used to inject light into the TM grating couplers [4]. A polarization maintaining fibre array was used to couple light in/out of the chip [www.plcconnections.com].

7 Analysis

Data analysis to extract waveguide group index, etc.

Comparison of experimental results with simulations.

8 Conclusion

The conclusion goes here.

9 Acknowledgements

I acknowledge the edX UBCx Phot1x Silicon Photonics Design, Fabrication, and Data Analysis course, supported by the Natural Sciences and Engineering Research Council of Canada (NSERC) Silicon Electronic-Photonic Integrated Circuits (SiEPIC) Program. We extend our gratitude to Prof. Chrostowski for his invaluable guidance as the instructor of this course. The devices were fabricated by Richard Bojko at the University of Washington's Nanofabrication Facility, part of the National Science Foundation's National Nanotechnology Infrastructure Network (NNIN), and by Cameron Horvath at Applied Nanotools, Inc. Measurements were performed by Enxiao Luan at The University of British Columbia. We also acknowledge Lumerical Solutions, Inc., IPKISS, and KLayout for providing the design software used in this work.

References

1. Xiang, C., et al., *Perspective on the future of silicon photonics and electronics*. Applied Physics Letters, 2021. **118**(22).
2. Shekhar, S., et al., *Roadmapping the next generation of silicon photonics*. Nature Communications, 2024. **15**(1): p. 751.
3. Jones, R., et al., *Heterogeneously integrated InP/silicon photonics: fabricating fully functional transceivers*. IEEE Nanotechnology Magazine, 2019. **13**(2): p. 17-26.
4. Selvaraja, S.K. and P. Sethi, *Review on optical waveguides*. Emerging Waveguide Technology, 2018. **95**: p. 458.