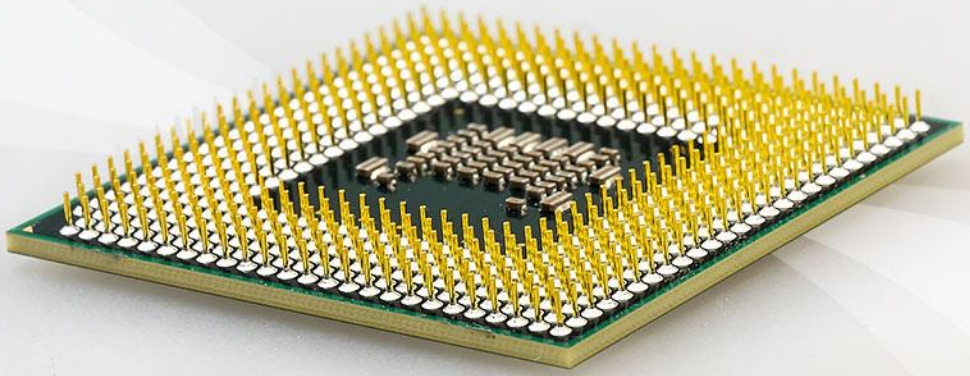


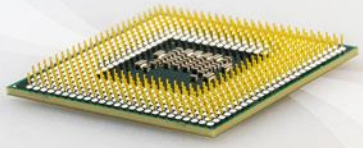
微算機應用實習

UART 中斷接收

課程編號 ： EE4801702

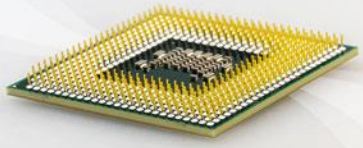
實習課助教 ： 曾子倫

Outline



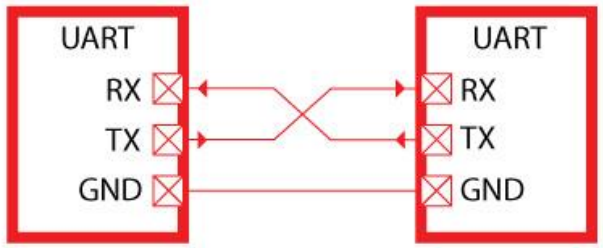
- UART 中斷接收介紹
- 溢出錯誤(Overrun error)
- 記憶體暫存器介紹

UART 介紹

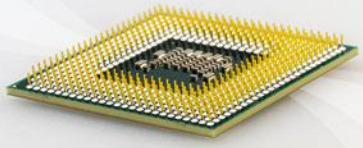


- UART
  (Universal Asynchronous Receiver/Transmitter)

- UART 是一種串列傳輸，通常會有兩條線，一條是Tx(Transmitter)，另一條是Rx(Receiver)，利用這兩條線讓CPU和周邊裝置或是實驗板之間進行資料傳遞。



UART 介紹



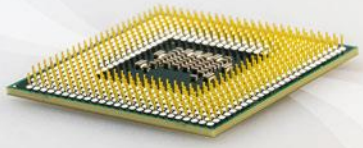
- 資料格式

Start bit	1bit
Data bit	5~8bits
Parity bit	1bit
Stop bit	1bit

- Baud rate（鮑率）

  資料傳輸的速度

UART 中斷接收介紹

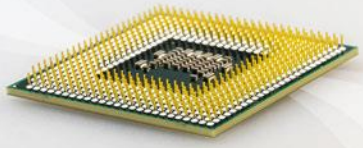


- UART的接收若不使用中斷接收時，通常會發生溢出錯誤(Overrun error)。

- 溢出錯誤(Overrun error)

在RXNE沒有重設的情況下，此時又接收到一筆新資料，則會發生溢出錯誤。

溢出錯誤(Overrun error)



```
main()
{
   while(1)
  {
    UARTReceive();
  }
}
```

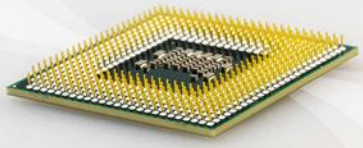
Overrun Error

```
main()
{
   while(1)
   {
     UARTReceive();
      Task
      Task
      Task
      Task
      Task
    }
 }
```

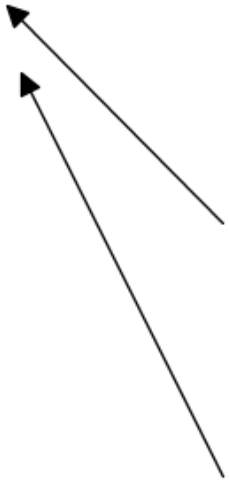
← 收到資料

← 收到資料

UART 中斷接收



```
interrupt()
{
  If(UART Interrupt Flag)
  {
    UARTReceive();
  }
}
```

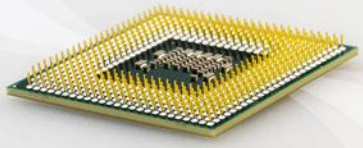


```
main()
{
  Set Uart Interrupt();
  while(1)
  {
    Task
    Task
    Task
    Task
    Task
  }
}
```

收到資料

收到資料

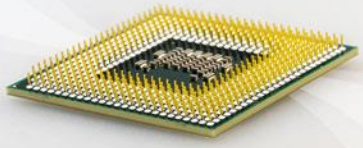
記憶體暫存器介紹



- UART 中斷Enable

114			31:20		Reserved
	0	R/W	15	IE1_I2C7	0: Disable I2C7 interrupt 1: Enable I2C7 interrupt
	0	R/W	14	IE1_I2C6	0: Disable I2C6 interrupt 1: Enable I2C6 interrupt
	0	R/W	13	IE1_I2C5	0: Disable I2C5 interrupt 1: Enable I2C5 interrupt
	0	R/W	12	IE1_I2C4	0: Disable I2C4 interrupt 1: Enable I2C4 interrupt
	0	R/W	11	IE1_I2C3	0: Disable I2C3 interrupt 1: Enable I2C3 interrupt
	0	R/W	10	IE1_I2C2	0: Disable I2C2 interrupt 1: Enable I2C2 interrupt
	0	R/W	9	IE1_IR	0: Disable IR interrupt 1: Enable IR interrupt
	0	R/W	8	IE1_I2C0	0: Disable I2C0 interrupt 1: Enable I2C0 interrupt
	0	R/W	7	IE1_SPI3	0: Disable SPI3 interrupt 1: Enable SPI3 interrupt
	0	R/W	6	IE1_SPI2	0: Disable SPI2 interrupt 1: Enable SPI2 interrupt
	0	R/W	5	IE1_SPI1	0: Disable SPI1 interrupt 1: Enable SPI1 interrupt
	0	R/W	4	IE1_SPI0	0: Disable SPI0 interrupt 1: Enable SPI0 interrupt
	0	R/W	3	IE1_UART3	0: Disable UART3 interrupt 1: Enable UART3 interrupt
	0	R/W	2	IE1_UART2	0: Disable UART2 interrupt 1: Enable UART2 interrupt
	0	R/W	1	IE1_UART1	0: Disable UART1 interrupt 1: Enable UART1 interrupt
	0	R/W	0	IE1_UART0	0: Disable UART0 interrupt 1: Enable UART0 interrupt

記憶體暫存器介紹



- RART address range

```
UART0: address range 0x0020_3000 ~ 0x0020_33FF
UART1: address range 0x0020_B000 ~ 0x0020_B3FF
UART2: address range 0x0020_3400 ~ 0x0020_37FF
UART3: address range 0x0020_B400 ~ 0x0020_B7FF
```

- Receive Data Register

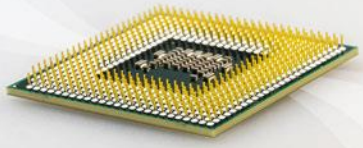
Index	Default	R/W	Bit	Name	Description
10			31:9	Reserved	
	0	R	8:0	RDR[8:0]	Receive Data value

```
char data = INW((0x0020B410));
```

- Transmit Data Register

Index	Default	R/W	Bit	Name	Description
0C			31:9	Reserved	
	0	W	8	TDR[8]	USART: Transmit USART Data value
	0	W	7:6	TDR[7:6]	USART: Transmit USART Data value.
	0	W	5:0	TDR[5:0]]	USART: Transmit USART Data value

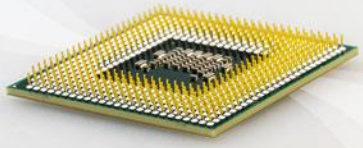
記憶體暫存器介紹



- UART Status Register

Index	Default	R/W	Bit	Name	Description
08			31:9	Reserved	
	0	R	8	IDLE	IDLE line detected 0: No Idle Line is detected 1: Idle Line is detected Clear by S/W write to 0
	0	R	7	BD	Break Detect 0: Break not detected 1: Break detected Clear by S/W write to 0
	1	R	6	TXE	Transmit data register empty 0: Data is not transferred to the shift register 1: Data is transferred to the shift register)
	0	R	5	TC	USART: Transmission complete 0: Transmission is not complete 1: Transmission is complete Clear by S/W write to 0 or Clear by H/W when transmit data register is not empty.
	0	R	4	RXNE	USART: Read data register not empty 0: Data is not received 1: Received data is ready to be read. Clear by S/W read Receive DATA Register or S/W write to 0
			3:0	Reserved	

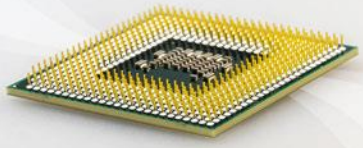
記憶體暫存器介紹



- UART Control Register

Index	Default	R/W	Bit	Name	Description
04			31:9	Reserved	
	0	R/W	8	IDLEIE	IDLE interrupt enable 0: Interrupt is inhibited 1: An UART interrupt is generated whenever IDLE=1
	0	R/W	7	BDIE	BD interrupt enable 0: Interrupt is inhibited 1: An UART interrupt is generated whenever BD=1
	0	R/W	6	TXEIE	TXE interrupt enable 0: Interrupt is inhibited 1: An UART interrupt is generated whenever TXE=1
	0	R/W	5	TCIE	Transmission complete interrupt enable 0: Interrupt is inhibited 1: An UART interrupt is generated whenever TC=1
	0	R/W	4	RXNEIE	RXNE interrupt enable 0: Interrupt is inhibited 1: An UART interrupt is generated whenever ORE=1 or RXNE=1
	0	R/W	3	EIE	Error Interrupt enable USART: 0: Interrupt is inhibited 1: An interrupt is generated whenever FER=1 or ORE=1 or NE=1.
			2:1	Reserved	
	0	R/W	0	PEIE	PE interrupt enable 0: Interrupt is inhibited 1: An UART interrupt is generated whenever PE=1

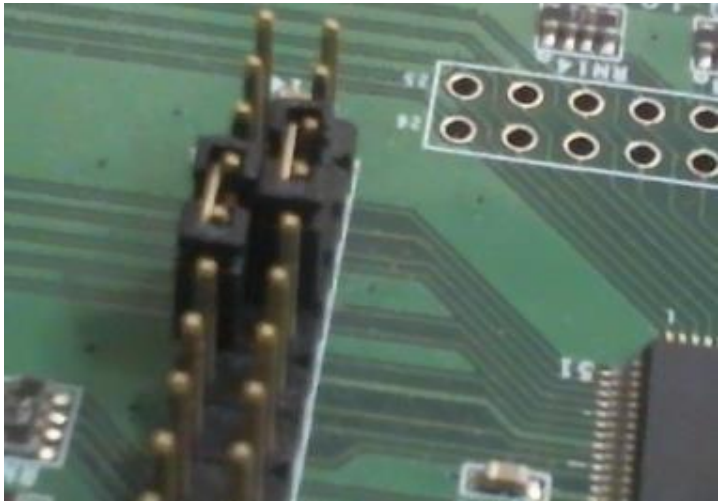
LAB10



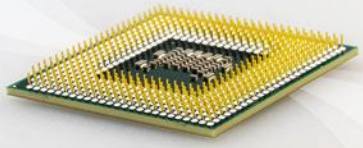
- UART中斷接收

  由電腦端Terminal傳送鍵盤的輸入，透過UART傳送至實驗版接收，並顯示在LCM上。

1. Backspace可刪除上一個字元。
2. 可連續輸入同一字元和連續刪除字元。
3. 最多輸入16個字元，不得超出LCD螢幕之外。



程式碼修改



```
void Init_Int(void)
{
    //Set UART Interrupt Enable
    OUTW(rINT0_IE1_ENABLE, );
}
```

```
void NDS32ATTR_ISR("not_nested;id=0") HW0_ISR(int vid, NDS32_CONTEXT * ptr)
{
    unsigned short int u16IntFlag1;
    u16IntFlag1 = (INW(rINT0_IE1_FLAG));
    if(u16IntFlag1 & 0x0008)  //UART Interrupt Flag Check
    {
        //Do your task
    }

}
```

```
void DRV_Printf(char *pFmt, U16 u16Val)
{
    U8 u8Buffer;

    //-----Pin configuration for UART3
    GPIO_PTC_FS = 0x0300;
    GPIO_PTC_PADINSEL = 0x0000;
    GPIO_PTC_DIR = 0xFEFF;
    GPIO_PTC_CFG = 0x0000;

    //UART Parameter
    OUTW(UART3_ADDR_BASE+0x00, UART_SET_CTL_PARA);

    //Set Baud rate with default sysclk
    OUTW(UART3_ADDR_BASE+0x14, ((BUARRATE_38400_MA

    OUTW(UART3_CR2, ); //Set UART CTL2
```