Virtual Memory Paging Simulator - Example Run

Example Inputs

Algorithm: LRU

Processes:

- PID 0, Size: 8192 bytes (2 pages)
- PID 1, Size: 12288 bytes (3 pages)

Accesses:

1. PID 0, Address 1000 -> P0-Pg0
2. PID 1, Address 4000 -> P1-Pg0
3. PID 1, Address 9000 -> P1-Pg2
4. PID 1, Address 11000 -> P1-Pg2 (already loaded)
5. PID 0, Address 5000 -> P0-Pg1
6. PID 1, Address 4000 -> P1-Pg0 (may trigger fault or not)

Expected: 4 frames total; LRU may trigger replacement

Gantt Chart - Frame State Over Time