

Mosfet Models: EKV2.6 and Level 1

COT 6905 Project Report

Circuit Design with EKV - Florida Atlantic University

Brandon S. Ramos; ramosb2022@fau.edu

Contents

1	Introduction	3
1.1	Summary of Topic	3
1.2	What did you do	4
2	Model Design	4
2.1	Level 1 Model	5
2.2	EKV2.6 Model	5
3	Implementation with Results	6
4	Discussion	24
5	Conclusion	25
5.1	Lessons learned	25
5.2	Knowing what you know now, would you make any changes to the project? . . .	25
5.3	Future work – what would you do to continue the project?	26
	End Table of Contents Page	

1 Introduction

In all of the inventions ever created within the field of computing, the transistor is arguably one of the more important allowing circuits to achieve such small form factors. Practically all modern electronics use the transistor as it is the fundamental component to creating logic gates and operational amplifiers. Not only when creating the layout on the device level can we design transistors, but we can take advantage of metal layers, poly layers and wells to create different passive components regularly seen in circuits. Creating resistors out of polysilicon or n-wells and capacitors out of a single transistor. It is clear that our world today would not be the same without the transistor.

With the increasing number of components packed into a single integrated structure, often times the thought of how these devices are tested and designed to be reliable goes overlooked. Although testing is best done with the physical circuit, it is not ideal considering the cost of sending a design to production and the process taking a better part of the year to be fabricated. Instead, modeling these designs using computer simulation has saved many resources when it comes to testing designs. But simulations are just that, a representation of how the circuit will react before physically creating the circuit with real components. These simulations use mathematical expressions to represent physical properties of transistors and other fundamental components. As simulations use man made concepts to define real world properties, we begin to see a trade-off between using a simplistic model versus an accurate simulation of the circuit.

This paper will serve as the final report for COT-6905 (Circuit Design with EKV) for the Spring 2024 semester. Although the report will be formatted to connect all of the student's implementations and notes, not all of the discussed topics will be in-depth as some areas were reviewed more than implemented. In this directed independent study project, the student is given the opportunity to explore MOSFET Compact Models using simulation software. With different level MOSFET models, the student can build simple circuits and experiment with different characteristics of each model.

1.1 Summary of Topic

The class Circuit Design with EKV was constructed to work with the student's current knowledge of analog design and build off of it. A good amount of the work replicated with the EKV model was created for Dr. Roth's undergraduate CMOS Amplifiers course which focuses around the Level 1 model. Creating weekly meetings with the professor and student to discuss relevant topics in the course and presenting deliverables, the student focused around Razavi's textbook [1] and the amplifier circuit design. First we will discuss the Level 1 MOSFET Model and why it is popular within academia. From the simplest model, we will discuss how other factors come into play with higher level models before jumping into the EKV2.6 Model. After reviewing the different models, we will look into how to build them in Advanced Design Systems [2] (ADS) and simulate their characteristics. Then we get into building simple circuits with the model and comparing the different models in some of the designs. Many of the circuits built will be in the area of amplifiers but the EKV Model can be used to simulate logic level designs as well. However in those designs the user will need to specify timing determine logic level tolerances. Overall, we will want to see if the EKV Model used from a third party can show the different characteristics of real transistors from a Verilog-A file off of EPFL's [3] website. Although there are more advanced technology sizes out there for the EKV even shown in EPFL's website, we will use the half micron design as the Level 1 Model will only be roughly accurate down to half a micron.

1.2 What did you do

This report is organized as to go over the course objectives sequentially. Each week, Dr. Roth and the student would meet to discuss the work for the week and to review what was done the week before. There were 11 weeks total where some weeks focused on the same topics. First was to find a EKV2.6 Compact Model to use within ADS and be able to use it to create a simple circuit. Later the student designed an inverter to show the functionality of the EKV Compact Model in ADS. Next the Level 1 Model was created, this model is built into ADS and all you will need to do is to add the parameters. The parameters used will be discussed in the Model Design 2. After the model was created for the EKV, the student reviewed the Common Source Amplifier with a resistive load, then later using a PMOS as the load. The next week was looking into Transient Analysis and long/short channel effects. This ended with a review on sub-threshold conduction effects. Then we move back to the CS Amplifier and redesign by scaling the transistor. The student goes over the Miller Effect, attempts to use Harmonic Balance and creating other designs provided from the first homework for the CMOS Amplifiers course. We go from $2\mu m$ to $0.5\mu m$ designs and then started to use Level 1 Model for comparisons. The student reviews voltage swings for transient input signals, current mirrors and differential amplifiers. Then we get into OTAs but not in-depth, as well as the Gilbert Cell is reviewed. With a continuation of some information on previous weeks, there is a review on differential amplifiers and a deep dive into the current equations listed from the course book [1]. Finally, ending off with total input testing on a differential amplifier which will include differential and transient mode analysis. There is some review of yield analysis but not applied to the EKV Model.

2 Model Design

To get started with simulating the transistor, we will need to create the model within ADS. This is quite simple and can be brought into the application many ways. For instance, the Level 1 MOSFET Model is built within ADS and only requires the engineer to grab a model card either by measurements from a manufacturer's datasheet or one provided by another source. As gathering measurements and using them to extract parameters for the model card is not necessary in this project, we will instead use a model card provided in Razavi's Textbook [1]. For the Level 1 Model, there are not many parameters to be aware of when using the model in ADS. However, if interested the textbook does go over each parameter and its use.

When the Level 1 Model is completed, we will create the EKV2.6 Model which will be more involved as the simulation code will need to be copied from another source. The EKV Model will have more parameters than the Level 1 as it will account for other effects either not seen in larger channel lengths or not included for simplicity. Since the EKV is not in ADS, we will have to create 3 files for simulating the transistor. First, we will use a Verilog-A file that will explain the characteristics of the transistor when given certain inputs at its base, gate, source and drain. On the same object, we create a symbol which can be either a PMOS or NMOS device which also needs to be specified in the code. Lastly, a schematic of the model needs to specify the number of connections should be expected for the device. This does not have to look pretty but will mainly require naming of the pins to the Verilog-A code.

2.1 Level 1 Model

This will be only a review as there is a lot of information out there for how to use the Level 1 Model in ADS. In the schematic, the components' palette will have Devices-MOS listed as an option. There are Level 1 Models as well as Level 2, Level 3 and even BSIM Models. Note that instances of the component will need a model to reference the characteristics. When you add the Level 1 Model to the schematic, you'll notice that there are a lot of different parameters to add values to. For simplicity, we will only look at a few of these parameters. In Razavi's Analog CMOS Textbook, Table 2.1 shown below has the cards for both PMOS and NMOS devices. Once the model is updated with the parameter set, you can reference instances using the model name.

Level 1 SPICE models for NMOS and PMOS devices.			
NMOS Model			
LEVEL=1	VTO=0.7	GAMMA=0.45	PHI=0.9
NSUB=9E+14	LD=0.08E-6	U0=350	LAMBDA=0.1
TOX=9E-9	PB=0.9	CJ=0.56E-3	CJSW=0.35E-11
MJ=0.5	MJSW=0.2	CGDO=0.4E-9	JS=1.0E-8
PMOS Model			
LEVEL=1	VTO=-0.8	GAMMA=0.4	PHI=0.8
NSUB=5E+14	LD=0.09E-6	U0=100	LAMBDA=0.2
TOX=9E-9	PB=0.9	CJ=0.94E-3	CJSW=0.32E-11
MJ=0.5	MJSW=0.3	CGDO=0.3E-9	JS=0.5E-8

2.2 EKV2.6 Model

The next model we need to create is the EKV Model. As this is not a step that is as easy as adding a parameter set, we will have to be creative with how we add the model. I created an in-depth tutorial on creating the EKV Models [4] using various sources, in this report we will briefly go over the tutorial and the information within. As the first week of the semester was used to find a way to simulate the EKV model within ADS, there was not a lot of information on how this was possible. There were various papers that described the model itself and simulation on open source software, but nothing really for Advanced Design System. I was able to find one paper on Free Open Source Software which put me in the direction of a GitHub repo [5] that contained the Verilog-A code for the EKV2.6 Model. From here, I was able to review the Verilog-A code and use this within ADS to simulate designs for the EKV Model. Although it is not mentioned where the values for the parameters were obtained, EPFL has some example parameter sets to go through. Although there was shorter channel technology, I chose to use the $0.5\mu m$ parameter set. This was due to many reasons including the least complex parameter set with less parameters and complexity in setting up the model using the values. I also noticed that the examples provided were in different formats that either had to be converted or added in manually. ADS does have a built-in method in converting SPICE parameters, I ended up pasting the parameter set values within the Verilog-A code instead. I found there to be issues with trying to convert the parameter sets and even with the Verilog-A code there were issues not setting the MOSFET type manually. There is a better way than manually modifying these values but for the time that I had in the semester, I did not want to waste time with setting up the model. Once the models were set up as shown in my tutorial, I then go ahead and move through the simulation process. By showing a quick test for the transistor model through

simulations, I can review the I_D vs V_{DS} curve for different values of V_{GS} for both PMOS and NMOS Models. Running the simulation, it was clear that the values were correctly being passed through the Verilog-A code and producing the expected output. Therefore the Level 1 and EKV2.6 Models were ready to be used for the semester in simple circuit design.

3 Implementation with Results

After the first week of researching fundamental material on the EKV Model and introducing myself to the topic, I implemented the EKV Model in ADS to use on different amplifier circuits. Before creating these, I went ahead and ran a simulation on both the NMOS and PMOS EKV transistors to show their I-V curve. Figure 1 is the schematic in which I tested the EKV NMOS Model in ADS. The EKV is supported down to $0.5\mu m$ but does not appear to have any upper limit from the creators. The voltage range is $|V_{gb}| < 3.3V$, $|V_{db}| < 3.3V$, $|V_{sb}| < 2V$ which $3.3V$ is typically used in simulation as the highest voltage. By sweeping V_{DS} and V_{GS} , we can obtain the I-V curve shown in Figure 2.

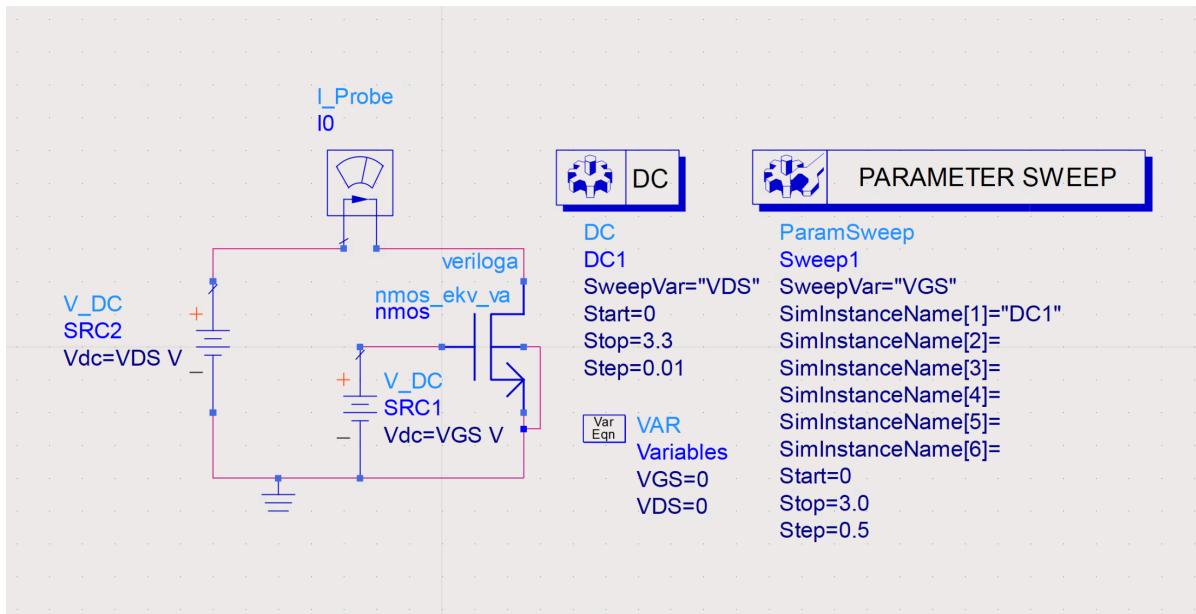


Figure 1: NMOS EKV Simulation Schematic

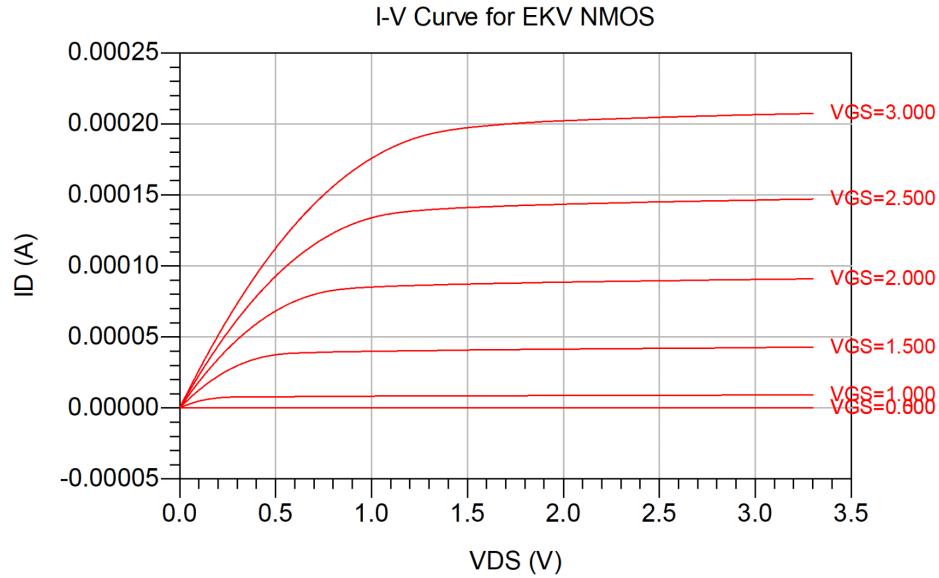


Figure 2: NMOS EKV I-V Simulation Curves

The PMOS design was very similar in schematic and the curves to the NMOS above. Figure 3 shows the PMOS testing schematic where the ranges for V_{DS} and V_{GS} are negative. Although the mobility for the PMOS is half that of the NMOS, later my values for the PMOS channel width will be double to compensate for timing purposes. Figure 4 will show the I-V curve for the PMOS.

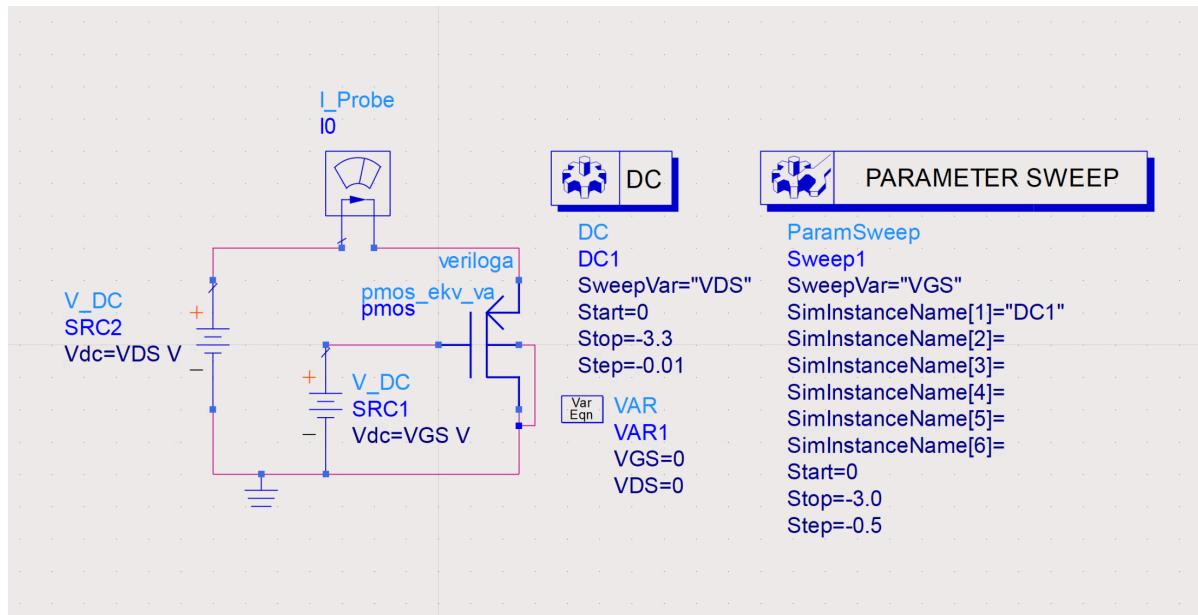


Figure 3: PMOS EKV Simulation Schematic

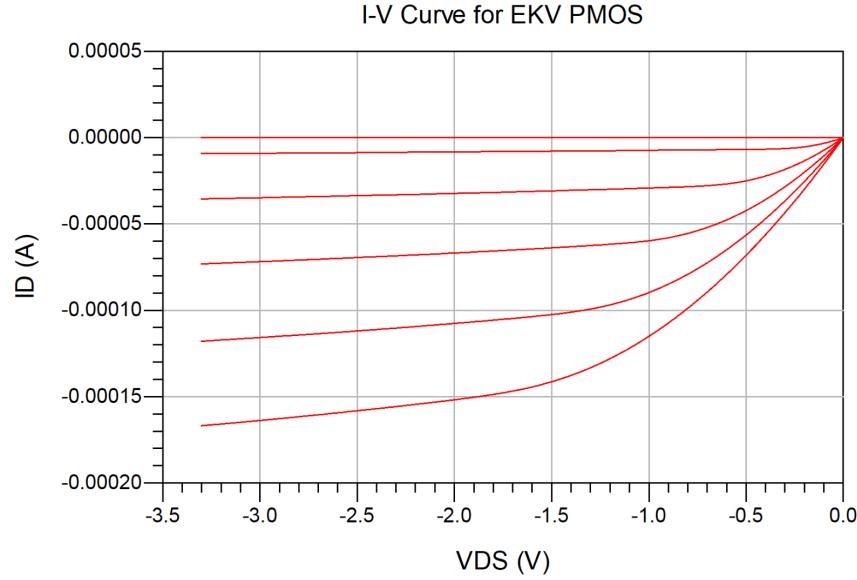


Figure 4: PMOS EKV I-V Simulation Curves

Next is the LEVEL 1 Model that was simulated to produce its I-V curves. Figure 5 is the schematic created to test the model within ADS. This schematic was the same and by creating the Model, adding the model card and simulating, Figure 6 shows the characteristics of the simplistic model.

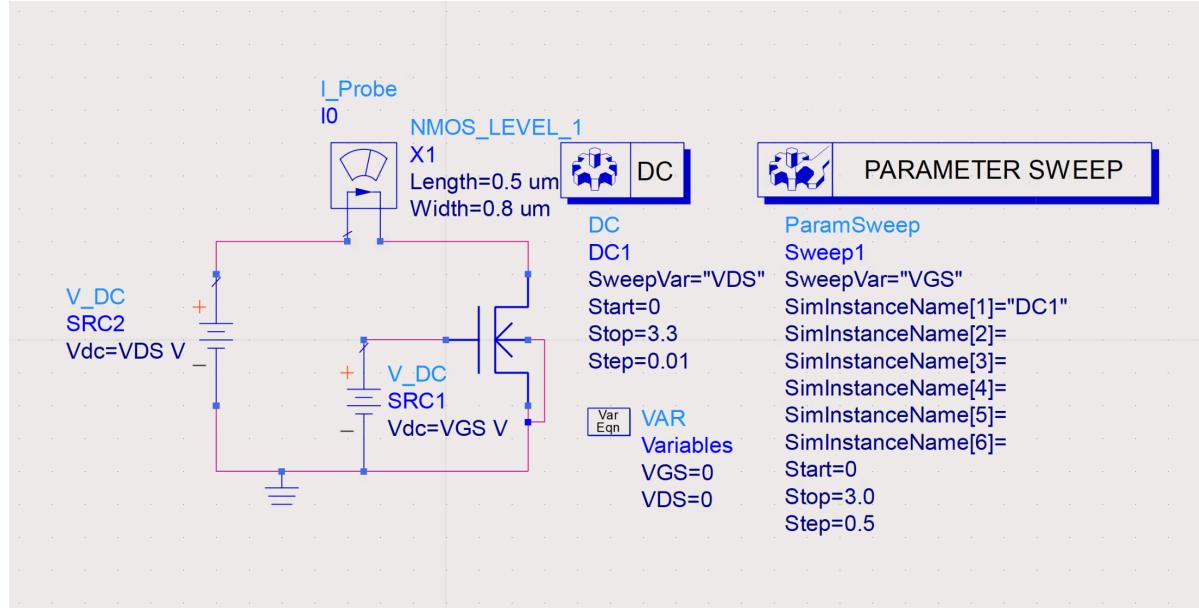


Figure 5: NMOS LEVEL 1 Simulation Schematic

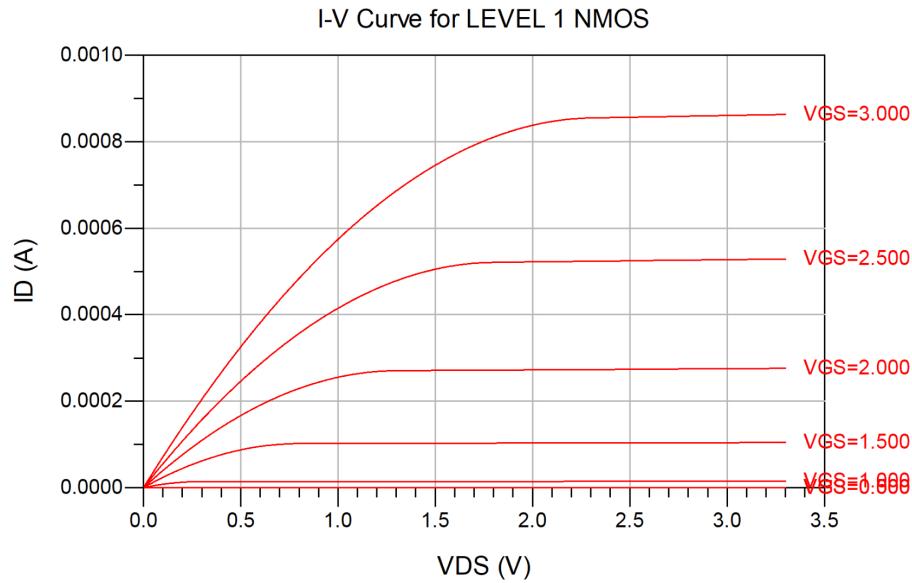


Figure 6: NMOS LEVEL 1 I-V Simulation Curves

Next is the LEVEL 1 PMOS simulation where Figure 7 shows the template schematic and Figure 8 is the LEVEL 1 PMOS characteristic curve.

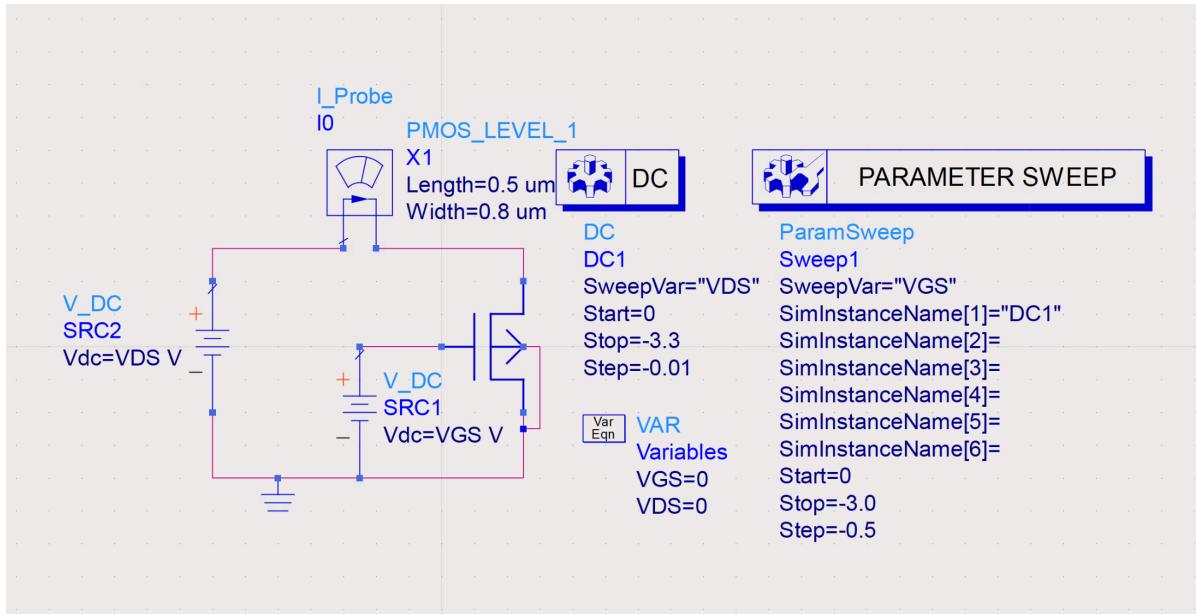


Figure 7: PMOS LEVEL 1 Simulation Schematic

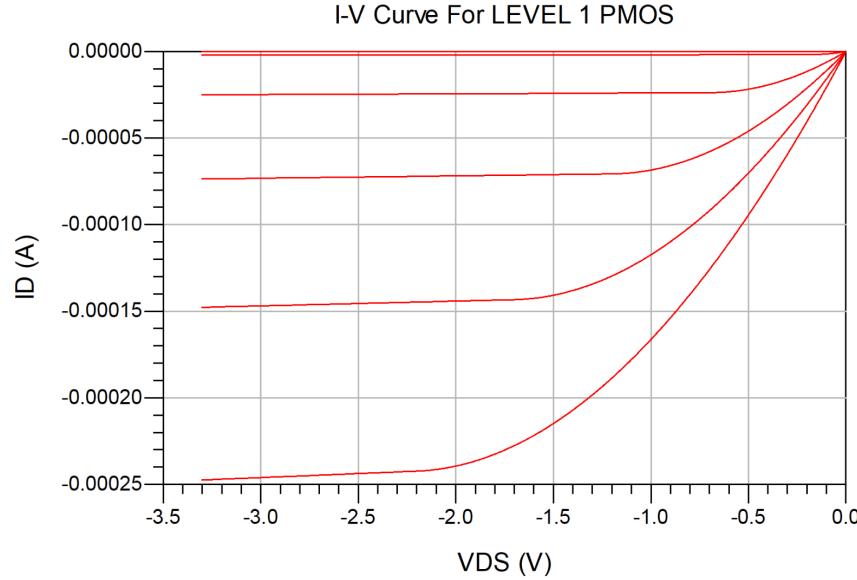


Figure 8: PMOS LEVEL 1 I-V Simulation Curves

Here we have the CMOS Inverter where we sweep the gate voltage of the 2 transistors from Ground to VDD. Figure 9 shows the use of the 2 EKV transistors where the input is VGS and the output is the intermediary of the 2 networks. Running the simulation, Figure 10 shows the inverter input/output curve.

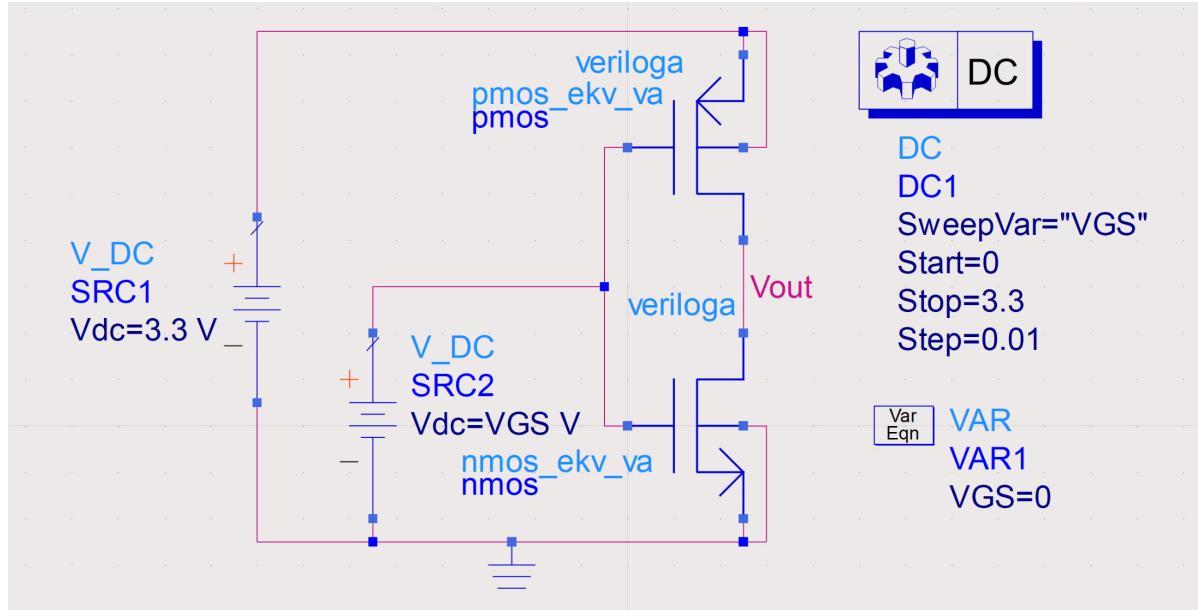
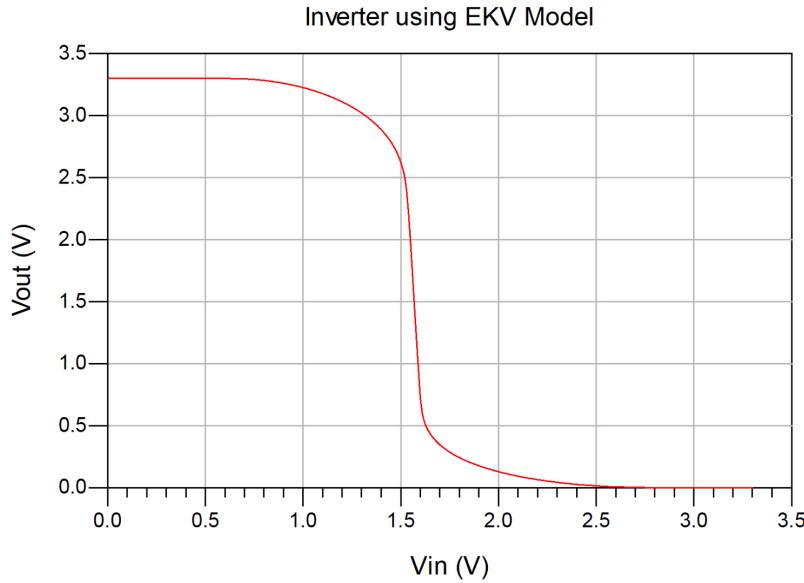


Figure 9: EKV Inverter Schematic

Figure 10: EKV Inverter V_{out} vs V_{in}

Next up is the Common Source Amplifier. Figure 11 shows the schematic where we use an NMOS transistor connected at the drain with a resistor. The value 2.5 kOhms was chosen arbitrarily while the gate voltage and channel width were tuned to achieve a high gain. By conducting an AC sweep, we can review the overall bandwidth of the circuit with a gain of 15dB shown in Figure 12.

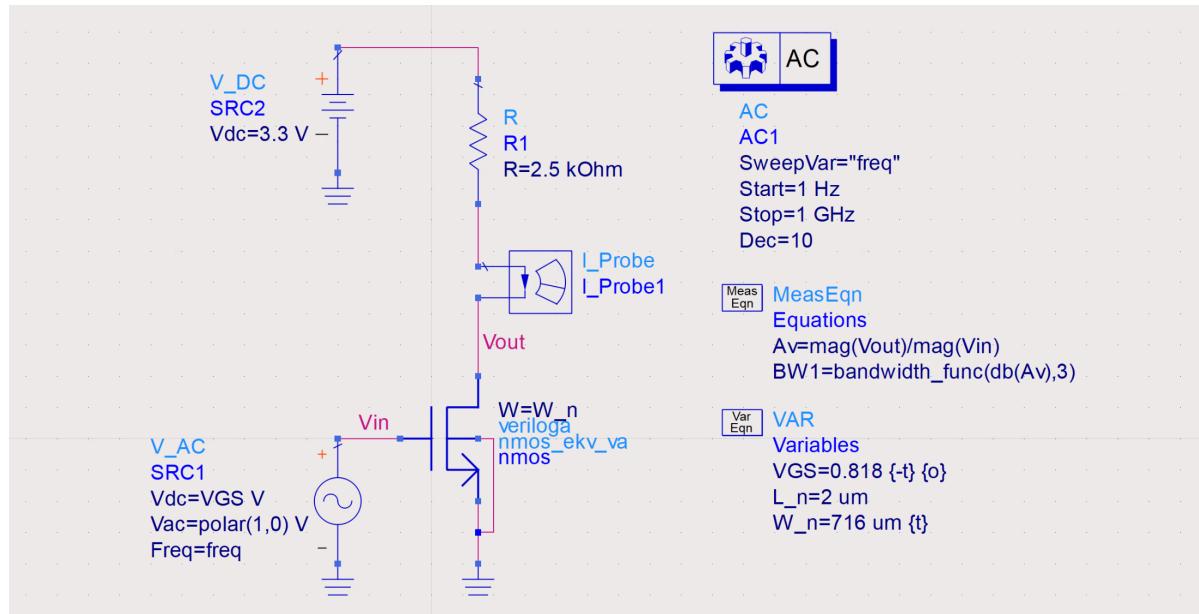


Figure 11: Common Source Amplifier with Resistive Load

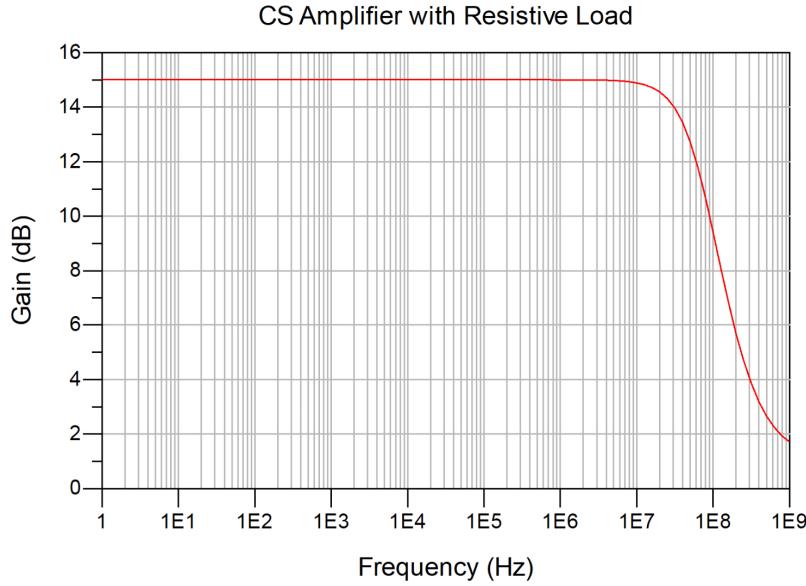


Figure 12: Gain of 15dB yields a Bandwidth of 8.034E7

Here is where we took a look at simulation requirements as setting a delay for Rise/Fall times is important. Not only do real ICs have delays when transitioning to different logic levels, but also simulated circuits must include this time otherwise high frequencies can spike the output of the circuit. Figure 13 shows the schematic where we use the inverter from before and instead of attaching a simple DC voltage to the gates, we now use a pulse wave. As many ICs have delays in the nanoseconds, we set the scale of the pulse to be in nanoseconds. First, we produce an output where the input signal does not have a delay between states. Figure 14 is a good example where the edges of the output square wave produce high voltage spikes above the max 3.3V. This can be reduced by capacitors if an input signal realistically could produce no delay between transitions, however instead in simulation we can change the delay. Figure 15 is the generated simulation where the Rise/Fall delay is increased from a non-zero value. In this case, we use 0.3ns which significantly reduces the voltage spike between the transition of logic states. Some things to keep into consideration when dealing with transition times between logic levels. The capacitance of a transistor can reduce the switching time ultimately playing a big role in critical paths when determining the fastest clock speed. The mobility of holes is twice as slow as its counterpart and must be compensate for a longer channel width in PMOS so that switching times are equivalent from high to low. Lastly, the engineer must determine what is an acceptable T_high and T_low voltage when determining logic levels.

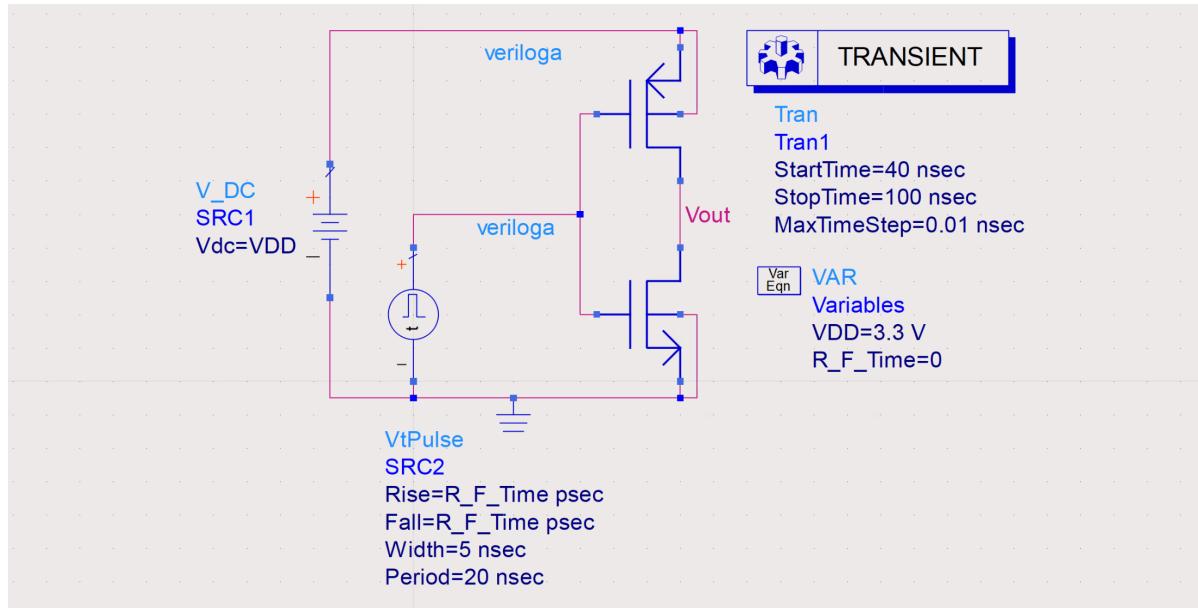


Figure 13: Square Wave Generator Schematic

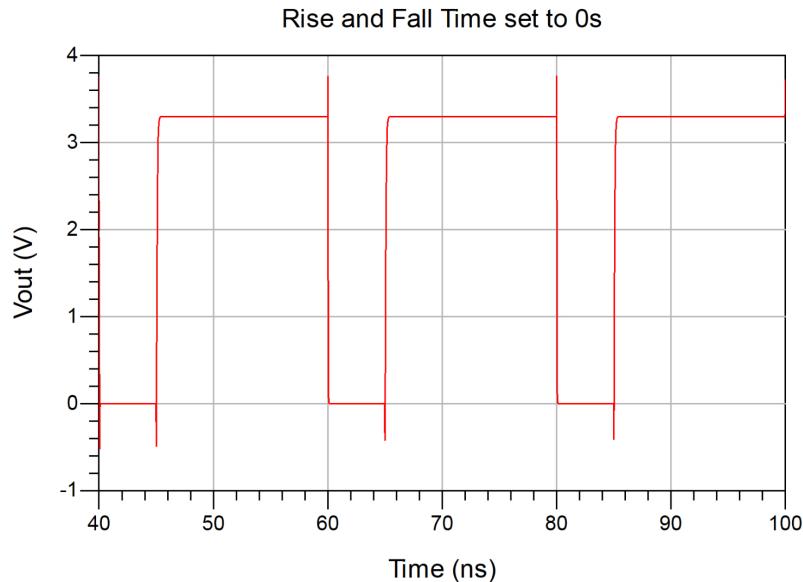


Figure 14: No Rise/Fall Delay

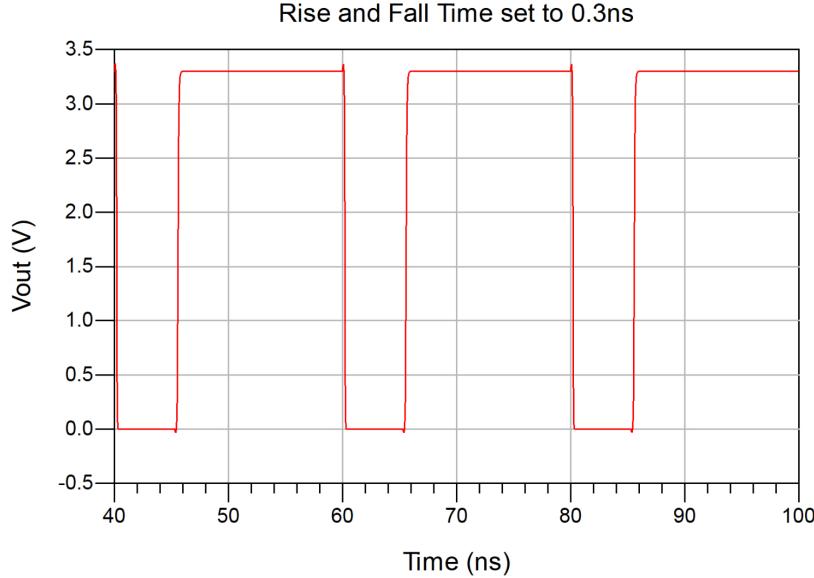


Figure 15: 0.3ns Rise/Fall Delay

From here we get into problems discussed in the CMOS Amplifiers coursework. These next couple of figures will be for Homework 1 modified to be replicated with the EKV Model. Showing in Figure 16 is the schematic for both EKV and LEVEL 1 where we design a CS Amplifier with a PMOS Current Source Load attached. By achieving a gain of $A_V = -69$ we assume that the input is sufficiently low as well as no resistive load. Figure 17 displays the results after tuning both models. Although the gain was not sufficient in either models after the first time around, we did get good bandwidth in both results.

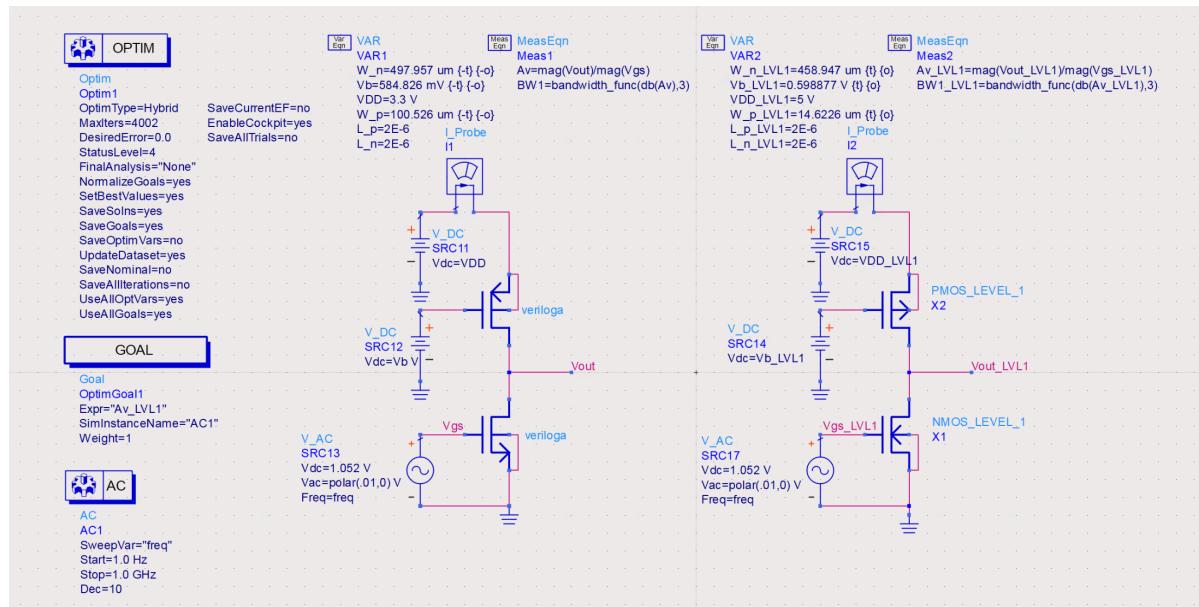


Figure 16: CS Amplifier with PMOS Current Source Load

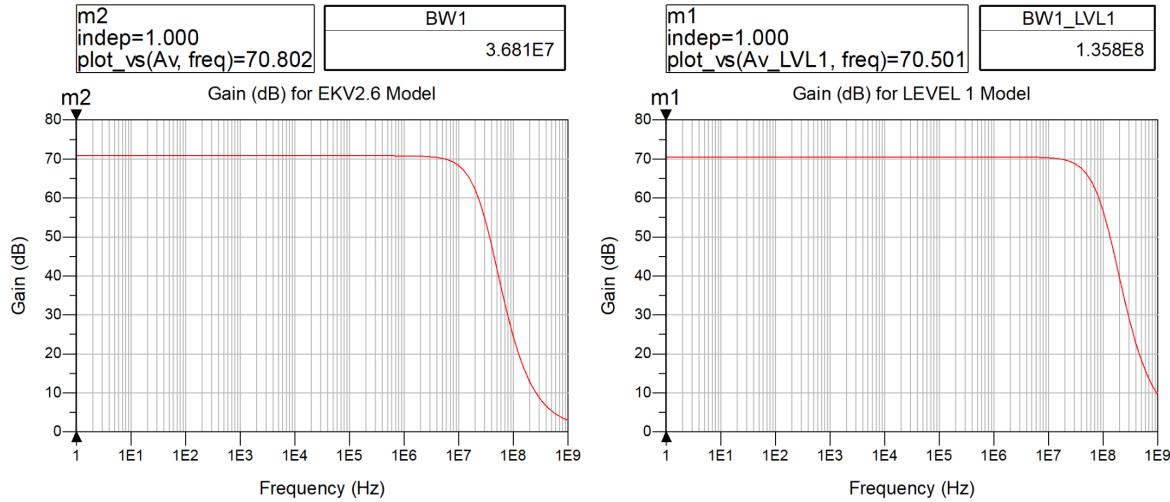


Figure 17: CS Amplifier EKV vs LEVEL 1

Next results came from question 2.3 from Homework 1 where we design a CS Amp. with a PMOS Diode-Connected Load for a gain of $A_V = -15$. Figure 18 shows the schematic used for both EKV and LEVEL 1 where the Optimizer was used to achieve a high gain. Figure 19 shows the simulated results where the goal was achieved for the gain.

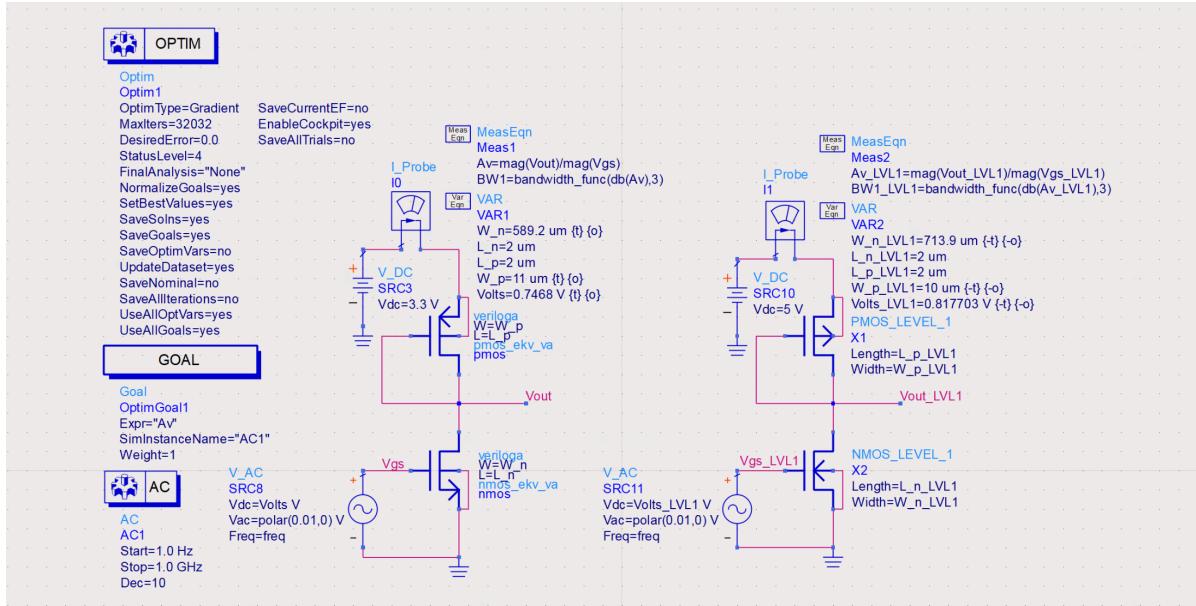


Figure 18: CS Amp. with PMOS Diode-Connected Load Schematic

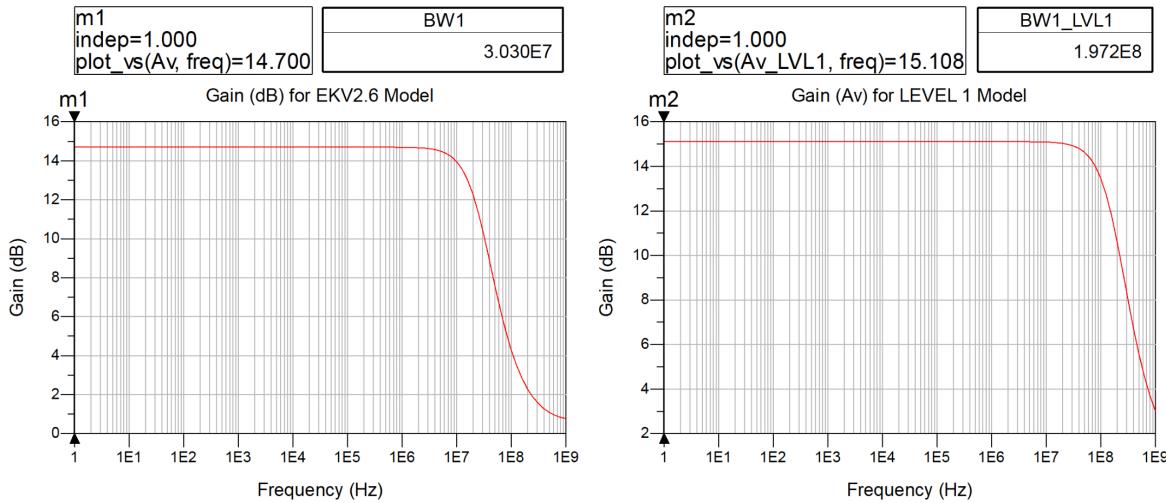


Figure 19: CS Amp. with PMOS Diode-Connected Load Results

Next is from question 2.4 where in a CS amplifier with current source load, there is no way to add a resistive load R_L between the drains and ground. The amplifier will stop working if such a load is connected. You need a buffer: A Source Follower Amplifier can be connected to the CS amplifier, and it can feed R_L . The overall voltage gain should be $A_V = -69$. Figure 20 shows both EKV and LEVEL 1 schematics where the CS Amplifier is used on a buffer stage to achieve the desired gain. Figure 21 shows the product of the buffer stage and CS Amp. stage is the total gain of the circuit. As the buffer stage will have a gain of less than unity, we compensate for this in the CS stage by achieving a higher gain.

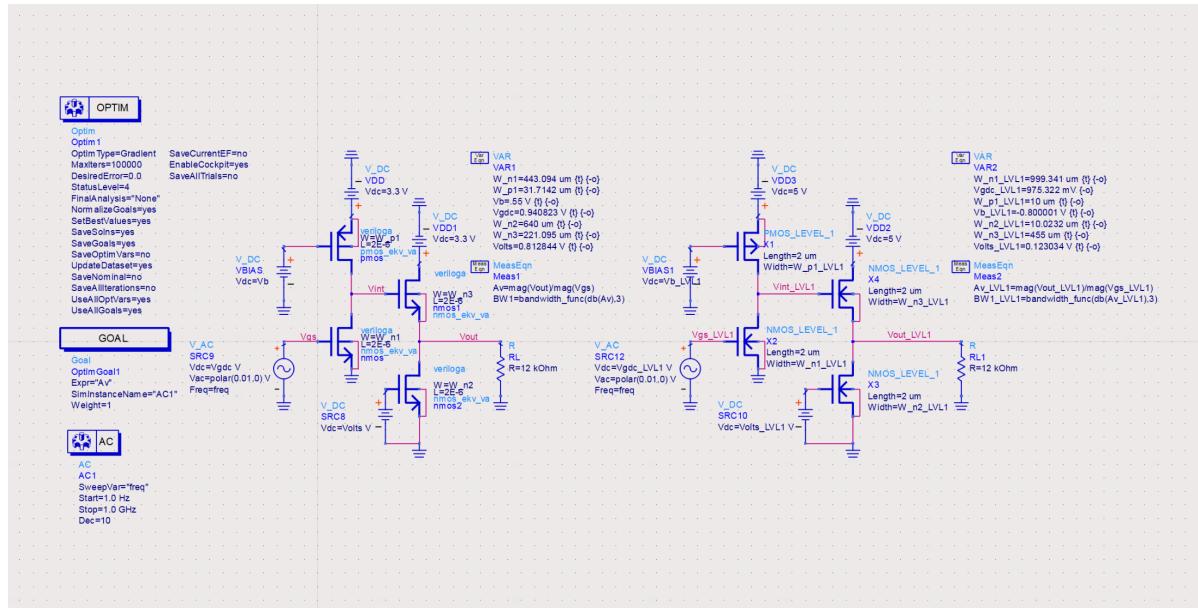


Figure 20: CS Amp. with Buffer Stage

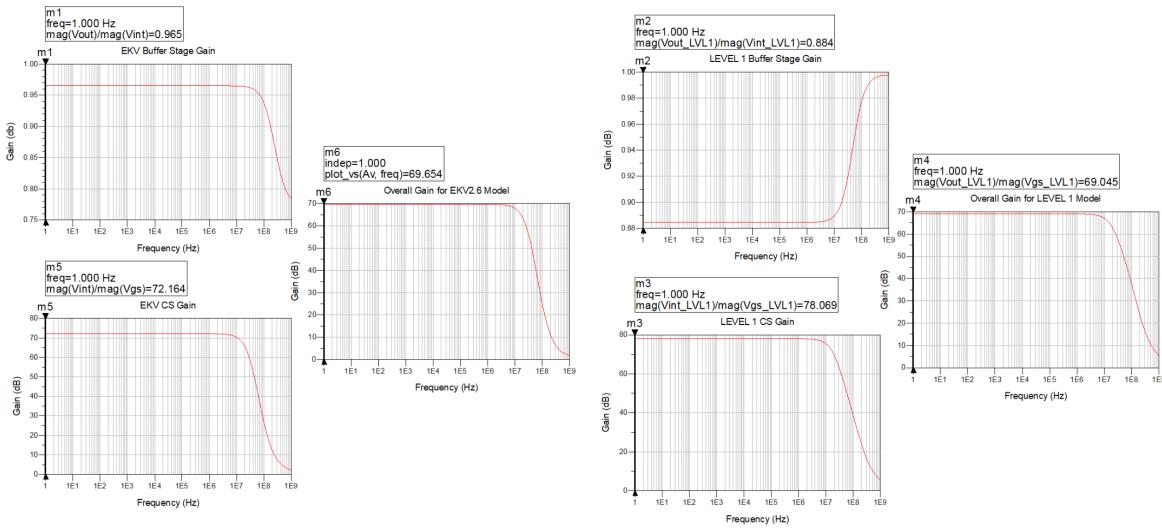


Figure 21: CS Amp. with Buffer Stage Results

For Figure 22 A voltage signal source has an internal resistance of $R_{sig} = 50\Omega$. It connects to a CG amplifier with a load via a coupling capacitor. By using the optimizer in ADS, we design a gain of $A_V = 25$ and $R_{in} = 50\Omega$. The Harmonic Balance tool was attempted with this design but I ran into several divide by zero error and was not able to get this working. Figure 23 will show the results for this design. Note that the EKV went through 2 different channel lengths and LEVEL1 only had the one simulated channel length used in all other simulations. In all results I was able to achieve relatively close values to the goals set in the optimizer.

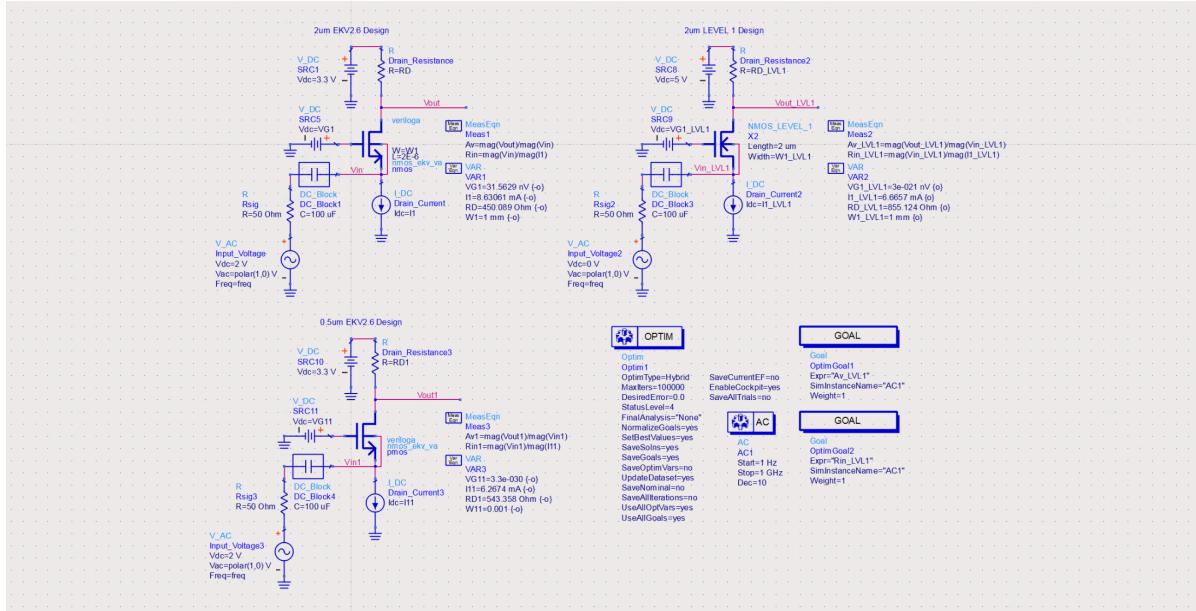


Figure 22: Problem 3.1 Schematic

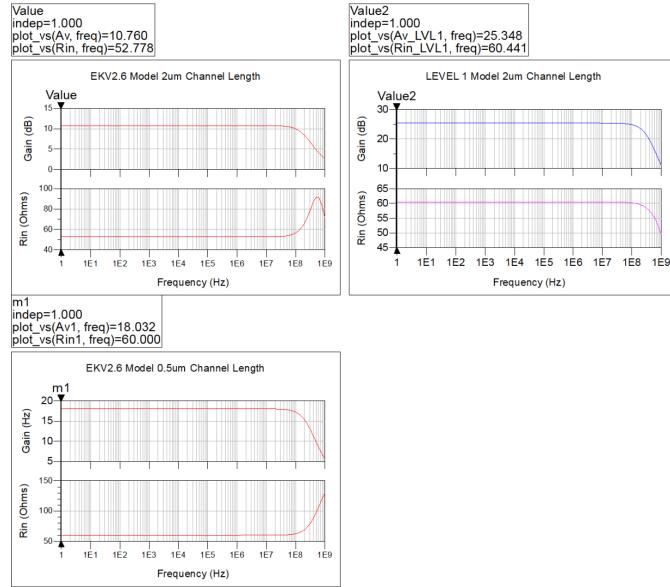


Figure 23: Problem 3.1 Results

Last problem from the homework set was to consider a cascode amplifier consisting of two stacked NMOS transistors being the driving stage feeding into a single PMOS current source load. Using only the ADS optimizer in this design and having six design parameters: VG of each MOSFET and W of each MOSFET, Figure 24 shows the EKV and LEVEL 1 design using the ADS optimizer. Figure 23 shows the results were great with the gain in all designs around 100dB.

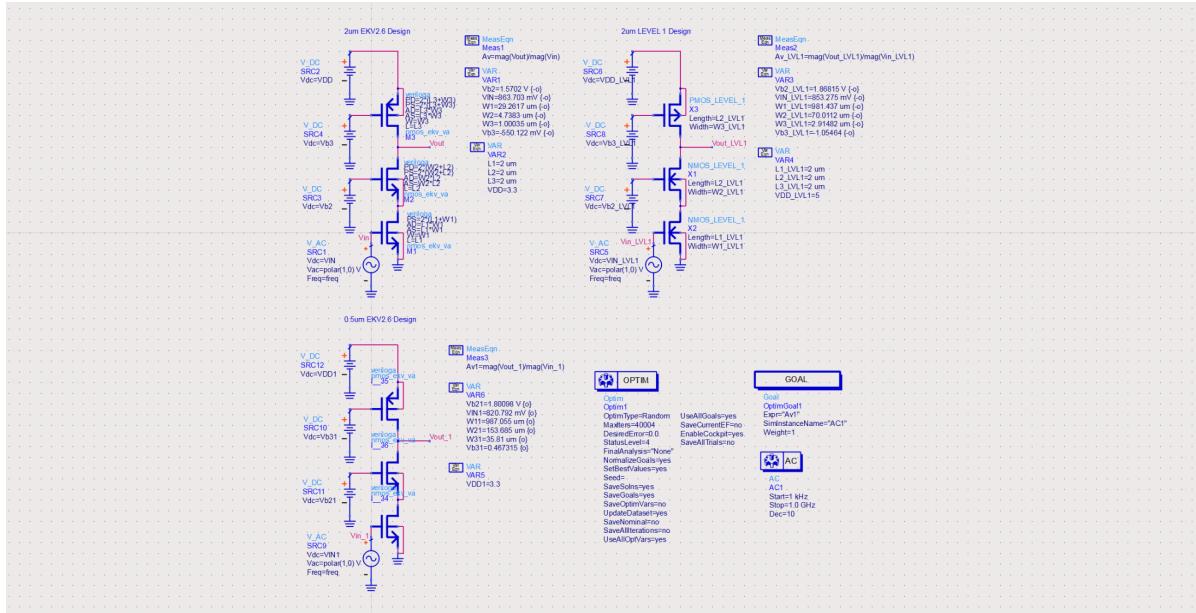


Figure 24: Cascode amplifier schematic

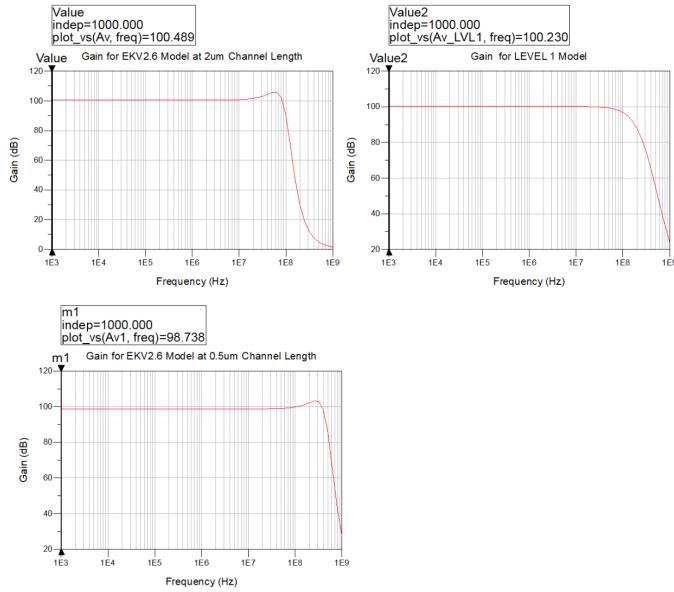


Figure 25: Cascode amplifier results

Below is the Gilbert Cell which can be used as a signal multiplier shown in Figure 26. Although this was simulated, I was not able to add the simulation results due to some challenges in design.

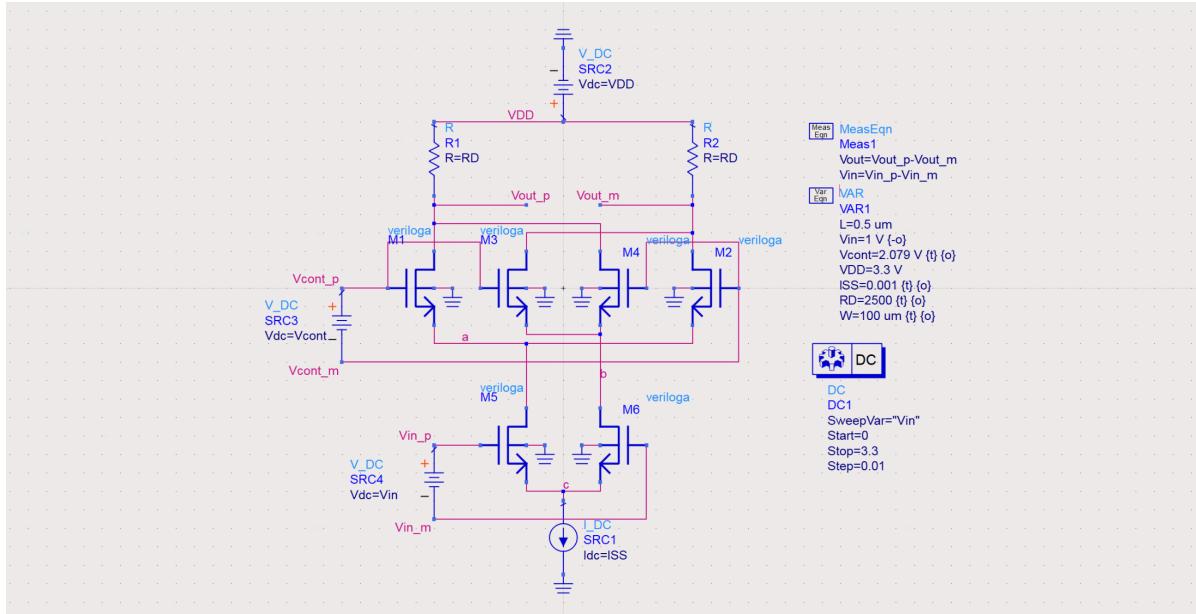


Figure 26: Gilbert Cell design using EKV

Finally is the Differential amplifier, this final design will go through testing the Differential Mode, Common Mode and Total Input testing. Figure 27 takes an AC sweep where Figure 28 is the results from the Differential Mode Gain.

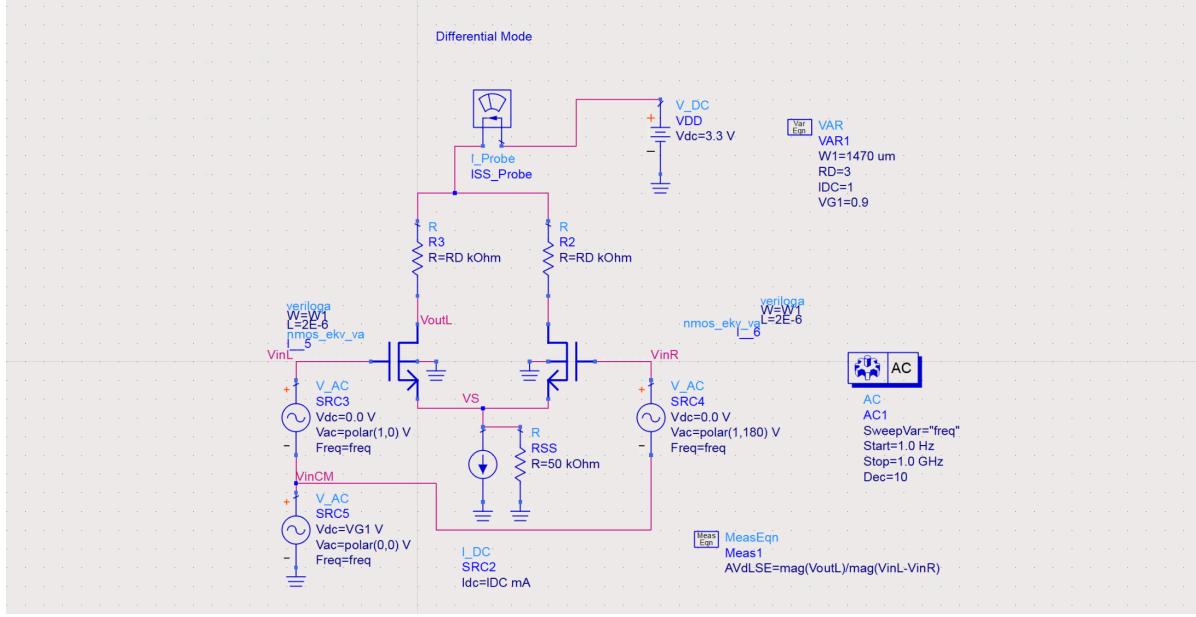


Figure 27: Differential Amplifier Differential Mode Schematic

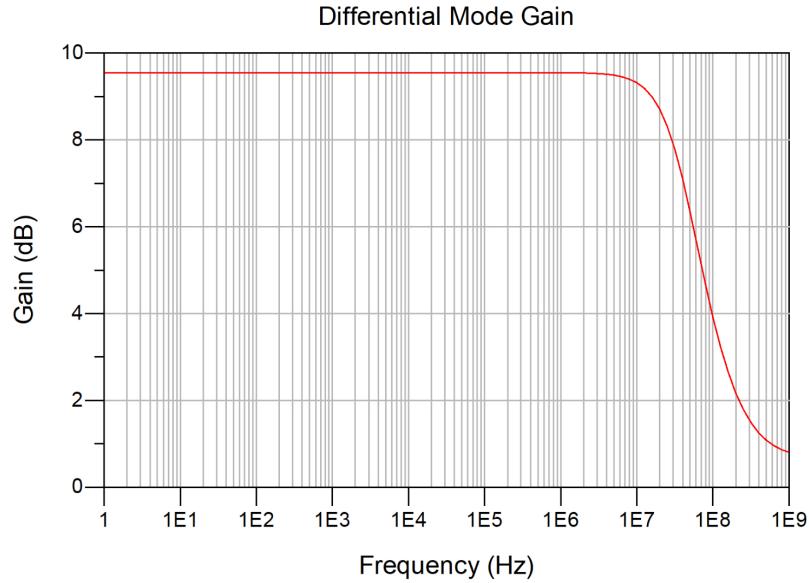


Figure 28: Differential Amplifier Differential Mode Results

Next is the transient analysis shown in Figure 29 where Figure 30 produces the simulation results.

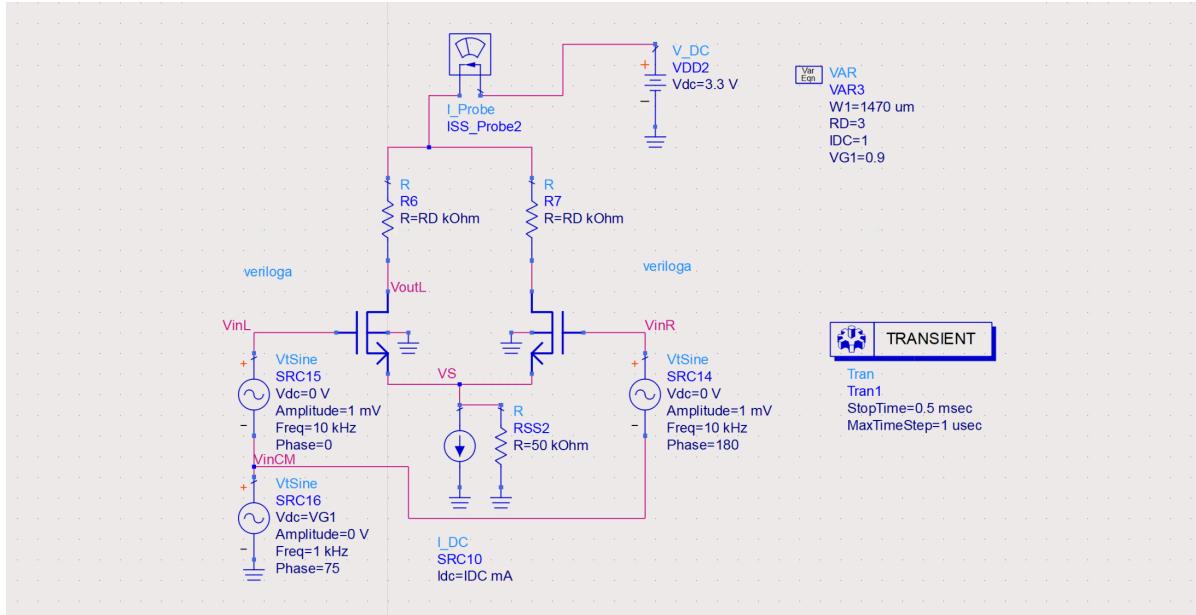


Figure 29: Transient Simulation Differential Mode Schematic

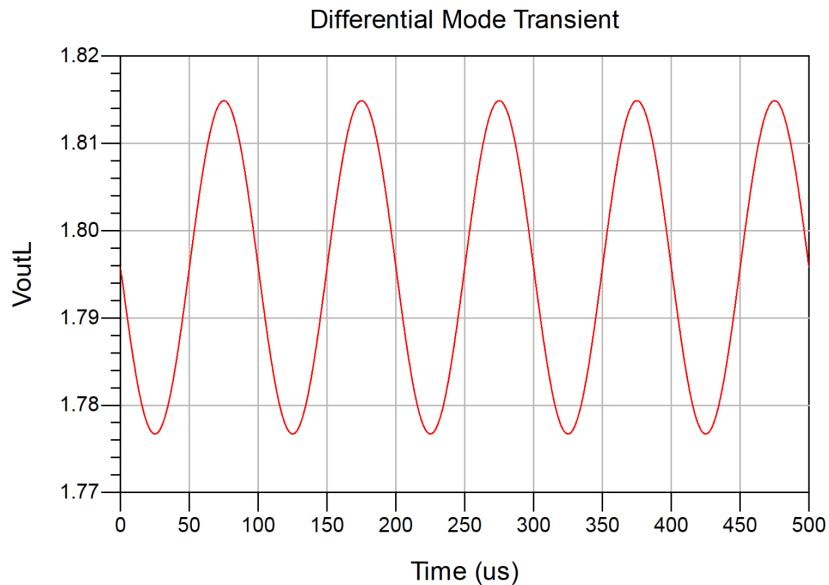


Figure 30: Transient Simulation Differential Mode Results

The Common Mode testing consist of shorting the 2 signals shown in Figure 31. Figure 32 is the AC sweep showing the gain of the design.

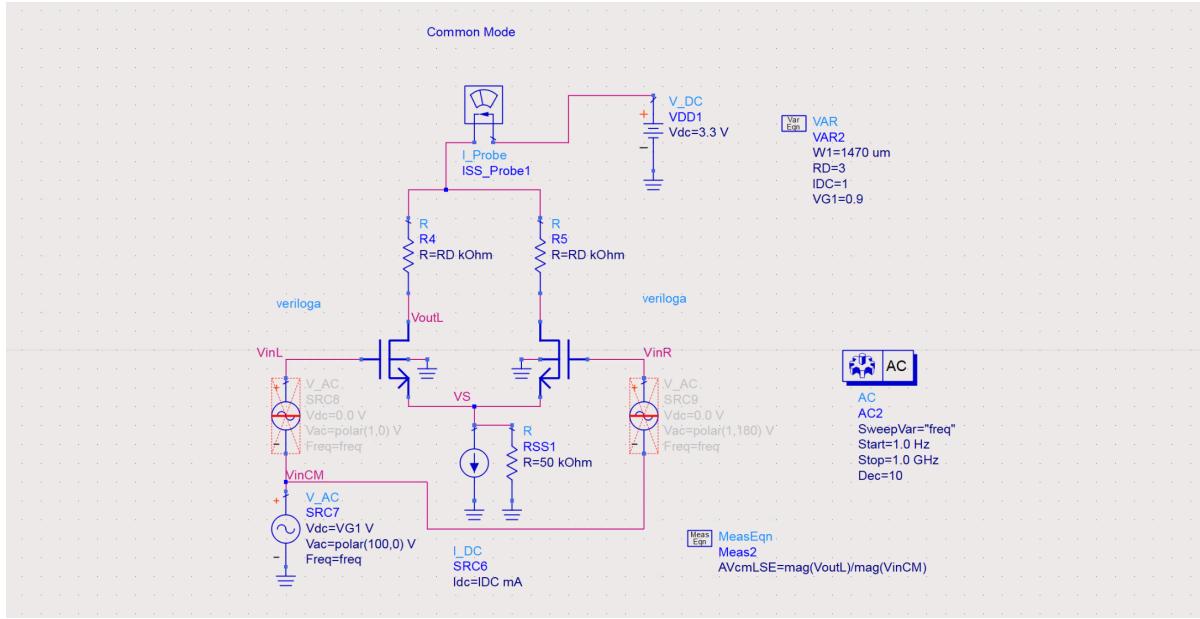


Figure 31: Differential Amplifier Common Mode Schematic

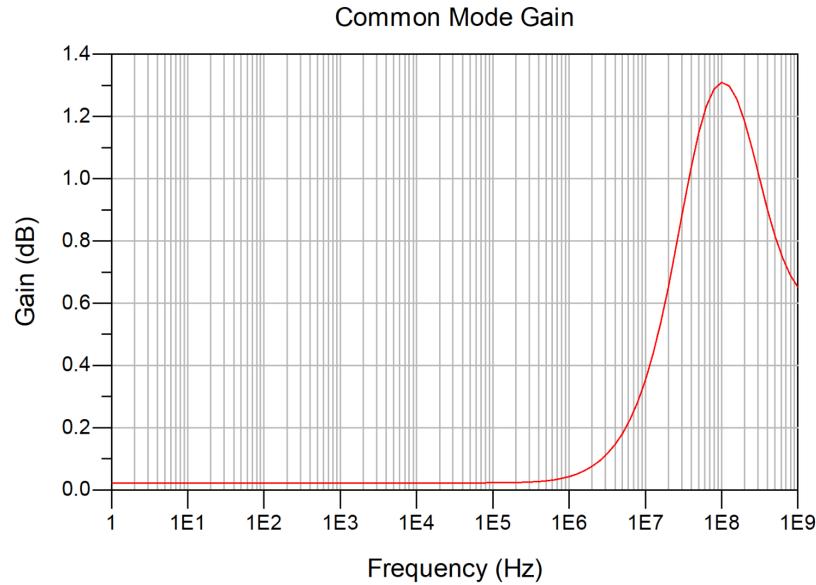


Figure 32: Differential Amplifier Common Mode Results

Figure 33 shows the Common Mode transient schematic where Figure 34 is the result.

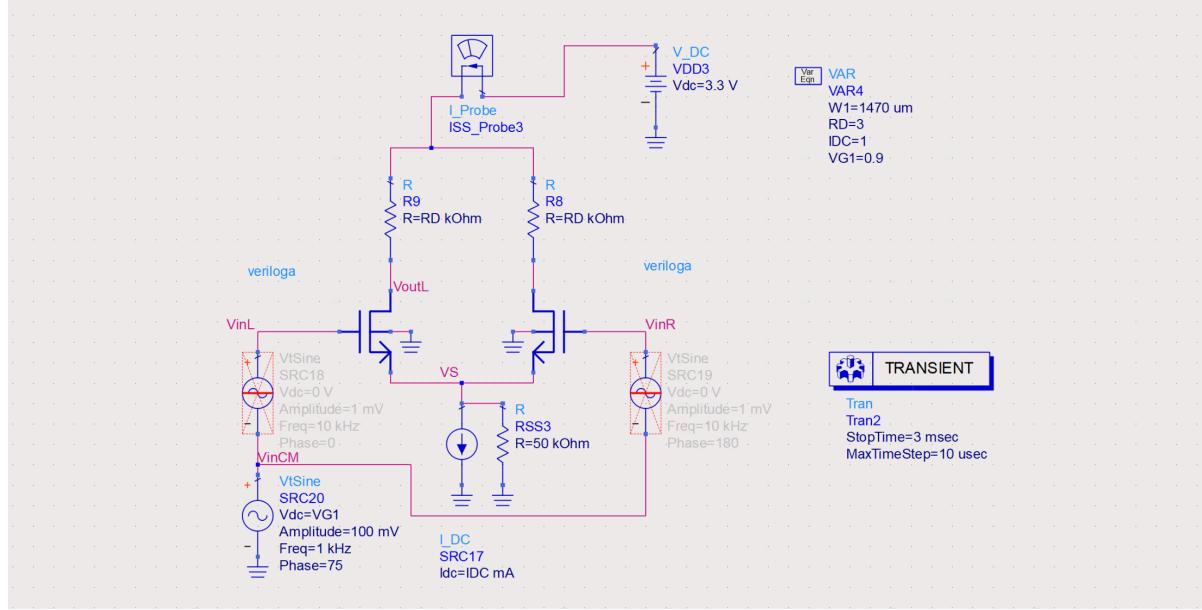


Figure 33: Transient Simulation Common Mode Schematic

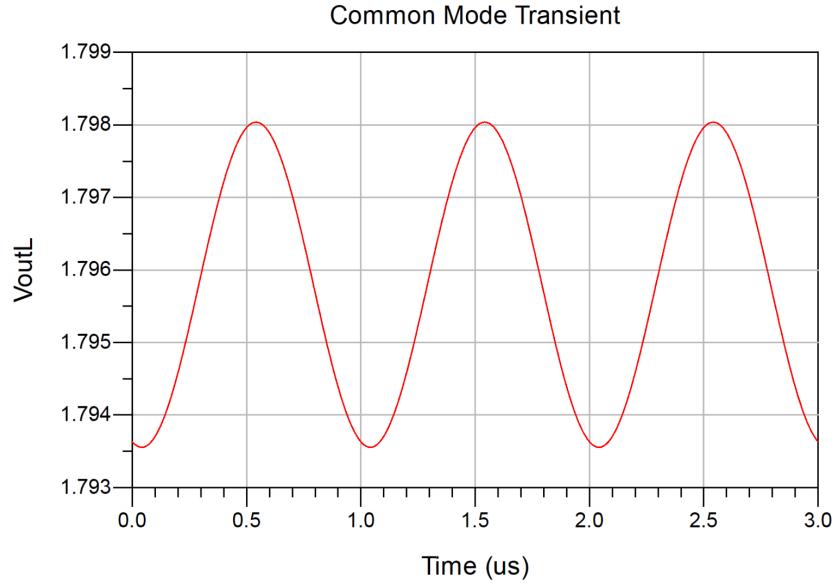


Figure 34: Transient Simulation Common Mode Result

Final figures are for the total input testing where we combine the previous 2 modes together in testing. Figure 35 shows the total input testing schematic where Figure 36 shows the outcome of both the common mode and differential mode testing.

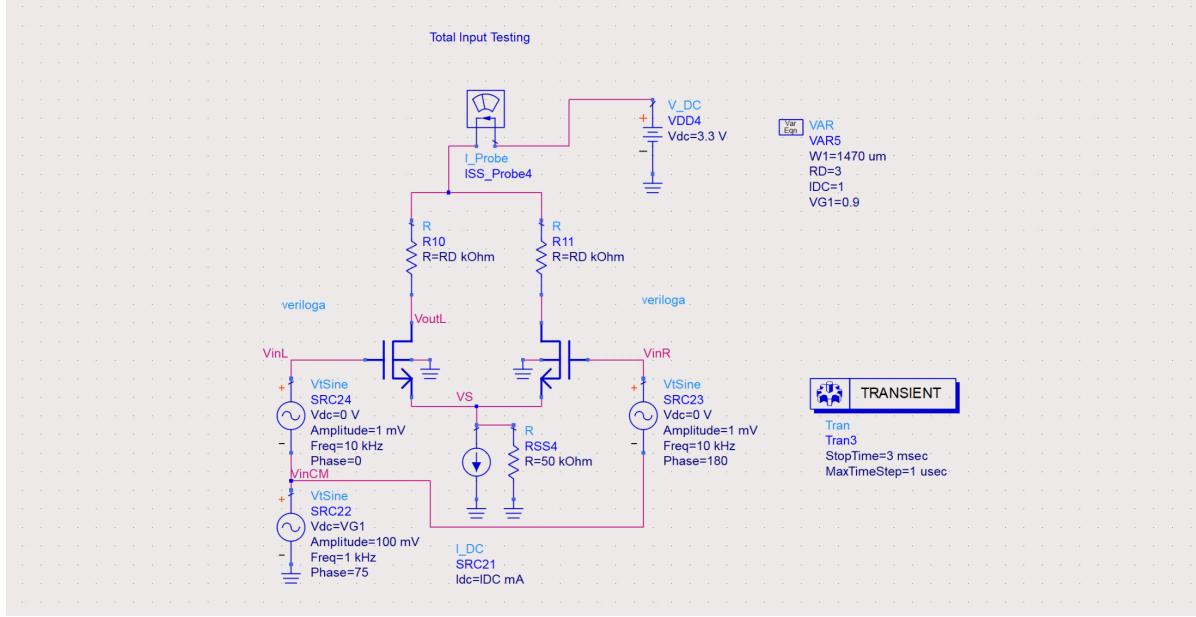


Figure 35: Total Input Testing Schematic

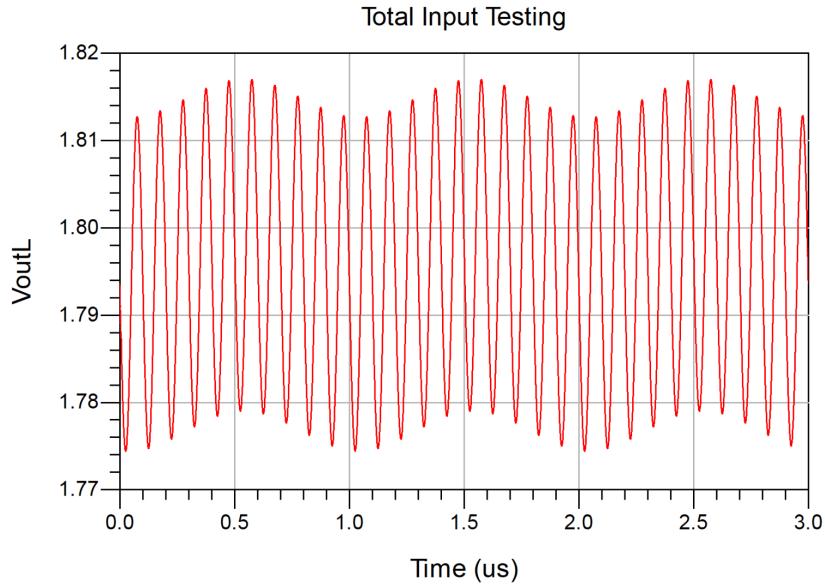


Figure 36: Total Input Testing Results

4 Discussion

The overall project this semester was informative on the different circuits that were discussed in the previous section. I had gathered much of my information for this semester from forums and the referenced book that had much to talk about amplifier circuits. Of course, much of the areas that I had researched came from my professor Dr. Roth who had guided me on what I should look into and the areas that were of interest to me. Going over the project as a whole,

was cautious when using the EKV model as my professor and I had some concerns with some of the curves shown in earlier simulations. Towards the end of the semester, I was invited to a meeting with an engineer from Keysight who went over some valuable information. They had discussed using the BSIM Model in ADS and the graphs shown had more realistic curves that included different effects of smaller transistor scaling. With this in mind, I had looked out for key differences in the LEVEL 1 Model and the EKV Model. While both models did have different curves when looking at the gain over a frequency sweep, I believe much of it also had to do with the different parameters used between models. This is why in some of my simulations I go over using $2\mu m$ designs where the LEVEL 1 is roughly accurate down to this size while others use $0.5\mu m$ channel length. The width was usually different due to optimization/tuning in ADS to achieve desired outcomes.

5 Conclusion

5.1 Lessons learned

This topic had plenty points of interest for me that I would like to review further. With only so many months in a single semester, there was not a lot of time to cover every single design in detail. The CMOS Amplifiers course taught by Dr. Roth had an extensive review on Razavi's topics on analog cmos design, with integrating much of the class into the research project, I found it difficult yet rewarding to keep up with each one of the topics presented to me to review. As we went over CS Amplifiers, Differential Amplifiers, Total Input Testing and much more discusses in this report. Being able to cover many topics provides the student the ability to choose what interested them and go out to research on their own. That Is what I did with many of the topics from my project. Throughout using the EKV Model from EPFL, I would like to have taken more time to try to review why this model acted similarly to the Level 1 Model instead of moving on with the project using the Verilog-A file so haphazardly. The BSIM3 Model is integrated into ADS and could have been chosen to use for my research, however I do not believe I would've learned more about how the higher-level models work as I had to review the Verilog-A code for the EKV. This way, using open source code I could find an easier time reviewing how the model evaluates input voltages.

5.2 Knowing what you know now, would you make any changes to the project?

If I had the current information back when I started this semester I would only make a few changes. Ultimately, I would continue on the EKV Model but instead try to find a different version and not use Verilog-A. It was not easy to understand the code and where some parameters came from. If I had the information back then, I would instead use my time to try to make my own compact model as to understand at a deeper level how the model works. Starting off from Level 1 and maybe going up to Level 3 depending on how far I would be able to get within a semester. I would also like to have reviewed more examples on my own about operational amplifier designs as this is what made me curious to find these in other designs within Integrated Circuits. Not only do I spot current mirrors and differential amplifiers more easily in designs, but I can understand those very designs better on why they were created and what purpose each amplifier has. Lastly, not quite on the transistor level of designs, but while working on a personal project on top of this class I found that Altium is free for students! I had started taking courses within Altium and printed some designs out for myself to use. I would

have like to implemented PCB design into my research as a side project but this would have incorporated much more work for only a semester long project.

5.3 Future work – what would you do to continue the project?

A continuation of this project would be something that I would be interested in doing on my own time, however without the license for the ADS software it is not something that I could invest in. There is open source software that can be used to do similar testing, but with Verilog-A not very common and other models that show more promising results it is not something I could pursue without the ADS license. Although simulations for EKV would be transitioned out and other compact models integrated in, I would like to add additional resources to finding where I could run reliable simulations for BSIM3 as an example. On top of reviewing other models, the information gathered from the textbook for CMOS Amplifiers had opened my eye on how important the operational amplifier is to analog design. Since then, I have been actively reviewing analog designs and when adding to my personal project of Integrated Circuits can spot different designs. Although I would eventually move away from using the EKV model, it has opened a new way of thinking in the world of analog design and has helped me look for other areas where I was less proficient and build what little knowledge I had. From analog to digital design, the EKV model has overall been a challenge to learn but broadened my analog expertise.

References

- [1] B. Razavi, *Design of analog CMOS integrated circuits*. McGraw-Hill Education, second edition ed.
- [2] Keysight, “PathWave advanced design system.” Section: Article Section.
- [3] “0.5um CMOS parameters — epfl.ch.”
- [4] B. Ramos, “J0ntrollston/ADS-EKV2.6-model.” original-date: 2024-01-20T05:05:09Z.
- [5] Wladek, “ekv26/model.” original-date: 2019-12-04T13:15:07Z.