USAF ACADEMY
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
ECE 383 GRADED REVIEW #2
SPRING 2016

Name: _____ **Section:** _____

Academic Security	This examination is not released from academic security until **1200** on **April 20, 2016**. Until this time, you may not discuss the examination contents or the course material with anyone other than your instructor.
Integrity	Your honor is extremely important. This academic security policy is designed to help you succeed in meeting academic requirements while practicing the honorable behavior our country rightfully demands of its military. Do not compromise your integrity by violating academic security or by taking unfair advantage of your classmates.
Authorized Resources	1. Equation Sheet 2. Any calculator
Instructions	▪ **Show all work for full credit.** ▪ Box or circle your final answer. ▪ For all numerical answers, use engineering notation and include units. ▪ Completely label all your diagrams, drawings, graphs, etc. for full credit. ▪ You have the remainder of the period to complete this exam.

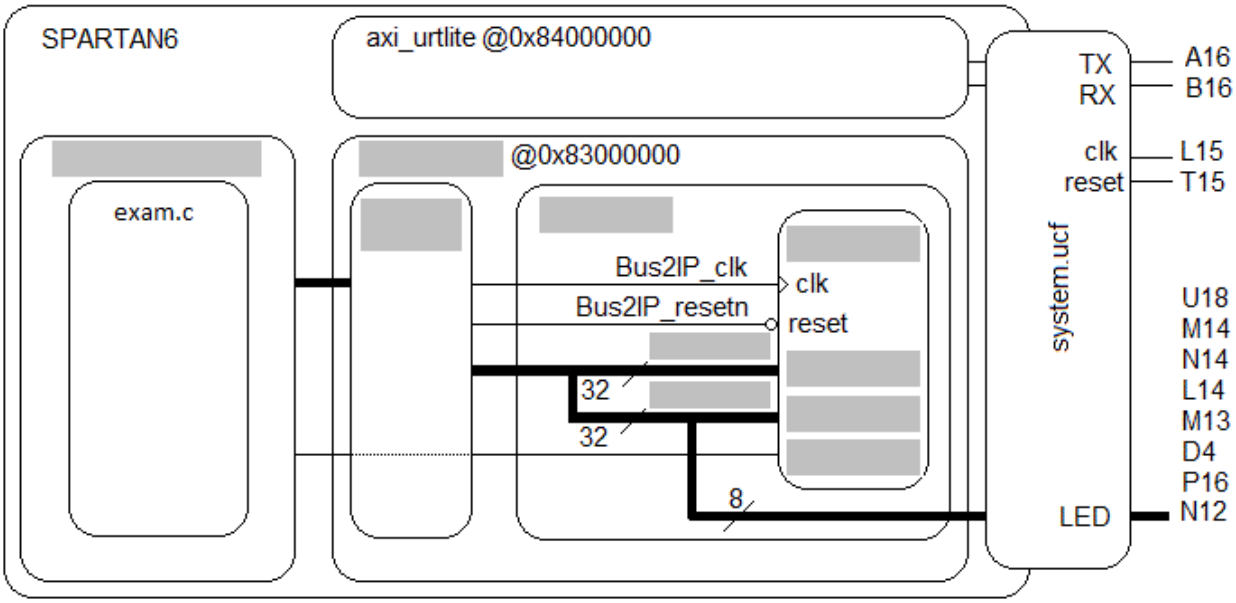
Problem	Value	Earned	Course Objective
1	15		Objective 2, 5
2	20		Objective 1
3	15		Objective 5
4	10		Objective 4
5	10		Objective 1
6	20		Objective 5
7	10		Objective 4
Total	100		

Problem 1 (15 points) *Tools, HW/SW partition* [Objective 2, 5]

You are given the following flag register that is instantiated (with N = 16) inside a component called **generator**. The set and ready signals are driven by logic internal to the **generator** component. The clear and Q signals are sent to/from the microBlaze. The ready signal is sent to the microBlaze as an interrupt. The clear signal is associated with slave register 3 and Q is associated with slave register 4. The **generator** component also connects the lower 8-bits of Q to an output called **LED**, sent to illuminate 8 LEDs on the ATLYS board. You are using the **generator** component to create a custom IP core called **examDriver** with a base address of 0x83_000_000.

```
entity flagRegister is
     generic(   N :          integer := 8);
     port(      clk :        in  STD_LOGIC;
                reset :      in  STD_LOGIC;
                set, clear: in std_logic_vector(N-1 downto 0);
                Q :          out std_logic_vector(N-1 downto 0));
end flagRegister
```

a. (5 pts) Complete the block diagram below by filling in the names of the signal and components in the 10 shaded boxes.



b. (5 pts) Write 1 line of C-code, running on the microBlaze, that executes a subroutine called **execute** when bit 2 of the flag register is 1.

c. (5 pts) Write a couple of lines of C-code, running on the microBlaze, to clear bit 2 of the flag register so that it can be set later by the logic inside the **generator** component.

Problem 2 (20 points) *Design to requirements* [Objective 1]

You are building a digital system that generates a sinusoid using direct digital synthesis. You are restricted to a 48kHz update rate, each sample is 16-bits wide. One period of the sinusoid is stored in a block RAM with 128 values. The output sinusoid is limited to 24kHz.

a. (5 pts.) What output frequency is generated with a phase increment of 4.68?

b. (5 pts.) What (decimal) phase increment generates a 1.2KHz waveform?

c. (5 pts.) How many bits are required for the integer portion of the phase increment?

d. (5 pts.) How many bits are required for the fractional portion of the phase-increment to allow frequency adjustments in at least 2 Hz increments?

Problem 3 (15 points) *Design digital system,* [Objective 5]

The following table contains a lookup table for the arc tangent function. The input, x, is an angle in degrees. The output in the rightmost column is a Q3.5 format fixed point number.

Index	x	cubeRoot(x)	Q3.5
0	0	0.00	0x00
1	32	3.17	0x65
2	64	4.00	
3	96	4.58	
4	128	5.04	0xA1
5	160	5.43	0xAD
6	192	5.77	
7	224	6.07	0xC2
8	256	6.35	0XCB

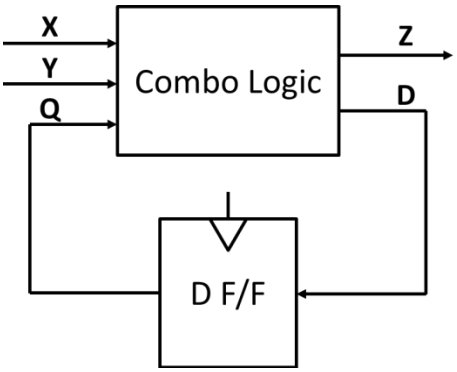
a. (5 pts.) Start by filling in the rightmost column (Q3.5) using the decimal values in the cubeRoot(x) column.

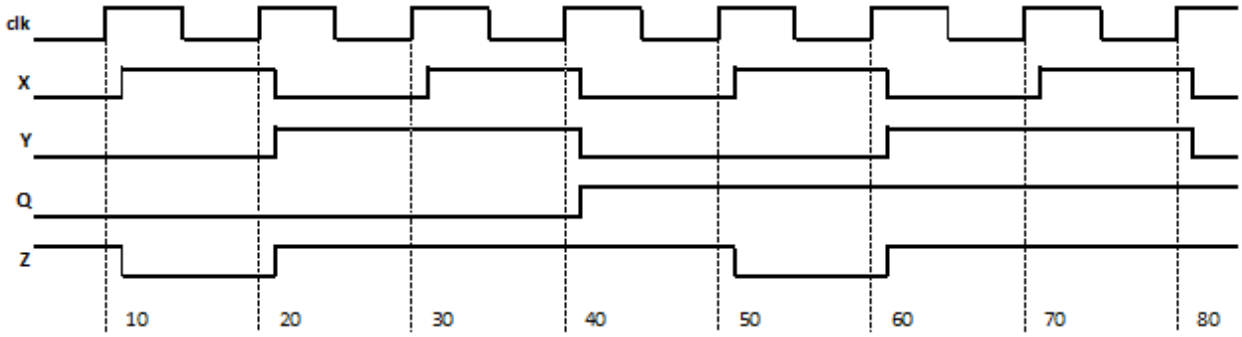
b. (5 pts.) Use linear interpolation on the values in the table to compute the cubed root of 140 using decimal arithmetic (show work for full credit).

c. (5 pts.) Write a C code snippet to compute the Q3.5 format output given a 9-bit input x. The Q3.5 hex LUT entries are store in an array called **cubeRoot**.

Problem 4 (10 points) *Timing Analysis* [Objective 4]

You are given the FSM below, constructed from 1 D flip flop and some combinational logic. The timing diagram to the right shows the response of the circuit to an input sequence X applied to it. The timing diagram shows small propagation delays. From the timing diagram you are to infer the contents of the combinational logic box.

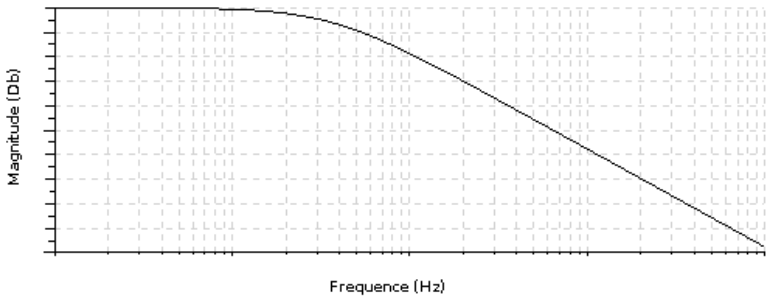




Write the equations for Z and D below.

Problem 5 (10 points) *Design to requirements* [Objective 1]

You are to design a filter using the following specifications. The signal of interest is from 0-10KHz and sampled using a 16-bit ADC. The maximum sampling rate is 250KHz.



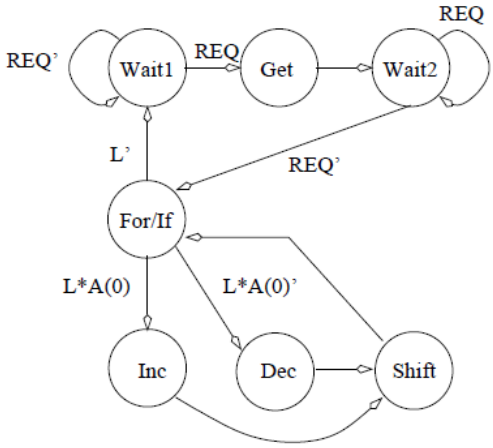
a) (5 pts.) The ADC will require how much attenuation to get the noise below 1 ulp?

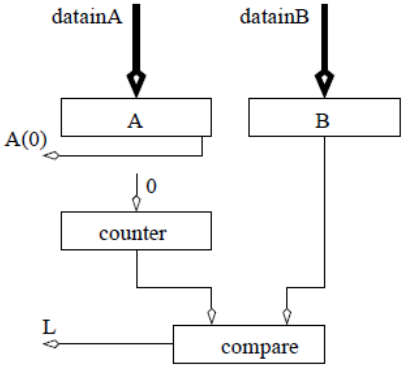
b) (5 pts.) What order filter do you need for this application?

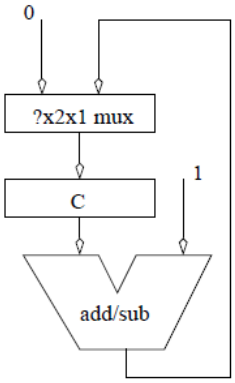
Problem 6 (20 points) *Design Digital Systems* [Objective 5]

This question deals with the construction of a digital circuit to accomplish the task specified by the following algorithm. A(0) refers to the LSB of A. A>> 1 refers to A shifted right 1 bit. Fill in the control word table below. Only fill in non-zero entries.

```
while(1) {
      ACK = 0;
      while(REQ == 0);
      A = datainA;
      B = datainB;
      ACK = 1;
      C = 0;
      while (REQ == 1);
      ACK = 0;
      for (i=0; i<B; i++) {
            if (A(0) == 1) then
                  C = C + 1;
            else
                  C = C - 1;
            A = A >> 1;
}     }
```







State	ACK	A	B	C	Mux	Count	Add/Sub
	0	00 hold	0 hold	0 hold	0 pass 0	00 hold	0 add
	1	01 load	1 load	1 load	1 pass C±1	01 down	1 sub
		10 SR				10 up	
		11 SL				11 load	
Wait1							
Get							
Wait2							
For/If							
Inc							
Dec							
Shift							

Problem 7 (10 points) *Timing Analysis* [Objective 4]

Complete the timing diagram below. Carry your work past the clock edge at time 50.