VHDL Lab 2

Name: يوسف علي رشيدي علي
ID: 23010999

Name: عبد الرحمن علي صلاح الدين
ID: 23010530

Name: علي عمرو عبدالله أحمد
ID: 23010589

Name: يوسف عاطف محمد غريب
ID: 23010993

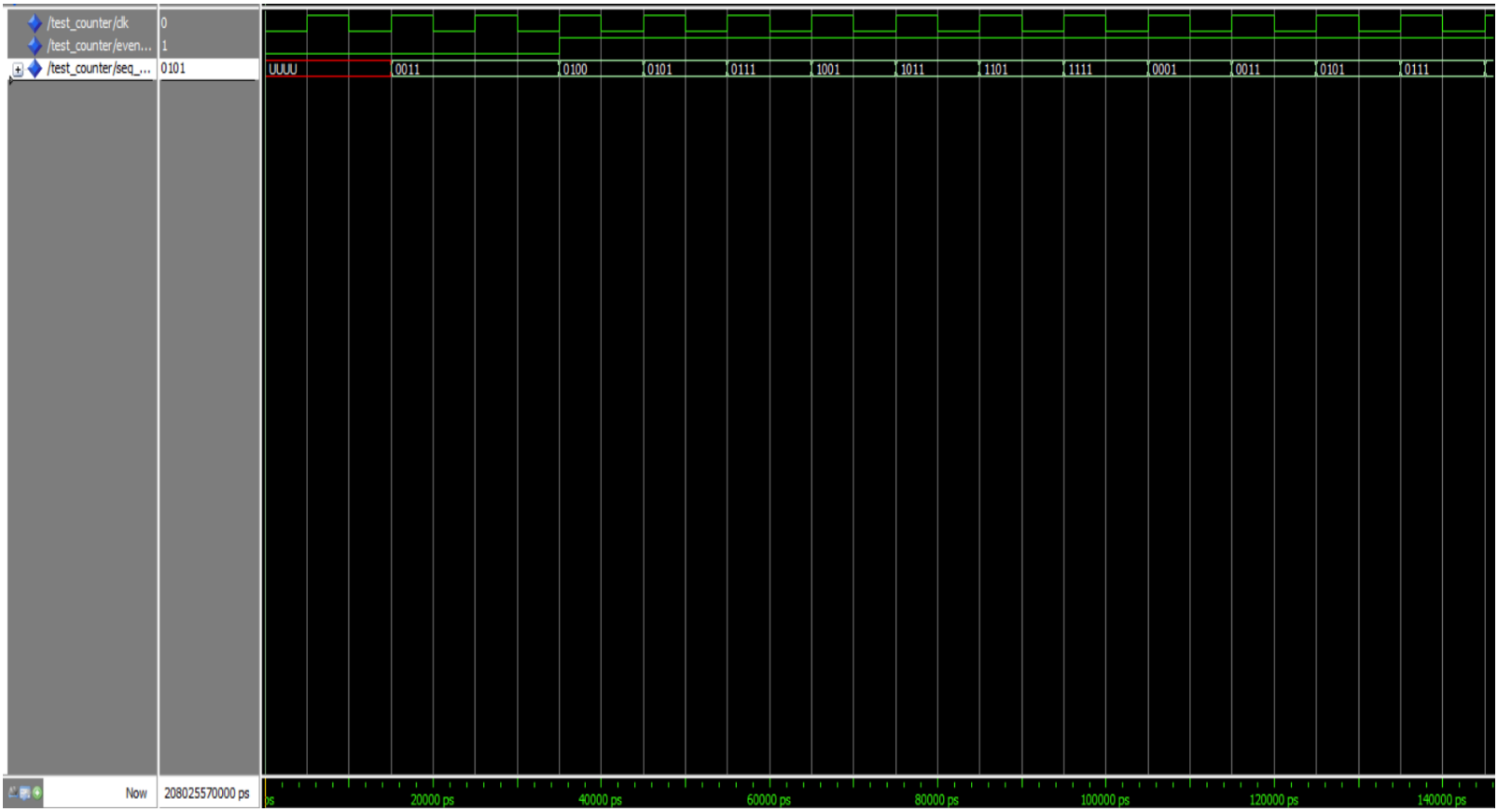
A. Problem Statement

Design a 4-bit even/odd synchronous Counter that has an input X.

The counter should work as follows:

- If input X = 0, the counter counts even numbers, otherwise, it counts odd numbers.
- If counting for even numbers, the counter's value should be: 0000, 0010, 0100…
- If counting for odd numbers, the counter's value should be: 0001, 0011, 0101…

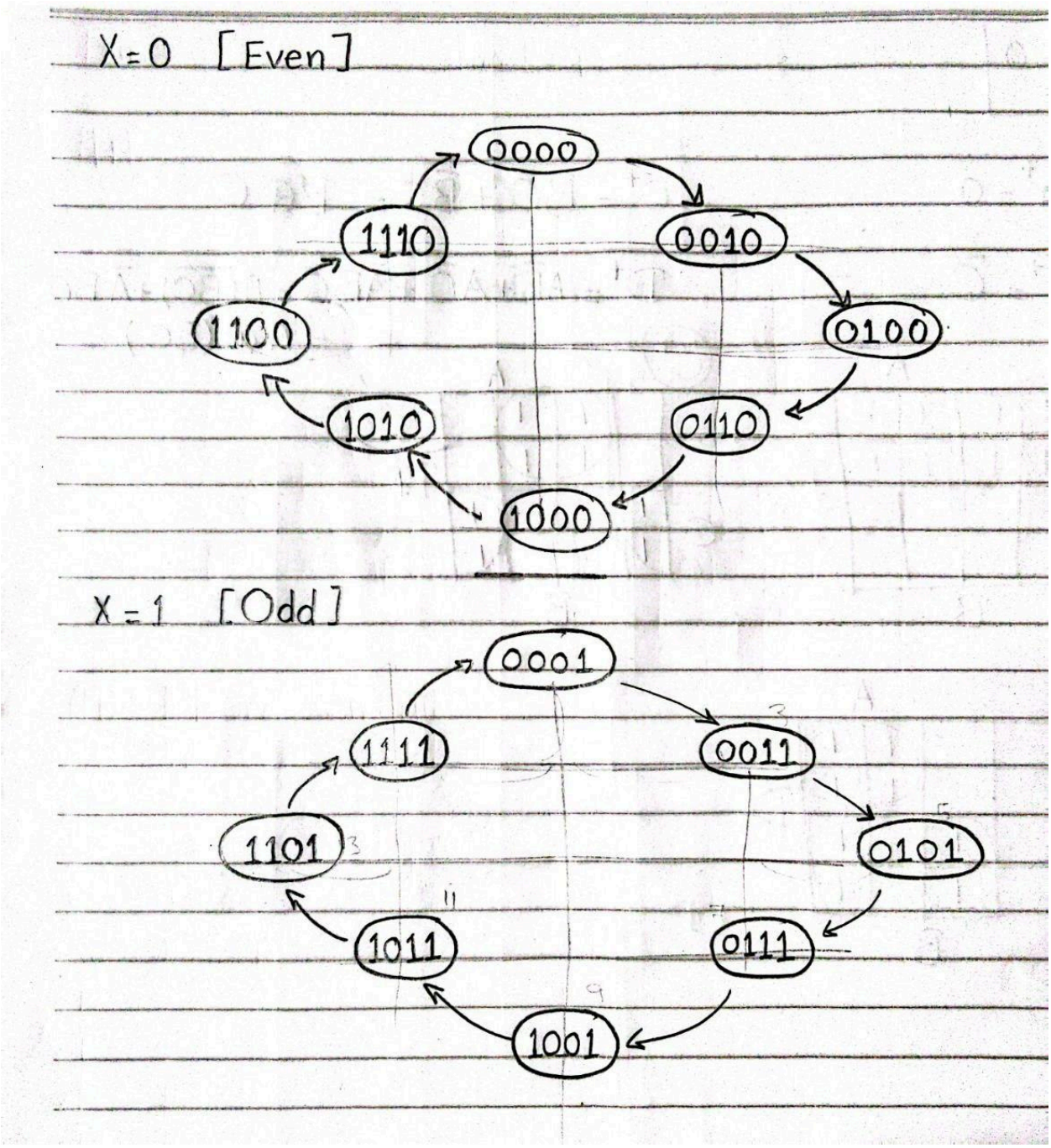
B. Simulation Samples



C. 1. Transition Table

Input				X = 0				X = 1			
D	C	B	A	D^+	C^+	B^+	A^+	D^+	C^+	B^+	A^+
0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	1
0	0	1	0	0	1	0	0	0	0	1	1
0	0	1	1	0	1	0	0	0	1	0	1
0	1	0	0	0	1	1	0	0	1	0	1
0	1	0	1	0	1	1	0	0	1	1	1
0	1	1	0	1	0	0	0	0	1	1	1
0	1	1	1	1	0	0	0	1	0	0	1
1	0	0	0	1	0	1	0	1	0	0	1
1	0	0	1	1	0	1	0	1	0	1	1
1	0	1	0	1	1	0	0	1	0	1	1
1	0	1	1	1	1	0	0	1	1	0	1
1	1	0	0	1	1	1	0	1	1	0	1
1	1	0	1	1	1	1	0	1	1	1	1
1	1	1	0	0	0	0	0	1	1	1	1
1	1	1	1	0	0	0	0	0	0	0	1

C. 2. State Graph



C. 3. Karnaugh Maps

BA \ DC	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	0	0	0
10	0	0	0	0

Result

F = 0

BA \ DC	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	0	0	0	0
10	1	1	1	1

Result

$$F = B\overline{A} + \overline{B}A$$

BA \ DC	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	0	0	0	0
10	0	0	0	0

Result

$$F = \overline{B}$$

BA \ DC	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

Result

F = 1

BA \ DC	00	01	11	10
00	0	0	1	1
01	0	0	1	1
11	0	1	0	1
10	0	0	1	1

Result

$$F = D\overline{C} + \overline{A}D + \overline{B}D + BA\overline{D}C$$

BA \ DC	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	1	0	0	1
10	0	1	1	0

Result

$$F = \overline{A}\,C + \overline{B}\,C + B\,A\,\overline{C}$$

BA \ DC	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	1	0	0	1
10	1	X	0	1

Result

$$F = B\overline{C} + \overline{B}C$$

BA \ DC	00	01	11	10
00	0	0	1	1
01	0	0	1	1
11	0	1	0	1
10	0	1	0	1

Result

$$F = D\overline{C} + \overline{B}D + B\overline{D}C$$

C. 4. Equations

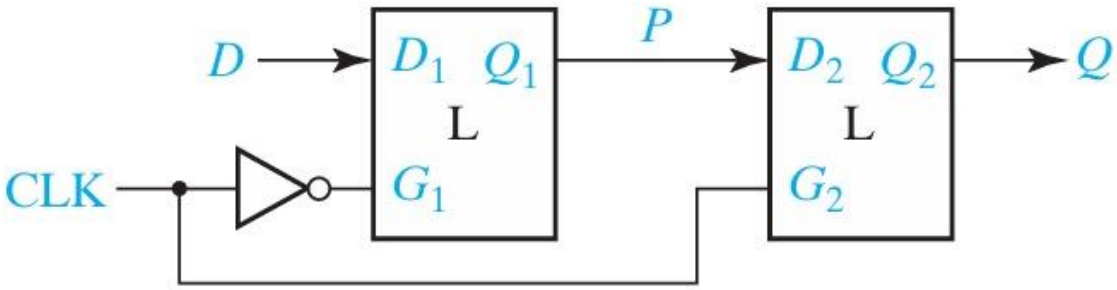
X = 0

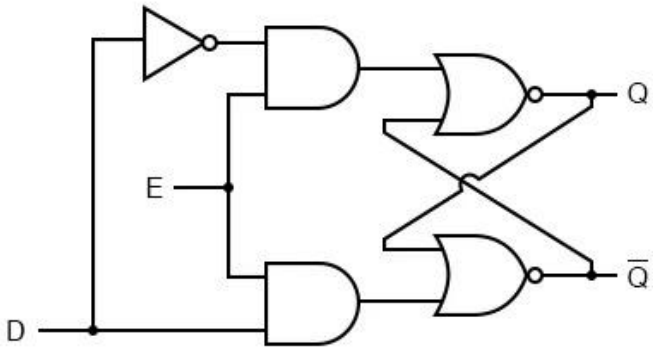
$A^+ \Rightarrow 0$
$B^+ \Rightarrow \bar{C}$
$C^+ \Rightarrow B\bar{C} + \bar{B}C \Rightarrow B \oplus C$
$D^+ \Rightarrow A\bar{B} + A\bar{C} + \bar{A}BC \Rightarrow A(BC)\bar{} + \bar{A}BC \Rightarrow A \oplus (B.C)$

X = 1

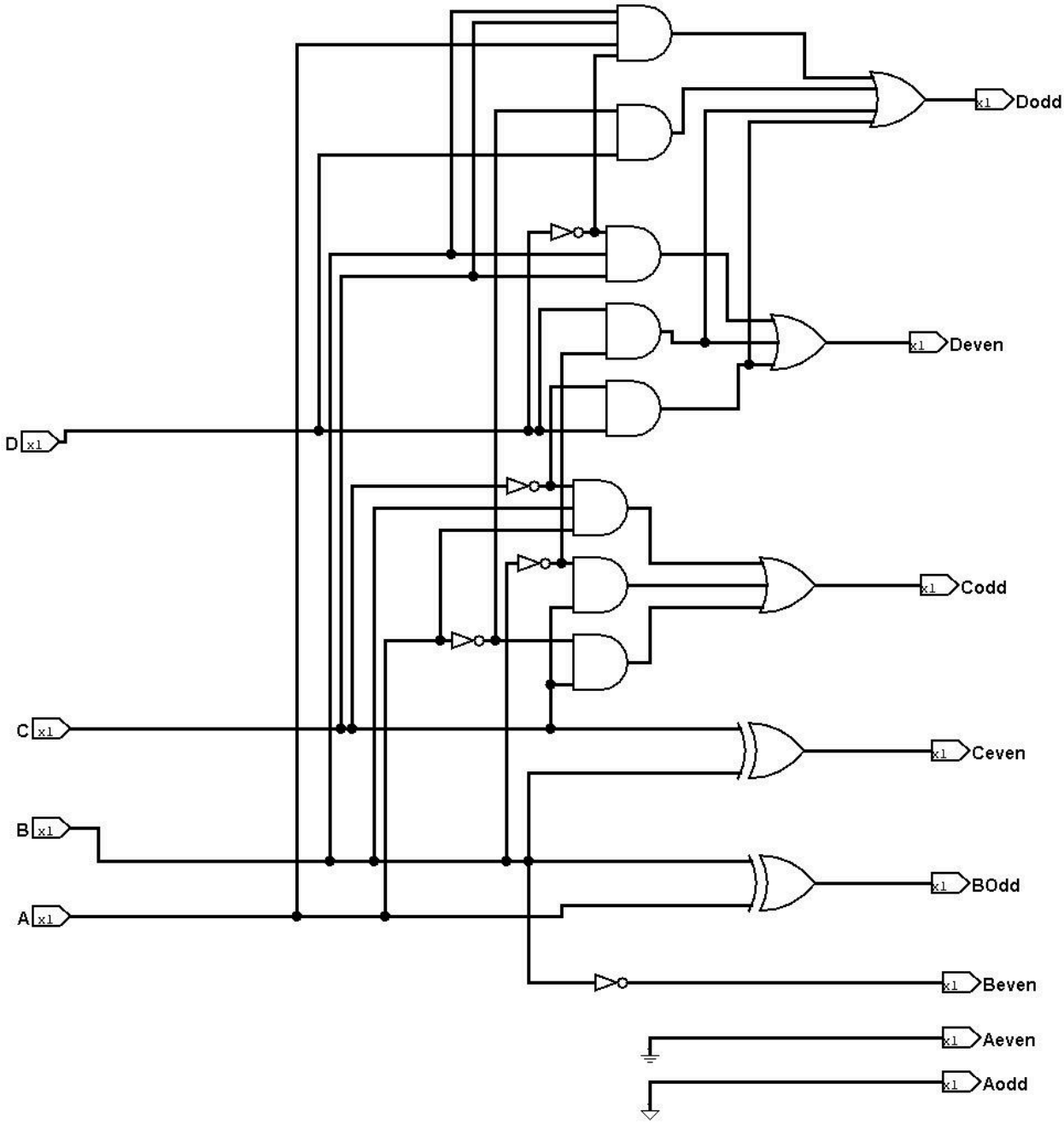
$A^+ \Rightarrow 1$
$B^+ \Rightarrow C\bar{D} + \bar{C}D \Rightarrow C \oplus D$
$C^+ \Rightarrow B\bar{C} + B\bar{D} + \bar{B}CD \Rightarrow B(CD)\bar{} + \bar{B}CD \Rightarrow B \oplus (C.D)$
$D^+ \Rightarrow \bar{A}BCD + A\bar{D} + A\bar{C} + A\bar{B} \Rightarrow \bar{A}(BCD) + A(BCD)\bar{} \Rightarrow A \oplus (B.C.D)$

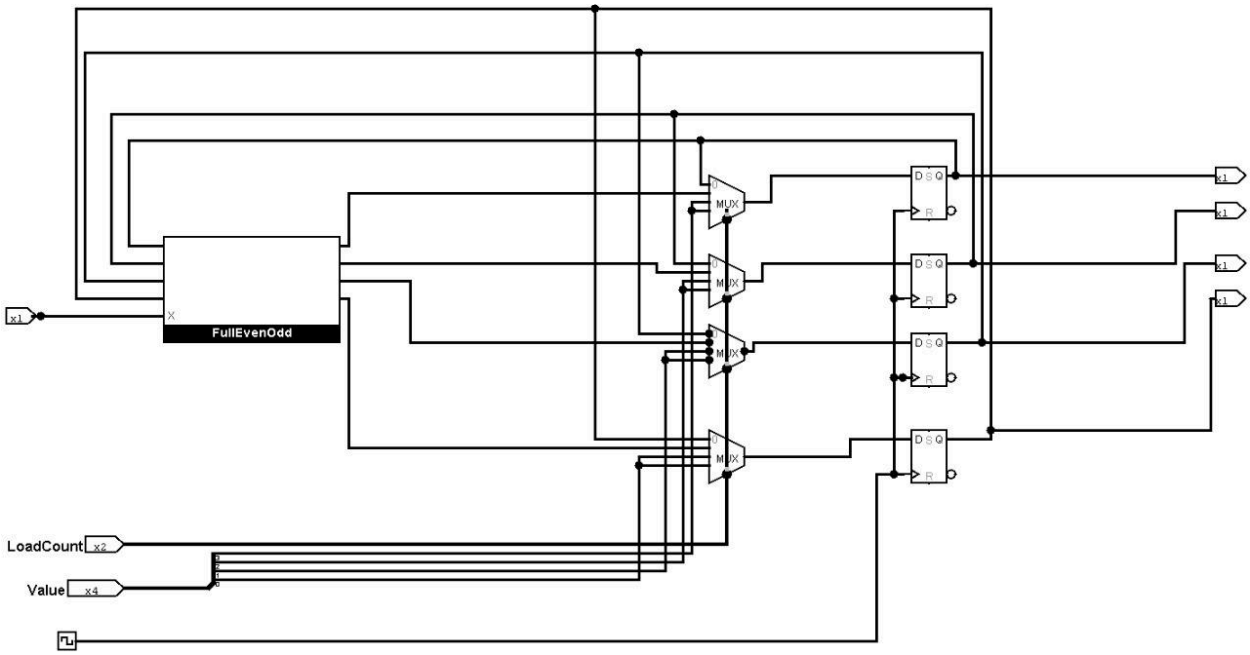
C. 5. Circuits Diagrams





E	D	Q	$\overline{Q}$
0	0	latch	latch
0	1	latch	latch
1	0	0	1
1	1	1	0


Dodd
Deven
D
Codd
C
Ceven
B
BOdd
A
Beven
Aeven
Aodd


x1
X
FullEvenOdd
MUX
MUX
MUX
MUX
D S Q
R
D S Q
R
D S Q
R
D S Q
R
x1
x1
x1
x1
LoadCount
x2
Value
x4

D. Assumptions

- Counter changes value on the rising edge of the clock.
- Load is prioritized over count.
- When **X = 0**, the counter is assumed to be even. If the current value is odd, it is incremented by 1 to ensure even parity.
- When **X = 1**, the counter is assumed to be odd. If the current value is even, it is incremented by 1 to ensure odd parity.