Alexandria University
Faculty of Engineering
Computer and Systems Engineering
First Year

Digital Systems Design
Spring 2025
Assigned: 16 March 2025
Due: 24 March 2025

Lab 2: Even\Odd Counter

Problem Statement

Design a 4-bit even/odd synchronous Counter that has an input X.

. The counter should work as follows:

- If input X = 0, the counter counts even numbers, otherwise, it counts odd numbers.
- If counting for even numbers, the counter's value should be: 0000, 0010, 0100...
- If counting for odd numbers, the counter's value should be: 0001, 0011, 0101…

Deliverables

1. Complete VHDL components.
2. VHDL test benches.
3. Report that includes:
    a. Problem statement.
    b. Simulation samples.
    c. Transition table, State graph, Karnaugh maps, equations and the circuit diagram.
    d. Important assumptions.

Notes:

1. You are free to design your interface (i.e., inputs and outputs) and the counter component(s) in any way. Include all the details in your report.
2. You are required to write your own test benches and add them to the report. Include edge test cases.
3. You are free to synchronize the events using a rising (or falling) edge (or level) clocksignal, but you must mention your choice in the report.