Alexandria University

Faculty of Engineering

Computer and Systems Engineering
First Year

Digital Systems Design

Spring 2025

Assigned: 24 February 2025
Due: 3 March 2025

Lab 1: 4-Bit Ripple Adder

Problem Statement

It is required to use VHDL to design and test a **4-bit Ripple Adder**, which adds 2 4-bit inputs introducing sum and carry signals.
You should implement the following modules:

1. Half Adder.
2. Full Adder using the Half Adder.
3. 4-bit Ripple Adder/Subtractor using the Full Adder.

Deliverables

1. Complete modular VHDL components.
2. VHDL test benches for each module.
3. Report that includes:
    a. Problem statement
    b. Any important design decisions or assumptions
    c. 2 Simulation Samples – at least - for each component (Half Adder, Full Adder, Ripple Adder and Ripple Subtractor)

Note: You should work in teams.
