Alexandria University
Faculty of Engineering
Computer and Systems Engineering
First Year

Digital Systems Design
Spring 2025
Assigned: 27 April 2025
Due: 5 May, 2025

Lab 3

Problem Statement

Design a sequential circuit that has one input X and one Moore-type output Z. The output is Z = 1 iff the total number of 1's received is divisible by 4 and the total number of 0's received is an odd number.

Note: Events should take place at each rising edge.

Interface

Signal	Type	Description
X	Input	Input of the state machine
Clk	Input	Clock to synchronize events
Z	Output	Output of the state machine

Bonus:

Redesign the circuit so that the output **Z** follows the Mealy model, and then report the differences between the Moore and Mealy designs. You must also include output **Z** snippets for both Moore and Mealy circuits based on the same input sequence.

Deliverables

1. Complete VHDL components.
2. VHDL test benches.
3. Report that includes:
    a. Problem statement.
    b. Minimized State diagram and State table
    c. Transition table, Karnaugh maps and equations.
    d. Any important design decisions or Assumptions
    e. Simulation samples.
4. For the Bonus part:
    a. You must provide the VHDL component(s)
    b. The report should include the previously mentioned comparison.