LINEAR ACTIVE QUENCHING CIRCUIT FOR CMOS SPADS

Daniel Kramnik

Changelog (Rev. 2):

- Added quench/reset slew rate adjustment
- Switched comp. latch delay line to an adjustable starved inverter
- Added SPAD anode test point for scope probe
- Added bias current sensing connector to external 50R term.
- Switched to higher precision output buffer biasing w/. matched FET cascoded mirrors
- Added STM32 MCU and DACs to replace all bias adjustments
- Switched control of V_A-V_Q to DAC instead of resistor divider
- Added USB-powered SMPS for all power supply rails, no more exteral supply required

Changelog (Rev. 3):

- Adjusted position of USB connector to be 1.6mm off edge of PCB
- Added 90-degree triple-LED inducator next to USB port
- Changed SMA package to have thinner signal pad for better impedance matching
- Added TVS diode to SPAD output as an ESD precaution
- Switched upper biasing mirror to THAT320 BJTs due to excessive VGS requirement in ALD MOSFET arrays
- Switched boost inductor to be larger to prevent saturation and improve max. conversion ratio
- Removed slew and delay generators, since we can trap ion and operate APDs as-is, or place a slowdown cap across load resistor of level shifter
- Switched to faster HFA3134/HFA3135 matched BJTs for output buffer, and added extra cascode stacks to prevent breakdown
- Redesigned level shifter circuit for faster speed and independent control of delta-V and VA
- Redesigned one-shot for lower jitter, and added option for digital one-shot using MCU

Layout Notes:

Max. unterminated length for t_rise = 1ns is ~1in.

IMPEDANCE CALCULATIONS:
(T = 1oz/ft^2, H = 9.58mil, Er = 4.6)

8mil = 52.3 Ohm SE
9mil = 50.3 Ohm SE
10mil = 48.5 Ohm SE

Ref. 4PCB 4-Layer Stackup Specifications

TABLE OF CONTENTS

TITLE: aqc-rev3

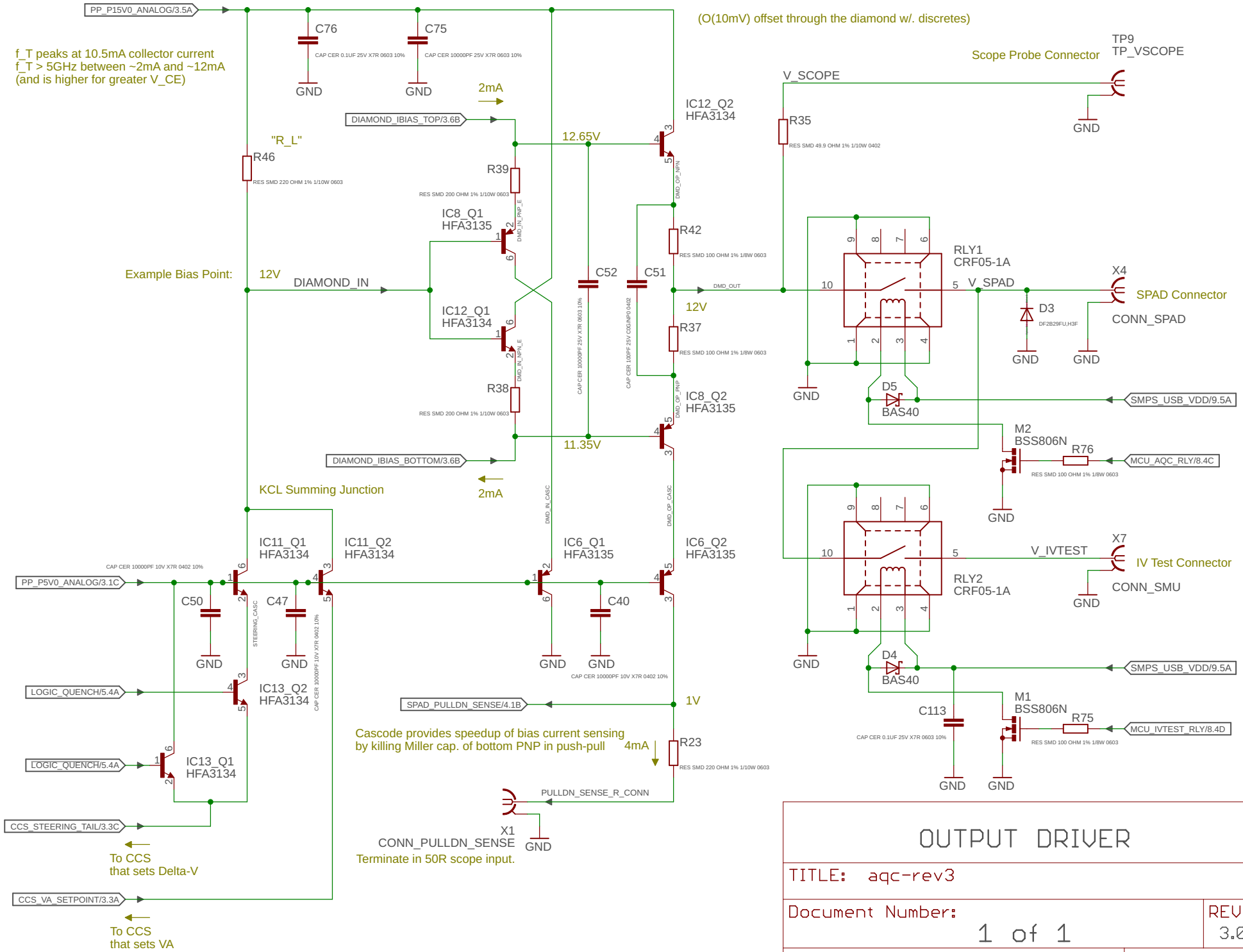
RLE LOGO

Document Number: 1 of 1

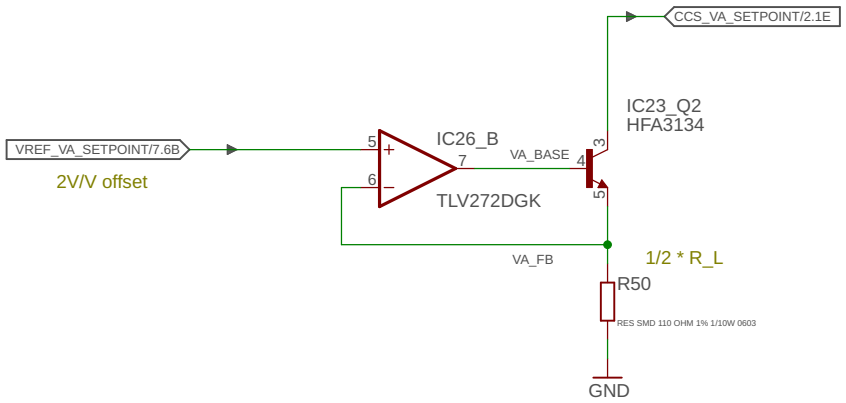
REV: 3.0

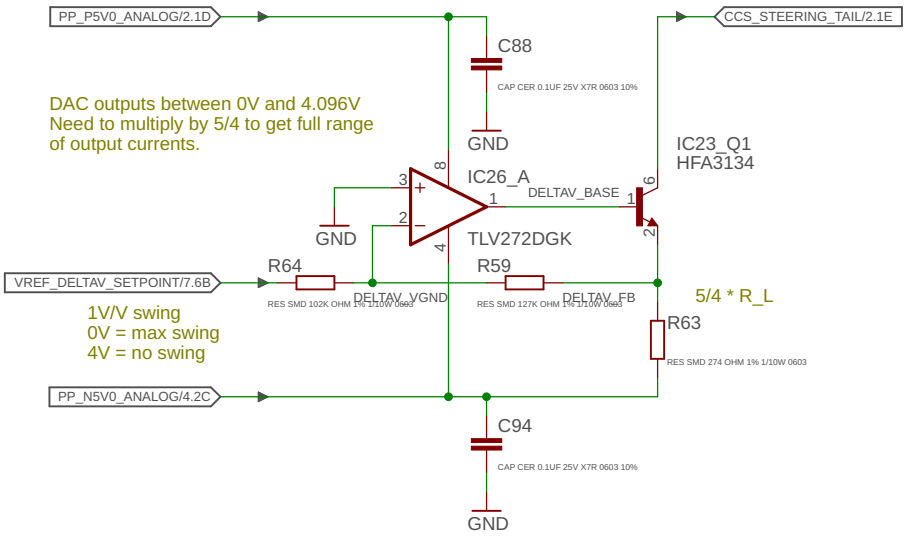
Date: 7/8/18 5:34 PM

Sheet: 1/12

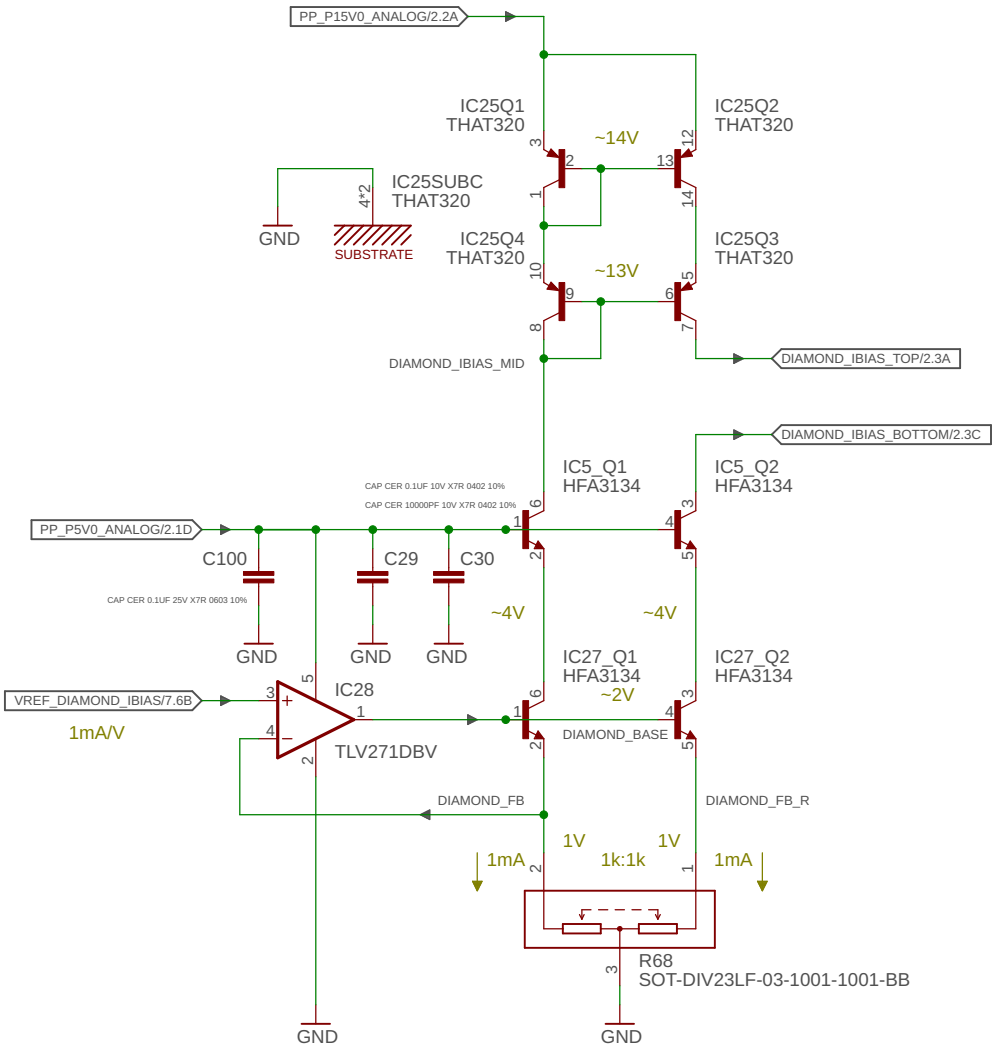

f_T peaks at 10.5mA collector current
f_T > 5GHz between ~2mA and ~12mA
(and is higher for greater V_CE)
PP_P15V0_ANALOG/3.5A
C76
CAP CER 0.1UF 25V X7R 0603 10%
C75
CAP CER 10000PF 25V X7R 0603 10%
GND
2mA
DIAMOND_IBIAS_TOP/3.6B
"R_L"
R46
RES SMD 220 OHM 1% 1/10W 0603
12.65V
R39
RES SMD 200 OHM 1% 1/10W 0603
IC8_Q1
HFA3135
IC12_Q2
HFA3134
R42
RES SMD 100 OHM 1% 1/8W 0603
Example Bias Point:
12V
DIAMOND_IN
IC12_Q1
HFA3134
C52
C51
CAP CER 10000PF 25V X7R 0603 10%
CAP CER 100PF 25V C0GJNP0 0402
DMD_OUT
12V
R37
RES SMD 100 OHM 1% 1/8W 0603
R38
RES SMD 200 OHM 1% 1/10W 0603
IC8_Q2
HFA3135
11.35V
DIAMOND_IBIAS_BOTTOM/3.6B
2mA
KCL Summing Junction
IC11_Q1
HFA3134
IC11_Q2
HFA3134
IC6_Q1
HFA3135
IC6_Q2
HFA3135
PP_P5V0_ANALOG/3.1C
CAP CER 10000PF 10V X7R 0402 10%
C50
C47
C40
GND
LOGIC_QUENCH/5.4A
IC13_Q2
HFA3134
LOGIC_QUENCH/5.4A
IC13_Q1
HFA3134
CCS_STEERING_TAIL/3.3C
To CCS
that sets Delta-V
CCS_VA_SETPOINT/3.3A
To CCS
that sets VA
SPAD_PULLDN_SENSE/4.1B
1V
Cascode provides speedup of bias current sensing
by killing Miller cap. of bottom PNP in push-pull
4mA
R23
RES SMD 220 OHM 1% 1/10W 0603
PULLDN_SENSE_R_CONN
X1
CONN_PULLDN_SENSE
Terminate in 50R scope input.
(O(10mV) offset through the diamond w/. discretes)
Scope Probe Connector
TP9
TP_VSCOPE
V_SCOPE
R35
RES SMD 49.9 OHM 1% 1/10W 0402
RLY1
CRF05-1A
V_SPAD
X4
SPAD Connector
CONN_SPAD
D3
DF2B29FU,H3F
D5
BAS40
SMPS_USB_VDD/9.5A
M2
BSS806N
R76
RES SMD 100 OHM 1% 1/8W 0603
MCU_AQC_RLY/8.4C
RLY2
CRF05-1A
V_IVTEST
X7
IV Test Connector
CONN_SMU
D4
BAS40
C113
CAP CER 0.1UF 25V X7R 0603 10%
M1
BSS806N
R75
MCU_IVTEST_RLY/8.4D
OUTPUT DRIVER
TITLE: aqc-rev3
Document Number:
1 of 1
REV:
3.0
Date: 7/8/18 5:34 PM
Sheet: 2/12

LEVEL SHIFTER BIASING





DIAMOND BIASING



OUTPUT DRIVER BIASING

TITLE: aqc-rev3

Document Number: 1 of 1

REV: 3.0

Date: 7/8/18 5:34 PM

Sheet: 3/12

Future design can try LTC6752 to reduce BOM cost, in exchange for an extra ~1.5ns of prop. delay
ECL Termination Reference: http://www.edn.com/Home/PrintView?contentItemId=4427861

PP_P5V0_ANALOG/5.2D
C24 C36
CAP CER 0.1UF 10V X7R 0402 10%
CAP CER 10000PF 10V X7R 0402 10%
GND GND

PP_P3V3/5.2A
C48 C49
CAP CER 0.1UF 10V X7R 0402 10%
CAP CER 10000PF 10V X7R 0402 10%
GND GND

PP_P3V3/5.2A
C28 C35
CAP CER 0.1UF 10V X7R 0402 10%
CAP CER 10000PF 10V X7R 0402 10%
GND GND

Place near input
~950mV
VREF_AV_DET/7.6D
C33 C34
CAP CER 0.1UF 10V X7R 0402 10%
CAP CER 10000PF 10V X7R 0402 10%
GND GND

IC4
ADCMP582
VTP 1
VP 2
VN 3
VTN 4
VCCI 5*2
VCCO 9*2
VEE
HYS
Q 11
Q̄ 10
GND 15
GND

SPAD_PULLDN_SENSE/2.3D

Pi Termination Network
Net Class: 100OHM_DIFF
COMP_Q_P
COMP_Q_N
R33
RES SMD 100 OHM 1% 1/10W 0402
R31 R22
RES SMD 150 OHM 1% 1/10W 0402
RES SMD 150 OHM 1% 1/10W 0402
GND GND

U3
SN65EPT21DGK
VCC 8
VBB 4
D 2
~D 3
NC_2 1
NC 6
GND 5
Q 7
HOLDOFF_TRIG/5.1B
GND

LVPECL to CMOS/TTL
VBB is at 2V bias
D, D̄ have symmetric 50k pulls

Zin = 50R when VTN grounded
R_HYS
R21 DNP
R36
RES SMD 10K OHM 1% 1/10W 0603
GND

LATCH
VTT LE LE̅
8 7 6
Active-Low for Latch Mode
(Note how Q0 goes to LE̅)

T Termination Network
(50R to VTT internally from LE and LE̅)
R20
RES SMD 49.9 OHM 1% 1/10W 0402
GND

PP_N5V0_ANALOG/3.1E
C37 C38
CAP CER 0.1UF 10V X7R 0402 10%
CAP CER 10000PF 10V X7R 0402 10%
GND GND

Net Class: 100OHM_DIFF
COMP_LE_N
COMP_LE_P

U2
SN65EPT22DGK
Q0 1
~Q0 2
Q1 3
~Q1 4
VCC 8
D0 7
D1 6
GND 5
GND

PP_P3V3/5.2A
C21 C23
CAP CER 0.1UF 10V X7R 0402 10%
CAP CER 10000PF 10V X7R 0402 10%
GND GND

PP_P3V3/5.2A
C44 C43
CAP CER 0.1UF 10V X7R 0402 10%
CAP CER 10000PF 10V X7R 0402 10%
GND GND

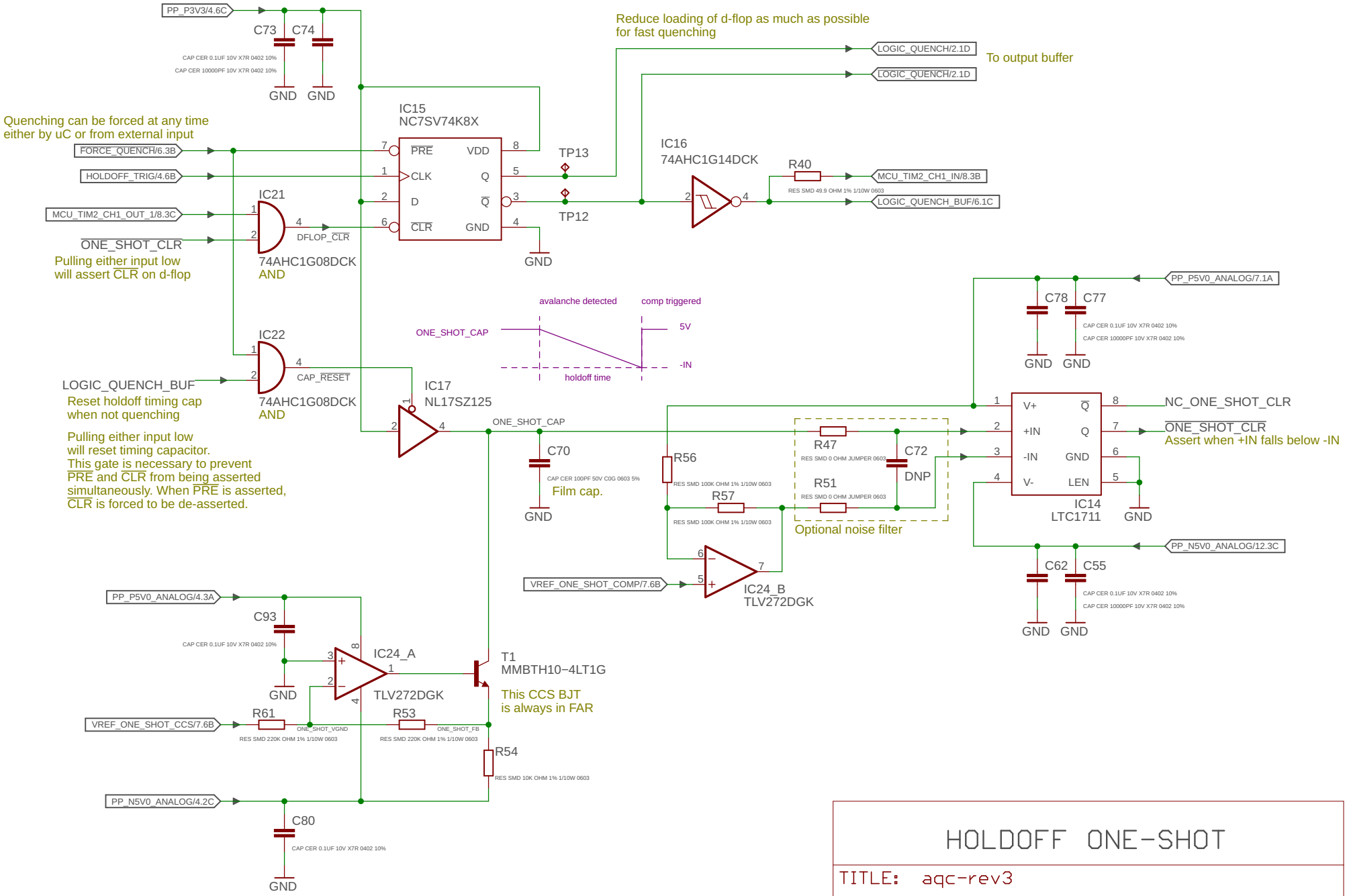
IC7
DS1100LU-45+
VCC 8
IN 1
GND 4
TAP1 7
TAP2 2
TAP3 6
TAP4 3
TAP5 5
R28 DNP
R24 DNP
R26 DNP
R25 DNP
R27 DNP
BLANKING_LATCH_EN
LOGIC_QUENCH_BUF/5.4B
GND

HIGH = Latch Enabled
LOW = Latch Disabled

Insufficient recovery blanking results in self re-triggering
Pick lowest delay tap that compensates a given coax cable
In the future, this process can be automated with a
digitally-tunable delay based on an ECL counter circuit.

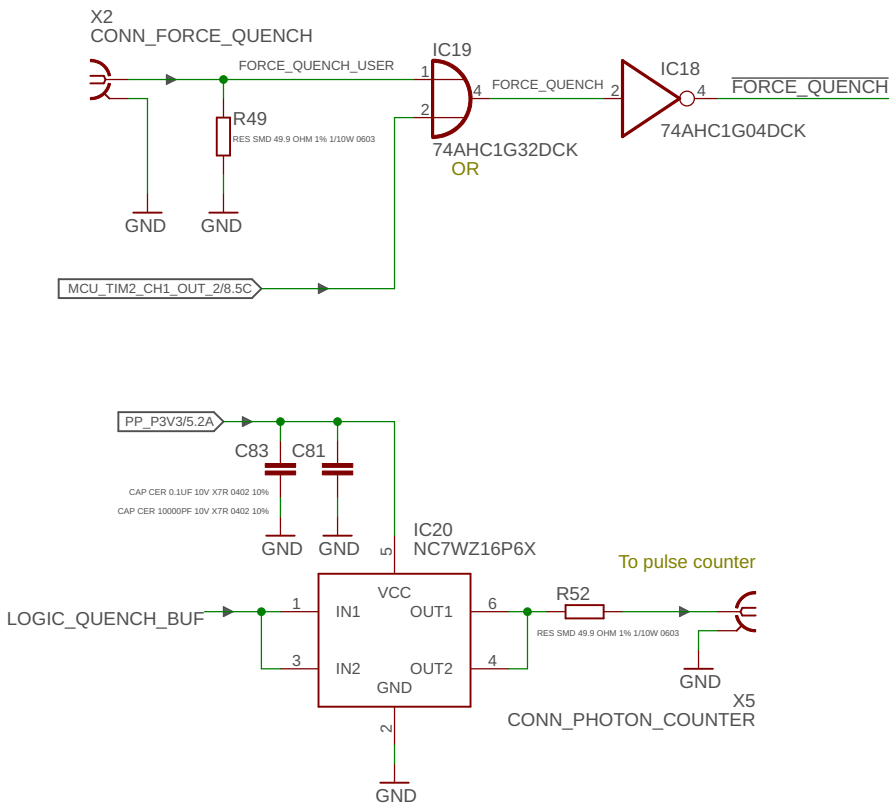
AVALANCHE DETECTOR

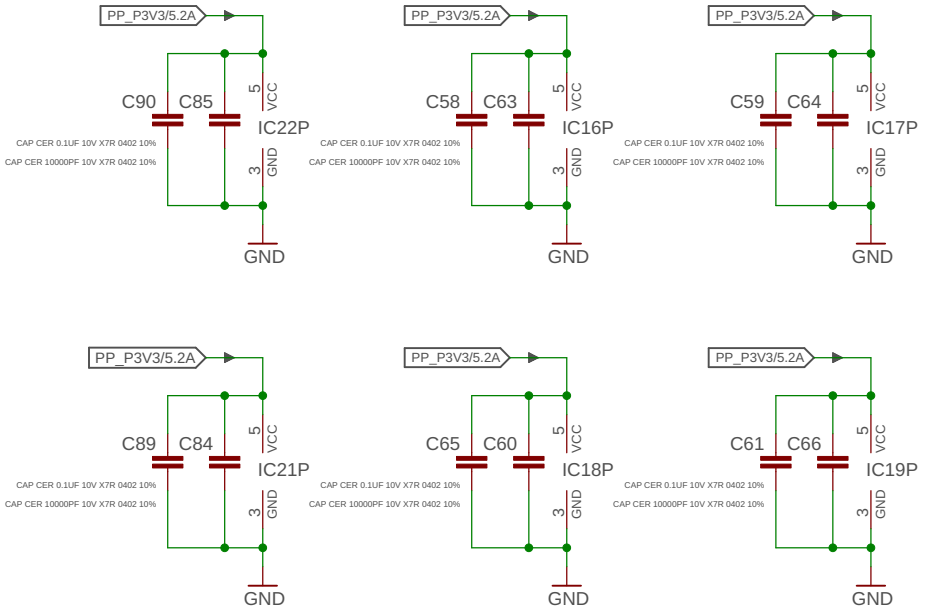
TITLE: aqc-rev3	
Document Number: 1 of 1	REV: 3.0
Date: 7/8/18 5:34 PM	Sheet: 4/12



HOLDOFF ONE-SHOT

TITLE: aqc-rev3	
Document Number: 1 of 1	REV: 3.0
Date: 7/8/18 5:34 PM	Sheet: 5/12





HIGH-SPEED USER IO GLUE LOGIC

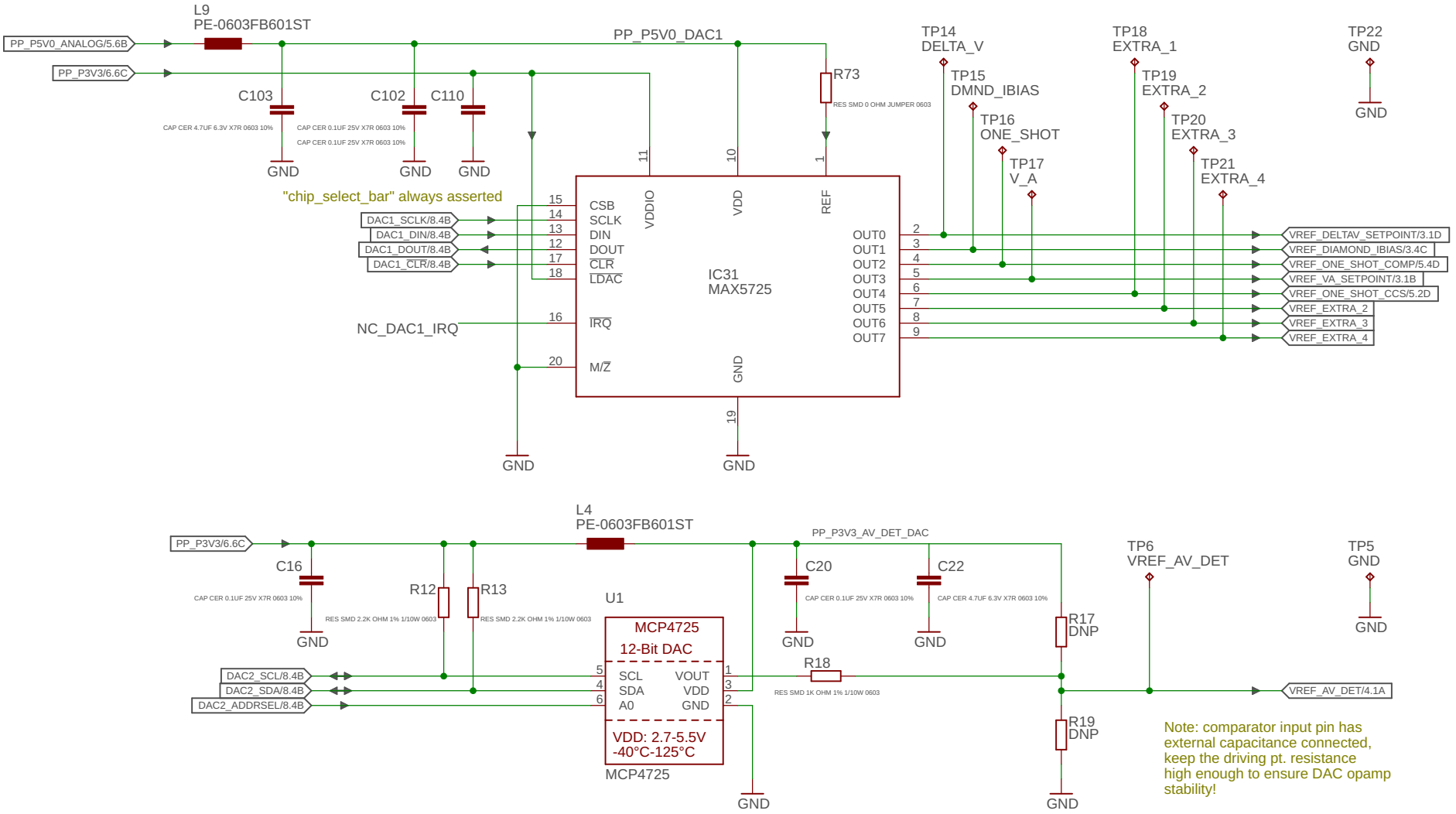
TITLE: aqc-rev3

Document Number: 1 of 1

REV: 3.0

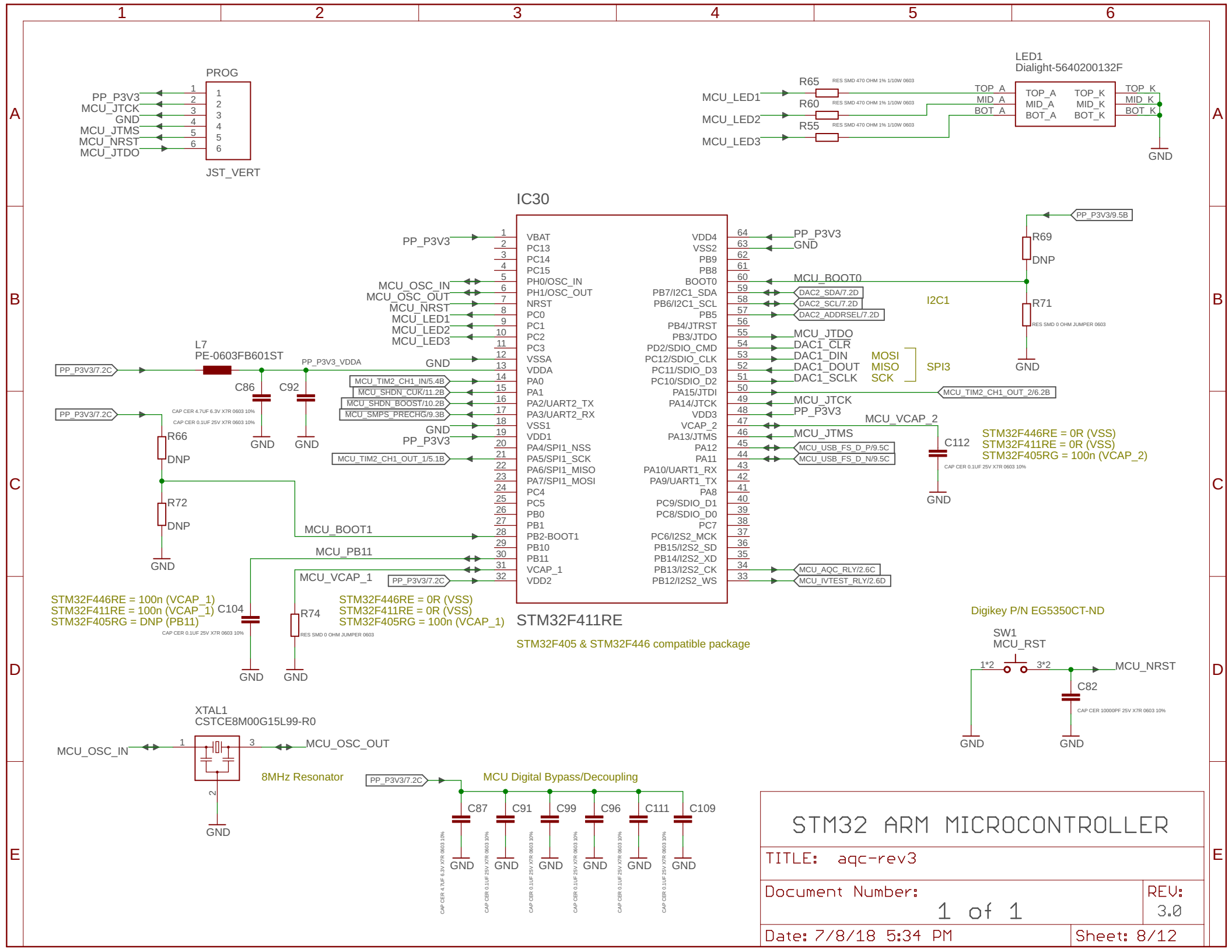
Date: 7/8/18 5:34 PM

Sheet: 6/12



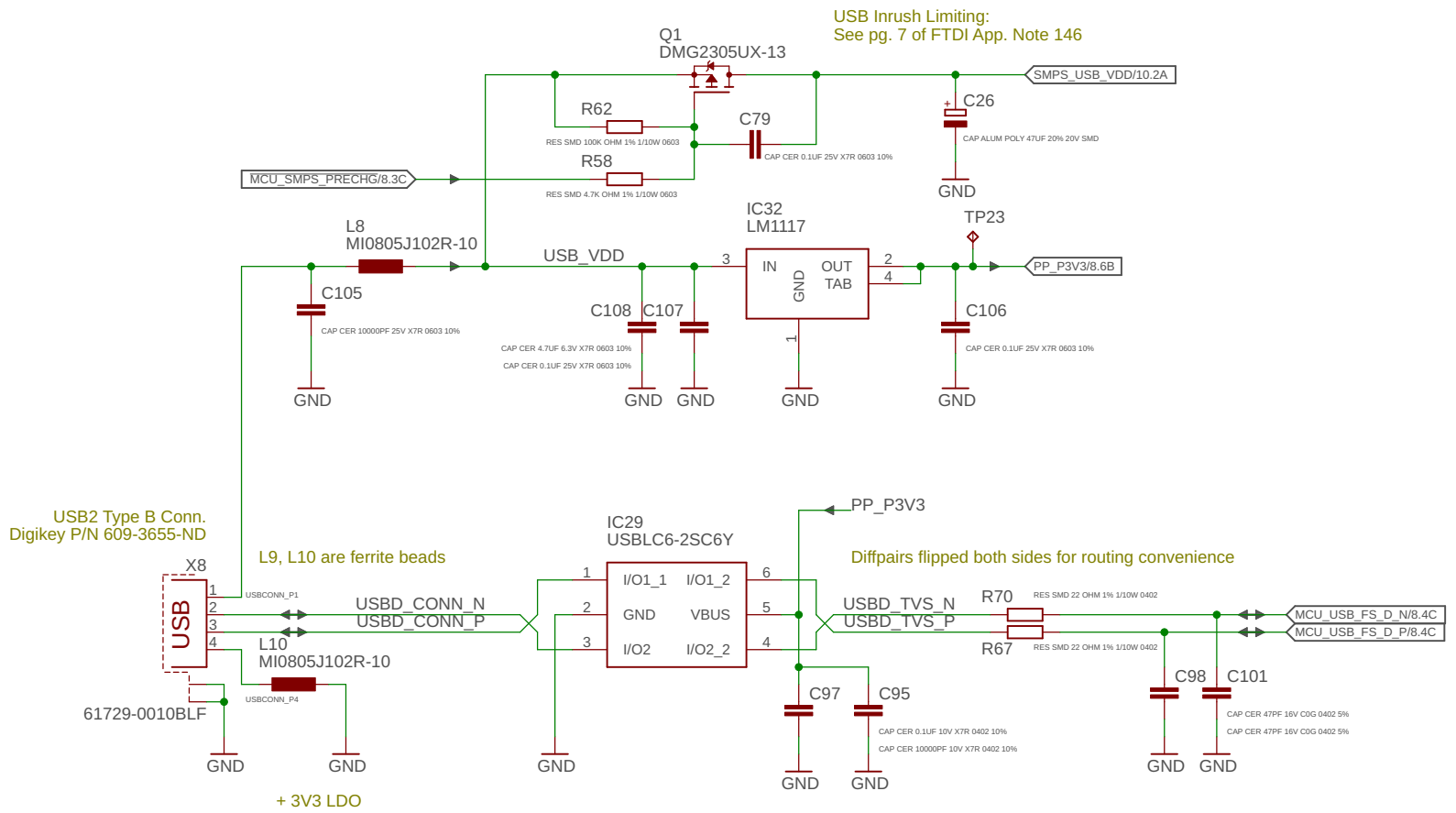
CONTROL DACS

TITLE: aqc-rev3	
Document Number: 1 of 1	REV: 3.0
Date: 7/8/18 5:34 PM	Sheet: 7/12



STM32 ARM MICROCONTROLLER

TITLE: aqc-rev3	
Document Number: 1 of 1	REV: 3.0
Date: 7/8/18 5:34 PM	Sheet: 8/12



USB INPUT AND INRUSH LIMITING

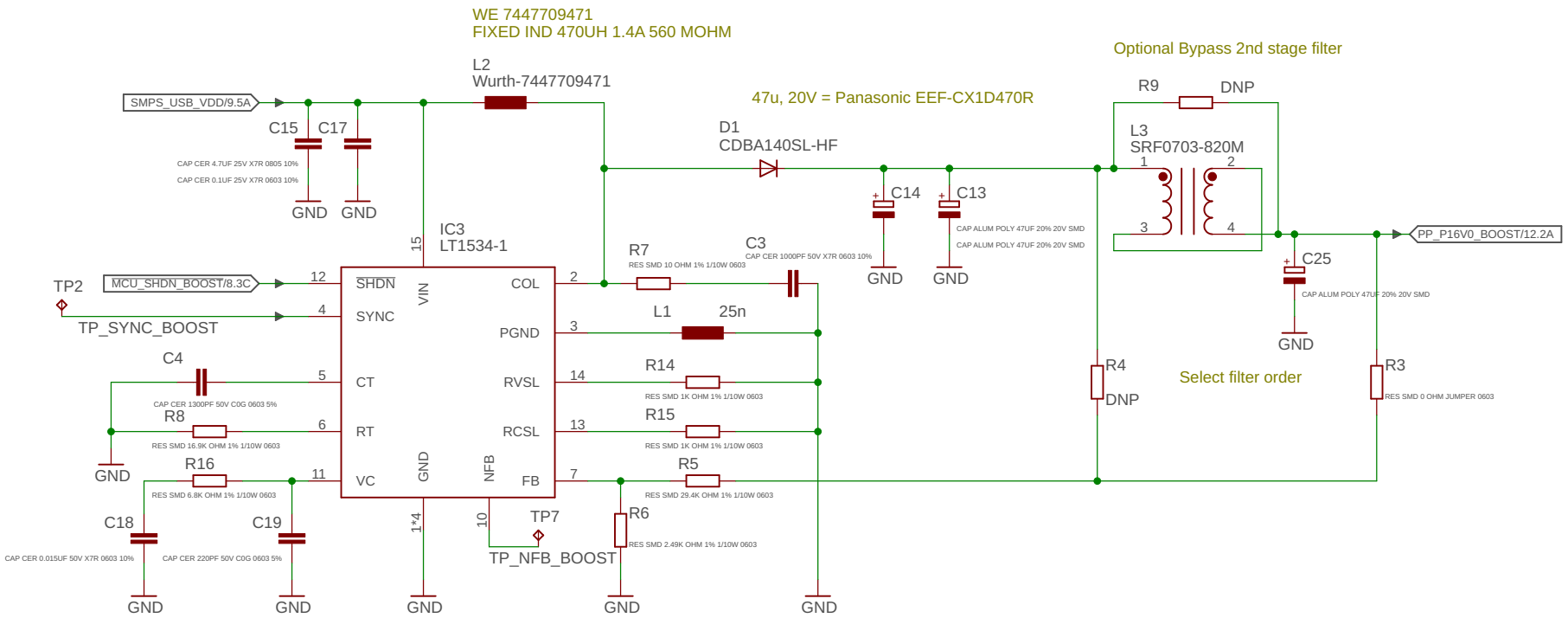
TITLE: aqc-rev3

Document Number: 1 of 1

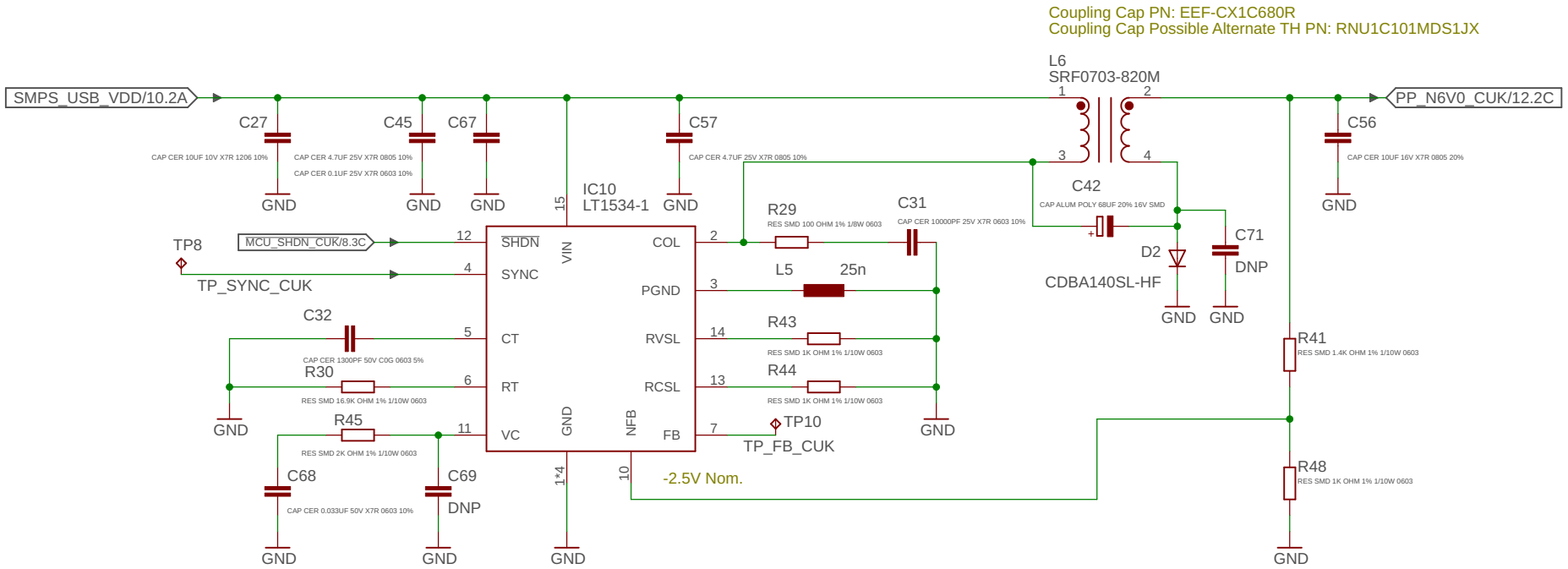
REV: 3.0

Date: 7/8/18 5:34 PM

Sheet: 9/12



POSITIVE DC/DC SMPS	
TITLE: aqc-rev3	
Document Number: 1 of 1	REV: 3.0
Date: 7/8/18 5:34 PM	Sheet: 10/12



NEGATIVE DC/DC SMPS

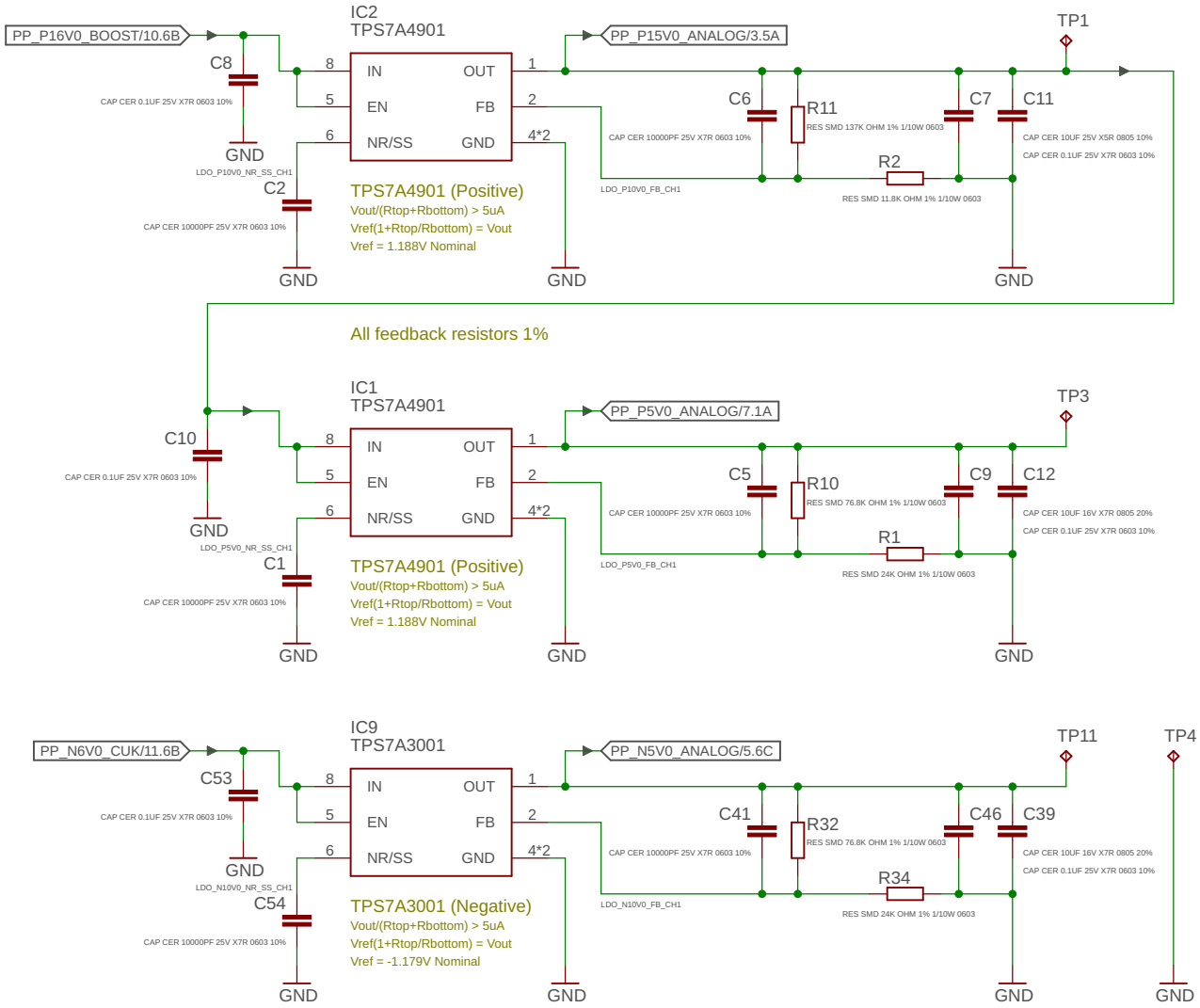
TITLE: aqc-rev3

Document Number: 1 of 1

REV: 3.0

Date: 7/8/18 5:34 PM

Sheet: 11/12



LINEAR POSTREGULATORS

TITLE: aqc-rev3		
Document Number: 1 of 1		REV: 3.0
Date: 7/8/18 5:34 PM	Sheet: 12/12	