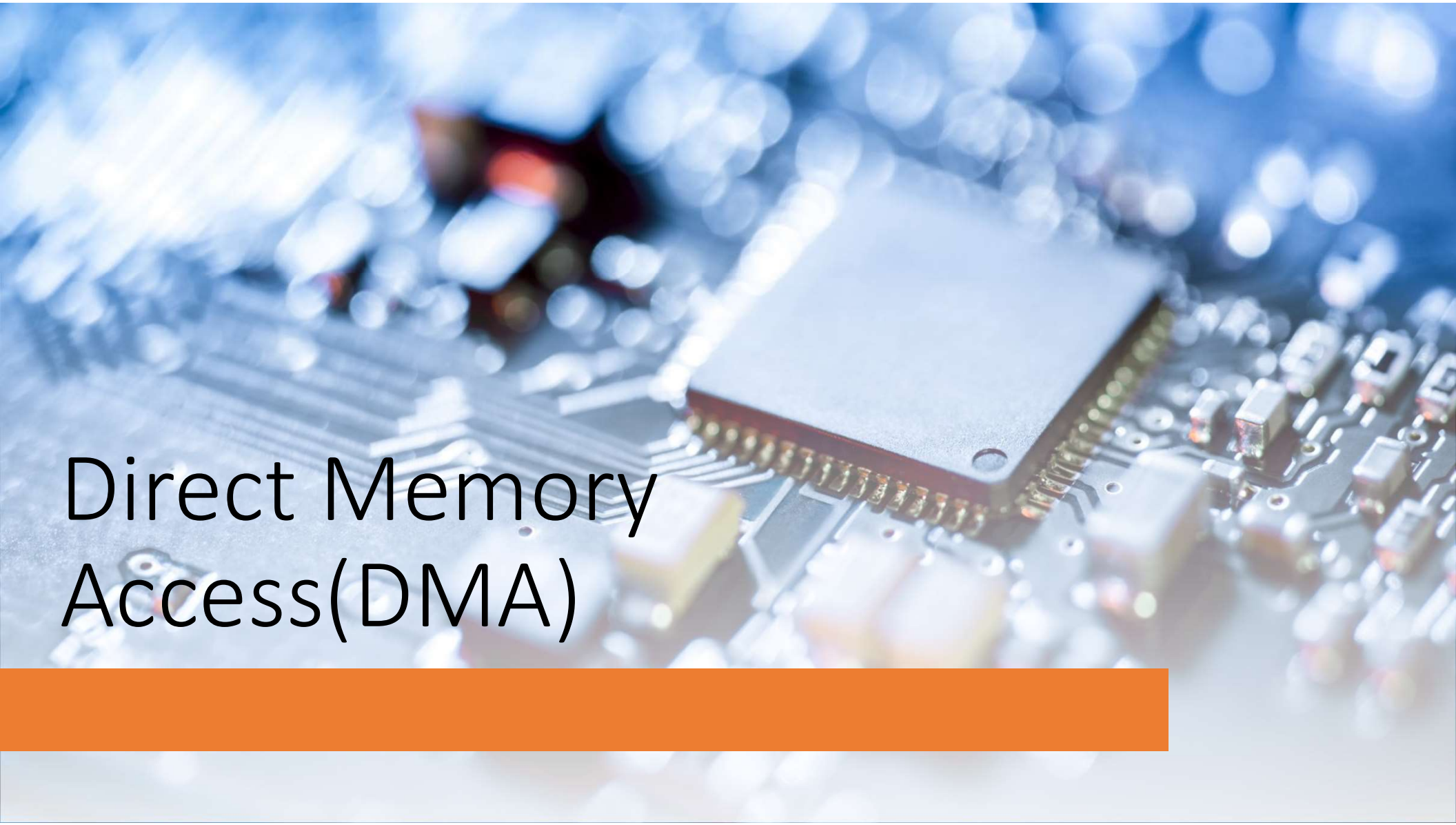
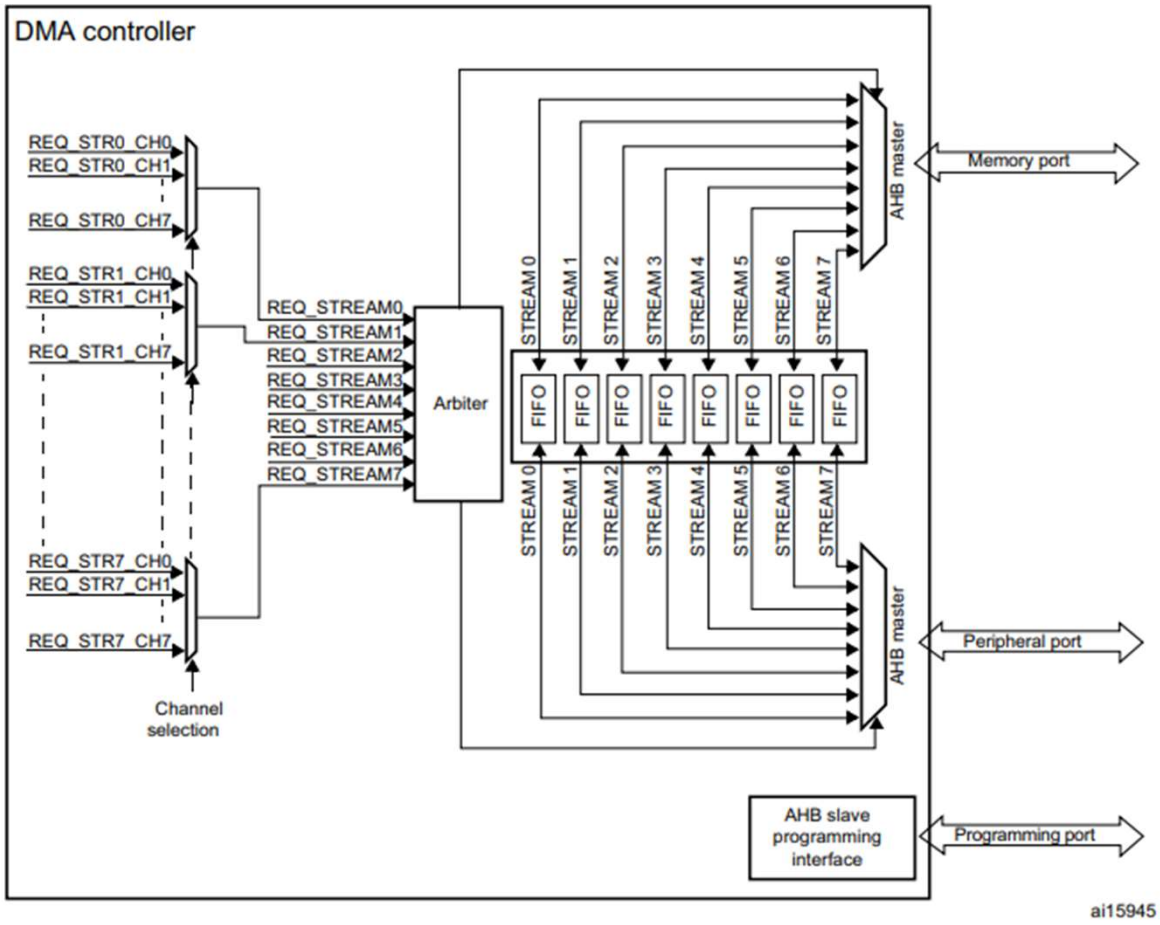


Direct Memory Access(DMA)

What is DMA ?

- DMA is method that allows an Input/Output device to send or receive data directly to or from the main memory bypassing the CPU to speed up memory operations.
- This process is managed by DMA controller(DMAC).

DMA Block Diagram



DMA Controller is an AMBA advanced high-performance bus(AHB) master module present in the microcontroller.

It can carry out the following transactions:

- peripheral-to-memory
- memory-to-peripheral
- memory-to-memory

It features three AHB ports, One slave port and Two Master ports(Memory and Peripheral) .

Each DMA controller consists of 8 streams and provides a unidirectional transfer link between a source and destination.

Each Stream can be configured to perform Memory to Peripherals, Memory to Memory and Peripherals to Memory transfers and only one stream will be active at any given time.

Table 27. DMA1 request mapping (STM32F411xC/E)

Peripheral requests	Stream 0	Stream 1	Stream 2	Stream 3	Stream 4	Stream 5	Stream 6	Stream 7
Channel 0	SPI3_RX	I2C1_TX	SPI3_RX	SPI2_RX	SPI2_TX	SPI3_TX	-	SPI3_TX
Channel 1	I2C1_RX	I2C3_RX	-	-	-	I2C1_RX	I2C1_TX	I2C1_TX
Channel 2	TIM4_CH1	-	I2S3_EXT_RX	TIM4_CH2	I2S2_EXT_TX	I2S3_EXT_TX	TIM4_UP	TIM4_CH3
Channel 3	I2S3_EXT_RX	TIM2_UP TIM2_CH3	I2C3_RX	I2S2_EXT_RX	I2C3_TX	TIM2_CH1	TIM2_CH2 TIM2_CH4	TIM2_UP TIM2_CH4
Channel 4	-	-	-	-	-	USART2_RX	USART2_TX	-
Channel 5	-	-	TIM3_CH4 TIM3_UP	-	TIM3_CH1 TIM3_TRIG	TIM3_CH2	-	TIM3_CH3
Channel 6	TIM5_CH3 TIM5_UP	TIM5_CH4 TIM5_TRIG	TIM5_CH1	TIM5_CH4 TIM5_TRIG	TIM5_CH2	I2C3_TX	TIM5_UP	USART2_RX
Channel 7	-	-	I2C2_RX	I2C2_RX	-	-	-	I2C2_TX

Table 28. DMA2 request mapping (STM32F411xC/E)

Peripheral requests	Stream 0	Stream 1	Stream 2	Stream 3	Stream 4	Stream 5	Stream 6	Stream 7
Channel 0	ADC1	-	-	-	ADC1	-	TIM1_CH1 TIM1_CH2 TIM1_CH3	-
Channel 1	-	-	-	-	-	-	-	-
Channel 2	-	-	SPI1_TX	SPI5_RX	SPI5_TX	-	-	-
Channel 3	SPI1_RX	-	SPI1_RX	SPI1_TX	-	SPI1_TX	-	-
Channel 4	SPI4_RX	SPI4_TX	USART1_RX	SDIO	SPI4_RX	USART1_RX	SDIO	USART1_TX
Channel 5	-	USART6_RX	USART6_RX	SPI4_RX	SPI4_TX	SPI5_TX	USART6_TX	USART6_TX
Channel 6	TIM1_TRIG	TIM1_CH1	TIM1_CH2	TIM1_CH1	TIM1_CH4 TIM1_TRIG TIM1_COM	TIM1_UP	TIM1_CH3	-
Channel 7	-	-	-	-	-	SPI5_RX	SPI5_TX	-

Arbiter

- An arbiter manages the 8 DMA stream requests based on their priority for each of the two AHB master ports (memory and peripheral ports) and launches the peripheral/memory access sequences.

Priorities are managed in two stages:

- **Software**: each stream priority can be configured in the DMA_SxCR register. There are four levels:
- – Very high priority
- – High priority
- – Medium priority
- – Low priority

• **Hardware**:

If two requests have the same software priority level, the stream with the lower number takes priority over the stream with the higher number. For example, Stream 2 takes priority over Stream 4.

DMA Transfer Sequence

Each time a request occurs data item is moved from source to destination and there are two modes of data transfer.

I. Direct mode(FIFO is used without threshold)

II. FIFO mode(FIFO is used with threshold)

Direct Mode : In direct mode the threshold level of the FIFO is not used.

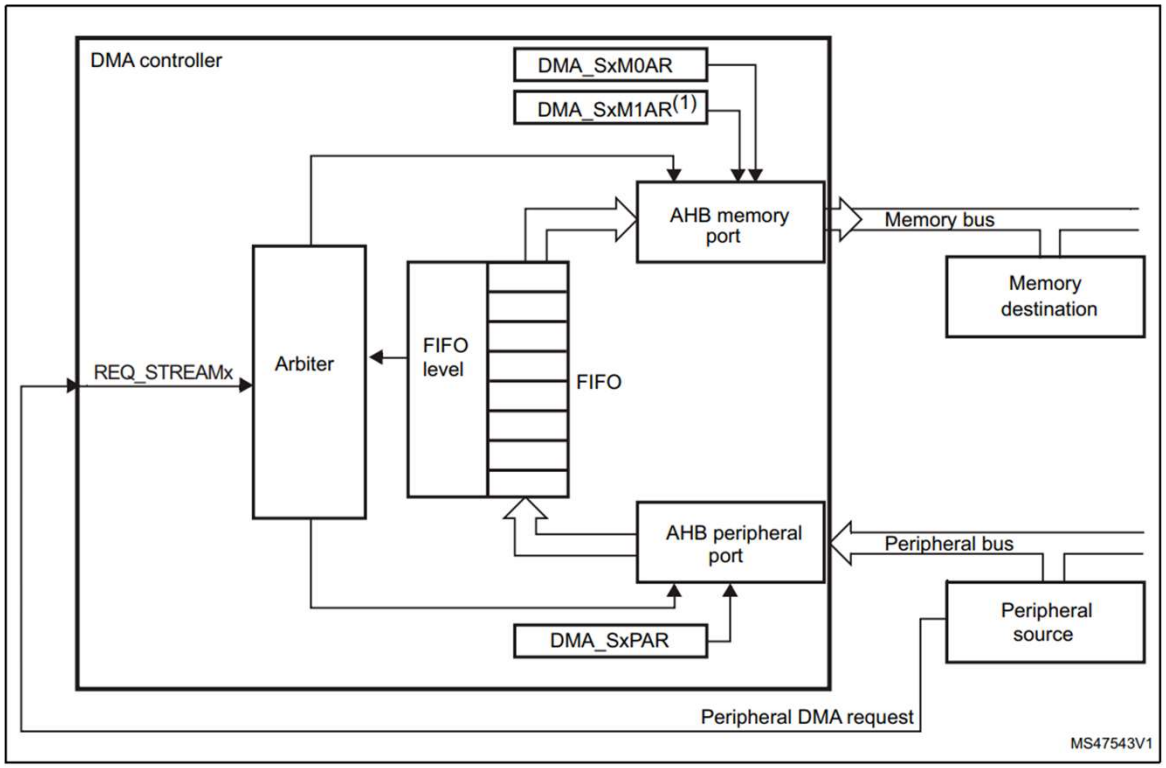
- After each single data transfer from the source to the FIFO, the corresponding data are immediately drained and stored into the destination.

FIFO Mode : In FIFO mode when the threshold level of the FIFO is reached, then the contents of the FIFO are drained and transferred to the destination.

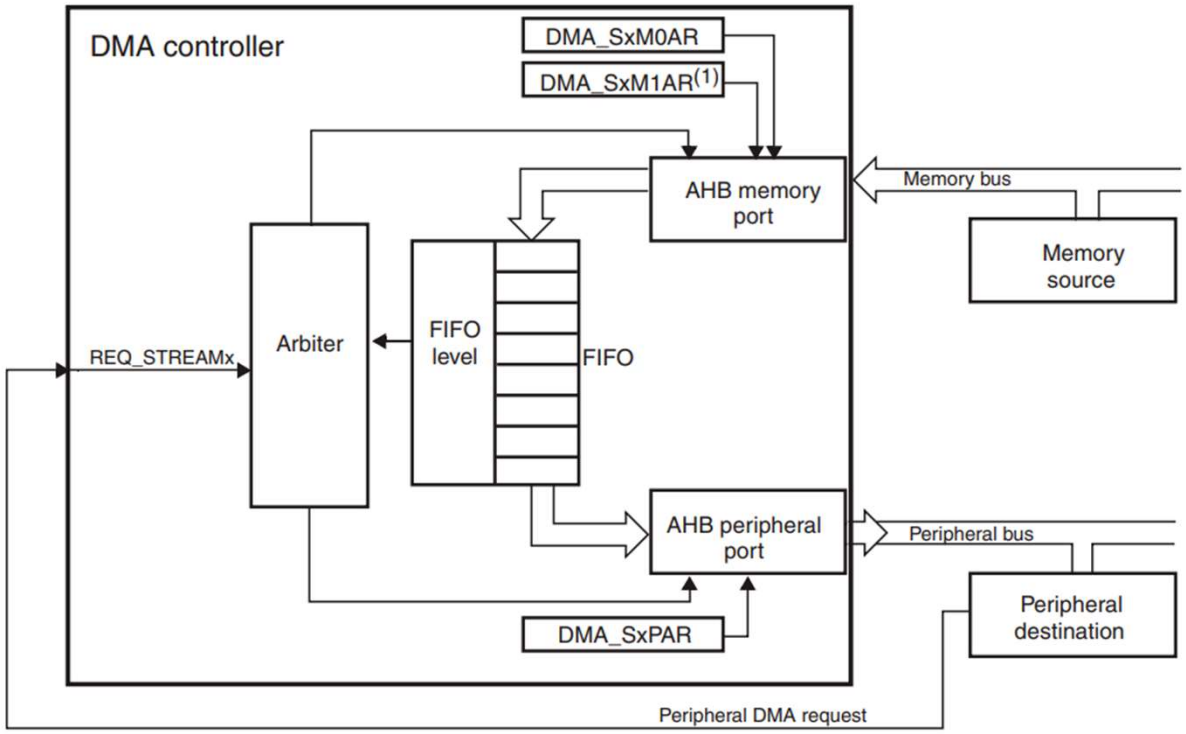
Advantages of FIFO method :

- Memory port is less accessed allowing other pending DMA requests to access the memory port.
- Allowing other bus masters to access the memory, thus decreasing the wait time for other masters.

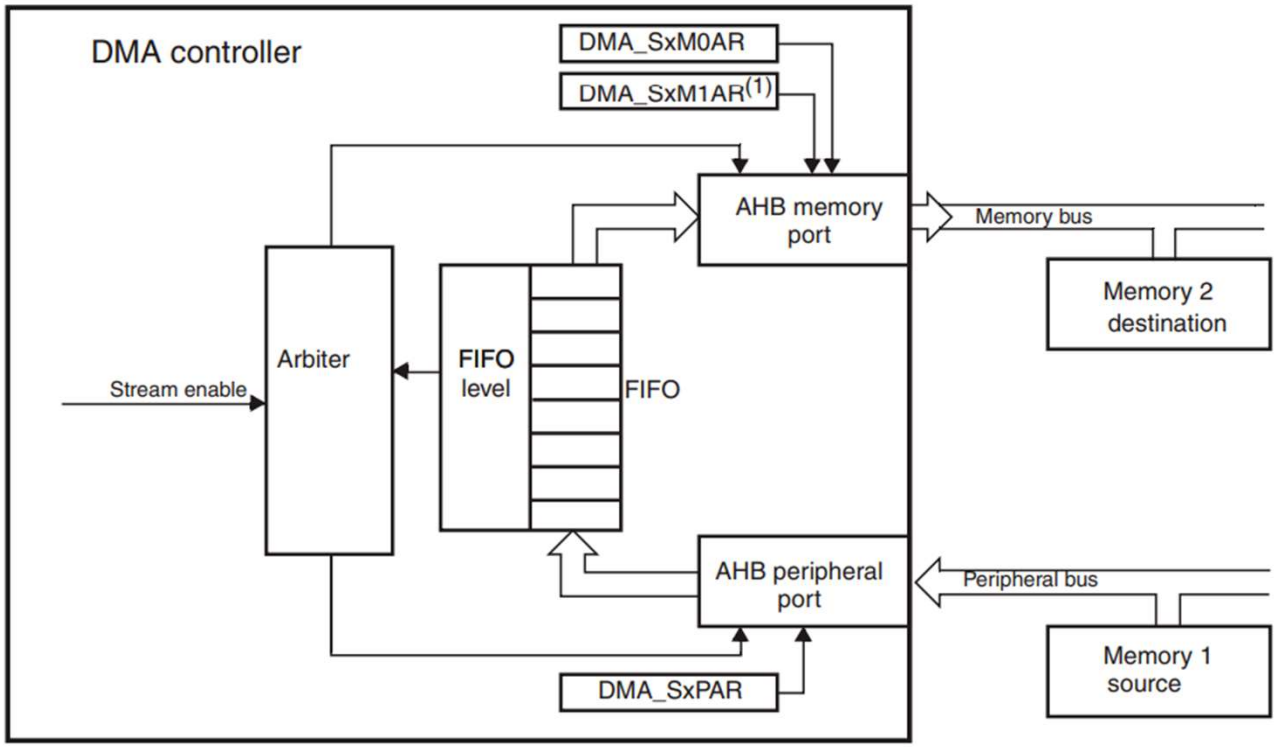
Peripheral-to-memory mode



Memory-to-peripheral mode



Memory-to-memory mode



Thank You