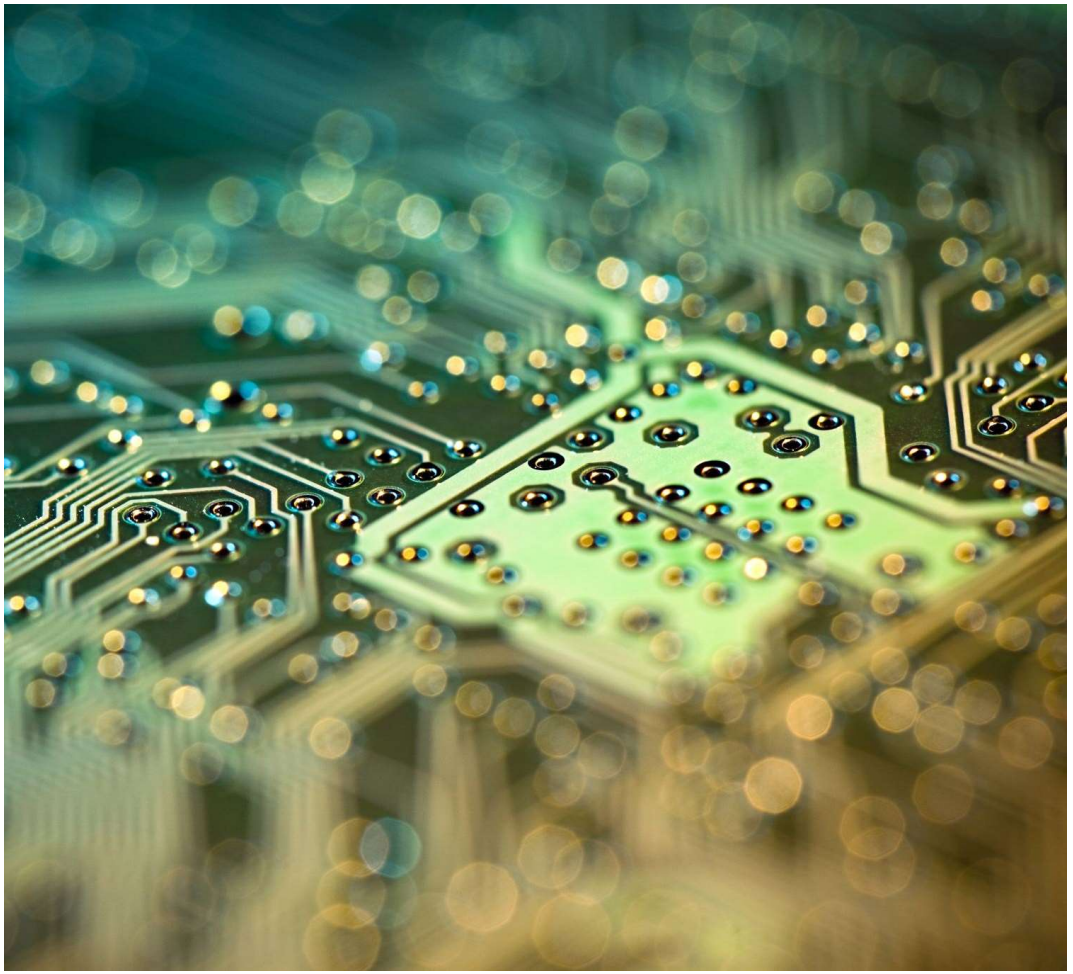
I2C

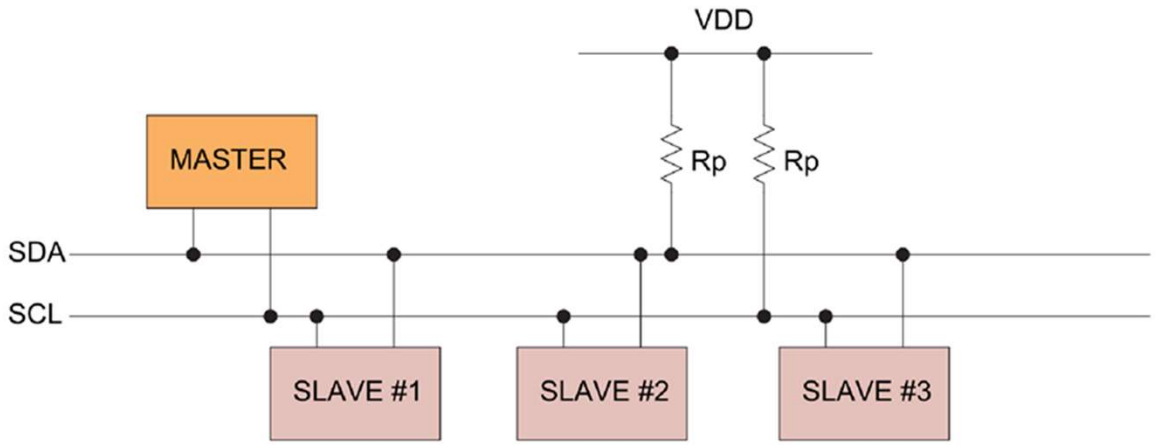


INTER-INTEGRATED CIRCUIT

- Developed by Philips Semiconductor (NXP) in 1982.
- Serial Communication
- Half-duplex communication.
- Widely used for short-distance.
- Two Wired Interface.
- Multi-Master / Multi-Slave Configuration.

CONNECTIONS

- Serial Data (SDA)
- Serial Clock (SCK)



I2C COMMUNICATION MODES

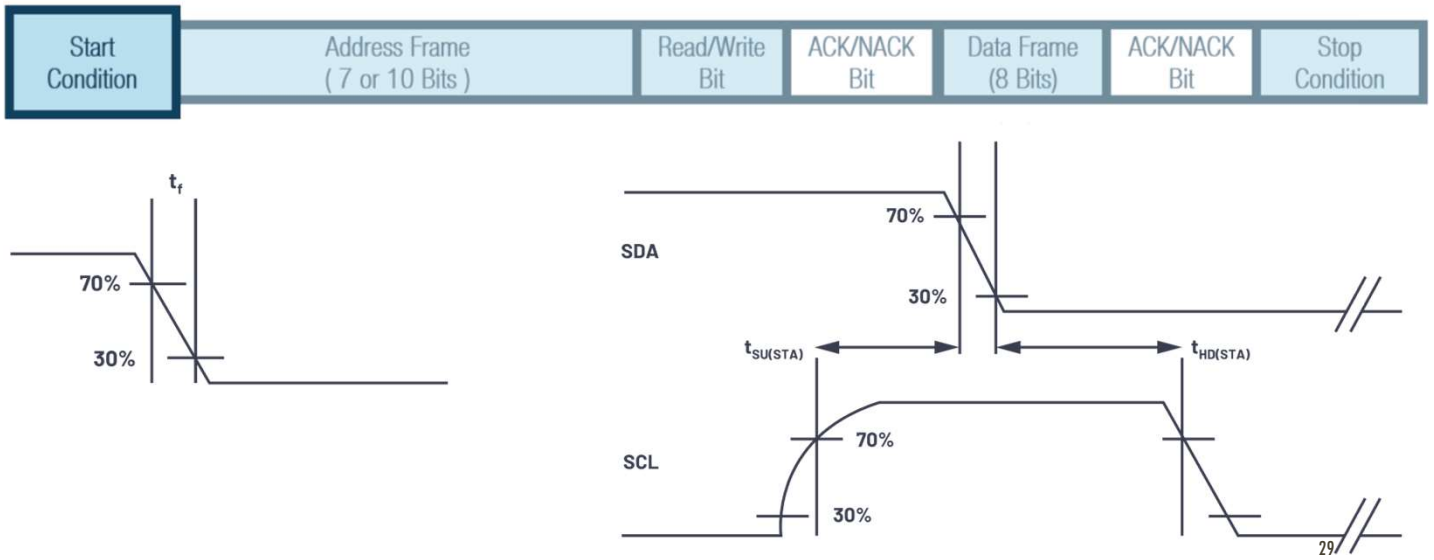
I2C Mode	Speed
Standard Mode	100 kbps
Fast Mode	400 kbps
Fast Mode Plus	1 Mbps
High Speed Mode	3.4 Mbps
Ultra-Fast Mode	5 Mbps

DATA FORMAT


Start Condition
Address Frame (7 or 10 Bits)
Read/Write Bit
ACK/NACK Bit
Data Frame 1 (8 Bits)
ACK/NACK Bit
Stop Condition

START CONDITION

- A start condition always occurs at the start of the transmission and Initiated by Controller (Master).
- SDA line switches from a high voltage level to a low voltage level.



REPEATED START CONDITION

- A start condition can be repeated during a transmission.
- This is a special case, called the repeated start, and is used for changing data transmission direction.

ADDRESS FRAME

The address frame contains a 7-bit or 10-bit sequence

READ/WRITE BIT

A single bit specifying whether the master is sending data to the slave (low voltage level) or requesting data from it (high voltage level).

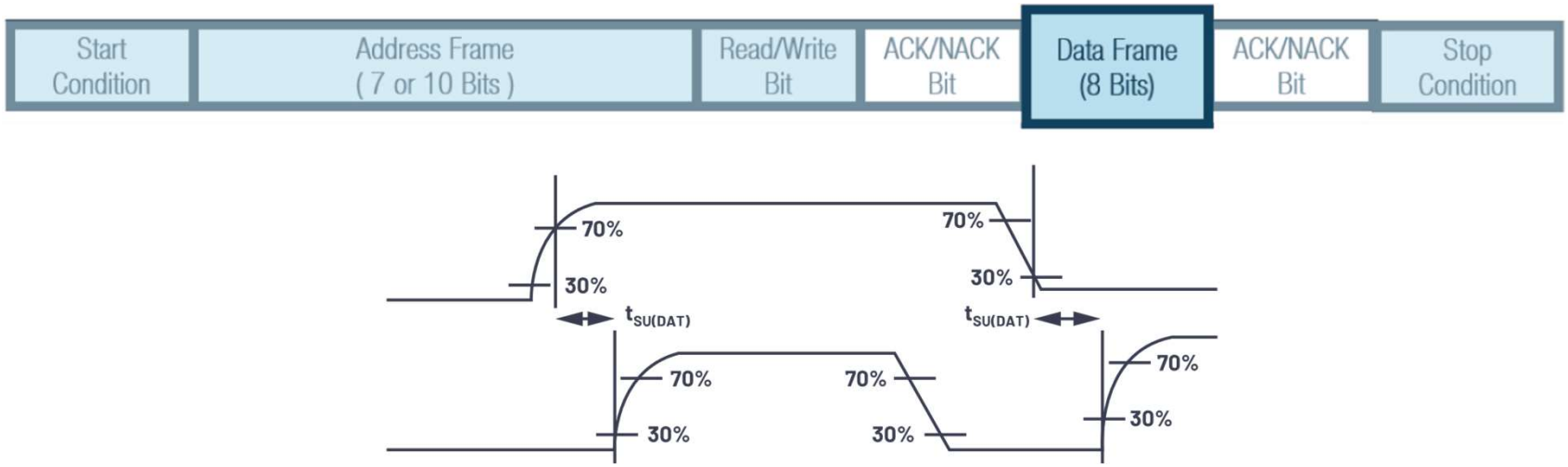
ACK/NACK BIT

Each frame in a message is followed by an acknowledge/no-acknowledge bit.

If an address frame or data frame was successfully received, an ACK bit is returned to the sender from the receiving device

DATA FRAME

After the master detects the ACK bit from the slave, the first data frame is ready to be sent.



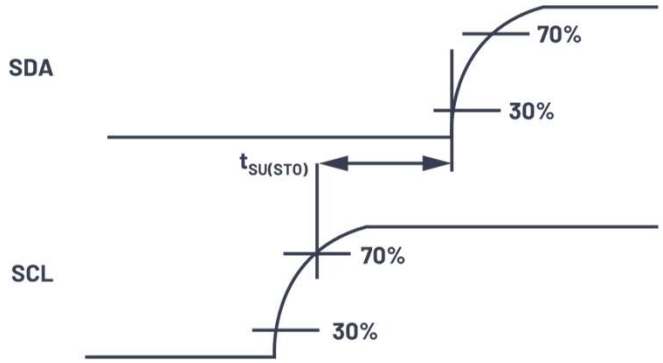
- The data frame is always 8 bits long and sent with the most significant bit first

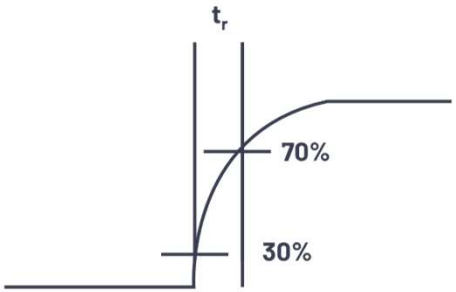
- Each data frame is immediately followed by an ACK/NACK bit to verify that the frame has been received successfully.

- The ACK bit must be received by either the master or the slave (depending on who is sending the data)

STOP CONDITION

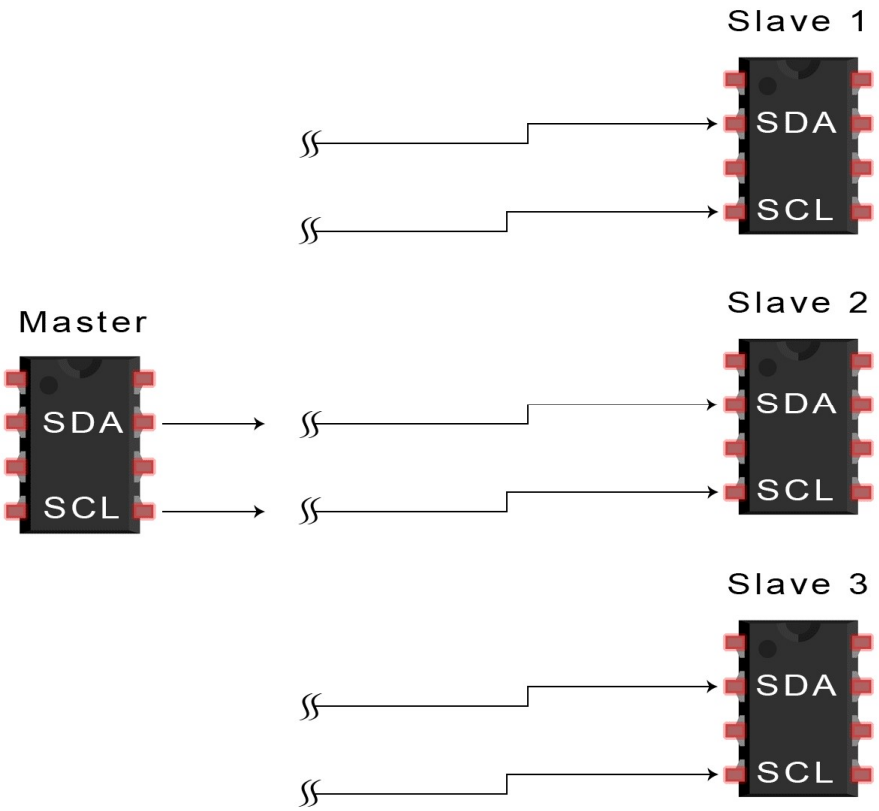
- After all the data frames have been sent, the master can send a stop condition to the slave to halt the transmission.
- SDA line switches from a low voltage level to a high voltage level.



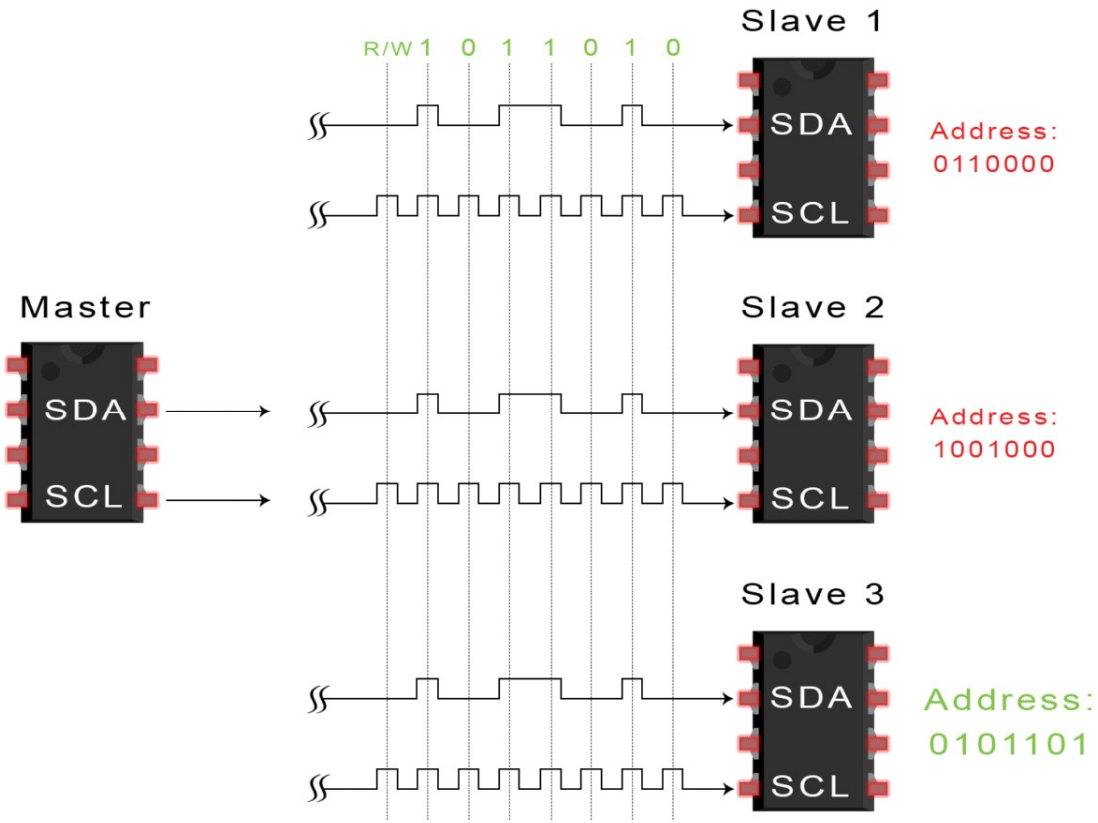


I2C DATA TRANSMISSION

1. The master sends the start condition to every connected slave by switching the SDA line from a high voltage level to a low voltage level before switching the SCL line from high to low.



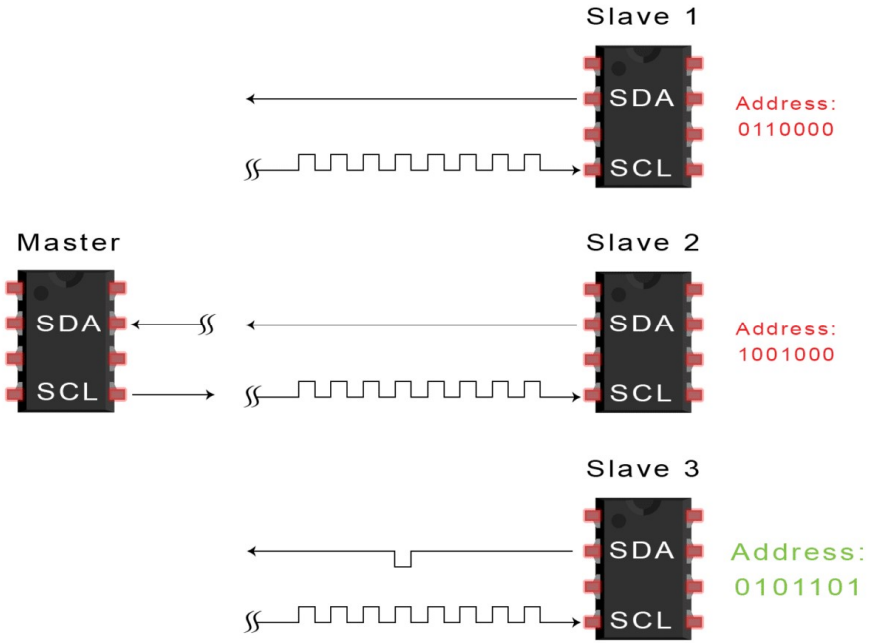
2. The master sends each slave the 7or 10-bit address of the slave it wants to communicate with, along with the read/write bit.



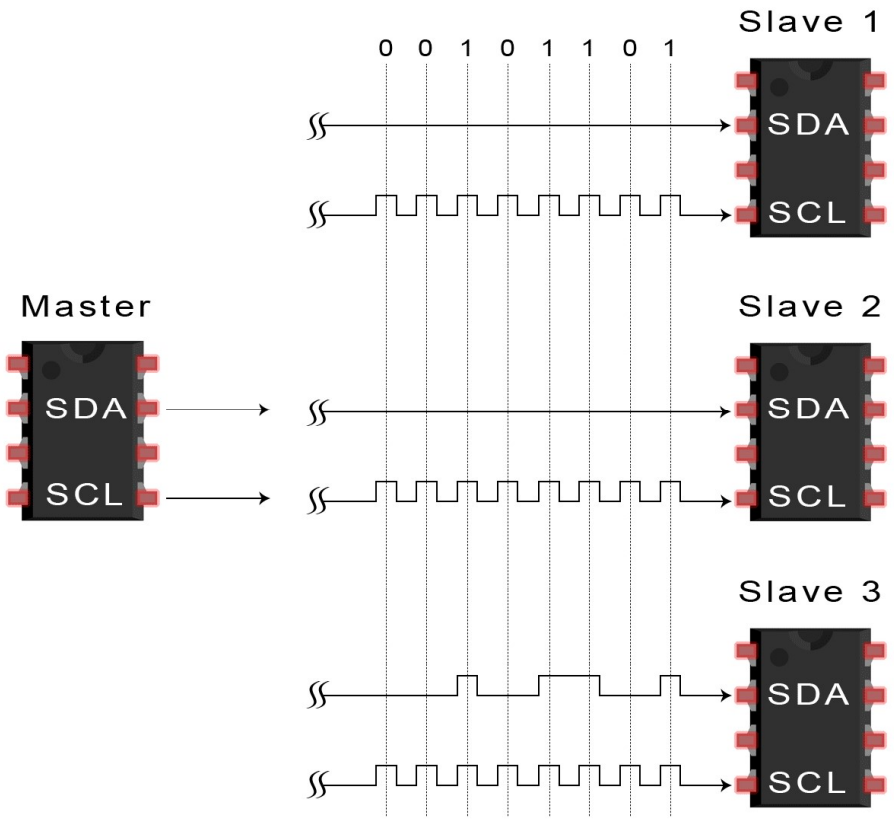
3. Each slave compares the address sent from the master to its own address.

If the address matches, the slave returns an ACK bit by pulling the SDA line low for one bit.

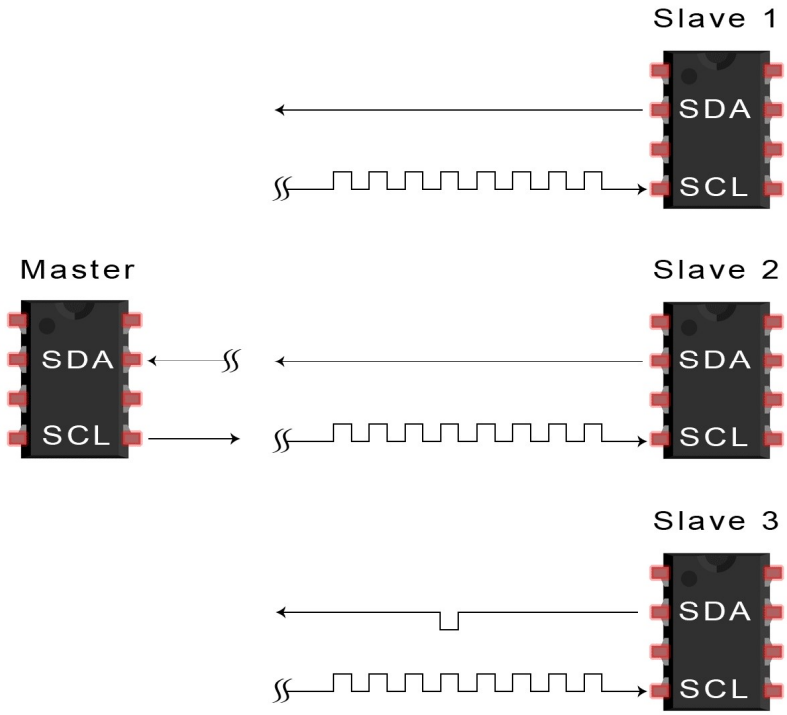
If the address from the master does not match the slave's own address, the slave leaves the SDA line high.



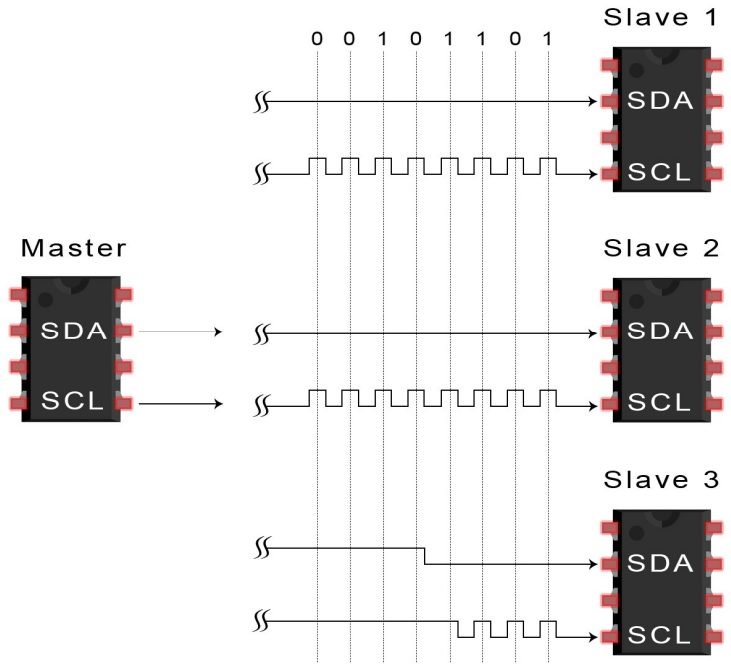
4. The master sends or receives the data frame.



5. After each data frame has been transferred, the receiving device returns another ACK bit to the sender to acknowledge successful receipt of the frame.



6. To stop the data transmission, the master sends a stop condition to the slave by switching SCL high before switching SDA high.

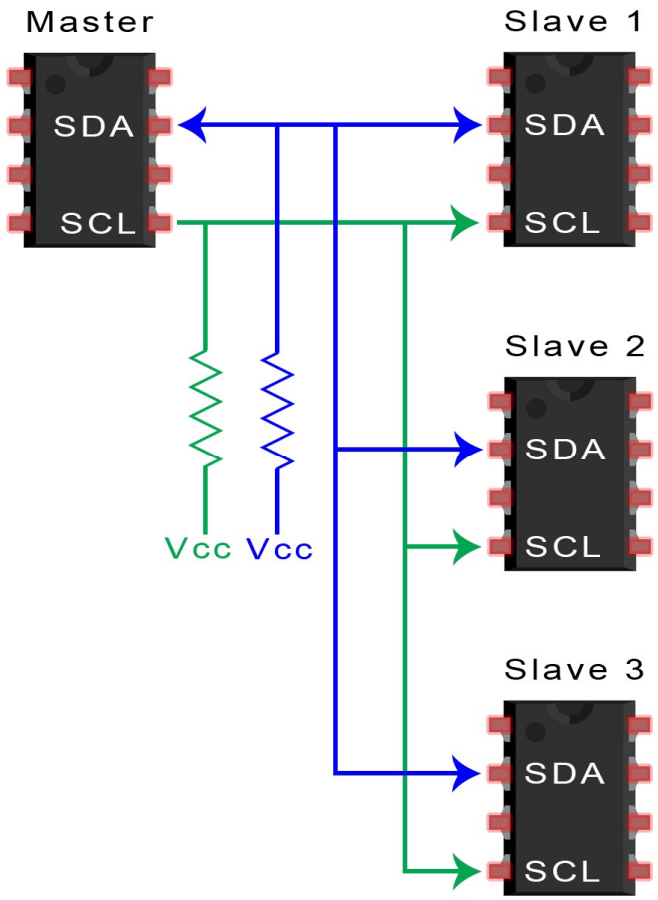


SINGLE MASTER WITH MULTIPLE SLAVES

Because I2C uses addressing, multiple slaves can be controlled from a single master.

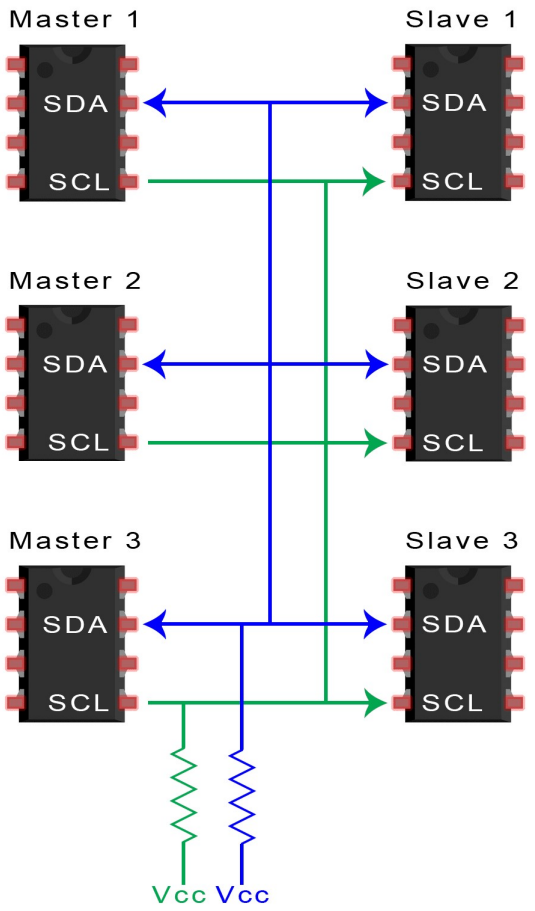
With a 7-bit address, 128 (2^7) unique address are available.

Using 10-bit addresses is uncommon but provides 1,024 (2^{10}) unique addresses.



MULTIPLE MASTERS WITH MULTIPLE SLAVES

Multiple masters can be connected to a single slave or multiple slaves.



ARBITRATION

- Bus arbitration occurs when two or more masters start a transfer at the same time.
- During the transfer, the master constantly monitor the SDA and SCL.
- If the SDA is found high when it was supposed to be low, it assumes that another main is active and immediately stops its transfer.
- This process is called Arbitration.
- The arbitration mechanism ensures that only one device has control of the bus at any given time, and that data is transmitted without any errors.

CLOCK STRETCHING

- An I2C slave is allowed to hold down the clock if it needs to reduce the bus speed.
- A transfer is suspended until the slave releases the SCL line.

PROS

Only uses two wires.

Supports multiple masters and multiple slaves.

ACK/NACK bit gives confirmation that each frame is transferred successfully.

Widely used protocol.

CONS

The size of the data frame is limited to 8 bits.

Slower data transfer rate than SPI

USE CASES

Sensors like TRH, Accelerometers, etc

Displays

Actuators

SUMMARY

Wires	2
Speed	Standard Mode = 100 kbps Fast Mode = 400 kbps Fast Mode Plus = 1 mbps High Speed Mode = 3.4 mbps Ultra-Fast Mode = 5 mpbs
Synchronous or Asynchronous?	Synchronous
Serial or parallel	Serial
No. Of Masters	Unlimited
No. of Slaves	128 (7 bit) or 1024 (10 bit)