

# Digital Systems & Microcontrollers

## Tutorial Quiz Week - 3

16th - 18th September, 2025

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### 16 September (Tuesday)

**Set-A:** What happens with overflow detection when adding:

- a) The most negative number to itself?
- b) The most positive number to the most negative number?
- c) The most positive number to itself?

**Hint:** Use any two n-bit numbers in 2's complement representation to check for overflow in above questions.

What logic design is used in circuits to detect overflow?

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**Set-B:** Using 4-bit two's complement, determine which additions cause overflow:

- a)  $7 + 1$
- b)  $(-8) + (-1)$
- c)  $6 + 3$

What logic design is used in circuits to detect overflow?

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## 17 September (Wednesday)

**Set-A:**

- a) A binary multiplier is used to find the product of an  $n$ -bit number and an  $m$ -bit number. What is the minimum number of bits required to represent the output of this multiplication?  
(Answer in terms of  $n$  and  $m$ )
- b) A  $3\text{-bit} \times 3\text{-bit}$  array multiplier requires how many AND gates and how many full adders?

**Intuition for (a):**

The minimum number of bits required to represent the output of multiplying an  $n$ -bit number and an  $m$ -bit number is  $n + m$  bits. This is because the maximum value of an  $n$ -bit number is  $2^n - 1$  and for an  $m$ -bit number it is  $2^m - 1$ . When you multiply these two maximum values, the result can be as large as  $(2^n - 1) \times (2^m - 1)$ , which is approximately  $2^{n+m}$ . Therefore, to accommodate this maximum product, you need  $n + m$  bits.

**Set-B:** Design a  $4\text{-bit} \times 3\text{-bit}$  array multiplier circuit.

An array multiplier is a digital combinational circuit used for multiplying two binary numbers by employing an array of full adders and half adders. (Taught in Lectures)

## 18 September (Thursday) Slot-1

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**Set-A:** Design a  $16 \times 1$  multiplexer using two  $8 \times 1$  multiplexers with enable.

Optional: You may use a  $2 \times 1$  multiplexer in place of enable

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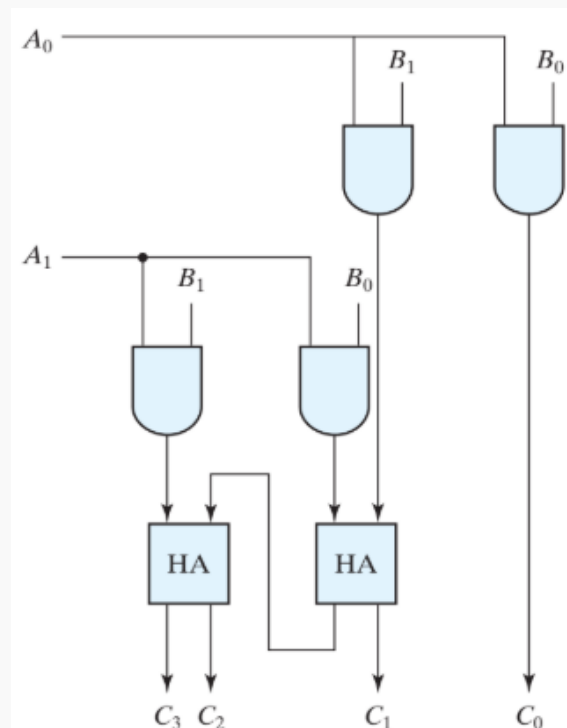
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**Set-B:** Design a  $4 \times 16$  demultiplexer using two  $3 \times 8$  demultiplexers with enable.

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## 18 September (Thursday) Slot-2

Say we create a 2-bit binary multiplier as shown below:



However, when we test the circuit, we find that the output is correct only for the four cases when  $A=10$  or  $11$  and  $B=01$  or  $11$ . We investigate and find out that because of a problem with the breadboard, one of the internal wires is permanently getting connected to either ground or VDD, i.e., it is either stuck at ground or VDD level. Can you find out which wire is problematic and what value it is getting stuck at?

[DSM 2023 Midsem]