BASIC LOGIC GATES AND DE MORGAN'S LAW

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ROLL NO.: 2025102061

TABLE NO.: 13

GROUP: G9

EXPERIMENT PART-A: Gate Identification

Aim:

To understand the architecture and logic of a given IC.

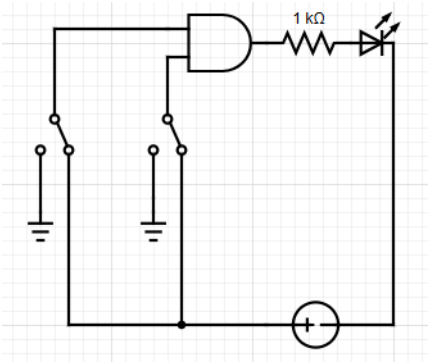
Components Required:

1. Digital Test Kit (DSM Lab Kit)
2. Connecting wires
3. Breadboard
4. Given IC

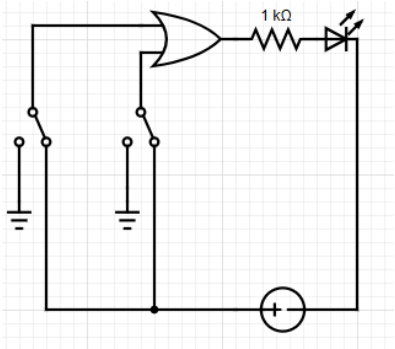
Circuit Implementation and Reference Circuit:

In this experiment, the given logic gate IC was connected to the Digital Test Kit to check its logic behavior and to identify the gate. The circuit was put together using standard digital logic methods.

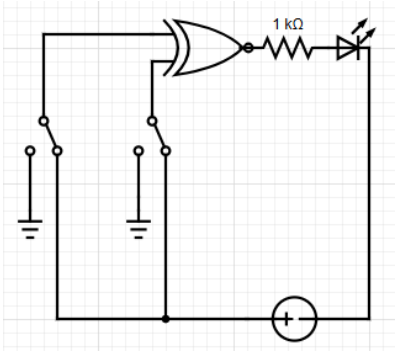
AND Gate



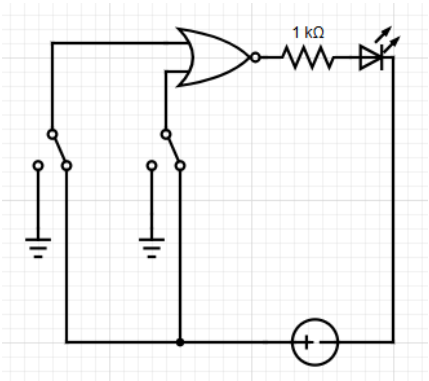
OR Gate



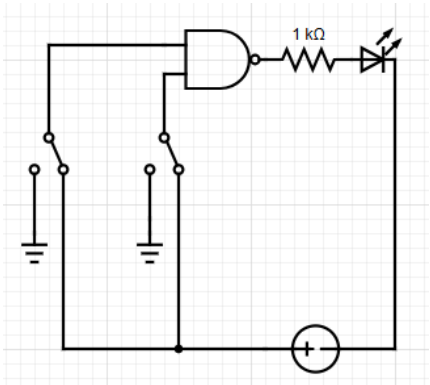
XOR Gate



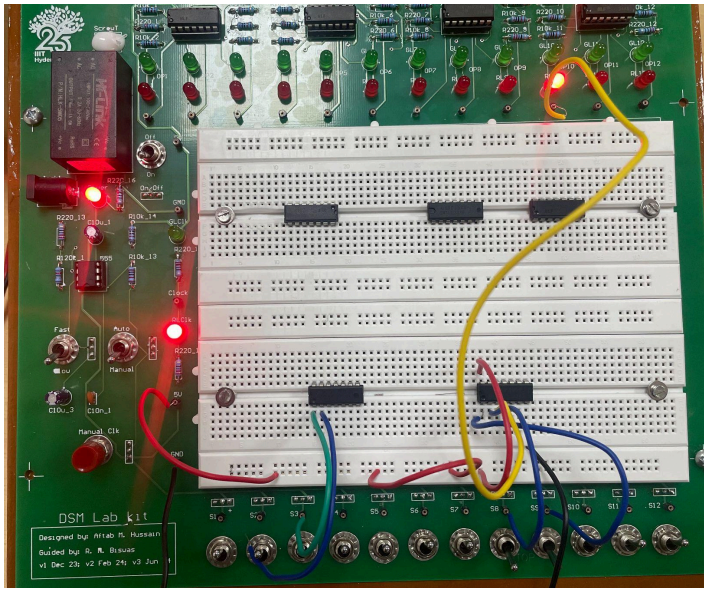
NOR Gate



NAND Gate



Visual Circuit:



Procedure:

1. Verify the functionality of Digital Test Kit by testing the LEDs and input switches.
2. Pick an IC and differentiate it as ‘74 series’ or ‘40 series’
3. Check the connections of the unknown IC with the breadboard properly.
4. Connect VCC and GND to the IC.
5. Connect input and output using the schematic of the gate type given in the lab manual.
6. Observe the output by changing the input signals.
7. Repeat this process for all of the given ICs.

Observation:

The experimental observations:

IC 7432

Input A	Input B	Output
1	1	1
1	0	1
0	1	1
0	0	0

IC 7408

Input A	Input B	Output
1	1	1
1	0	0
0	1	0
0	0	0

IC 7486

Input A	Input B	Output
1	1	0
1	0	1
0	1	1
0	0	0

IC 7400

Input A	Input B	Output
1	1	0
1	0	1
0	1	1
0	0	1

IC CD4001 B

Input A	Input B	Output
1	1	0
1	0	0
0	1	0
0	0	1

Result and Analysis:

The gates can be concluded from the truth table as follows:

IC 7432 - OR Gate

IC 7408 - AND Gate

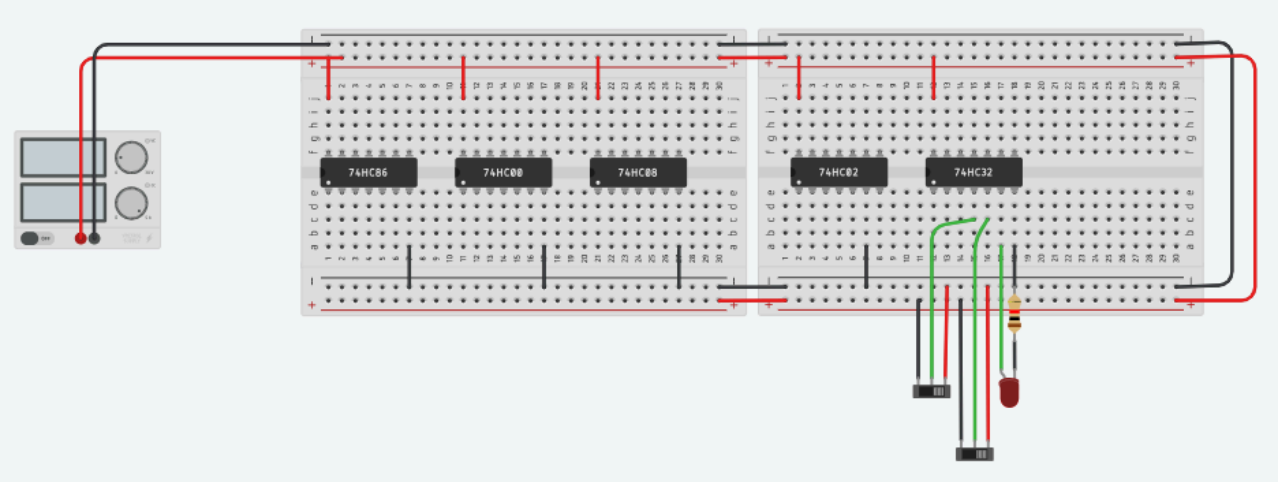
IC 7486 - XOR Gate

IC 7400 - NAND Gate

IC CD4001 B - NOR Gate

Circuit Simulation:

https://www.tinkercad.com/things/7qSBiYLhjgr-lab-2-part-a?sharecode=LMoKx4CBqSeWD5WlaJNE71lXfYEc1tbx8fqu4JAhCBQ



Conclusion:

The experiment was successfully carried out, leading to the following outcomes:

- **IC Identification:** Understood the pin configuration, power connections, and internal logic of the given IC.
- **Practical Familiarity:** Gained hands-on experience in handling and testing ICs using breadboards and digital kits.
- **Functional Verification:** Validated the logical behavior of the IC against its datasheet specifications.
- **System Insight:** Strengthened the link between theoretical IC architecture and its practical implementation.

The experiment confirmed that the IC performed as expected, enhancing understanding of logic device structure and usage in digital systems.

EXPERIMENT PART-B: De Morgan's Law

Aim:

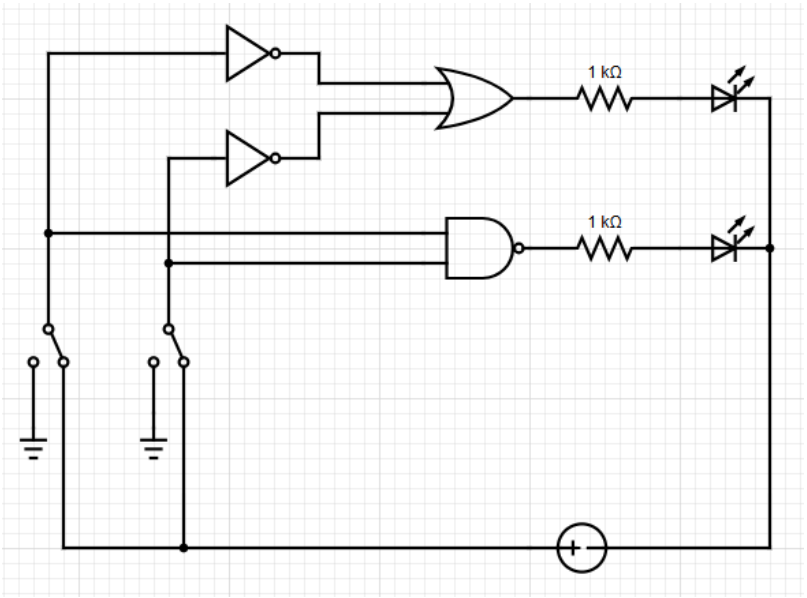
To verify the two De Morgan's laws using logic gates (ICs) by designing and implementing equivalent logic circuits, and to observe their truth tables experimentally.

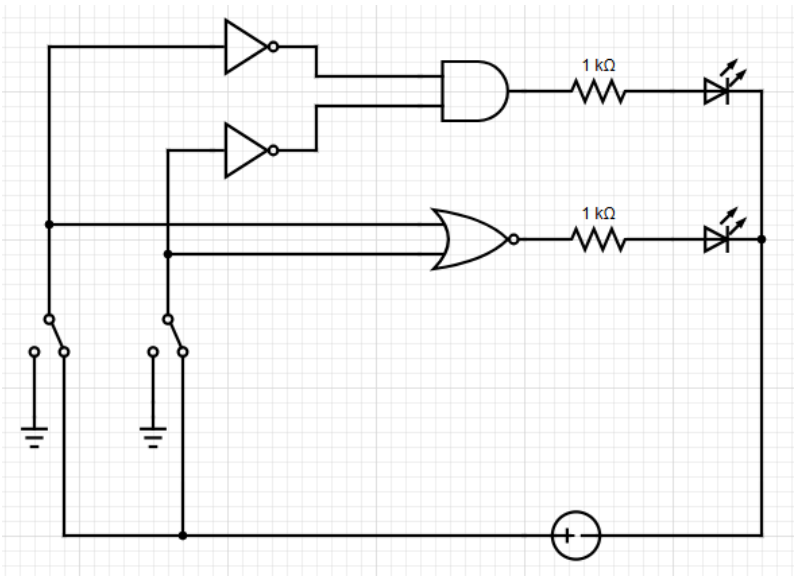
Components Required:

1. Digital Test Kit (DSM Lab Kit)
2. Connecting wires
3. Breadboard
4. NAND Gate, NOR Gate, AND Gate, OR Gate, NOT Gate
   (note: the circuit can be performed without using NOT Gate)

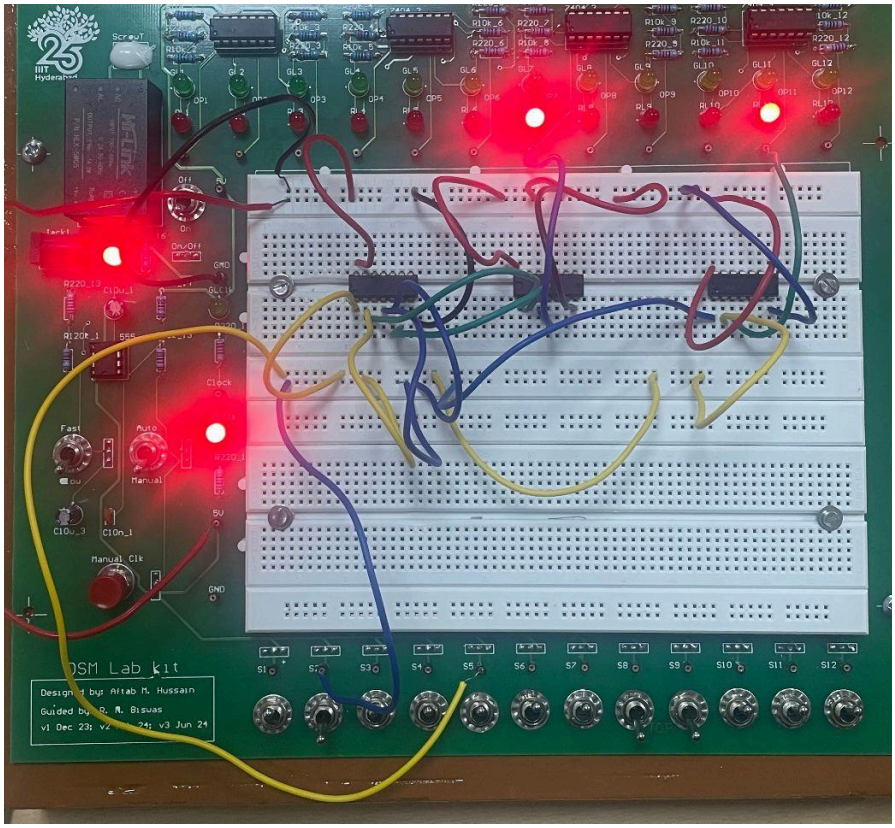
Circuit Implementation and Reference Circuit:

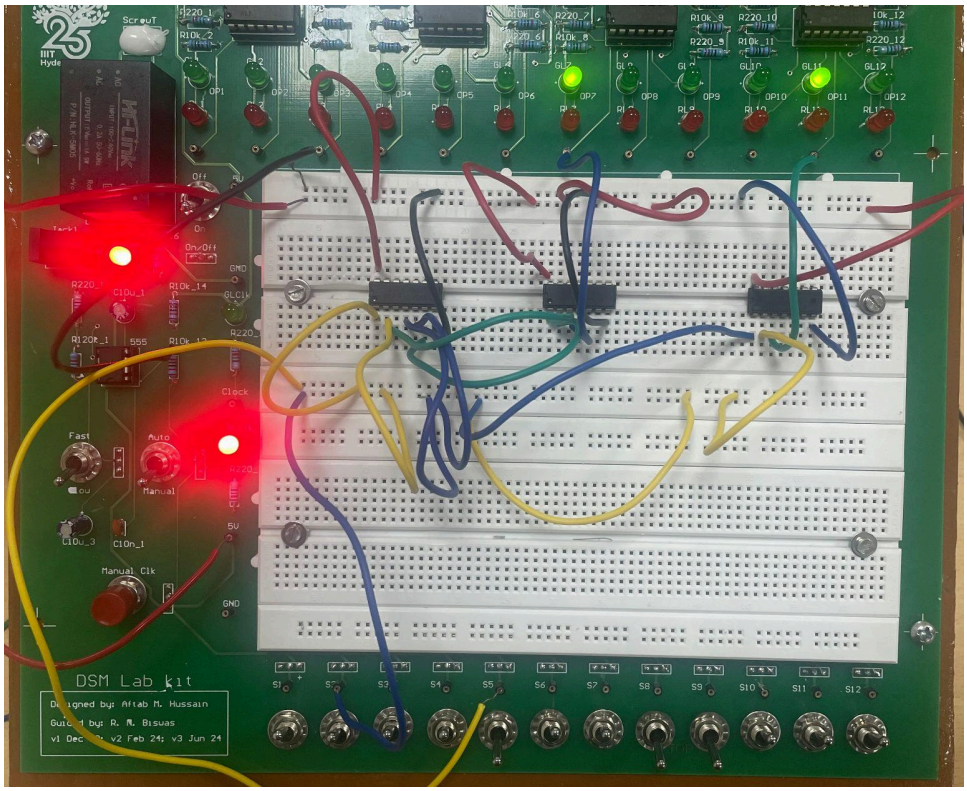
In this experiment, De Morgan's laws were verified using NAND and NOR gates. A NAND gate is equivalent to a NOT gate followed by an OR gate, while a NOR gate is equivalent to a NOT gate followed by an AND gate. Using these equivalences, both laws were implemented and their outputs observed on LEDs with common VCC and GND connections.





Visual Circuit:





Procedure:

1. Test the Digital Test Kit by checking LEDs and switcher.
2. Collect the required ICs: 7400, 7402, 7404, 7408, 7432.
3. Place the ICs on the breadboard and connect VCC and GND.
4. Connect inputs A and B using switches from the test kit.
5. Build the first De Morgan’s law using a NAND gate and its equivalent (NOT + OR).
6. Build the second De Morgan’s law using a NOR gate and its equivalent (NOT + AND).
7. Connect outputs to LEDs through resistors.
8. Change input combinations and observe the outputs.

Observation:

Upon varying the values of the inputs using the digital kit, the following observations can be made:

NOR Gate and its equivalent:

Input A	Input B	Output - A'.B'
0	0	1
0	1	0
1	0	0
1	1	0

Input A	Input B	Output - (A+B)'
0	0	1
0	1	0
1	0	0
1	1	0

From the obtained observations it is clear that NOR gate is equivalent to NOT gate followed by AND gate.

NAND Gate and its equivalent:

Input A	Input B	Output - A'+B'
0	0	1
0	1	1
1	0	1
1	1	0

Input A	Input B	Output - (A.B)'
0	0	1
0	1	1
1	0	1
1	1	0

From the obtained observations it is clear that NAND gate is equivalent to NOT gate followed by OR gate.

Result and Analysis:

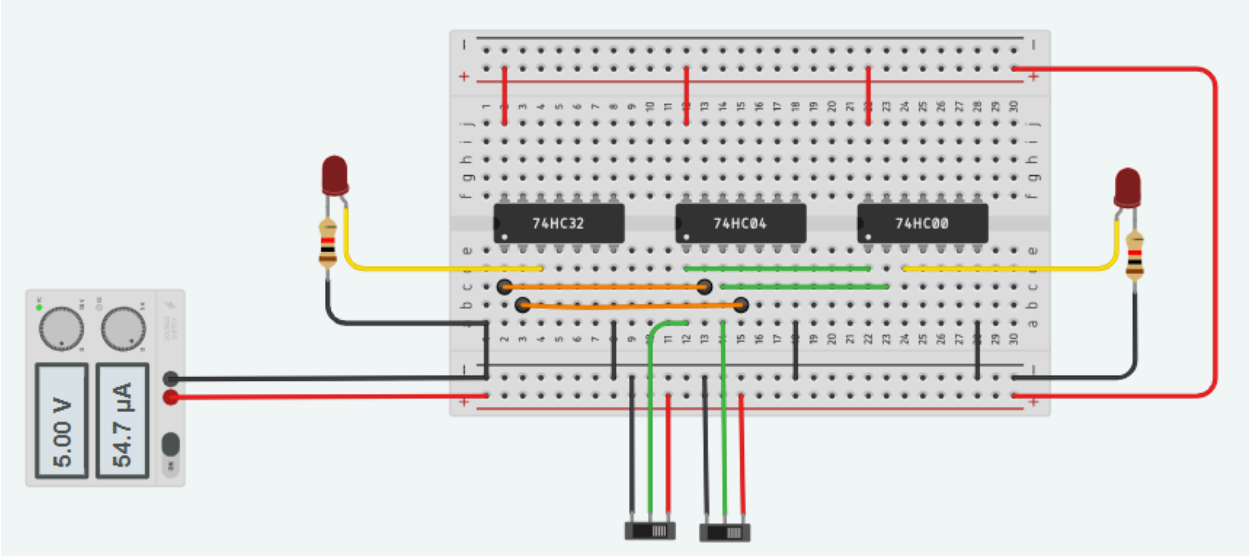
From the experiment it is clear that:

1. (A'+B') = (A.B)'
2. (A'.B') = (A+B)'

Hence, De Morgan's Law is Proved.

Circuit Simulation:

https://www.tinkercad.com/things/9f3m1IDlB8I-de-morgans-law-1?sharecode=JH79MrhqhzrIYT0wOZOKhtqrke0LOnaJMINL8VgJIGg



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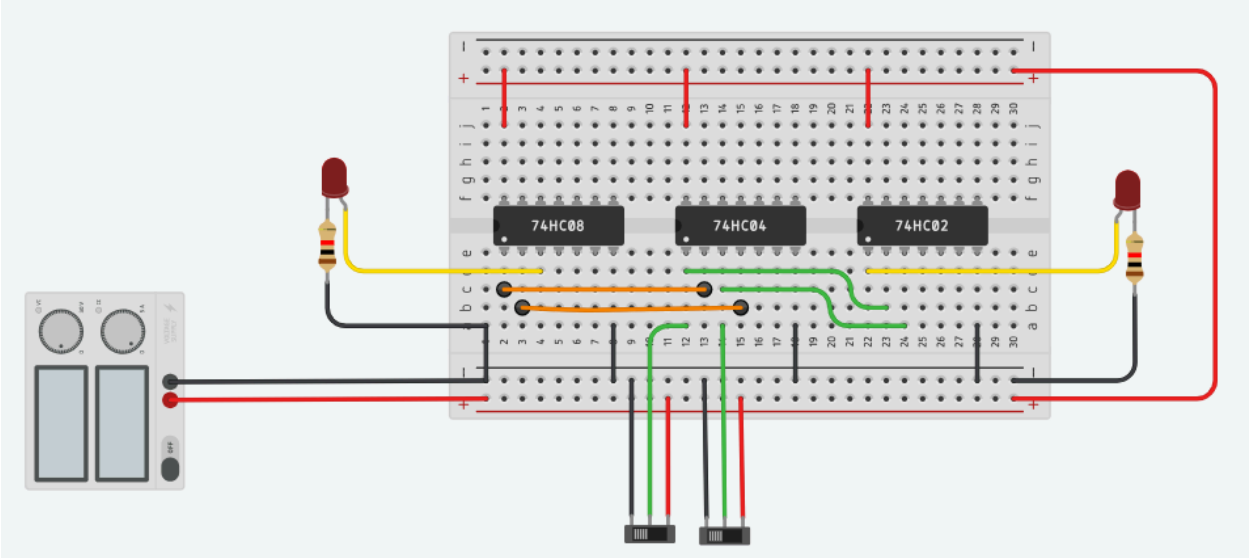

Conclusion:

The experiment was successfully carried out, resulting in the following outcomes:

- **Law Verification:** Both of De Morgan's laws were experimentally verified using equivalent logic gate circuits.
- **Truth Table Analysis:** Observed truth tables matched theoretical predictions, confirming the equivalence.
- **Circuit Design Skills:** Practiced designing and implementing gate-level circuits for logical expressions.
- **Conceptual Clarity:** Reinforced understanding of Boolean algebra and its physical realization using ICs.

The experiment demonstrated that the designed circuits accurately reflected De Morgan's theorems, validating fundamental principles of digital logic.