International Institute of Information Technology, Hyderabad

EC2.101 - Digital Systems and Microcontrollers

Model Exam - Grading Rubric & Solutions Outline (Unofficial)

General Instructions to Graders

- **Process over Product:** For design questions, full marks should be awarded for correct logic and minimization steps (K-Maps), even if a minor transcription error occurs in the final circuit drawing.
- **Transistor Counts:** Allow for small variations in transistor counts if the student uses a valid alternative topology (e.g., Transmission gates vs. standard CMOS), provided they state their assumptions.
- **Assembly Code:** Logic and comments are more important than exact syntax, provided the pseudo-code/mnemonics align with the instruction set provided in the course.

Detailed Marking Scheme

Q. No	Expected Solution & Criteria	Marks
	Q1. Base System Concepts [15 Marks]	
1(a)	**Base-5 Even/Odd Proof**	**[5]**
	• Student represents number as $N = 5k + r$.	[1]
	• Mathematical Argument: Since 5 is odd, $5k$ alternates parity depending on k. Therefore, r (LSD) alone is insufficient to determine total parity.	[2]
	• Counter-example provided (e.g., $(12)_5 = 1 \times 5 + 2 = 7$ which is Odd, but LSD is 2 which is Even).	[2]
1(b)	**Base-3 Divisibility Logic**	**[10]**
	• Truth Table construction: Inputs 4 bits (representing two ternary digits A_1A_0), Output 1 if Value % 4 == 0. *Note: Input combinations representing digits ¿ 2 must be treated as Don't Cares (X).*	[3]
	• K-Map Simplification: Correct grouping including Don't Cares.	[4]
	• Final Circuit Drawing: Logic gates matching the expression.	[3]
	Q2. Arithmetic Optimization [15 Marks]	
2(a)	**Absolute Difference** $\|A - B\|$	**[8]**
	• Truth Table: 4 inputs (A=2 bits, B=2 bits), 2 outputs.	[2]
	• K-Maps: Separate maps for Output Bit 0 and Bit 1.	[3]
	• Minimized Expressions: Correct SOP or POS equations.	[3]
2(b)	**CMOS Implementation & Comparison**	**[7]**
	• CMOS Schematic: Correct Pull-up (PMOS) and Pull-down (NMOS) networks corresponding to the logic.	[3]
	• Transistor Count (Custom): Calculation based on the schematic.	[2]
	• Comparison: Correctly estimating transistors for (Adder + XORs for inversion) and concluding which is smaller.	[2]
	Q3. Sequential Design (Fibonacci) [15 Marks]	
3(a)	**JK Counter Design**	**[10]**
	• State Sequence: Identifying states ($0000 \to 0001 \to 0010 \to 0011 \to 0101 \to 1000 \to 1101 \to 0000$).	[2]
	• Excitation Table: Correct use of JK excitation ($0 \to 0, 0 \to 1, 1 \to 0, 1 \to 1$).	[2]

	• K-Maps: 4 maps (or 8 for separate J and K) solving for inputs. • Circuit/Equation: Correct expressions for J_A, K_A, etc.	[4] [2]
3(b)	**Self-Correction** • Unused States Identification: Listing states not in Fibonacci sequence (e.g., 4, 6, 7, 9...). • Logic Implementation: Ensuring 'Next State' for these unused states points to '0000' or a valid sequence state.	**[5]** [2] [3]
Q4. Circuit Analysis [10 Marks]		
4(a)	**Timing Diagram** • Correct initialization (0000). • Correct shifting behavior for first 3 cycles. • Correct handling of the inverted feedback ($E' \to A$). • Correct handling of the clock gating (B' driving C's clock).	**[4]** [1] [1] [1] [1]
4(b)	**State Diagram** • Identifying all valid states in the loop. • Identifying the cycle length (how many states before repeat).	**[4]** [3] [1]
4(c)	**Johnson Counter Theory** • Correct formula stated ($2k$ or $2n$ states).	**[2]** [2]
Q5. Microcontroller Assembly [10 Marks]		
5(a)	**Search Algorithm Code** • Initialization: Loading pointers (0x200, 0x201) and Loop Counter (from 0x220). • Fetch Loop: Correctly incrementing memory pointer and fetching data. • Comparison Logic: Subtraction or XOR to check equality with Target V. • Control Flow: Branch if Zero (Match found) vs Branch if Counter != 0 (Continue).	**[10]** [2] [3] [3] [2]
Q6. Conversions [5 Marks]		
6	**Calculations** (a) $(45.6)_{10} \to$ Binary (101101.1001...). (b) Base 5 $\to$ Base 8 (Intermediate Base 10 step implied: $123_5 = 38_{10} = 46_8$). (c) 2's Complement Subtraction (1001 + (0101)... check for overflow). (d) Signed Mag (10001111) and 2's Comp (11110001).	**[5]** [1] [1] [1] [2]