Digital Voting Machine using Verilog HDL

Project Report

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Introduction

The digital voting machine is designed using Verilog HDL to simulate an electronic voting system. It allows multiple candidates to be voted for, and the system keeps track of the votes in a secure manner. The main objective of this project is to demonstrate how digital systems and HDL can be used to implement real-world applications such as voting machines.

Block Diagram

The block diagram of the voting machine consists of the following components:
1. Clock & Reset Unit – Provides synchronization and initializes the system.
2. Candidate Inputs – Buttons or signals representing votes for each candidate.
3. Voting Logic – Determines which candidate receives the vote.
4. Vote Counter – Maintains the count of votes for each candidate.
5. Display/Output Unit – Shows the final count of votes.

Circuit Explanation

The circuit works by taking input signals from voters corresponding to each candidate. When a candidate button is pressed, the respective counter increments by one. The clock synchronizes the operations, and the reset signal initializes the counters. At the end of the voting process, the system displays the total count for each candidate.

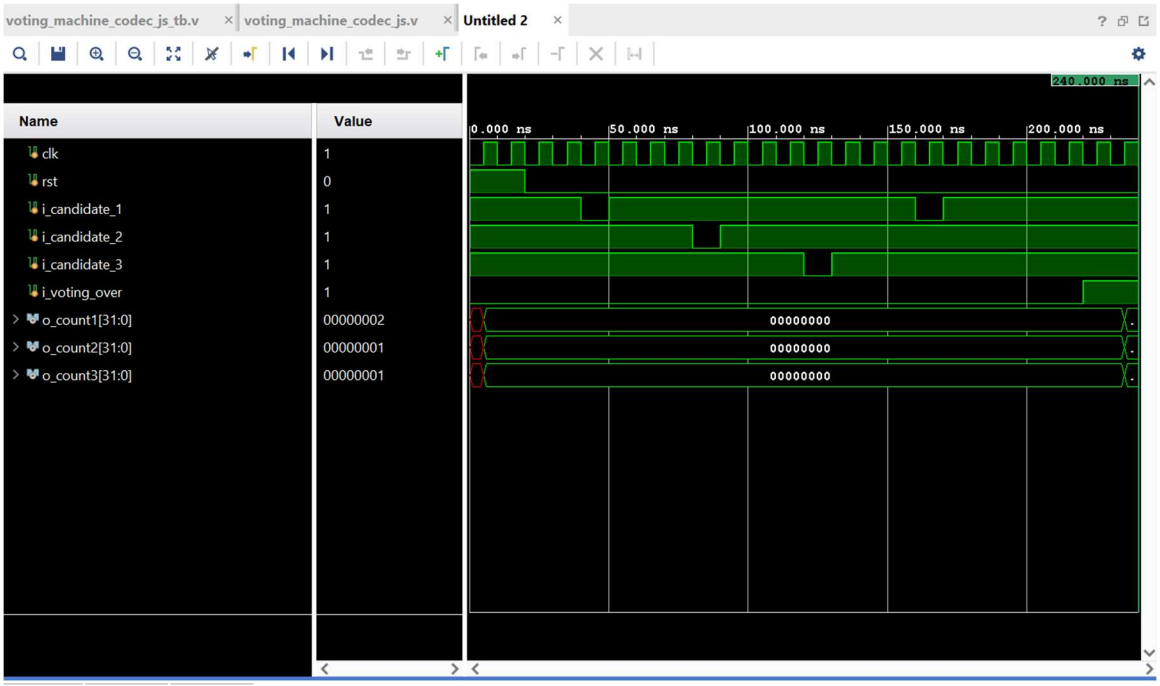
Verilog Code Explanation

The Verilog code is divided into two modules:
1. Main Module (voting_machine_codec_js.v): Implements the voting logic and counters.
2. Testbench Module (voting_machine_codec_js_tb.v): Provides test inputs and simulates the system.

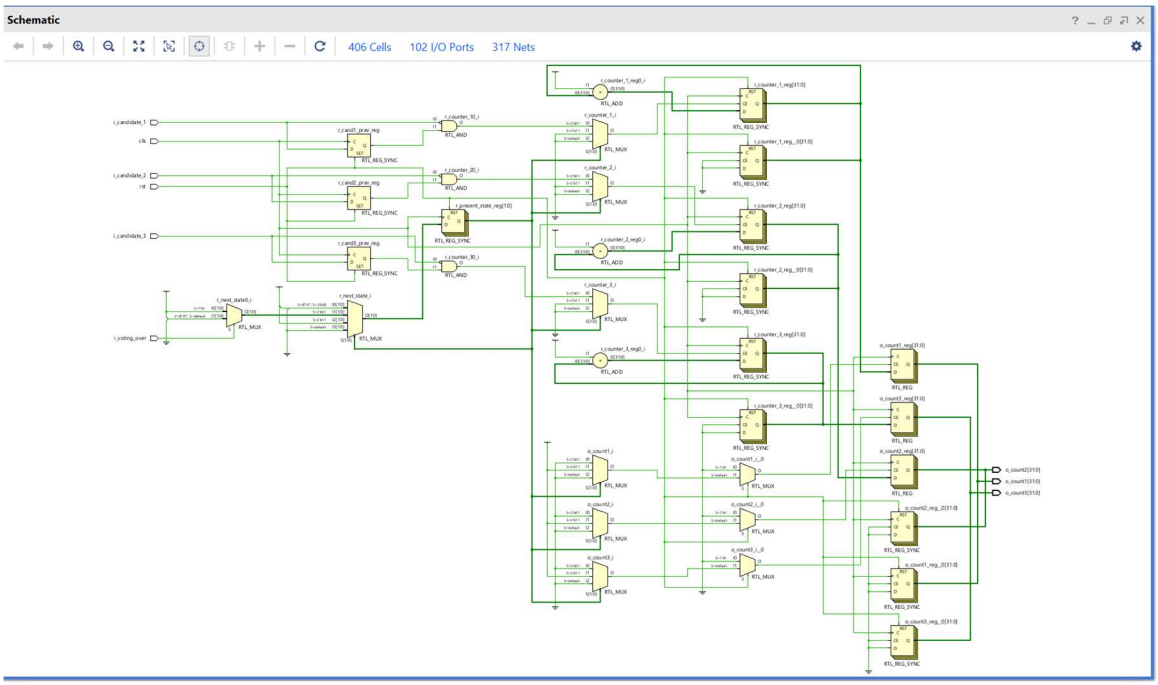
Key signals used:
- clk: Clock signal
- rst: Reset signal
- i_candidate_X: Candidate input signals
- i_voting_over: Indicates when voting is completed
- o_countX: Outputs that display the total votes for each candidate

Simulation Waveform

The simulation waveform below shows the operation of the voting machine:



Schematic Diagram



Results & Conclusion

The digital voting machine designed in Verilog HDL successfully simulates the process of voting. Each candidate receives votes, and the counters accurately store the results. The simulation waveform confirms the correct functioning of the design.

Conclusion:

1. The project demonstrates the practical application of Verilog in digital systems.
2. The counters accurately track the votes for each candidate.
3. The design can be extended to include more candidates and advanced features.
4. This project shows the importance of HDL in implementing real-world systems.