Time Division Multiplexing

석사: 박 제 창(JAICHANGPARK)

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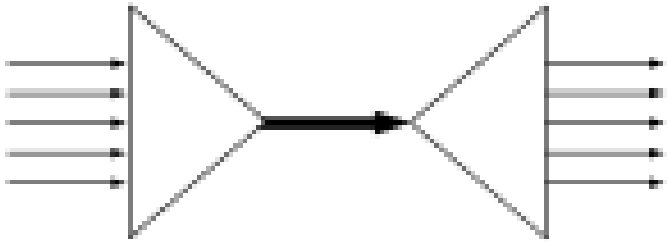
목표

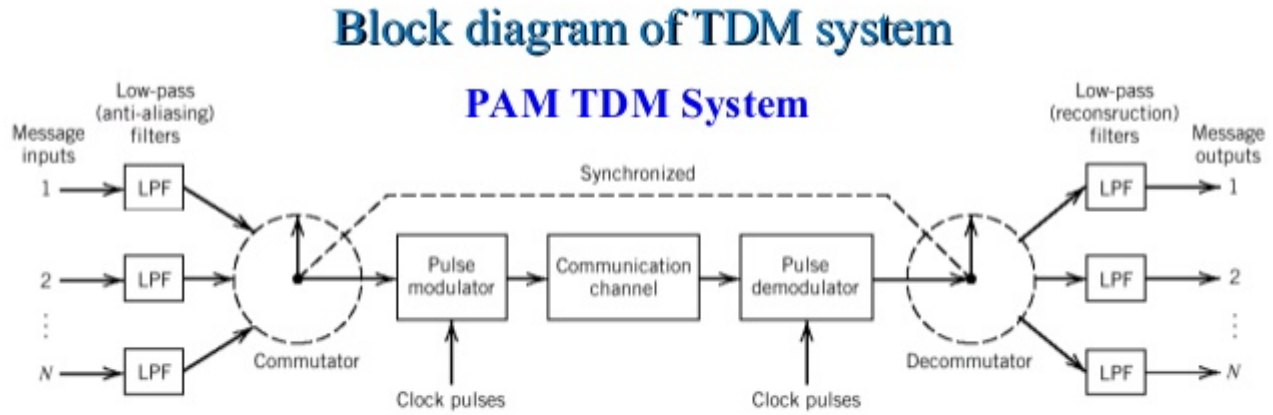
- DE2 Board를 활용한 시분할 멀티플렉싱 구현
- 송신부 클럭 기반 시분할 멀티플렉싱 구현
- 수신부 클럭 기반 시분할 멀티플렉싱 구현
- (단 클럭 신호는 DE2보드 내부 발진기 클럭을 사용한다.)

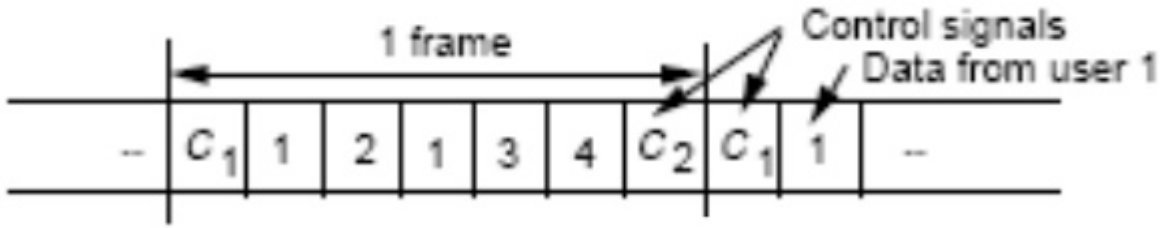
- **시분할 다중화**(Time Division Multiplexing, **TDM**)이란 전송로를 점유하는 시간을 분할하여 한 개의 전송로에 여러 개의 가상 경로를 구성하는 통신 방식이다.



기본적인 멀티플랙싱 구조도

Time Division Multiplexing





A Typical Framing Structure for TDM

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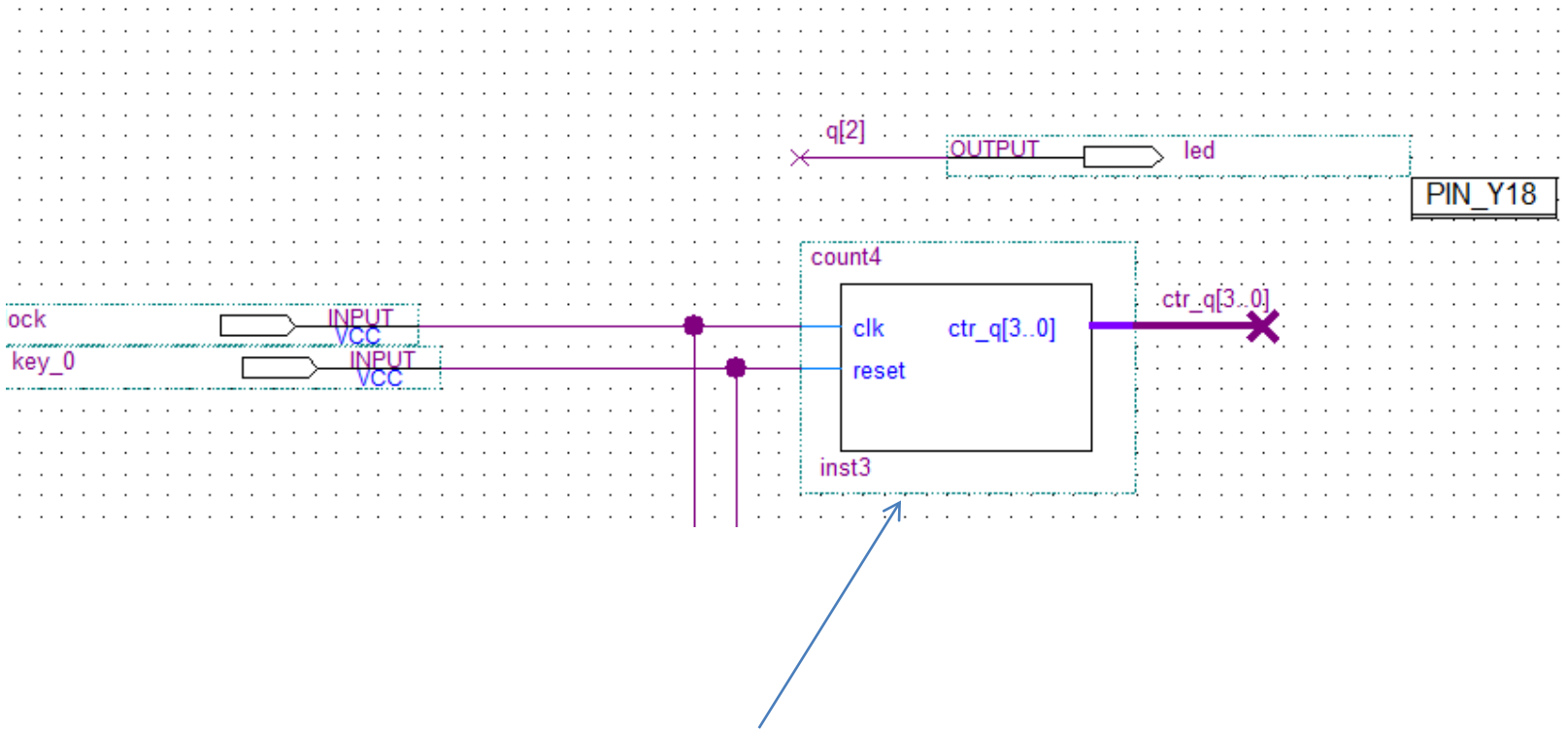
출처:
https://www.google.co.kr/url?sa=i&source=images&cd=&cad=rja&uact=8&ved=2ahUKEwiCt4Gpip3eAhWJyrwKHS0YC-UQjhx6BAgBEAM&url=https%3A%2F%2Fwww.slideshare.net%2FSpanditLenka%2Ftime-division-multiplexing-77643125&psig=AOvVaw3yyDfHLUmYrjPoAcsHlY7N&ust=1540401869378521

- 클럭부 (송, 수신부 공통 사용)



입력 클럭 신호 4분주

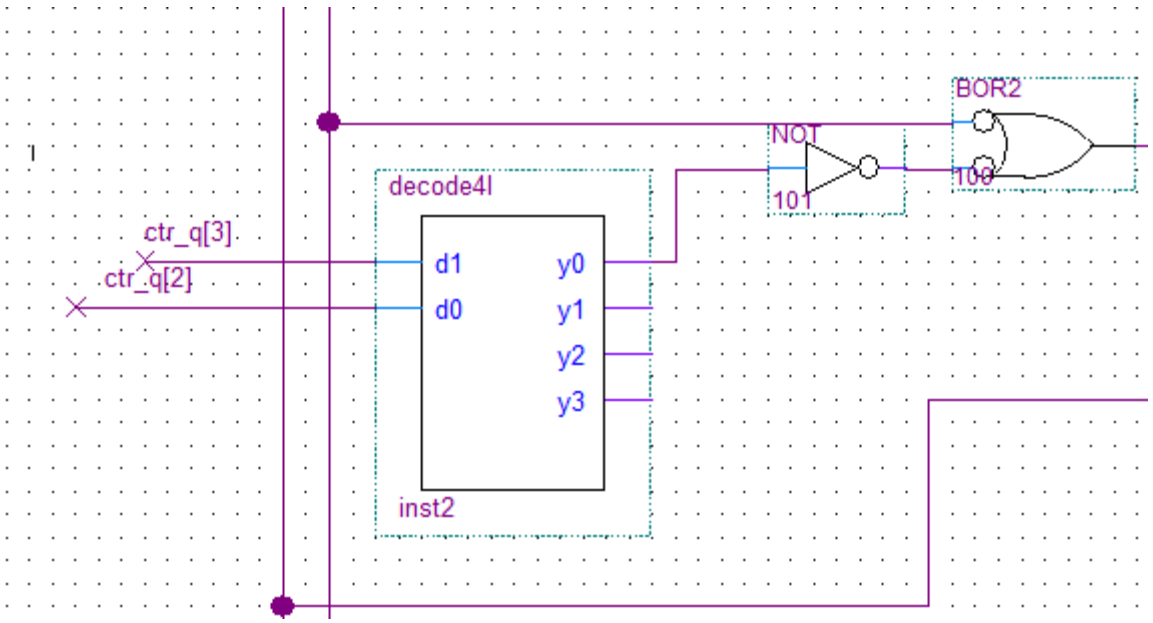
Time Division Multiplexing

➢ 클럭부

```
-- count4.vhd
-- Four-bit binary counter based on a component
--   from the Library of Parameterized Modules (LPM)
-- Counter has an active-LOW reset

LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
LIBRARY lpm;
USE lpm.lpm_components.ALL;

ENTITY count4 IS
    PORT(
        clk, reset  : IN    STD_LOGIC;
        ctr_q       : OUT   STD_LOGIC_VECTOR (3 downto 0));
END count4;

ARCHITECTURE count OF count4 IS
    SIGNAL clrn : STD_LOGIC;
BEGIN
-- Instantiate 5-bit counter
    clock_divider: lpm_counter
        GENERIC MAP (LPM_WIDTH  =>  4)
        PORT MAP (  clock       =>  clk,
                    aclr        =>  clrn,
                    q           =>  ctr_q(3 DOWNTO 0));

    clrn    <=  not reset;
END count;
```

Time Division Multiplexing

- 송신부 디코더 설계



Time Division Multiplexing

- 송신부 디코더 설계

```
ENTITY decode41 IS
PORT(
    d1, d0 : IN BIT;
    y0, y1, y2, y3: OUT BIT);
END decode41;

ARCHITECTURE a of decode41 IS
    SIGNAL inputs : BIT_VECTOR(1 downto 0);
    SIGNAL outputs: BIT_VECTOR(0 to 3);
BEGIN
    inputs <= d1 & d0;
    WITH inputs SELECT
        outputs <=  "0111" WHEN "00",
                    "1011" WHEN "01",
                    "1101" WHEN "10",
                    "1110" WHEN "11";
    y0 <= outputs(0);
    y1 <= outputs(1);
    y2 <= outputs(2);
    y3 <= outputs(3);
end a;
```

Time Division Multiplexing

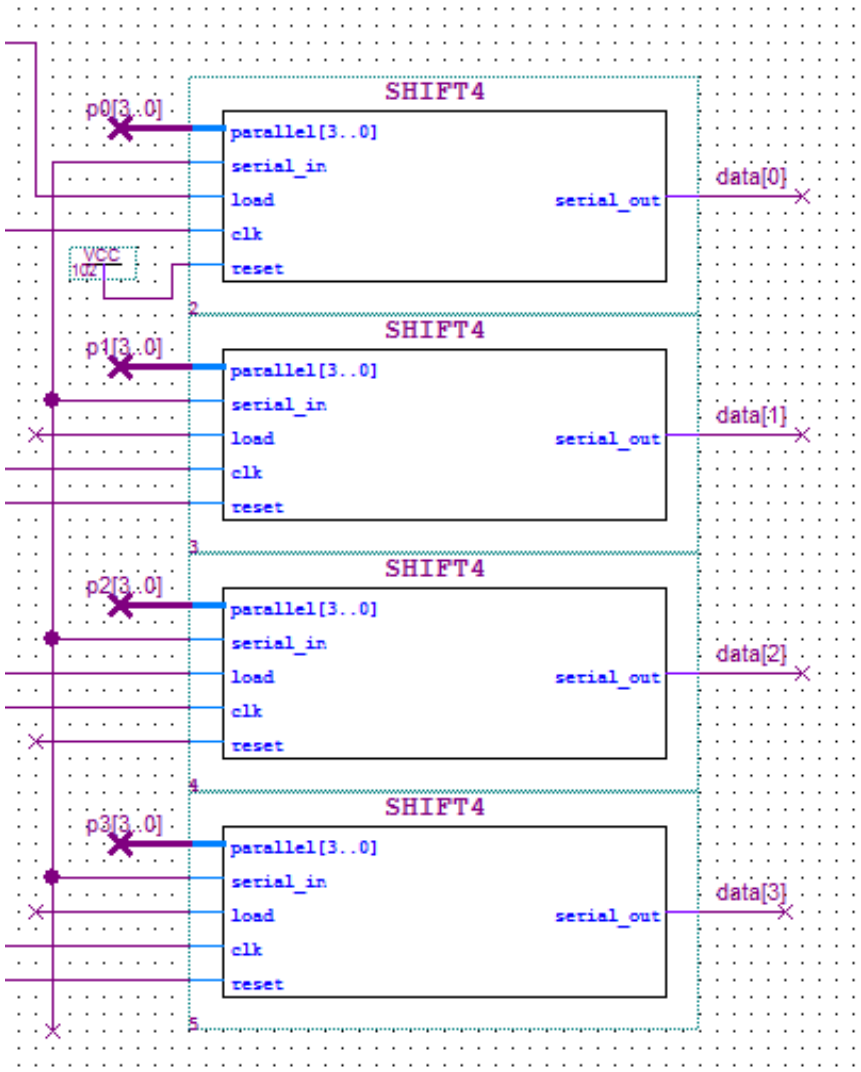
- 송신부 4비트 시프터 설계

디코더 출력

접지

클럭

초기화 스위치



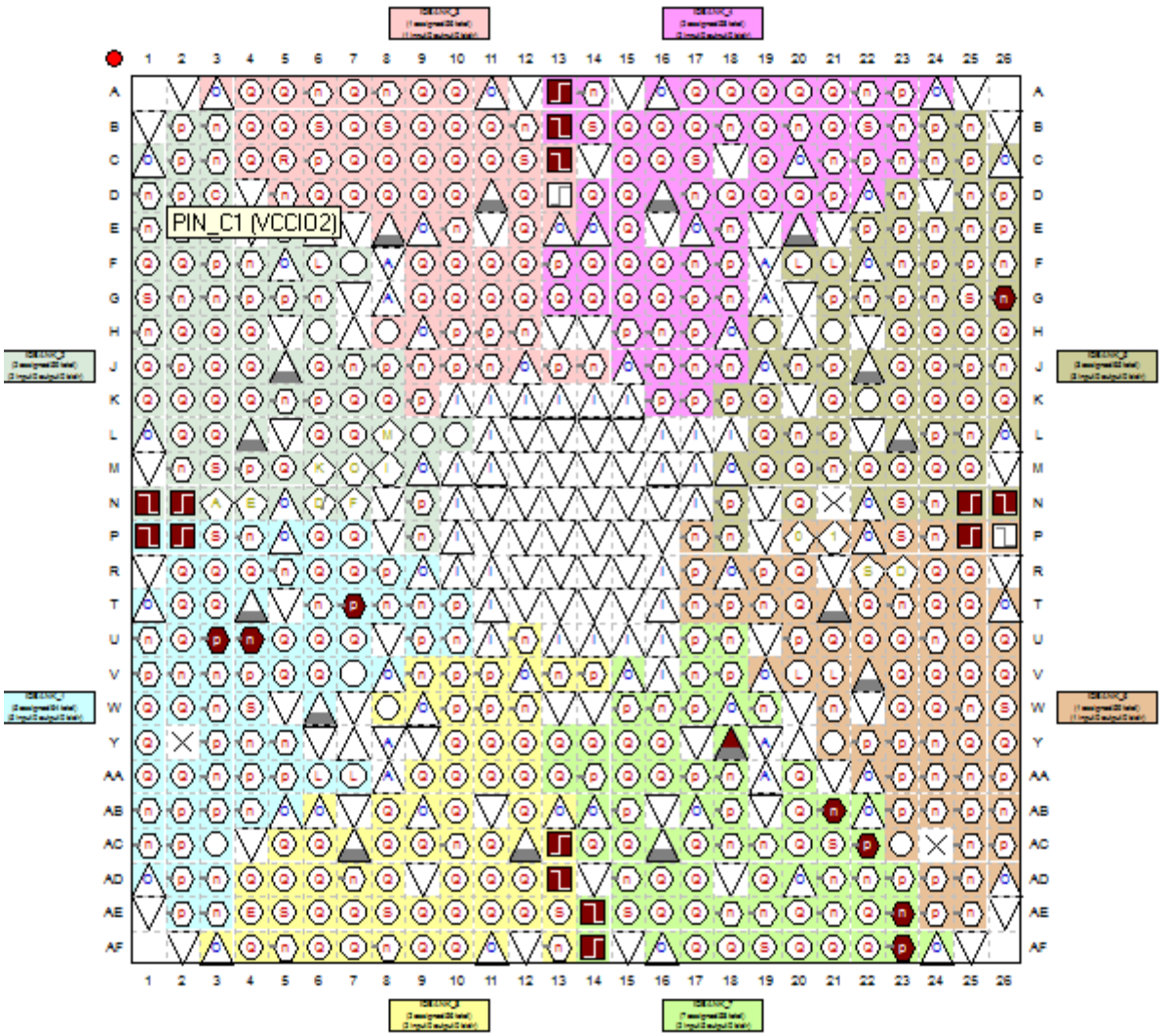
Time Division Multiplexing

- 송신부 4비트 시프터 설계

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
LIBRARY lpm;
USE lpm.lpm_components.ALL;

ENTITY shift4 IS
    PORT(
        parallel            : IN    STD_LOGIC_VECTOR(3 downto 0);
        serial_in           : IN    STD_LOGIC   := '0';
        load, clk, reset    : IN    STD_LOGIC;
        serial_out          : OUT   STD_LOGIC);
END shift4;

ARCHITECTURE shift OF shift4 IS
    SIGNAL  clrn:   STD_LOGIC;
BEGIN
-- Instantiate 4-bit shift register
    four_bit_shift: lpm_shiftreg
        GENERIC MAP (LPM_WIDTH  => 4, LPM_DIRECTION => "RIGHT")
        PORT MAP (  aclr        => clrn,
                    clock       => clk,
                    load        => load,
--                  shiftin     => serial_in,
                    data        => parallel(3 downto 0),
                    shiftout    => serial_out);

    clrn    <=  not reset;
END shift;
```

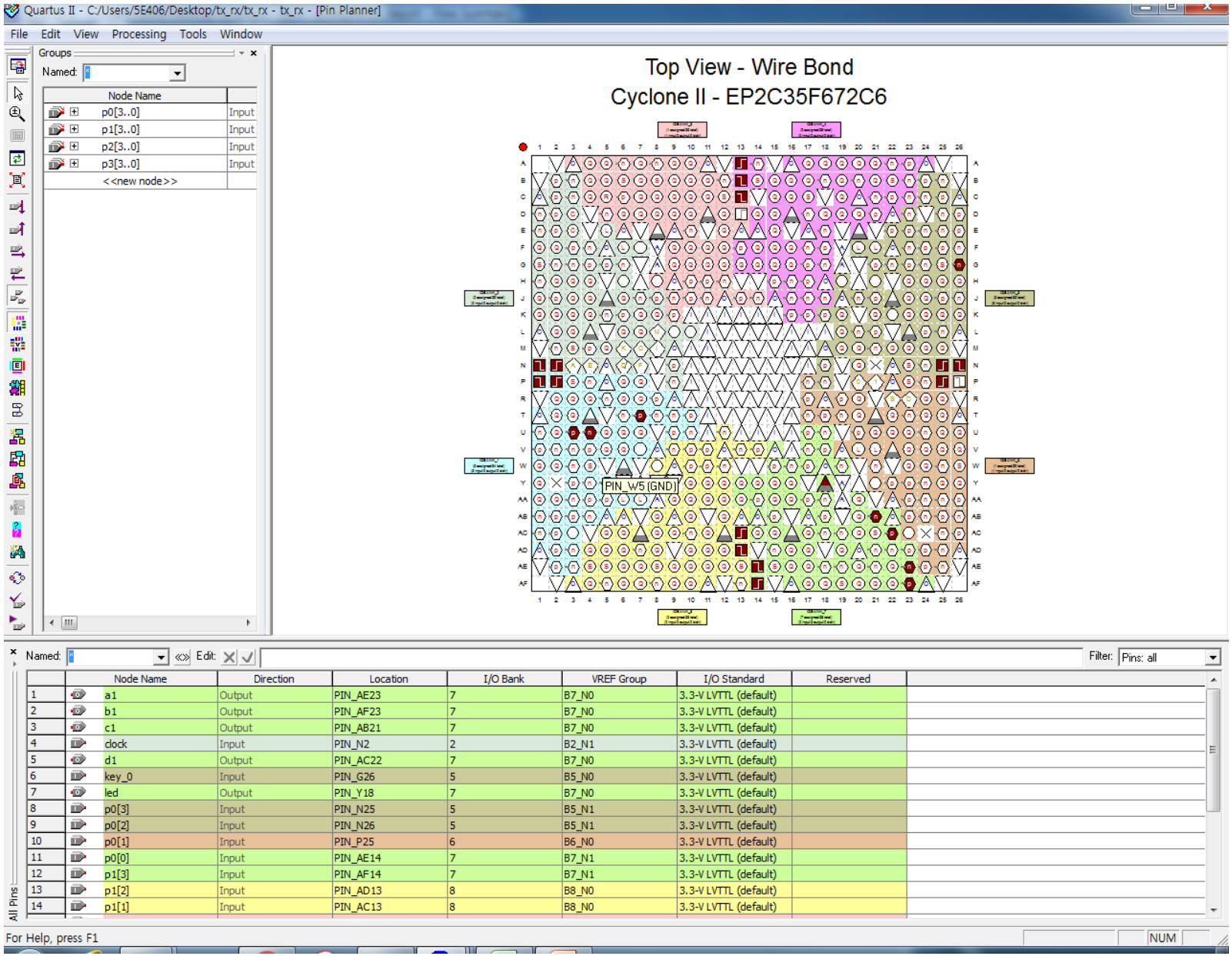
Time Division Multiplexing

- 1차 핀 설정



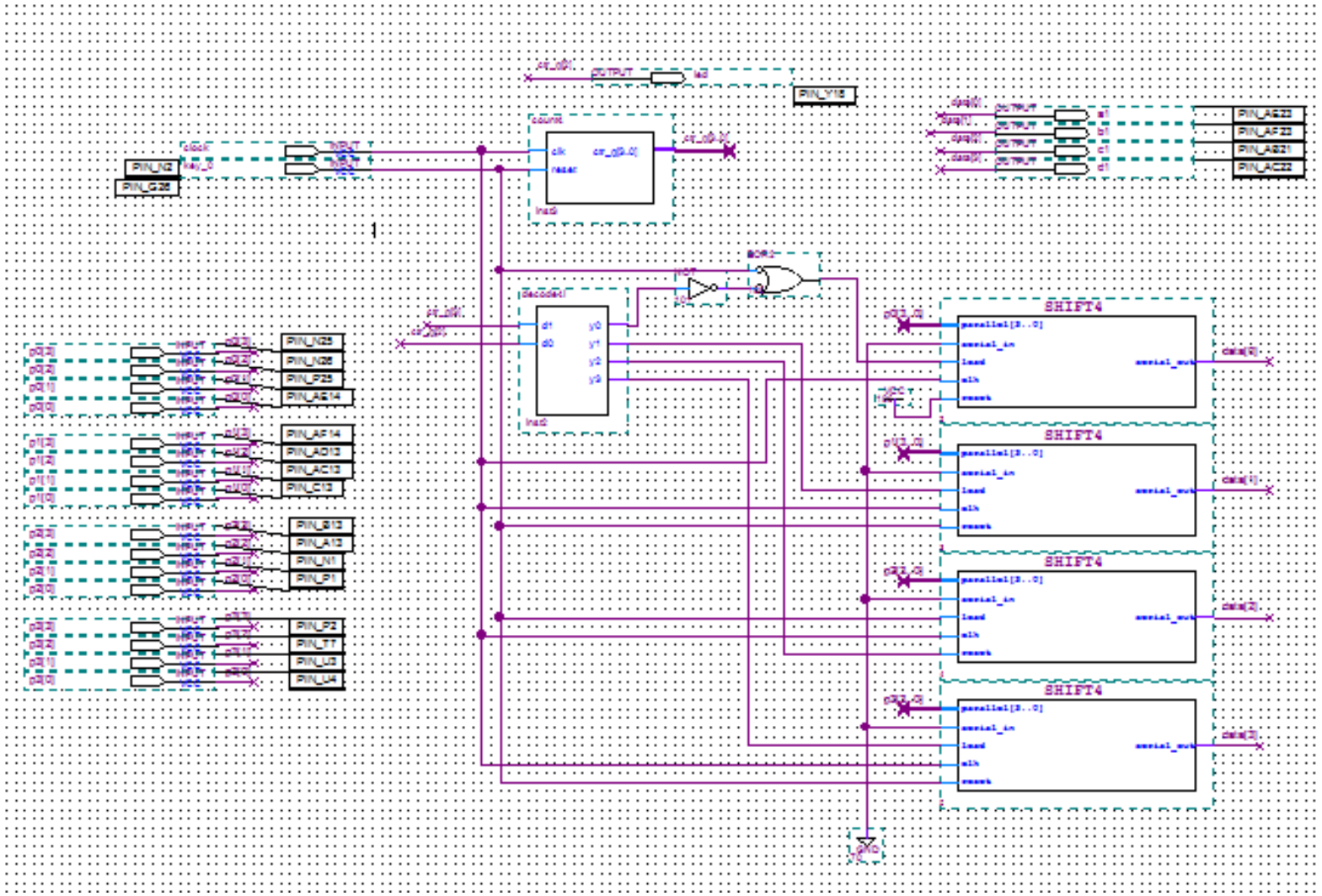
Time Division Multiplexing

- 1차 핀 설정



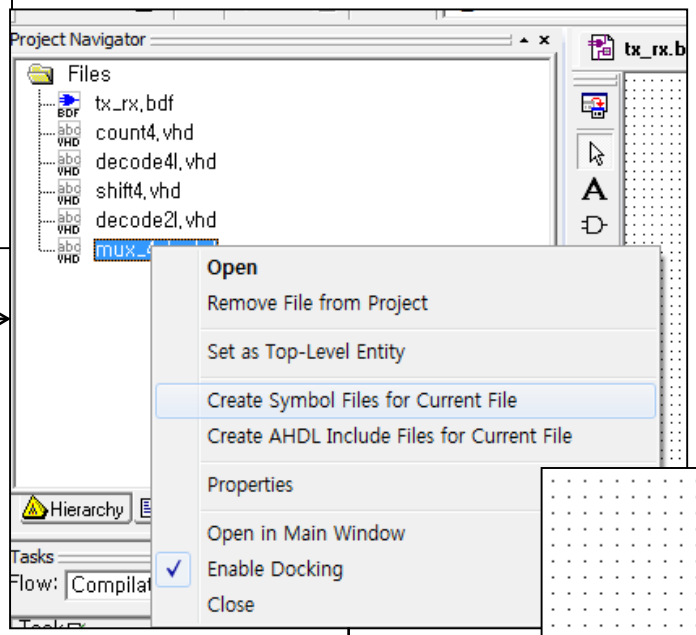
Time Division Multiplexing

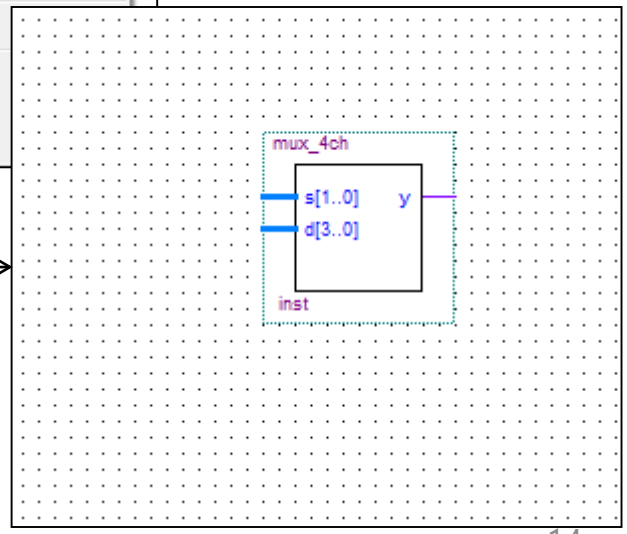
- 1차 회로 구성



Time Division Multiplexing

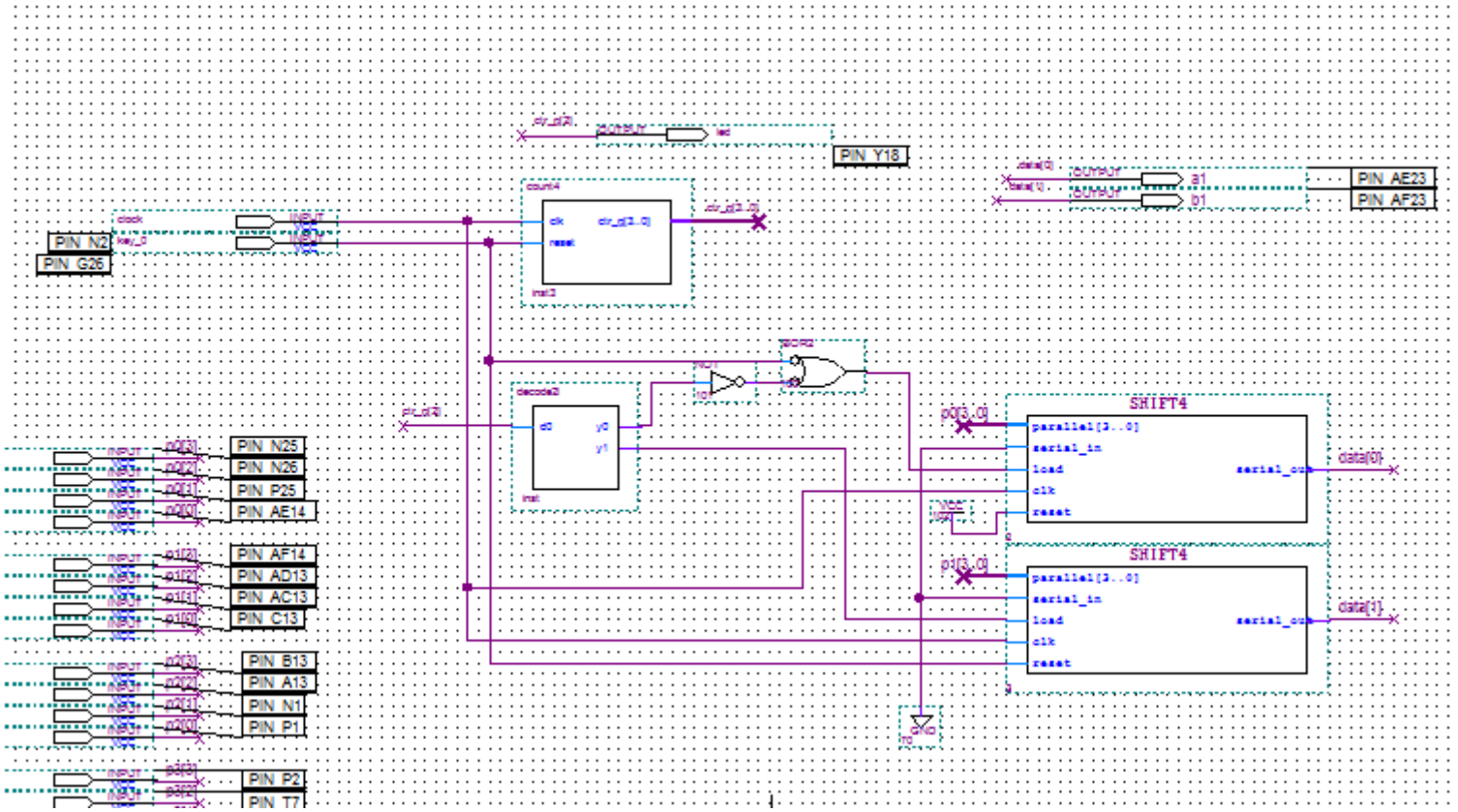
```
ENTITY mux_4ch IS
    PORT(
        s   : IN    BIT_VECTOR (1 downto 0);
        d   : IN    BIT_VECTOR (3 downto 0);
        y   : OUT   BIT);
END mux_4ch;

ARCHITECTURE a OF mux_4ch IS
BEGIN
    --  Selected Signal Assignment
MUX4:   WITH s SELECT
        y   <=  d(0) WHEN "00",
                d(1) WHEN "01",
                d(2) WHEN "10",
                d(3) WHEN "11";
END a;
```





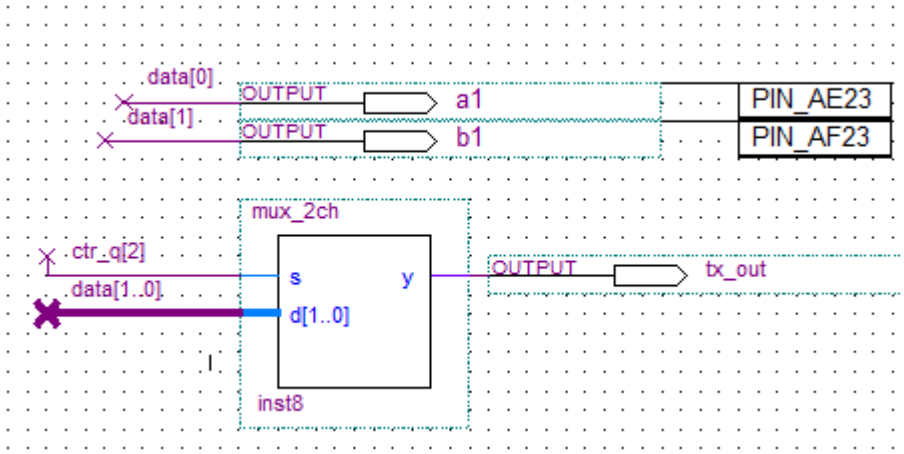
Time Division Multiplexing

Led수 부족으로 다음과 같이 시프트 레지스터
개수를 줄이고 디코더 개수 또한 줄임.



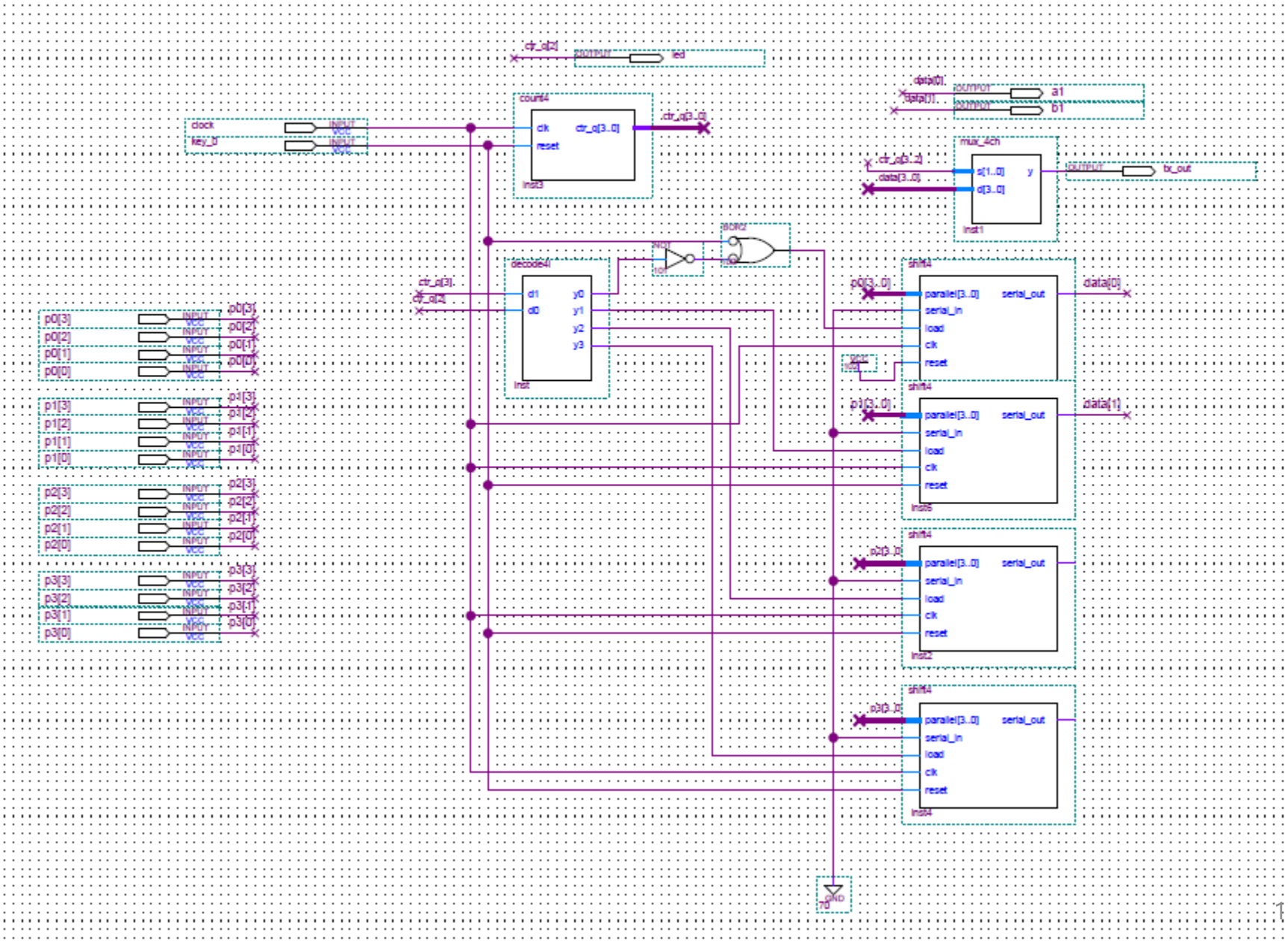
Time Division Multiplexing

```
1  ENTITY mux_2ch IS
2      PORT(
3          s   : IN    BIT;
4          d   : IN    BIT_VECTOR (1 downto 0);
5          y   : OUT   BIT);
6  END mux_2ch;
7
8  ARCHITECTURE a OF mux_2ch IS
9  BEGIN
10     --  Selected Signal Assignment
11 MUX2:   WITH s SELECT
12         y   <=  d(0) WHEN '0',
13                 d(1) WHEN '1';
14
15 END a;
16
17
```



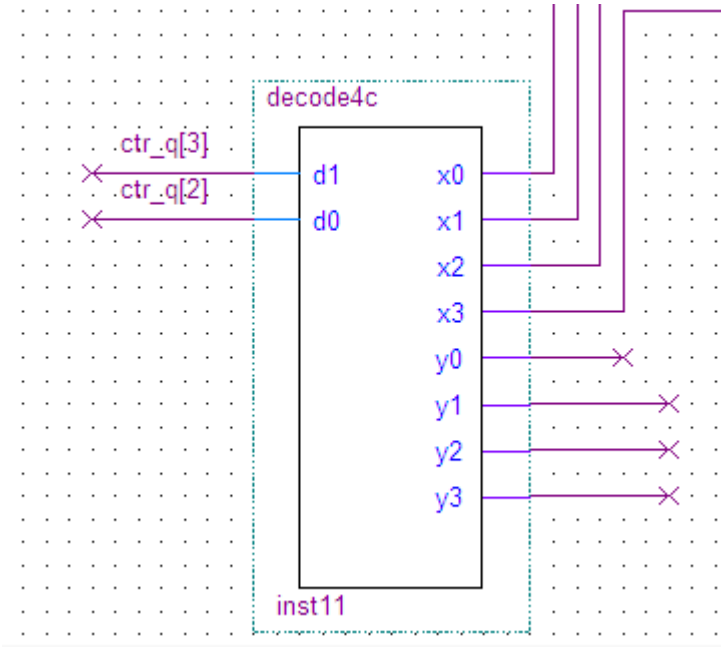
Date: October 24, 2018

송신부 2차 회로 설계 입력 결과



Time Division Multiplexing

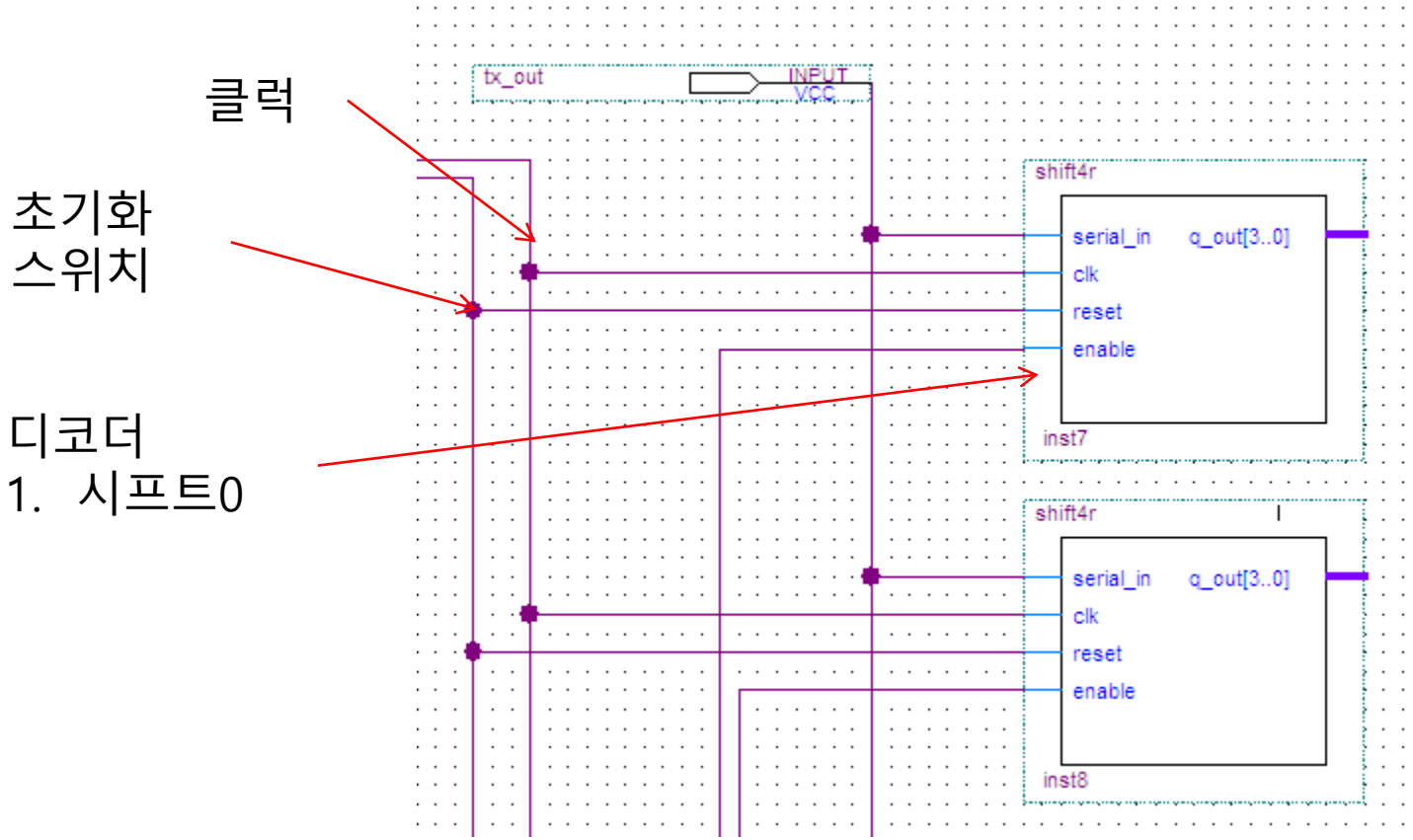
- 수신부 디코더 설계




```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

-- Define inputs and outputs
ENTITY decode4c IS
    PORT(
        d1, d0                          : IN    STD_LOGIC;
        x0, x1, x2, x3, y0, y1, y2, y3  : OUT   STD_LOGIC);
END decode4c;

-- Define i/o relationship
ARCHITECTURE four_ch_decode OF decode4c IS
BEGIN
    --  Concurrent Signal Assignment
    x0  <=  (not d1) and (not d0);  -- input 00: output x0 HIGH
    x1  <=  (not d1) and (    d0);  -- input 01  output x1 HIGH
    x2  <=  (    d1) and (not d0);  -- input 10: output x2 HIGH
    x3  <=  (    d1) and (    d0);  -- input 11: output x3 HIGH

    y0  <=  not ((not d1) and (not d0));    -- input 00: output x0 HIGH
    y1  <=  not ((not d1) and (    d0));    -- input 01  output x1 HIGH
    y2  <=  not ((    d1) and (not d0));    -- input 10: output x2 HIGH
    y3  <=  not ((    d1) and (    d0));    -- input 11: output x3 HIGH
END four_ch_decode;
```

Time Division Multiplexing

- 수신부 4비트 시프트 설계



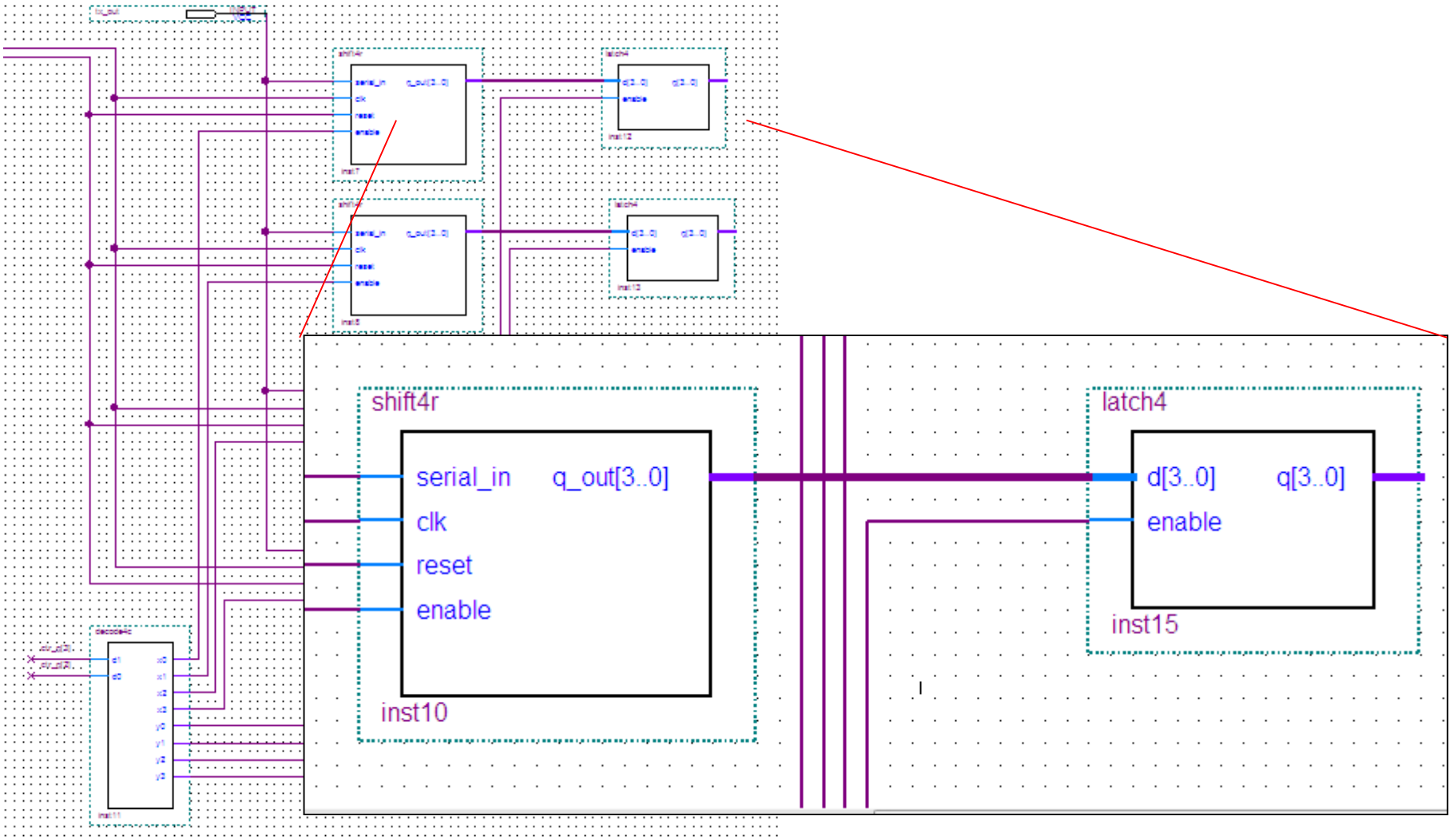
Time Division Multiplexing

- 수신부 4비트 시프트 설계

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
LIBRARY lpm;
USE lpm.lpm_components.ALL;

ENTITY shift4r IS
    PORT(
        serial_in           : IN    STD_LOGIC;
        clk, reset, enable  : IN    STD_LOGIC;
        q_out               : OUT   STD_LOGIC_VECTOR(3 downto 0));
END shift4r;

ARCHITECTURE shift OF shift4r IS
    COMPONENT lpm_shiftreg
        GENERIC (LPM_WIDTH: POSITIVE;LPM_DIRECTION: STRING);
        PORT (clock: IN STD_LOGIC;
            enable: IN STD_LOGIC := '1';
            shiftin: IN STD_LOGIC := '1';
            aclr: IN STD_LOGIC := '0';
            q: OUT STD_LOGIC_VECTOR(LPM_WIDTH-1 DOWNTO 0));
    END COMPONENT;

    SIGNAL  clrn:   STD_LOGIC;
BEGIN
--Instantiate 4-bit shift register
    four_bit_shift: lpm_shiftreg
        GENERIC MAP (LPM_WIDTH  => 4, LPM_DIRECTION => "RIGHT")
        PORT MAP (  aclr        => clrn,
                    clock       => clk,
                    enable      => enable,
                    shiftin     => serial_in,
                    q           => q_out(3 downto 0));

    clrn    <=  not reset;
END shift;
```

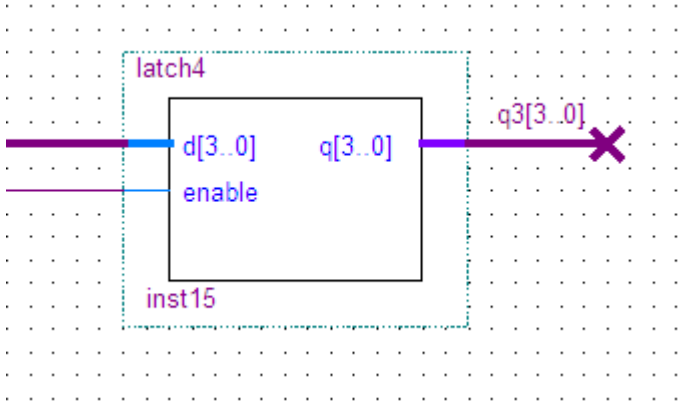
Time Division Multiplexing

- 수신부 레치 설계



Time Division Multiplexing

- 수신부 레치 설계

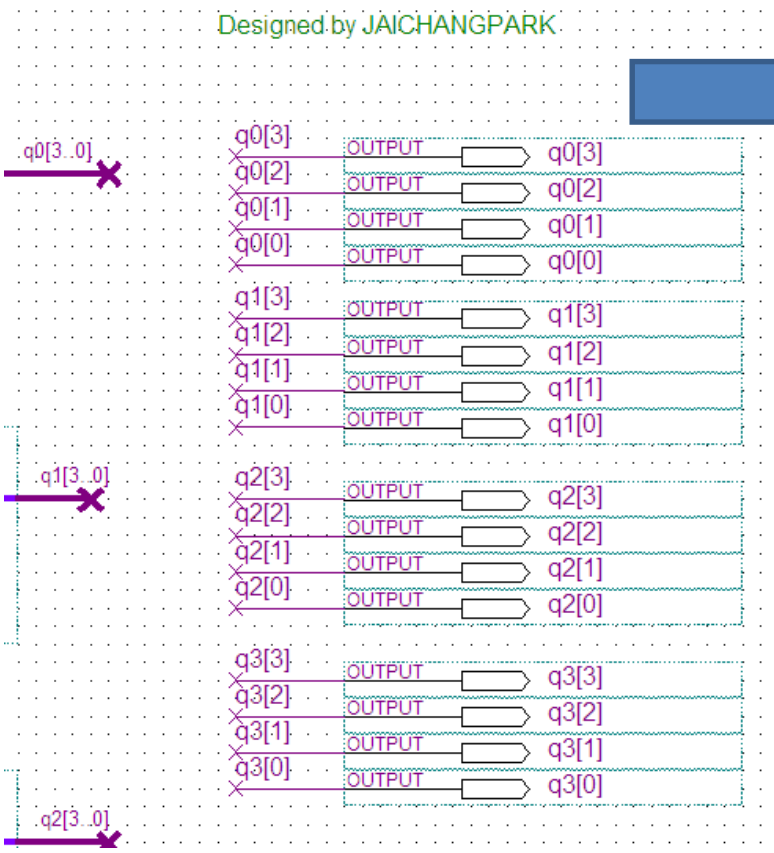


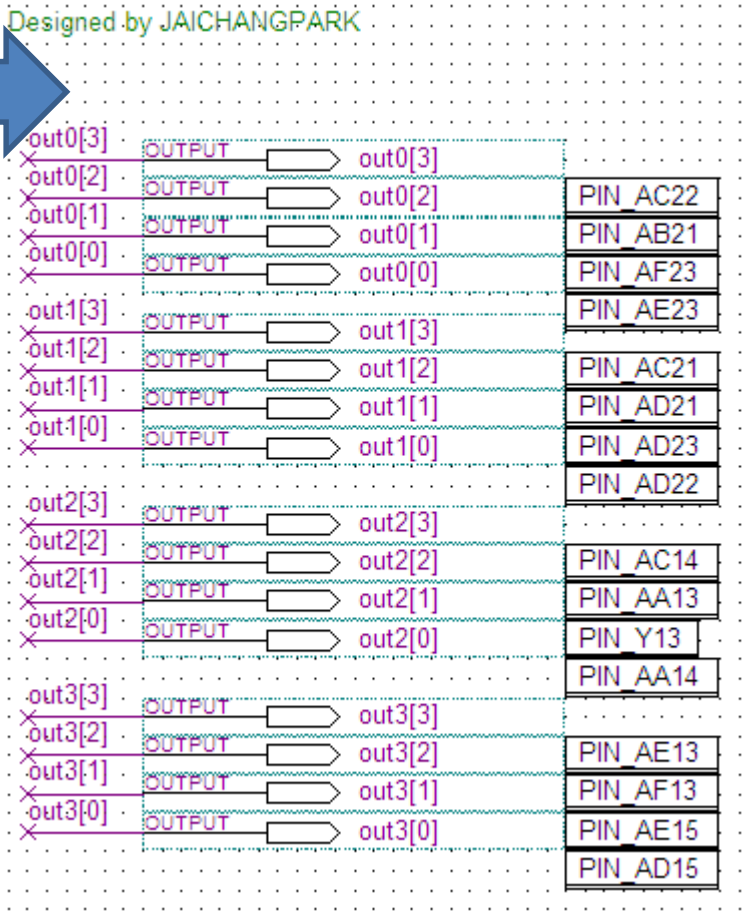

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
LIBRARY lpm;
USE lpm.lpm_components.all;

ENTITY latch4 IS
    PORT(
        d       : IN    STD_LOGIC_VECTOR (3 downto 0);
        enable  : IN    STD_LOGIC;
        q       : OUT   STD_LOGIC_VECTOR (3 downto 0));
END latch4;

ARCHITECTURE latch OF latch4 IS
BEGIN
    four_bit_latch: lpm_latch
        GENERIC MAP(LPM_WIDTH   =>  4)
        PORT MAP(data   =>  d(3 downto 0),
                 gate   =>  enable,
                 q      =>  q(3 downto 0));
END latch;
```

Time Division Multiplexing

- 수신부 출력 포트 <- 레치로 부터 나오는 신호

※단일 보드 내에서 동작 확인을 위한 변수명 변경





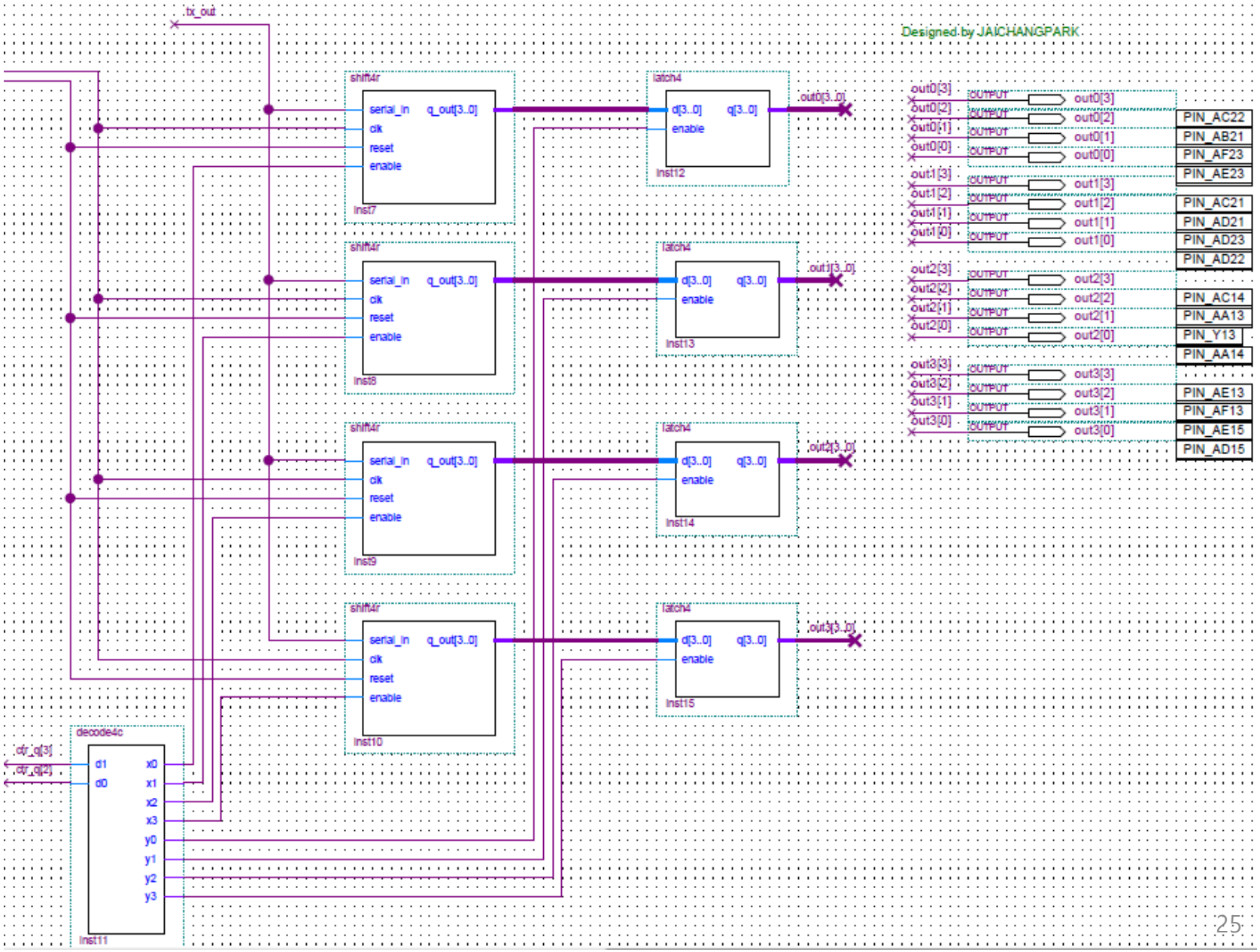
Time Division Multiplexing

- De2 포트핀 설정

a1	Location	PIN_AE22
b1	Location	PIN_AF22
clock	Location	PIN_D13
key_0	Location	PIN_G26
led	Location	PIN_W19
out0[0]	Location	PIN_AE23
out0[1]	Location	PIN_AF23
out0[2]	Location	PIN_AB21
out0[3]	Location	PIN_AC22
out1[0]	Location	PIN_AD22
out1[1]	Location	PIN_AD23
out1[2]	Location	PIN_AD21
out1[3]	Location	PIN_AC21
out2[0]	Location	PIN_AA14
out2[1]	Location	PIN_Y13
out2[2]	Location	PIN_AA13
out2[3]	Location	PIN_AC14
out3[0]	Location	PIN_AD15
out3[1]	Location	PIN_AE15
out3[2]	Location	PIN_AF13
out3[3]	Location	PIN_AE13
p0[0]	Location	PIN_N25
p0[1]	Location	PIN_N26
p0[2]	Location	PIN_P25
p0[3]	Location	PIN_AE14
p1[0]	Location	PIN_AF14
p1[1]	Location	PIN_AD13
p1[2]	Location	PIN_AC13
p1[3]	Location	PIN_C13
p2[0]	Location	PIN_B13
p2[1]	Location	PIN_A13
p2[2]	Location	PIN_N1
p2[3]	Location	PIN_P1
p3[0]	Location	PIN_P2
p3[1]	Location	PIN_T7
p3[2]	Location	PIN_U3
p3[3]	Location	PIN_U4
tx_out	Location	PIN_Y12

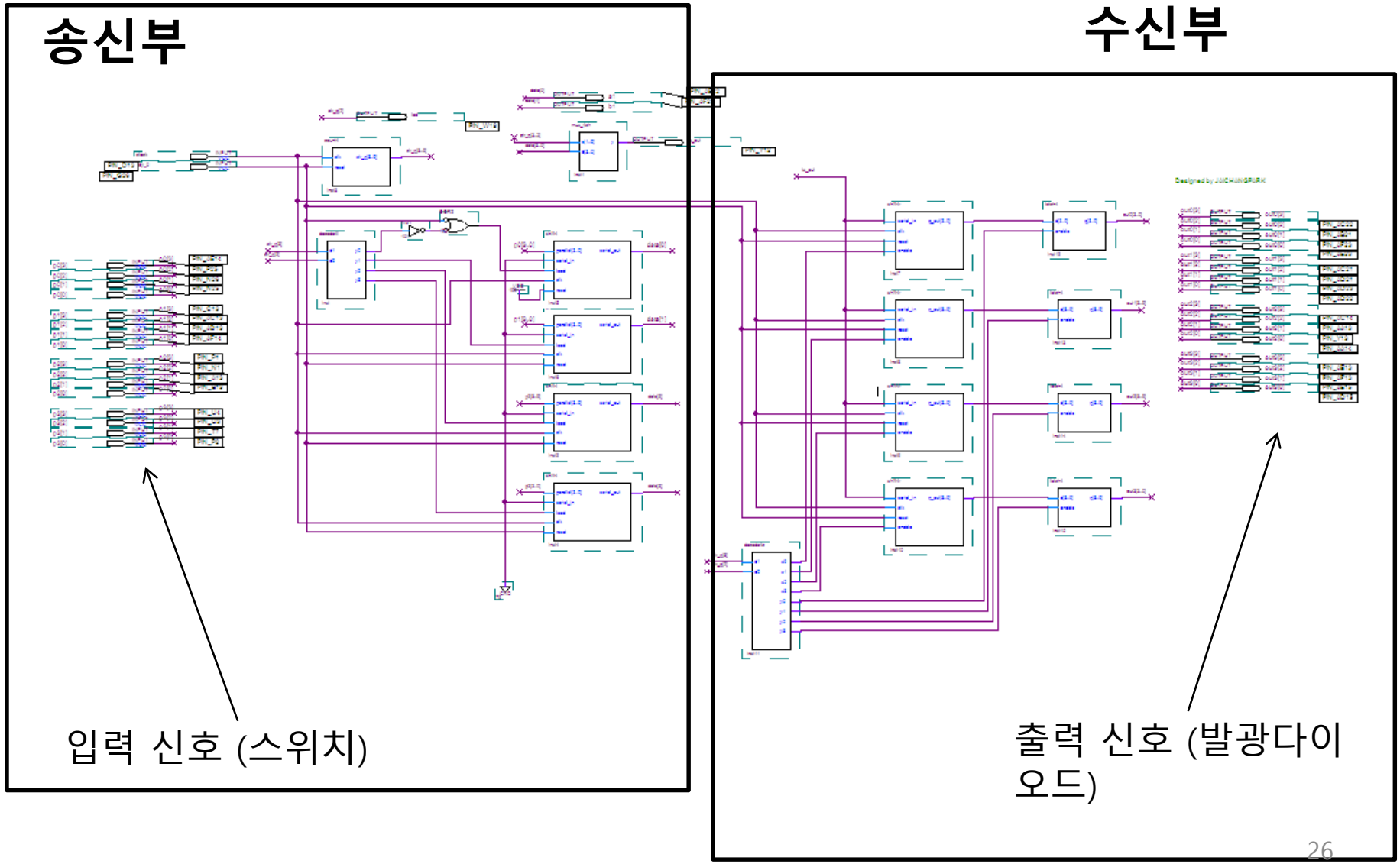
Time Division Multiplexing

수신부 : 2차 회로 구성 결과



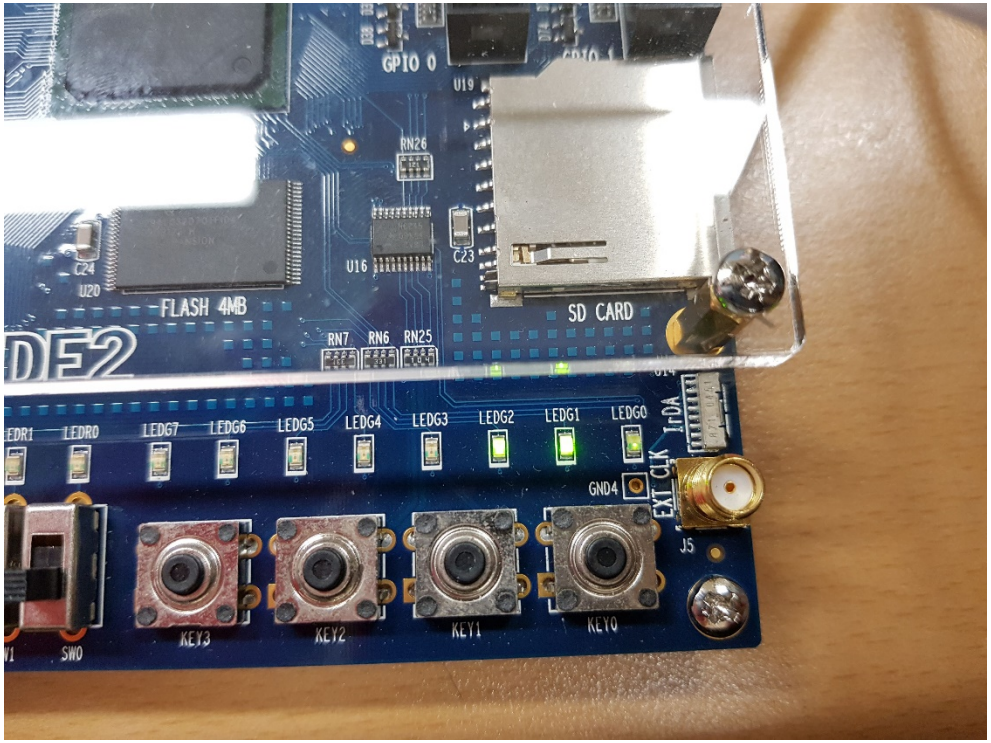
Time Division Multiplexing

- 전체 회로 구성도



Time Division Multiplexing

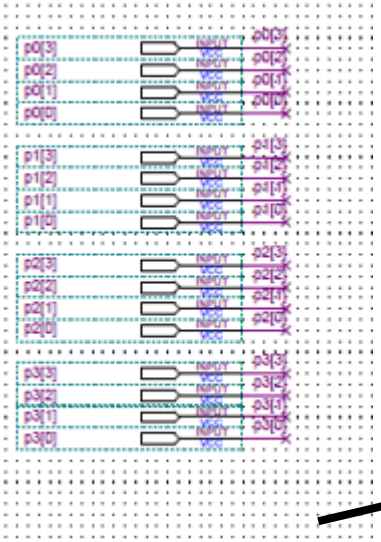
- 결과 사진

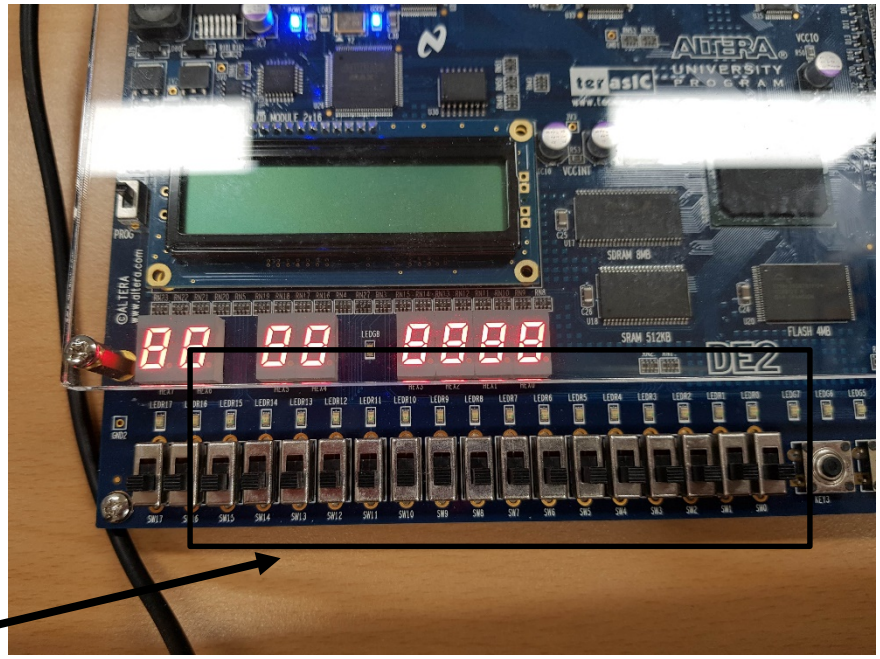


회로 동작 상태 확인을 위한 led

Time Division Multiplexing

- 결과 사진





모든 입력 스위치를 0으로 설정했을 때

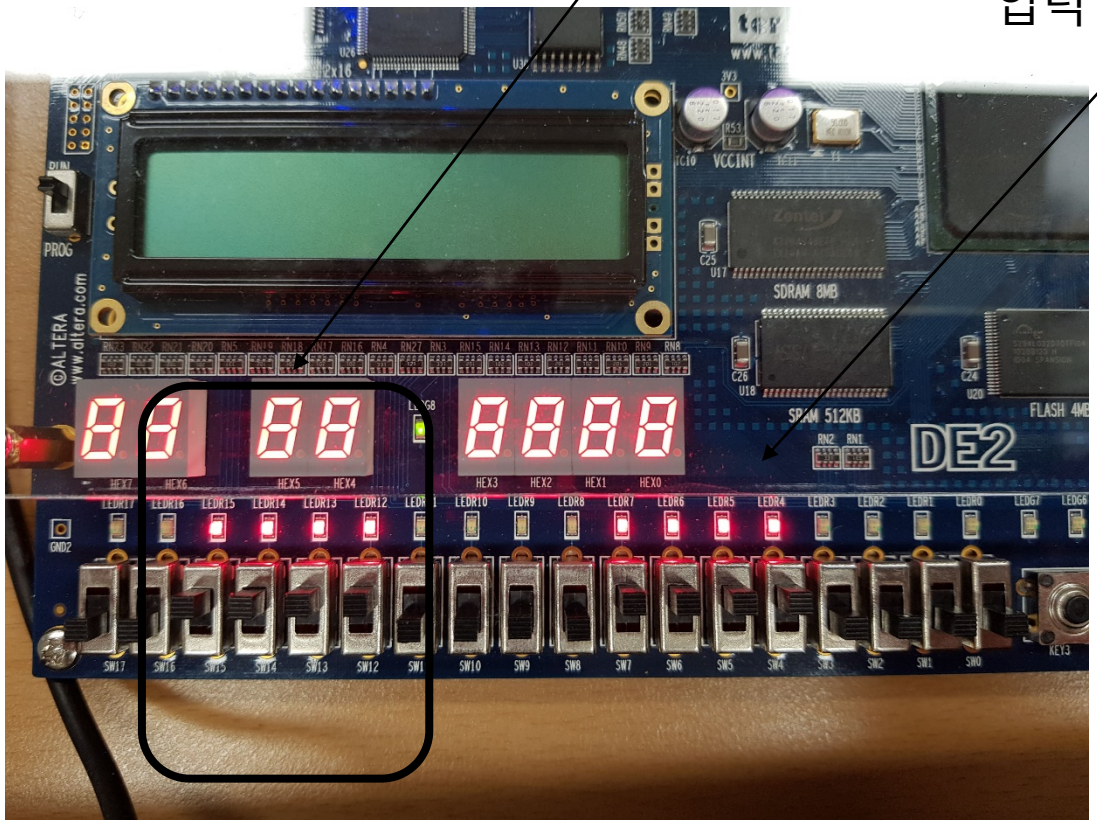
※입력부의 신호는 모두 0이기 때문에 수신부에서 수신한 발광 다이오드는 모두 발광하지 않고 꺼져있는 상태를 가진다.

Time Division Multiplexing

- 결과 사진

- 입력 Q3[3..0]
- 출력 out3[3..0]

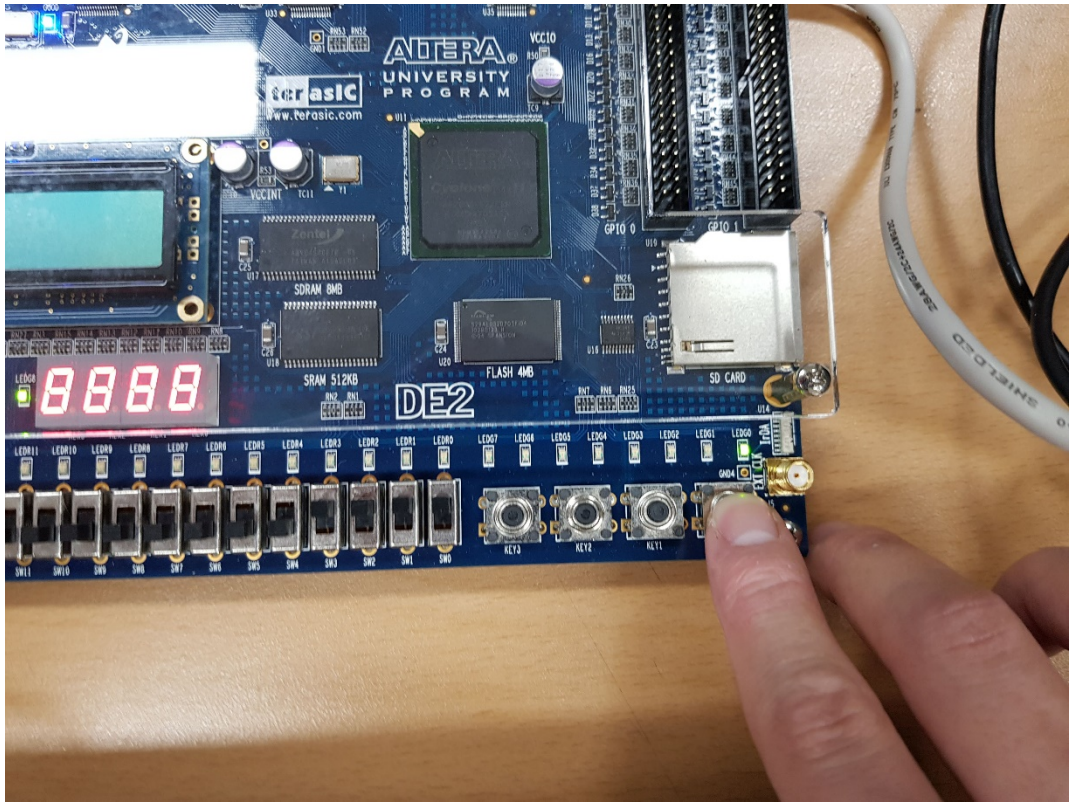
입력 Q1[3..0]



입력 신호 스위치 q1, q3의 모든 스위치를 High state로 위치시켰을 때 설계한 시분할 멀티플렉서의 동작 확인 결과.
송신부의 신호가 수신부의 신호로 정확하게 전달됨을 확인했다.

Time Division Multiplexing

- 결과 사진



리셋 스위치 동작 시 모든 신호 Low state 전환으로 송신부 입력 스위치에 신호가 high state를 가져도 수신부의 신호는 전달 되지 못함

- 결론

- 시분할 멀티플렉싱을 각 기능별 블록으로 제작해 전체 시스템 회로를 구성했다.
- 동작 검증은 1개의 DE2 단일 보드로 진행했으며 송신부의 입력은 스위치로 수신부의 수신 신호 확인은 led 발광다이오드로 동작을 확인했다.

Thank you

JAICHANG PARK