1. What are the various methods to contain power during RTL coding?
    - Clock Gating: Enable clocks only when needed.
    - Data Gating: Block unnecessary data changes.
    - Operand Isolation: Use "enable" signals to prevent needless computations.
    - Memory Access Optimization: Reduce access to power-hungry memory blocks.
    - Use of Low Power States: Design logic to support low-power modes (e.g., sleep or idle).
2. How can the switching of data input to the flip-flop help in power reduction?
   Reducing unnecessary toggling of data inputs reduces dynamic power. For example, adding enable signals to flip-flops prevents updates when data doesn't change.
3. Explain with an example how clock gating can help in power reduction.
   Clock gating involves using an enable signal to control the clock feeding flip-flops. If a block doesn't need to operate, the clock is gated (disabled), reducing dynamic power. In RTL, it looks like:
   ```
   if (enable)
     flop <= data;
   ```
   Power savings occur because the clock signal is stopped when the block is inactive.
4. What are the side effects of latched clock gating logic, and how is it fixed?
    - Glitches: Incorrect data latching due to metastability.
    - Solution: Use *synchronous* clock gating logic or place flip-flops after the gate to prevent glitches.
5. What are a few other techniques of power saving that can be achieved during the RTL design stage?
    - Bus Segmentation: Partition buses and disable unused segments.
    - Finite State Machine (FSM) Optimization: Simplify states or use one-hot encoding.
    - Resource Sharing: Share resources to minimize activity.
6. What are a few system-level techniques, apart from RTL, that can influence in reduction of power for the chip?
    - Dynamic Voltage and Frequency Scaling (DVFS): Adjust frequency/voltage based on workload.
    - Power Islands: Separate blocks into power domains that can be turned off when not in use.
    - Low Power IO Design: Optimize peripheral connections for power savings.
7. What are a few power reduction techniques that can be achieved through static timing?
    - Reducing Clock Buffers: Minimizing the number of clock buffers reduces dynamic power.
    - Multi-Voltage Threshold Cells: Use high-threshold voltage (HVT) cells in non-critical paths to save power.
8. What are a few power reduction techniques that can be implemented during the backend analysis?
    - Power Grid Optimization: Ensure efficient distribution of power with minimal IR drop.
    - Minimize Wire Capacitance: Use shorter routes and reduce metal layers to minimize wire capacitance.
9. What are a few power reduction techniques that can be implemented during board design?
    - Power Supply Optimization: Use efficient power converters and regulators.
    - Signal Integrity: Minimize unnecessary power loss due to signal integrity issues like crosstalk.
    - Low Power Components: Choose components optimized for low power consumption.