1. Given the flip-flop circuit with a delay (dly) between input and output and the clock (clk). What will be the expression for the minimum time period(Tmin) and maximum clock frequency(fmax)? Derive it by considering clock to Q delay (Tclock_Q), setup time (Tsetup_time) and hold time(Thold_time) of the flip flop.
   Tmin >= Tsetup_time + Tclock_Q + dly
   Thold_time <= Tclock_Q - dly
2. Setup time of the flop is 6ns, the hold time of the flop is 2ns, and the clock to output (Q) delay is 10ns.
   a. Calculate the minimum clock period required to handle the circuit by drawing a digital logic circuit for the function clock frequency divided by 2.
      Tmin = 10 + 6 = 16ns
      Fmax = 1/16ns = 62.5MHz
   b. Determine the status of the hold time violation.
      Tclock - delay = 16 - 10 = 6ns > hold time. Therefore there is no timing violation.