1. Explain the difference between ‘reg’ and ‘wire’ with an example.
   A wire is used to represent combinational logic or continuous connections. It is typically driven by assign statements or outputs of gates and modules. It reflects the value of whatever is driving it, and cannot hold or store a value.
   A reg is a data type used to represent sequential logic or variables that store values. It is updated inside procedural blocks like always or initial. Even though it's called reg, it doesn't necessarily correspond to a physical register unless the design is synthesized that way.
2. Explain the ternary operator(?) with an example.
   In Verilog, the ternary operator (? :) is a conditional operator used to choose between two values based on a condition. It is a shorthand for an if-else statement, commonly used in combinational logic.
   Syntax: (condition)? value_if_true : value_if_false;
3. Identify the base formats of the numbers in the following declarations
   a. 1234 - Decimal.
   b. ‘o25 - Octal.
   c. ‘h9 - Hexadecimal.
   d. ‘b1 - Binary.
4. What is the following declarations:
   a. 1’bz - high impedance.
   b. 32’h1x792 - 67474 up to 128914.
   c. 16’o4z - 32 and the last bit is high impedance.
   d. 16’h2xz - 512 up to 752 with the last bit in high impedance.
5. Explain how negative numbers can be declared and stored in Verilog.
   In Verilog, negative numbers can be declared and stored using two's complement representation, which is the standard for representing signed numbers in digital systems.
   Example

```
module test;
        reg signed [7:0] a;
        reg signed [7:0] b;
        reg signed [7:0] result;
        initial begin
                a = -5; // a = 1111 1011
                b = 10; // b = 0000 1010
                result = a + b; // result = 0000 0101 (which is 5)
                end
endmodule
```

6. Explain the following keywords in Verilog with an example:
   a. Time
      The time keyword is used to represent simulation time in Verilog. It is often used in testbenches to track or control the simulation time.
   b. Integer
      The integer keyword is used to declare variables that can hold integer values. It is a 32-bit signed integer by default.
   c. Parameter
      The parameter keyword is used to define constants that can be used throughout a module.
      Parameters are typically used for module configuration and are set when the module is instantiated.
   d. Defparam

The defparam keyword is used to override the parameter values of a module instance. It is less commonly used in modern Verilog code because parameter values are typically set during module instantiation.