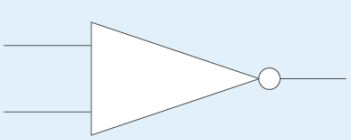
1. Which are the basic gates? Explain working with the truth table.
There are 7 basic gates. NOT, AND, OR, NAND, NOR, XOR,XNOR.

NOT

NOT gate has one input and one output. It gives us the negation of the given input.



Input 1	Output
1	0
0	1

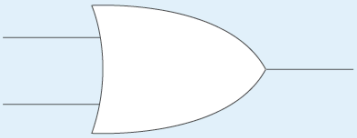
AND

AND gate has two inputs and one output. It gives the output as one only when both the inputs are one, in the rest of the cases the output is zero.

Input 1	Input 2	Output
0	0	0
0	1	0
1	0	0
1	1	1

OR

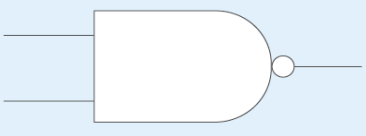
OR gate has two inputs and one output. It gives the output as one if either of the inputs is one.



Input 1	Input 2	Output
0	0	0
0	1	1
1	0	1
1	1	1

NAND

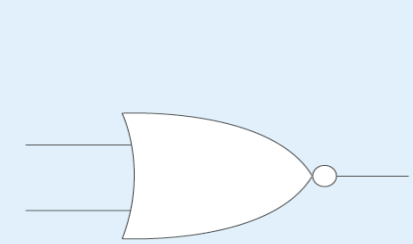
NAND gate has two inputs and one output. It is the negation of the AND gate.



Input 1	Input 2	Output
0	0	1
0	1	1
1	0	1
1	1	0

NOR

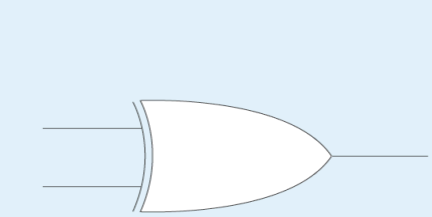
NOR gate has two inputs and one output. It is the negation of the OR gate.



Input 1	Input 2	Output
0	0	1
0	1	0
1	0	0
1	1	0

XOR

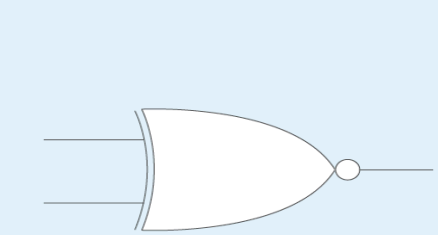
XOR gate has two inputs and one output. It gives the output as one when there is an odd number of inputs as one.



Input 1	Input 2	Output
0	0	0
0	1	1
1	0	1
1	1	0

XNOR

XNOR gate has two inputs and one output. It gives the output as one when there is an even number of inputs as one. It is the negation of the XOR gate.



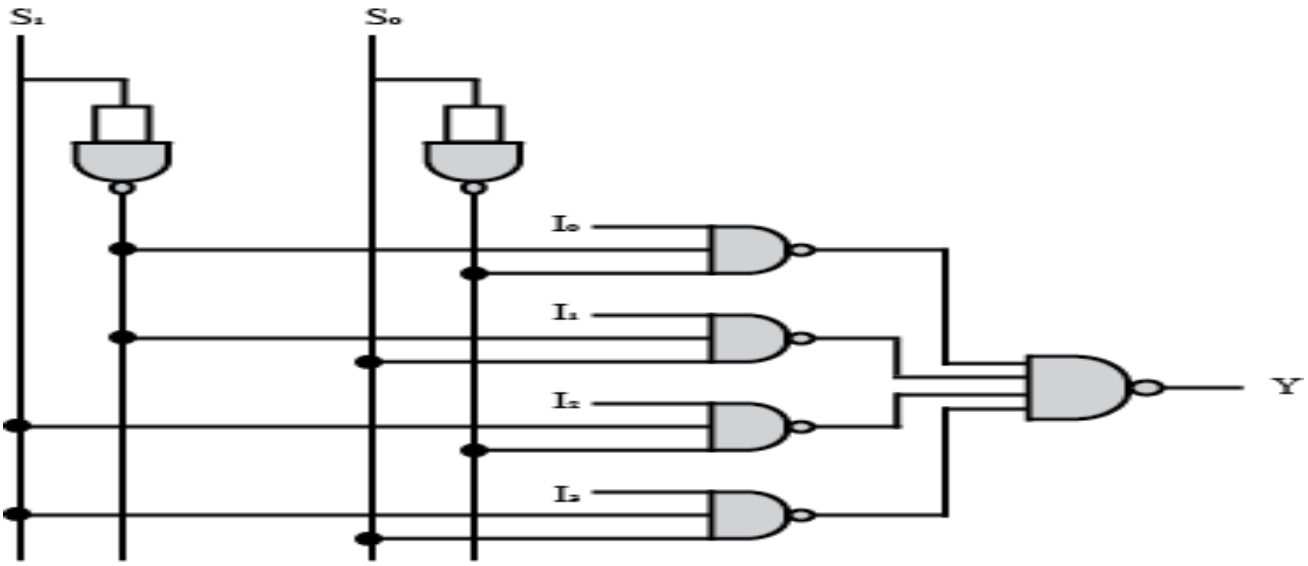
Input 1	Input 2	Output
0	0	1
0	1	0
1	0	0
1	1	1

2. Why are NAND and NOR called universal gates? What are the advantages of universal gates?

NAND and NOR gates are called universal gates because all the basic gates can be derived using these gates. They can be used to simplify designs in digital circuits. As it is economical and easier to fabricate NAND and NOR gates, they are the primary gates used in ICs which are then used to derive other gates.

3. Design a 4:1 MUX using universal gates

NAND



NOR

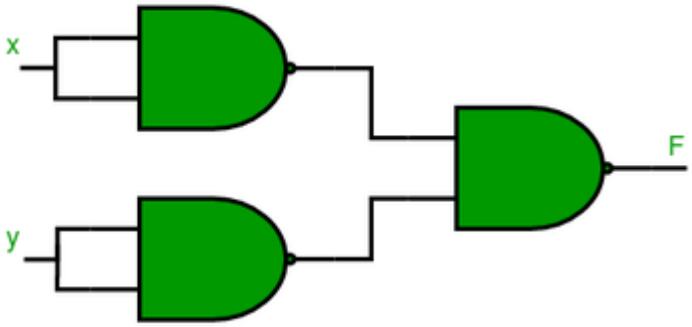
4. What are the applications of NAND and NOR gates?

- They are the building blocks of digital circuits.
- They can be used to implement any digital circuit.
- They are also used to create RAM modules.

5. Design OR, AND, XOR, NOT using universal gates

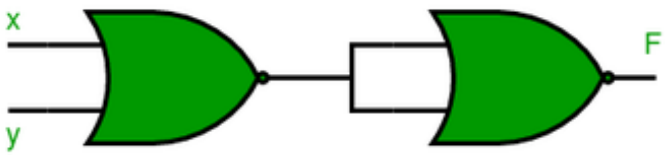
OR

Using NAND



x	y	F
0	0	0
0	1	1
1	0	1
1	1	1

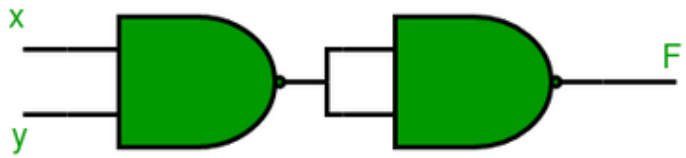
Using NOR



x	y	F
0	0	0
0	1	1
1	0	1
1	1	1

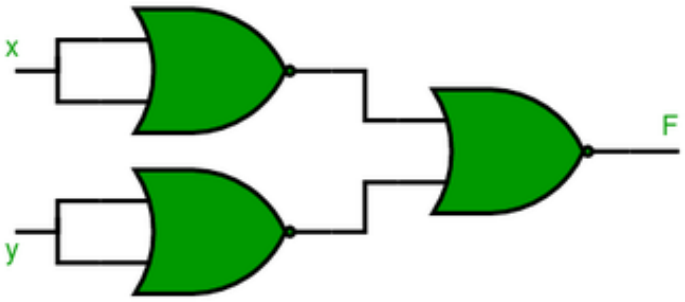
AND

Using NAND



x	y	F
0	0	0
0	1	0
1	0	0
1	1	1

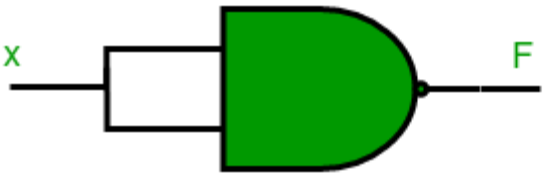
Using NOR



x	y	F
0	0	0
1	0	0
1	1	1
0	1	0

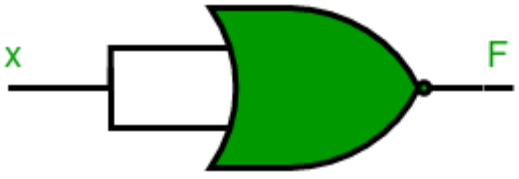
NOT

Using NAND



x	F
0	1
1	0

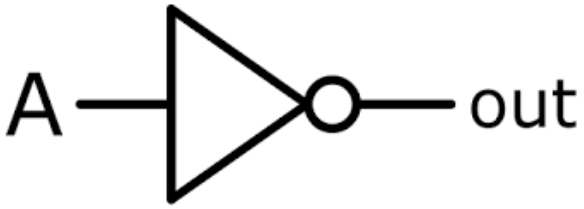
Using NOR



x	F
0	1
1	0

6. Design the below, using logic gates

a. Inverter



b. Adder