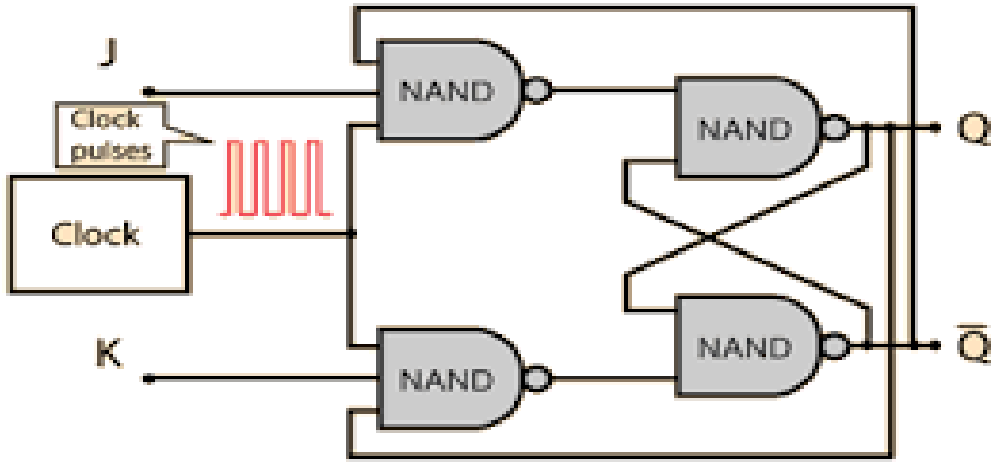
1. Explain the functioning of JK and SR flip-flop.

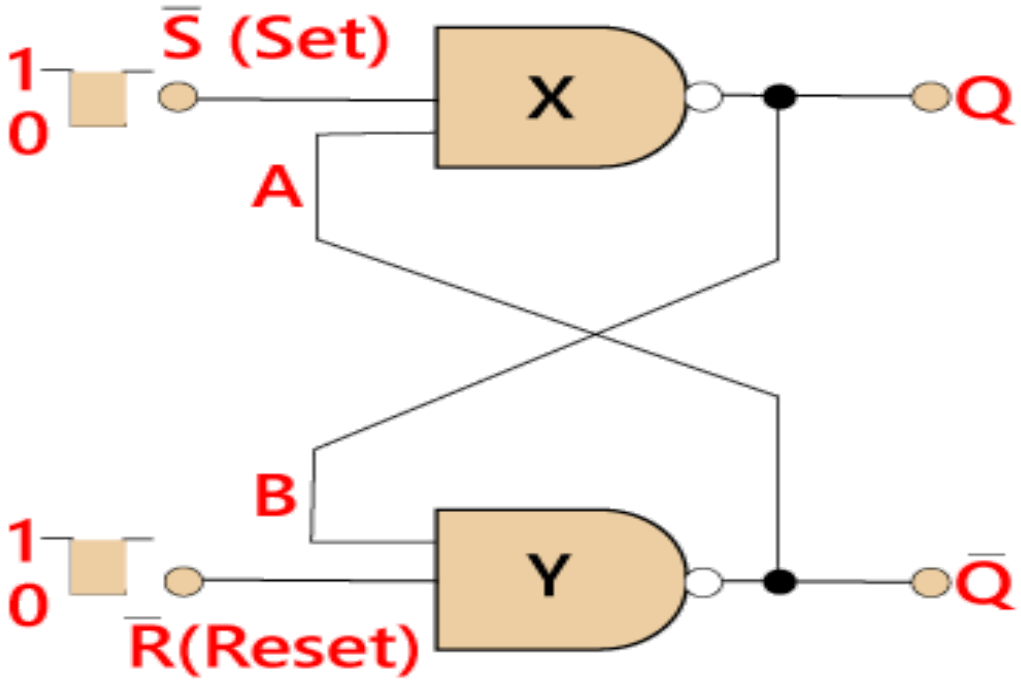
JK Flip Flop

The JK flip-flop is a sequential circuit with 4 states: set, reset, store and toggle. It has 3, inputs set(J) and reset(K) and a clock. The flip-flop works only when the clock is positive or one. It has 2, outputs Q and Q' where Q' is just the not of Q. When both J and K are zero the flip-flop stores the value that existed during the previous cycle. When J is one the output is set to one. When K is one the output is reset to zero and when both are one the output toggles from its previous state.



SR Flip Flop

The SR flip-flop is a sequential circuit that has 3 states: set, reset, and store. It also has 3 inputs set(S), reset(R) and a clock. When S is one the output is set to one. When R is one the output is set to zero and when both are zero the output is retained. The only issue with the SR flip-flop is that when both the inputs S and R are one the flip-flop enters race condition as the circuit is in an invalid state where it cannot decide if the output is one or zero. To solve this race condition JK flip-flops were created.



2. Difference between flip flop and latch.

Flip-Flop

- Flip-flops are edge-triggered devices.
- It works on a clock signal.
- They are constructed using latches and a clock.
- They are slower compared to latches.

Latches

- Latches are level-triggered devices.
- They do not work on a clock signal.
- They are constructed using logic gates.
- They are faster in comparison,

3. Why latches are faster than flip-flops.

Due to the presence of master-slave architecture that is made using latches, they are slower.

4. Explain the use of

a. Flip flops

They are used as a permanent data storage unit in a device. One flip-flop is capable of storing one bit of data.

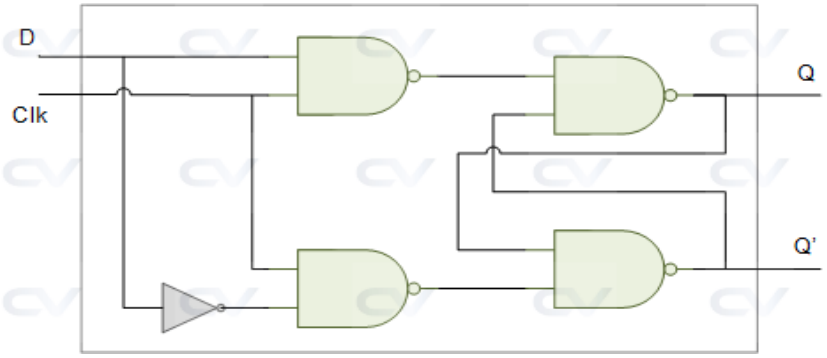
b. Latches

They are the building blocks of sequential circuits. They can also be used for temporary storage of data.

5. Why are Gated SR flip-flops called Asynchronous latch.

Because the device immediately responds to input change and does not wait for the clock to be positive. They do not contain clock input.

6. D flip-flop using NAND gates.



7. D flip-flop using 2:1 MUX