1. What is the difference between time borrowing and time stealing?
   Time borrowing refers to a technique used with latches where a portion of the timing budget from one clock cycle is borrowed from the next clock cycle. Latches, which are level-sensitive, allow data to propagate through when the clock signal is high (or low, depending on the latch type), thereby borrowing time from the next cycle to meet the timing requirements.
   Time stealing is typically used in the context of edge-triggered flip-flops and refers to deliberately adjusting clock skew so that one flip-flop (register) "steals" time from the next flip-flop in the data path. This is done to shift timing constraints from one part of the circuit to another, effectively "stealing" time from future stages.
   Key differences
   Time borrowing
   - Applies to level-sensitive latches.
   - The circuit borrows time from the next clock cycle by keeping the latch open for a part of the next cycle.
   - Occurs naturally due to the transparency of the latch (while the clock is high or low).
   - Adjusts timing by allowing extra time within the current clock cycle and reducing the time in the next.
   - Helps manage long combinational logic paths in latch-based designs.
   - Typically doesn't require intentional skew manipulation.

   Time stealing
   - Applies to edge-triggered flip-flops.
   - Involves stealing time from the next stage in the same clock cycle by manipulating clock skew.
   - Requires intentional clock skew adjustment to delay or advance the clock signal at a particular flip-flop.
   - Adjusts timing by redistributing slack between different registers in the same cycle.
   - Used to optimize critical path timing in flip-flop-based designs.
   - Can introduce potential hold time violations if not managed carefully.
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2. What is the timing path? What are the start and end points?
   In digital circuit design, a timing path refers to the sequence of logic elements (such as gates and flip-flops) that a signal travels through between two specific points in the circuit. It is the route that a signal takes from its starting point to its destination within a digital circuit, including all intermediate logic elements and their delays. Understanding timing paths is crucial for analyzing and ensuring that a design meets its timing constraints.
   Start point: The point where the timing path begins. This is typically the source of the signal in the path.
   End point: The point where the timing path terminates. This is where the signal is expected to be captured or used.
3. Explain the following:
   a. Launch edge.
      The clock edge at which a flip-flop or latch captures and holds the input data for the start of the timing path.
   b. Capture edge.
      The clock edge at which a flip-flop or latch captures the data arriving from the combinational logic at the end of the timing path.
   c. Reset assertion.
      The act of activating a reset signal to initialize or clear the state of a flip-flop, register, or circuit to a known condition.
   d. Reset de-assertion.

The act of deactivating the reset signal, allowing the circuit to resume normal operation and the previously reset elements to take on new values.

e. Critical path
   The longest path through the combinational logic and flip-flops that determines the maximum operating frequency of the circuit.
f. False path
   A timing path that is not functionally used or does not affect the circuit's performance, often ignored in timing analysis to reduce complexity.
g. Multicycle path
   A timing path that spans more than one clock cycle, allowing data to be propagated across multiple clock edges before being latched.