

FROM RESEARCH TO INDUSTRY



FAULTING REAL-WORLD DEVICES WITH X-RAYS BEAMS?

ANR MITIX

CEA-CESTI / SIMAP

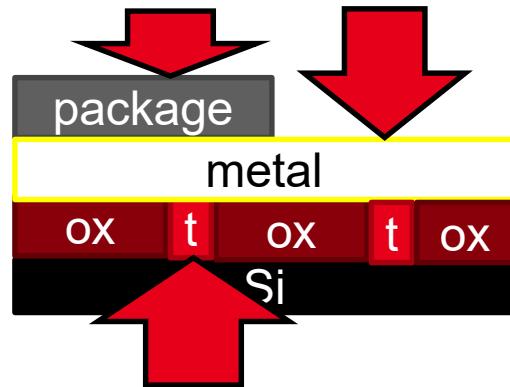
+ partenaires TIMA / CEA-LTSO / ONERA

Stéphanie Anceau / Sophie Bouat / Luc Salvo / Laurent
Maingault / Gwendal Jugault / Pierre Lhuissier / Emrick
Belliard / Rémi Tucoulou

Laser perturbation (VIS-IR)

Resolution limited by its wavelength
(IR $\sim 1 \mu\text{m}$)

Unpackage the device / bakside
illumination



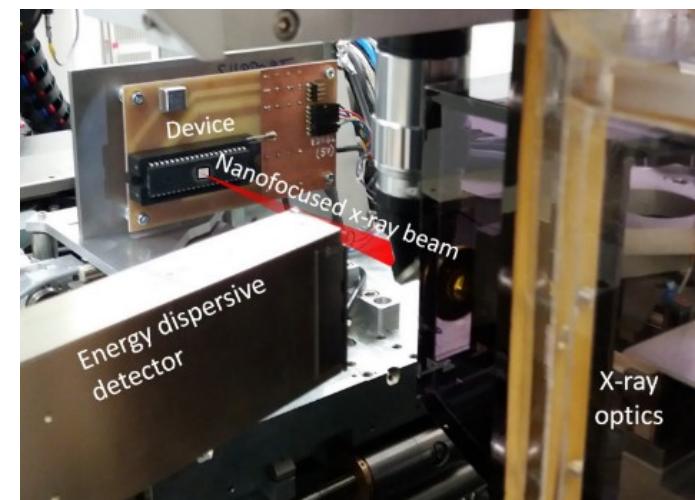
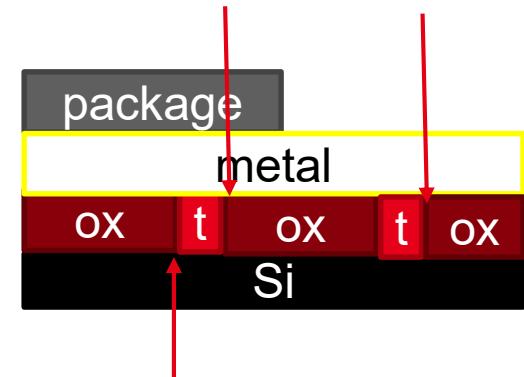
Preuve de concept :

Attaques sur transistor unique démontrée sur des cellules **mémoires** (RAM / FLASH) en technologie $> 90 \text{ nm}$ avec un faisceau **synchrotron nano-focalisé**.

X ($\sim 10 \text{ keV}$)

Wavelength $< 1 \text{ nm}$

Package, thin metal layers \rightarrow
 \sim transparent



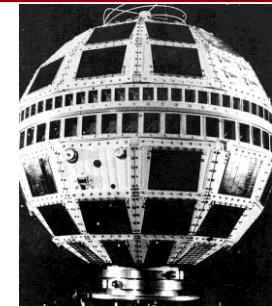
Spatial
Années 60

412

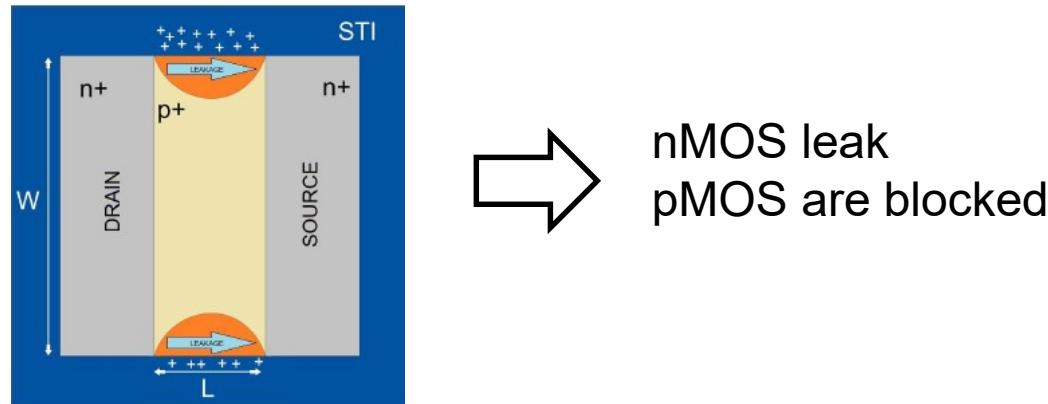
IEEE TRANSACTIONS ON ELECTRONIC COMPUTERS, VOL. EC-16, NO. 4, AUGUST 1967

Design and Use of Fault Simulation for Saturn Computer Design

FRED H. HARDIE AND ROBERT J. SUHOCKI



- Perturbation des oxides de manière semi-permanente (TID)



- Recuit nécessaire pour enlever la faute
- Modification possible des cellules de Flash
- Faisceau petit mais difficile à focaliser (synchrotron)

→ Nouveau type de fautes (Persistent Fault Attacks)

Attaques sur transistor unique démontrée sur des cellules mémories (RAM / FLASH)
en technologie > 90 nm avec un faisceau

CHES 2017, September 25-28, 2017, Proceedings, 2017, p. 1

Minimum sur la technologie ?

Cellules logiques ?

I. Manip ESRF avec
microcontrôleur 28 nm

Avec un générateur X de
laboratoire ?

II. Masques sur tomographe
(SIMAP)

GRENOBLE, FRANCE

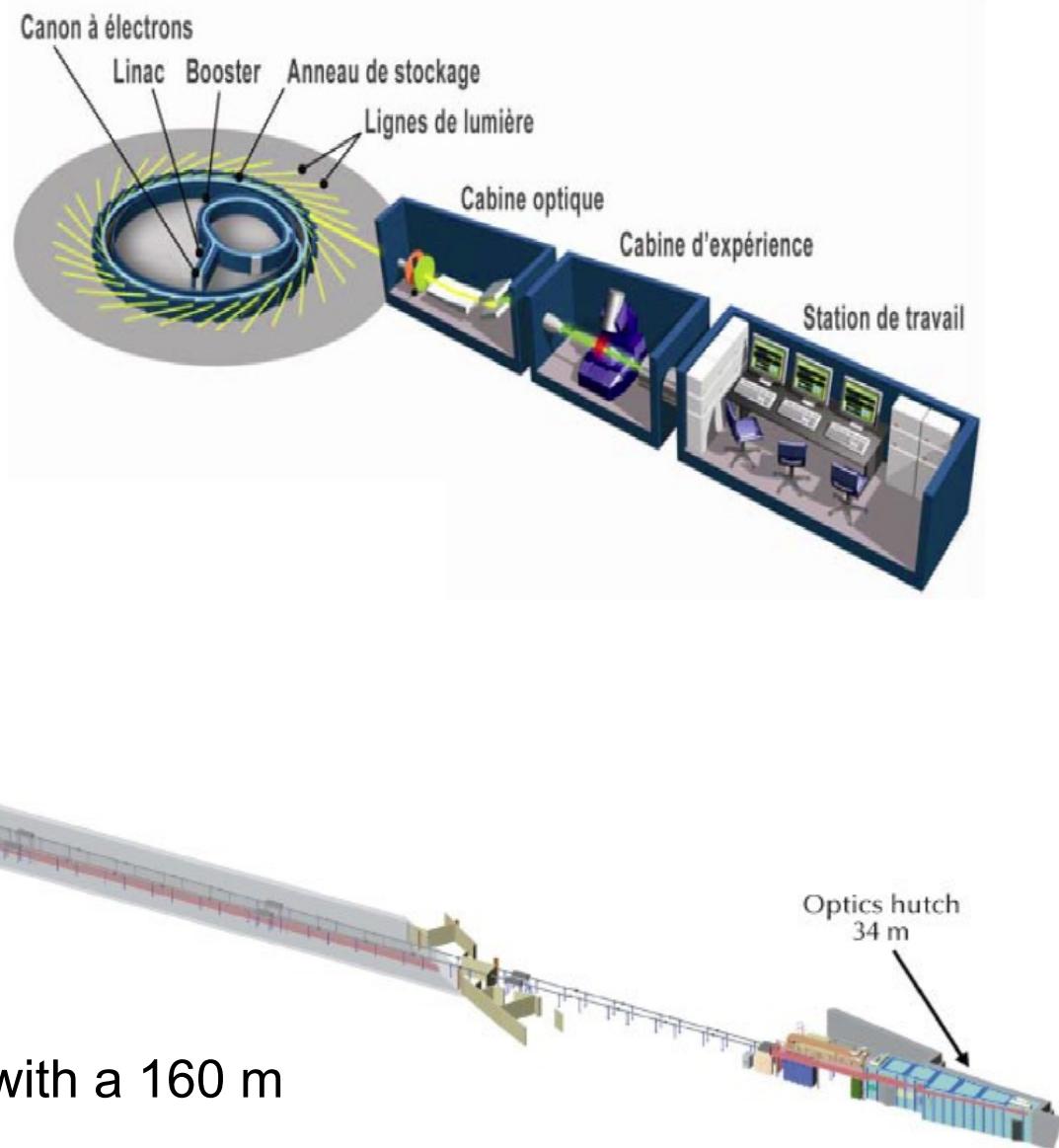
Léti ITSEF

European Synchrotron Radiation Facility
(ESRF)

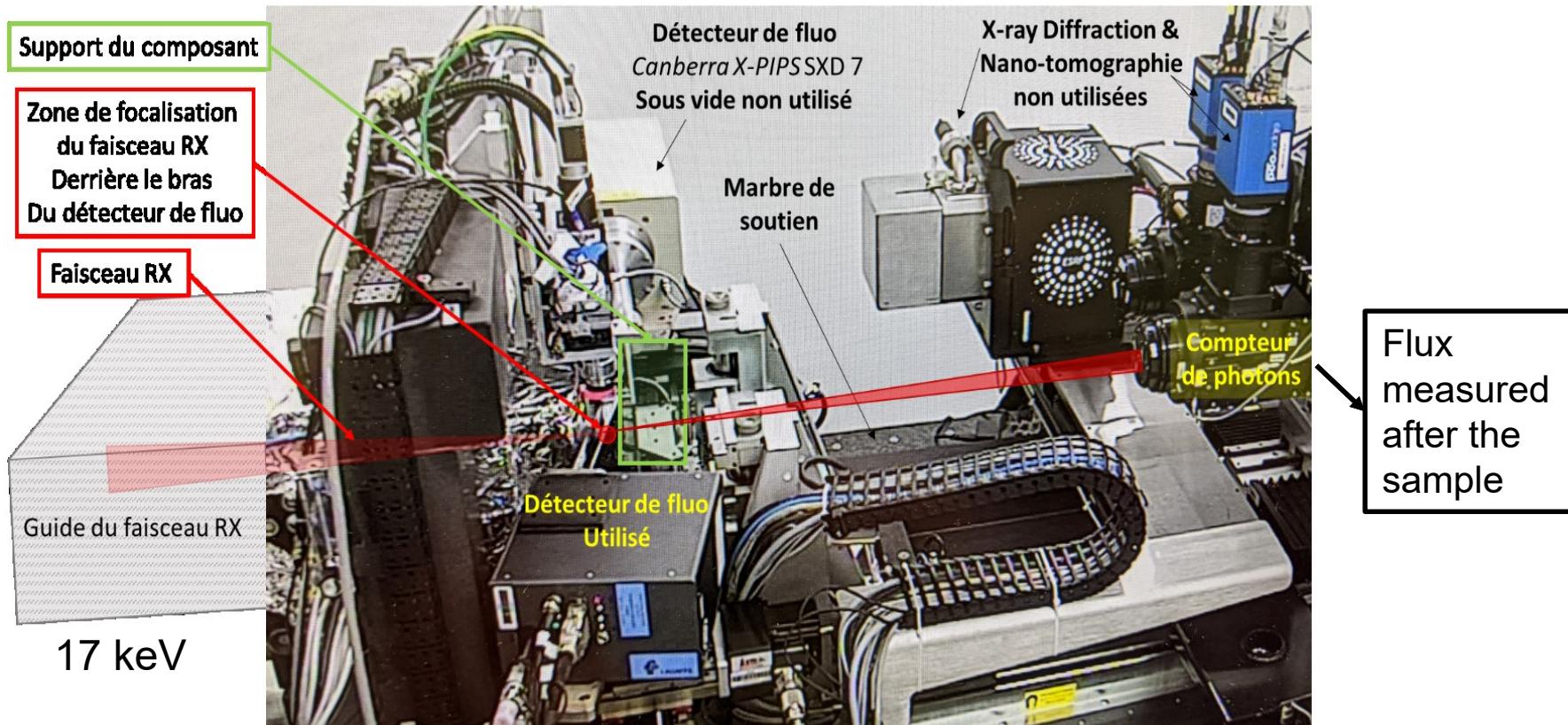


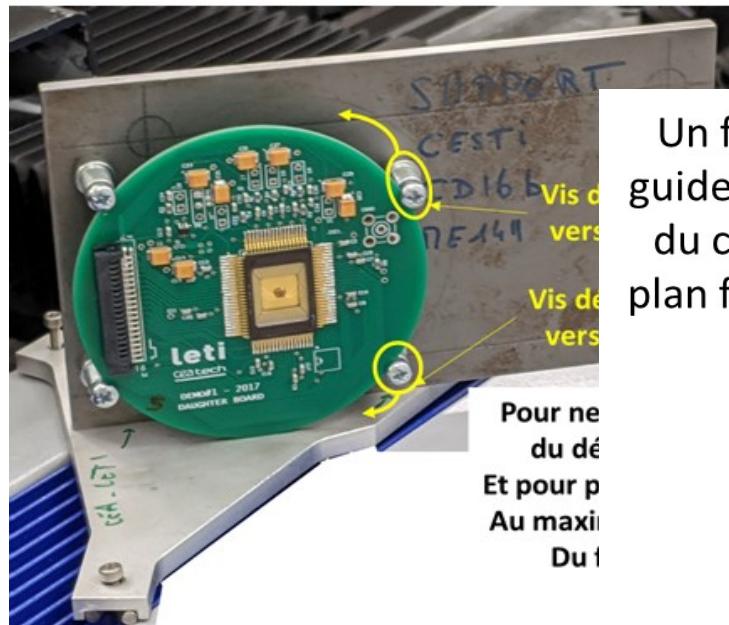
500 m

- Electron packets circulate in the loop
- Photon emitted w/h bending magnets and undulators



60 nm stable nanobeam with a 160 m focalization length

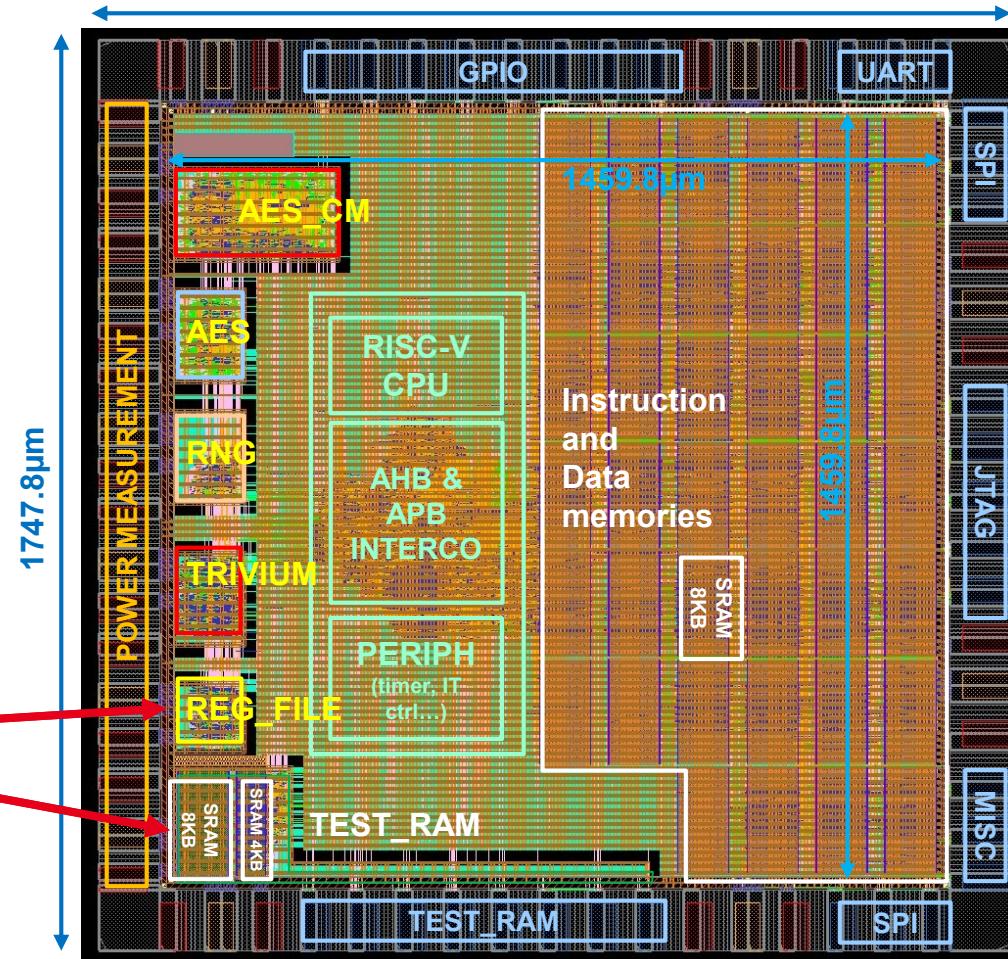


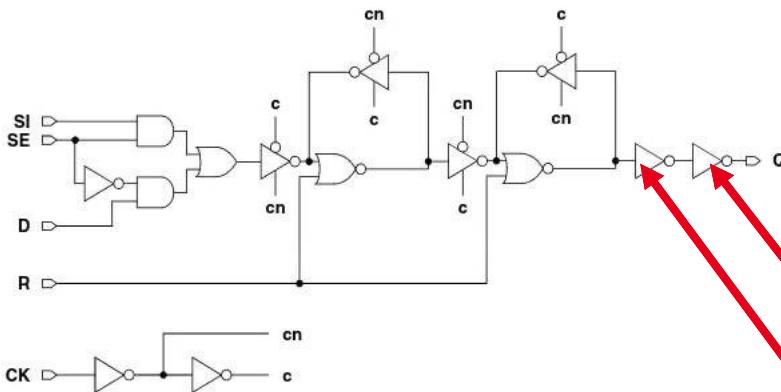


Un faisceau lumineux
guide le positionnement
du composant dans le
plan focal du faisceau RX

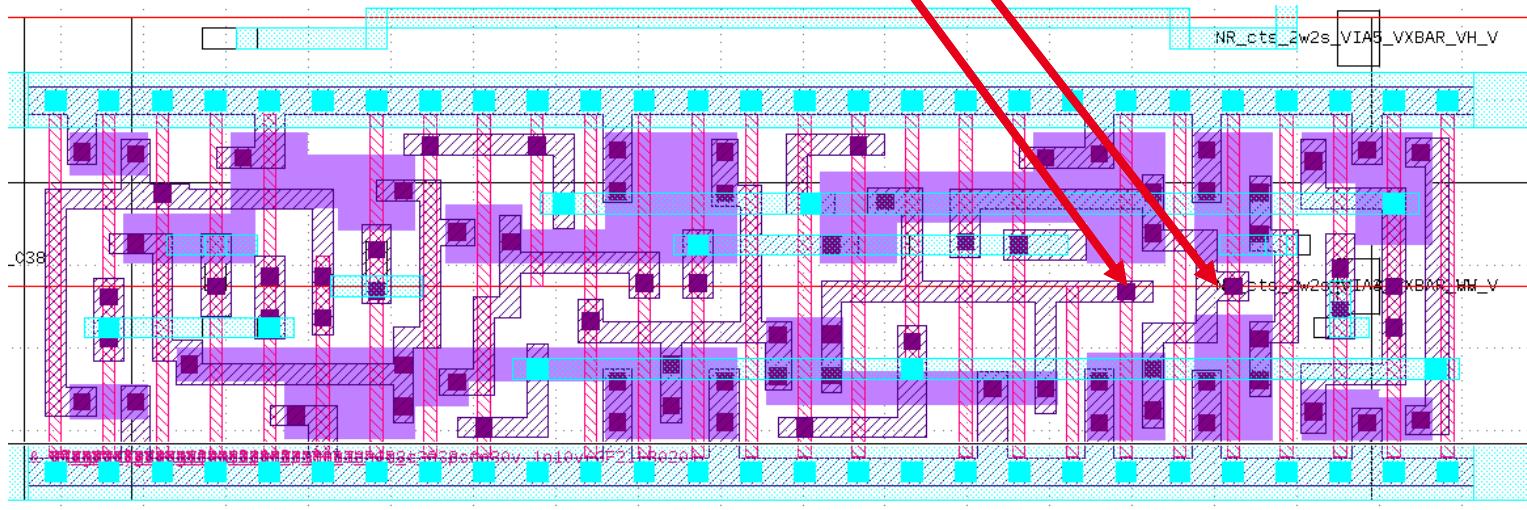


- **TEST COMPONENT : critical knowledge of the TOE**
 - BULK 28 nm technology node / RISC-V CPU
 - Gds2 available





Flip-flop register

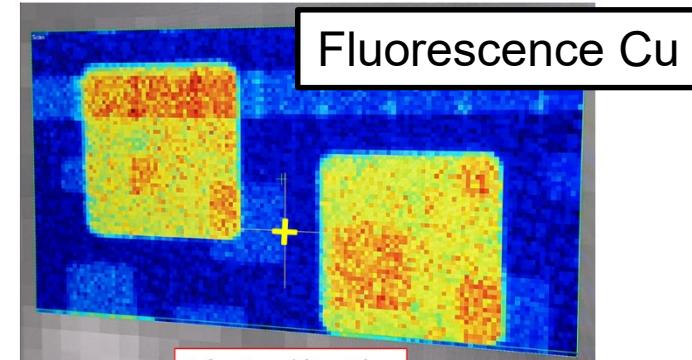


Position 1 – Registre (bloc 5) : 1 min – flux $2,3 \times 10^8$ photons/s (avec atténuateurs Si 3,5 mm)
+ 1 min – flux $6,6 \times 10^{10}$ photons/s (sans atténuateur)

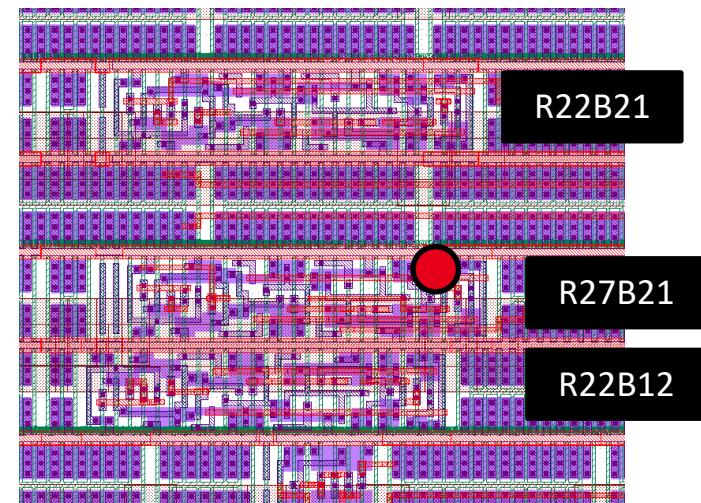
Positions des attaques dans le registre (bloc 5)



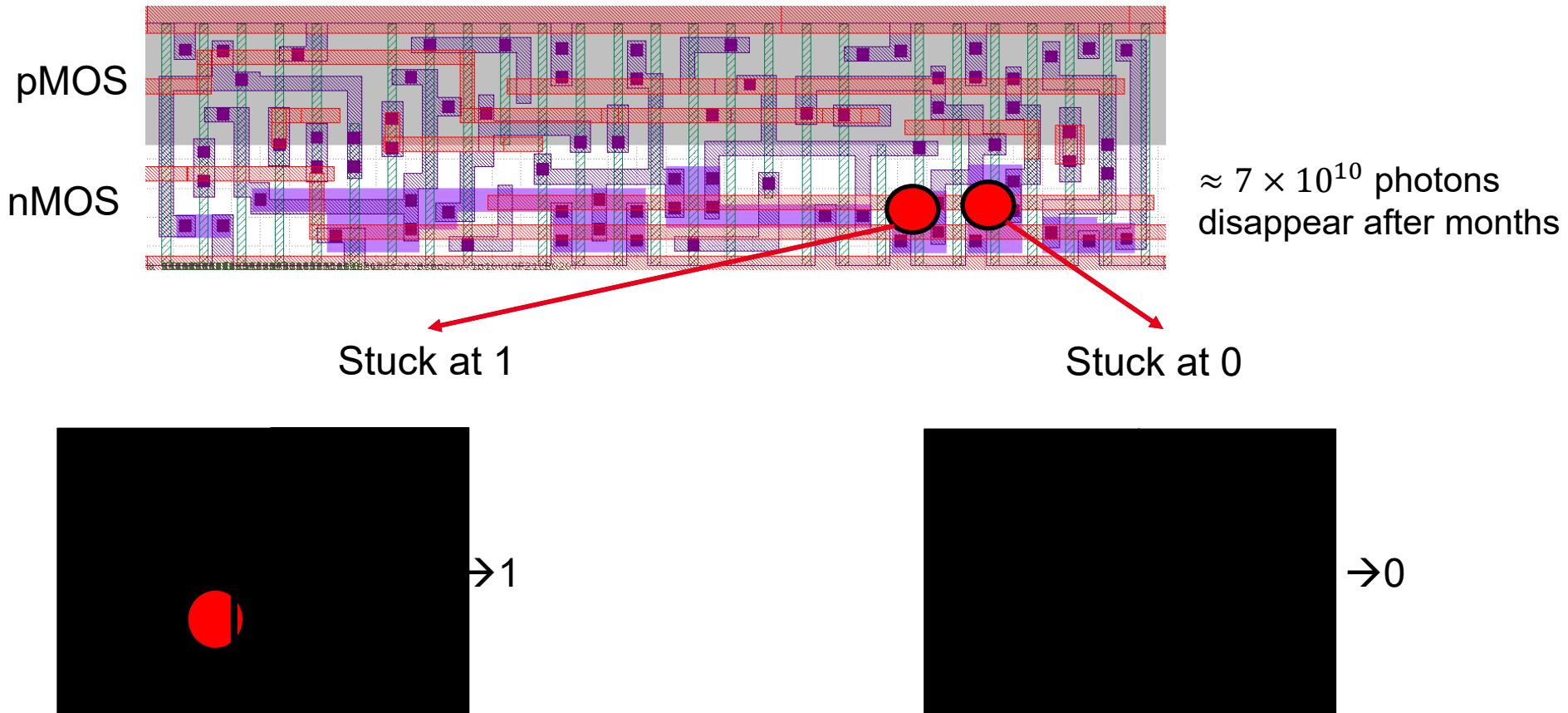
Images optiques



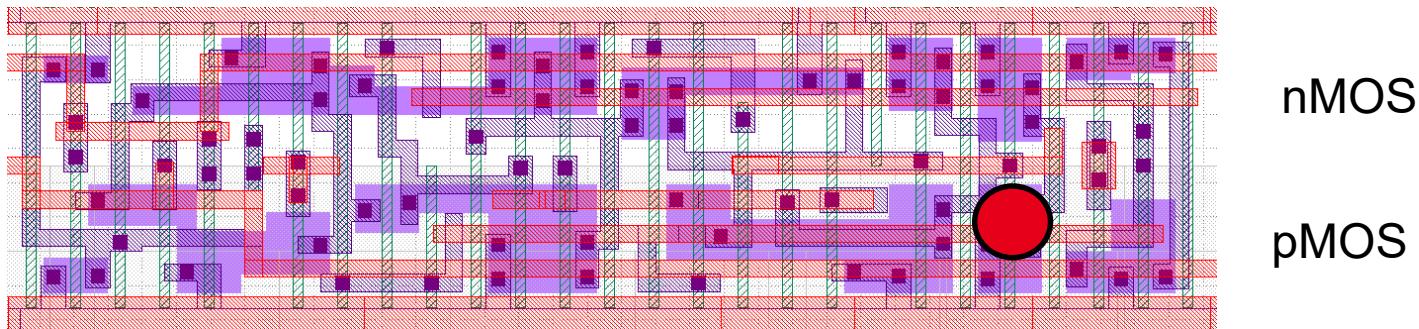
Localization thanks to M6-M7 dummies



STUCK AT 0 OR STUCK AT 1 REG

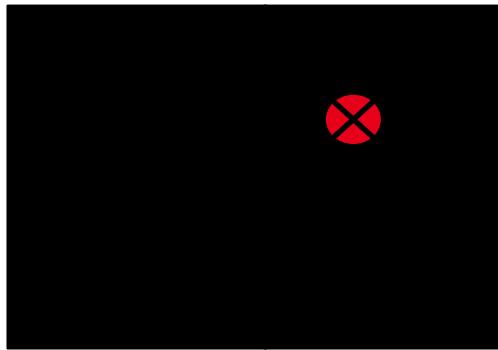


$\approx 3 \times 10^{11}$ photons
Stable after months



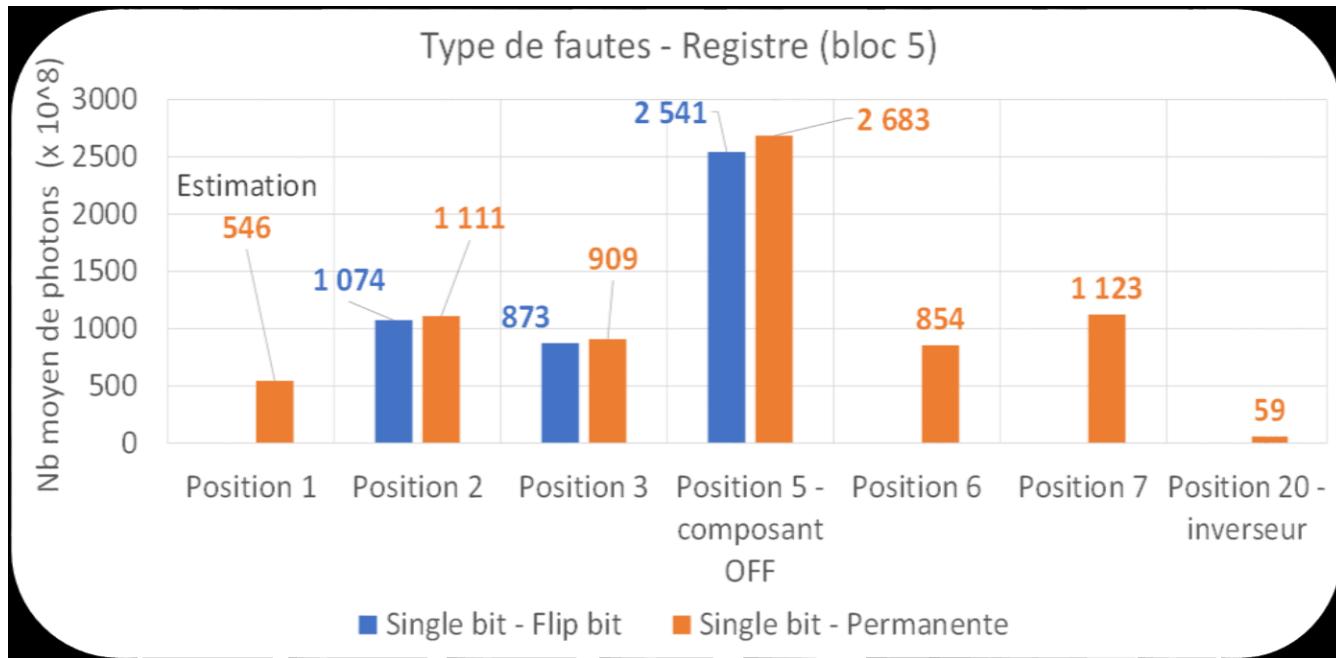
nMOS

pMOS

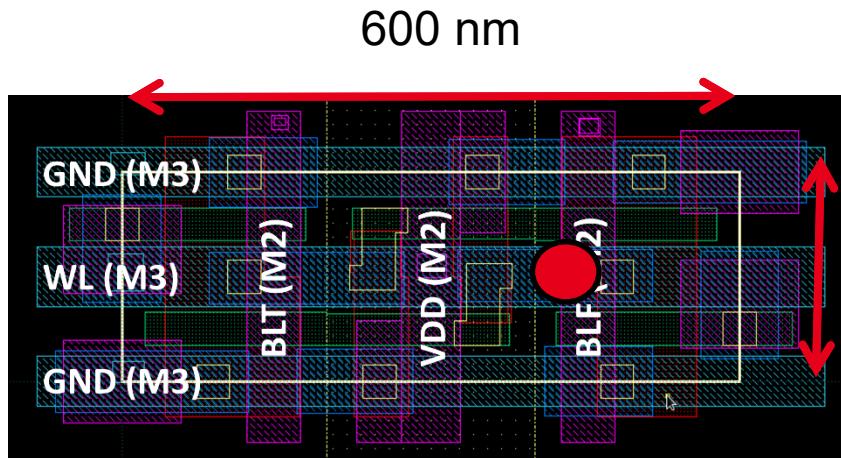


→ Impossible to reach '1'

- Fine tuning => single bit fault made (power on and off)



- Short term fault duration shall be investigated, on-off cycle, annealing.



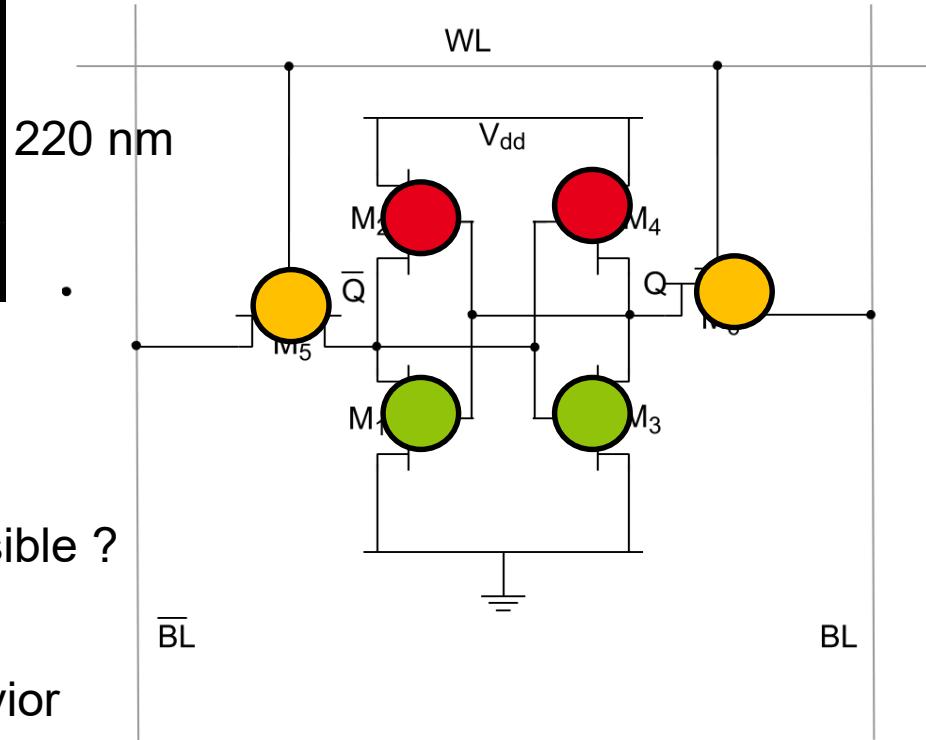
Bit set/reset nMOS



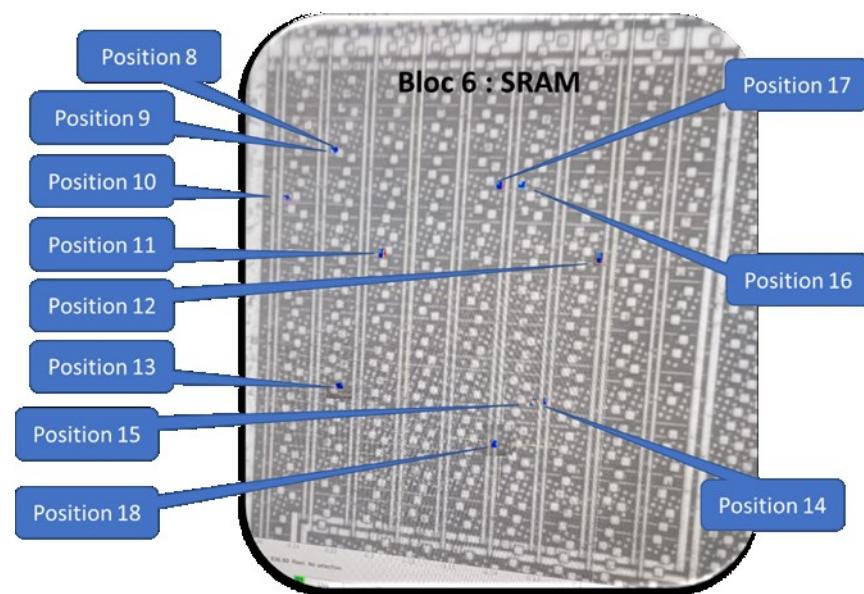
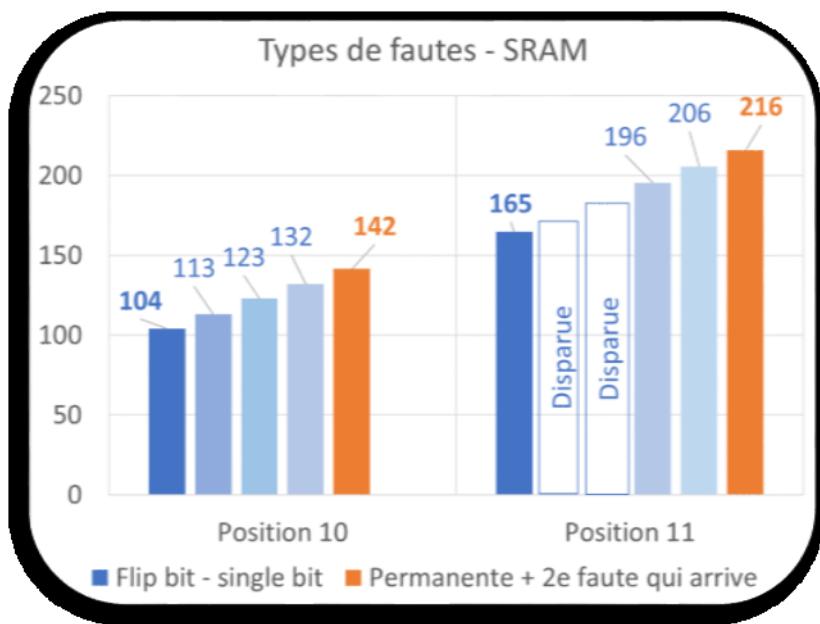
Bit set/reset pMOS possible ?



Whole line faulted behavior



$\sim 150 - 200 \times 10^{18}$ photons pour Single bit fixé
Single bit possible

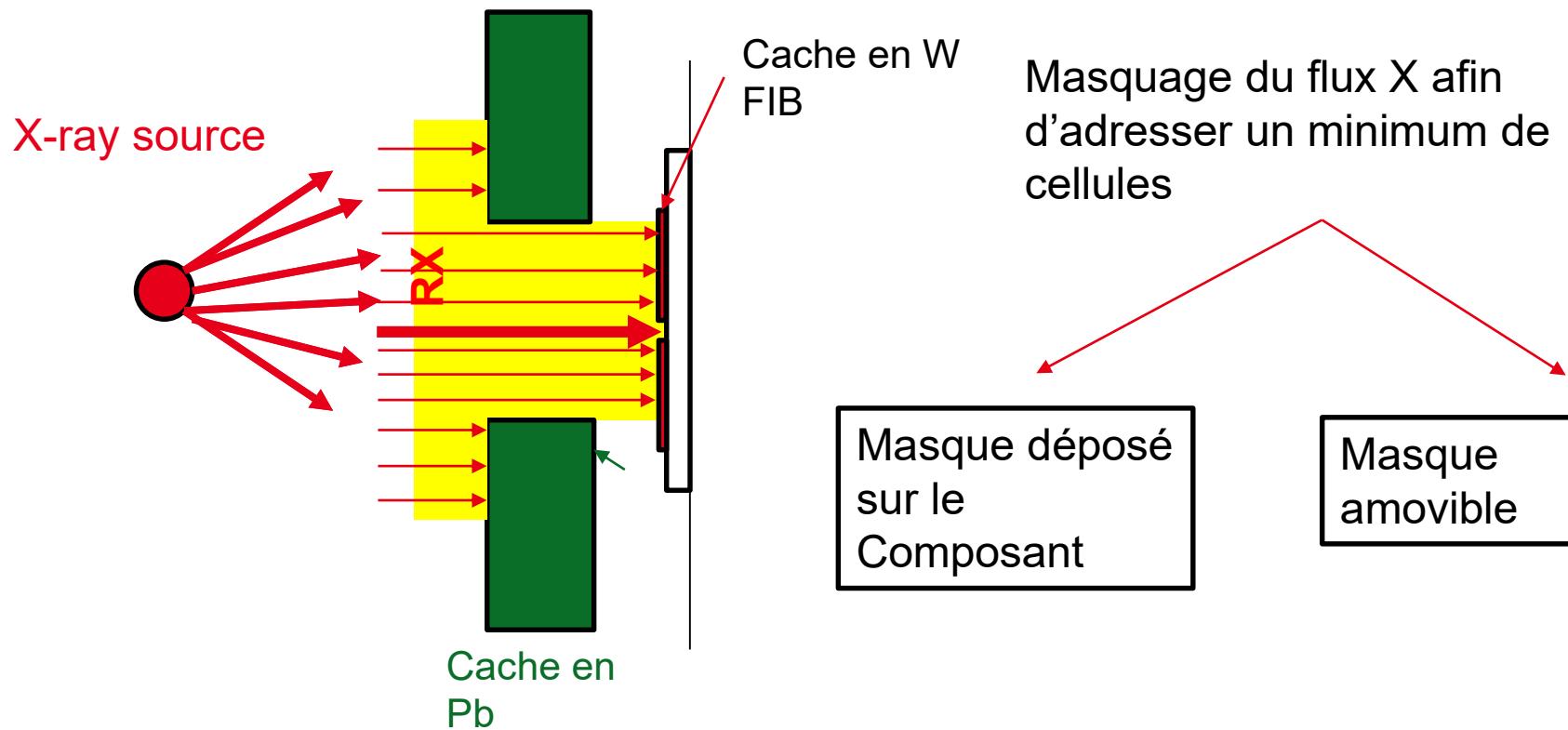
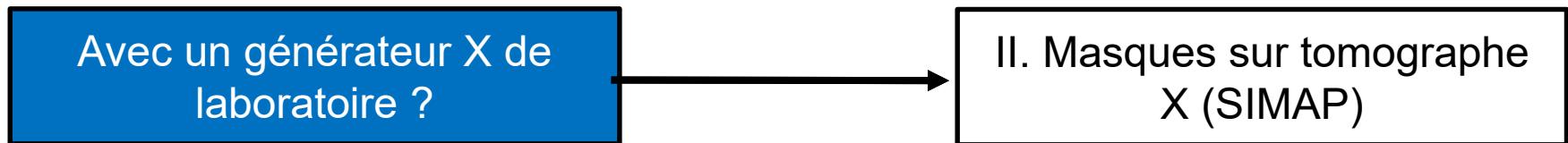


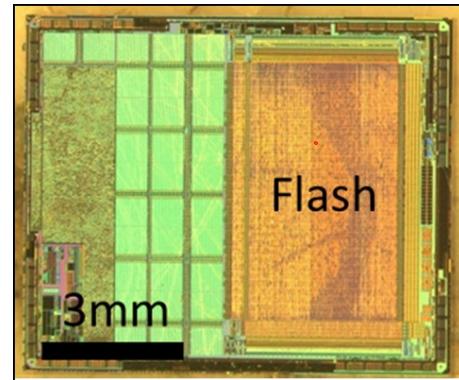
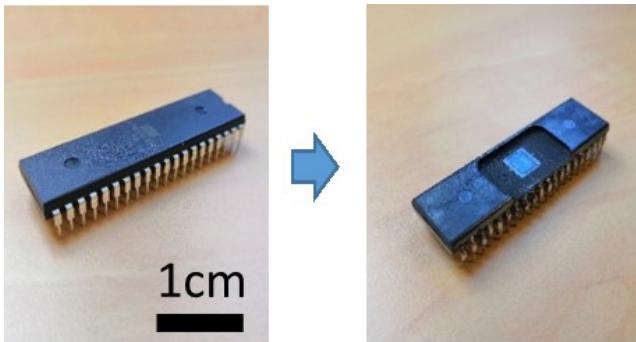
- Possible to modify single transistors with recent MCU technology nodes (28 nm)
- Targetting specific cells is easy with non destructive fluorescence imaging
- Multiple faults shall be simple

Future works (with high attack potential) :

- Demonstration of Persistent Fault Attacks on AES (PFA), new attacks in CPU logic...
- FDSOI 22 nm, lower technology nodes ?

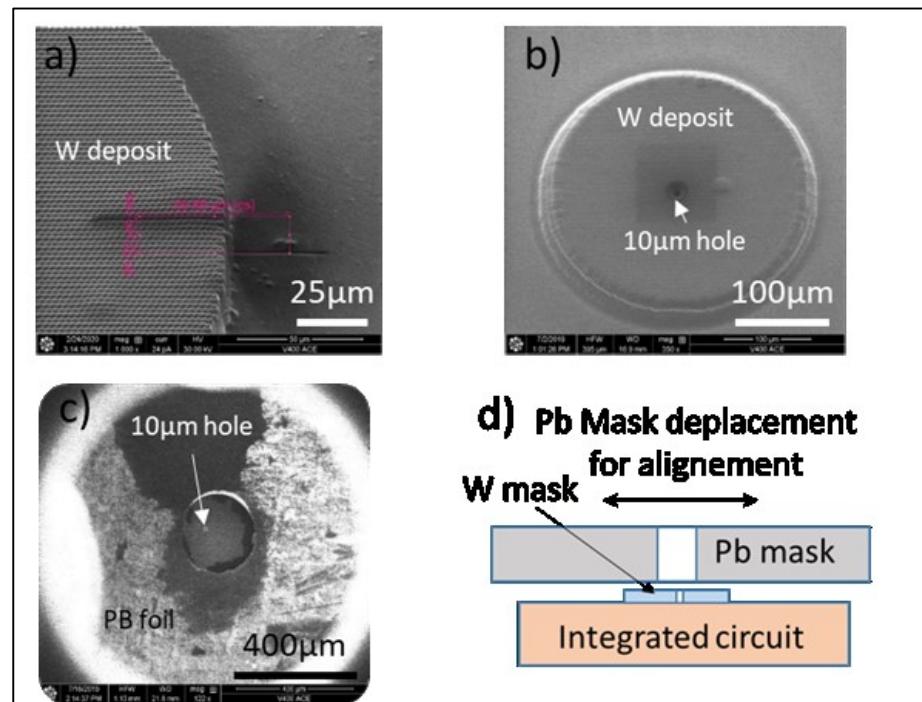
Point de départ: Fautes FLASH & SRAM sur ATMega 128 (0.35 µm) à l'ESRF

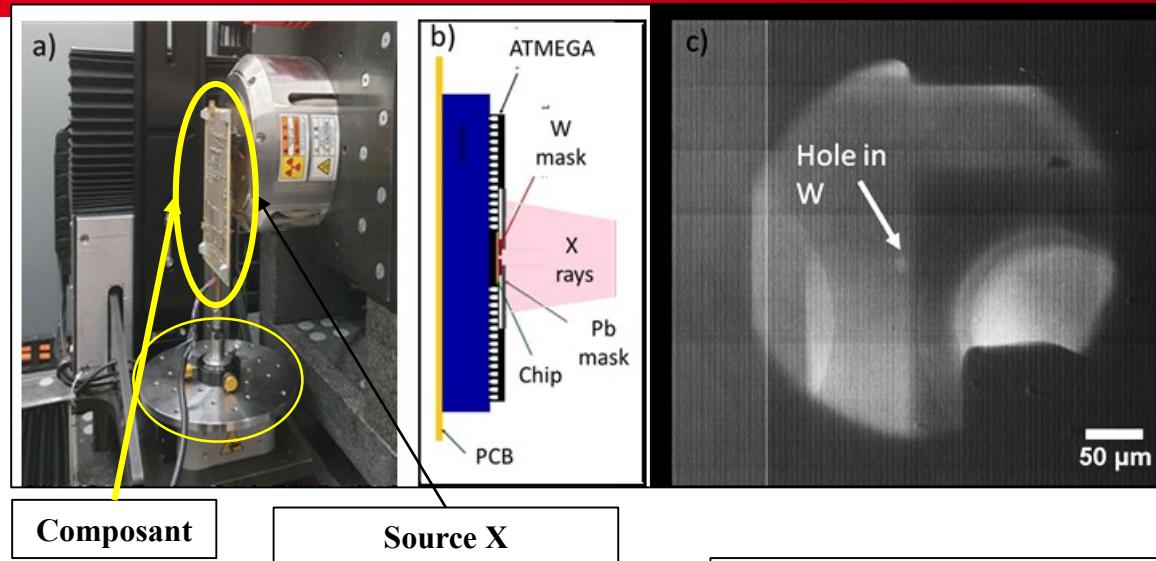




Etapes process:

- Dépôt W (\varnothing 300 μm x ép. 20 μm) au FIB
- & c) avec un trou traversant creusé au FIB (\varnothing 10 μm)
- recouvert par une feuille de Pb (ép. 300 μm) trouée (\varnothing 250 μm)



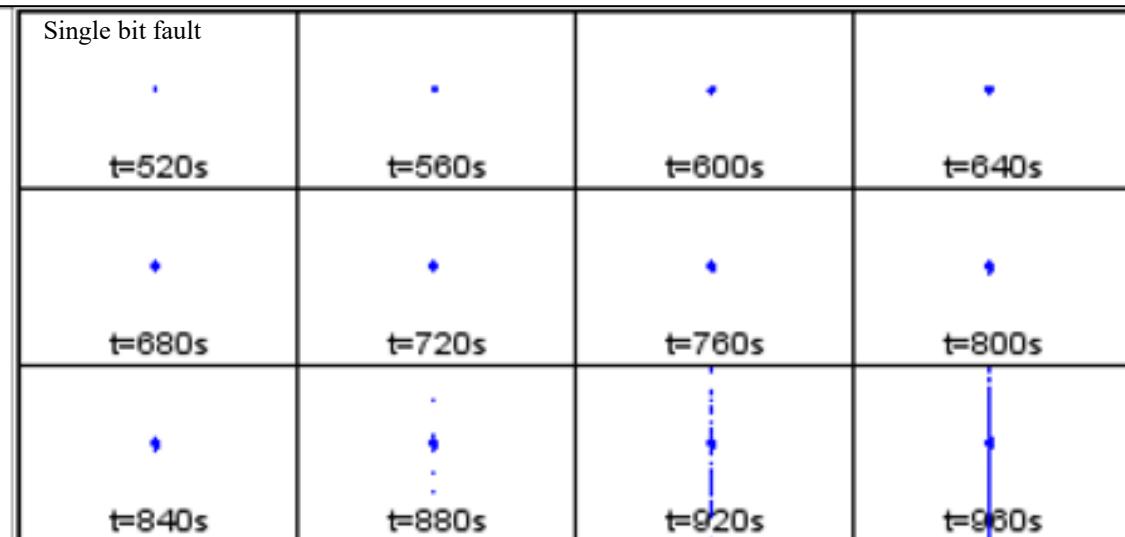
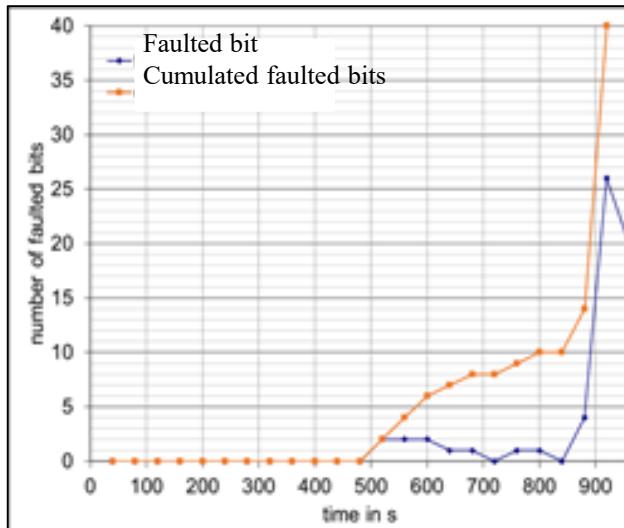


Composant

Source X

Trou $\sim 10 \mu\text{m}^2$

Faute random single bit suivie par un accumulation de bits fautés

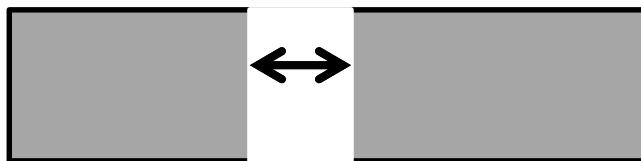


Contrôle position perturbation Cache amovible



Feuille Pb : 50 µm

Plusieurs possibilités

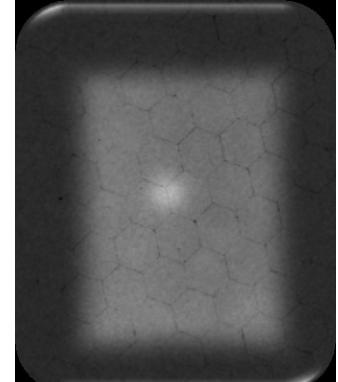
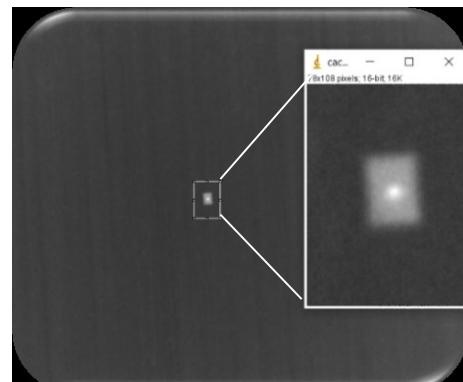
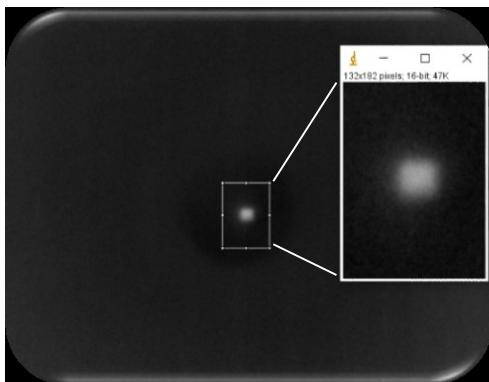


Trou large $30 \mu\text{m}^2 \times 25 \mu\text{m}$
épaisseur

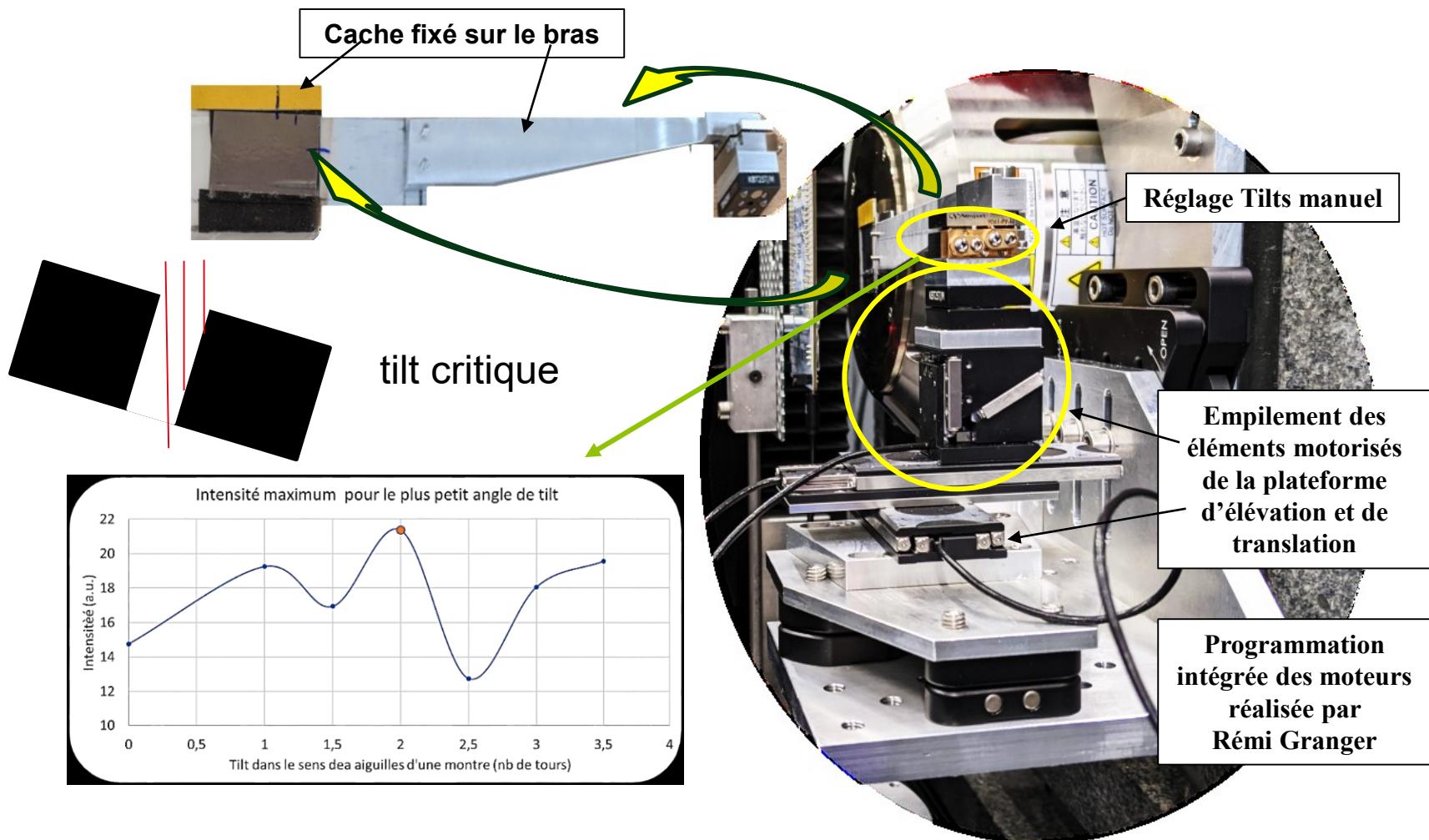


Trou FIB
10 µm

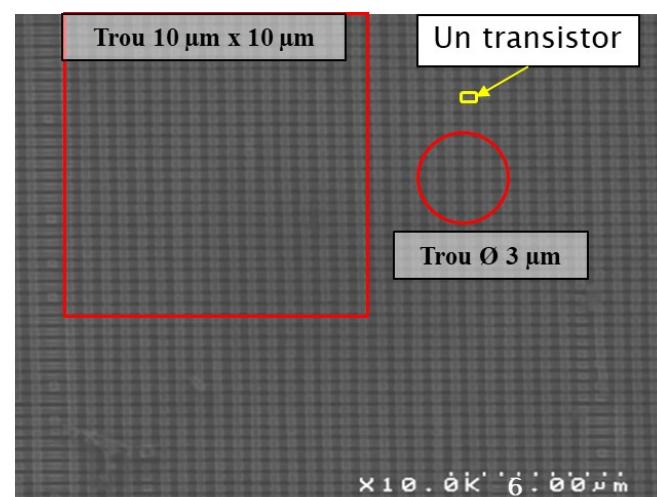
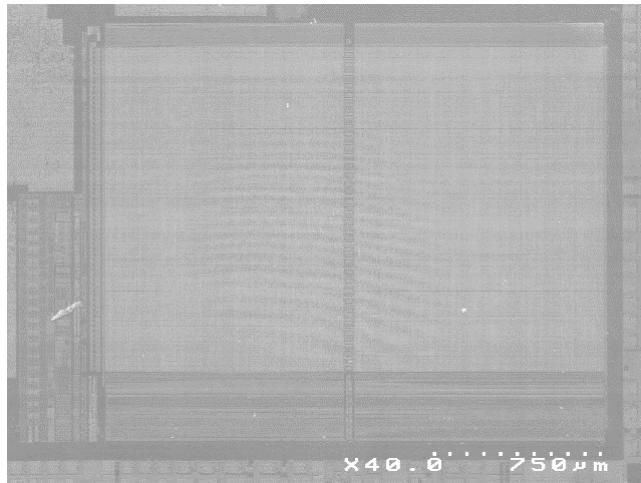
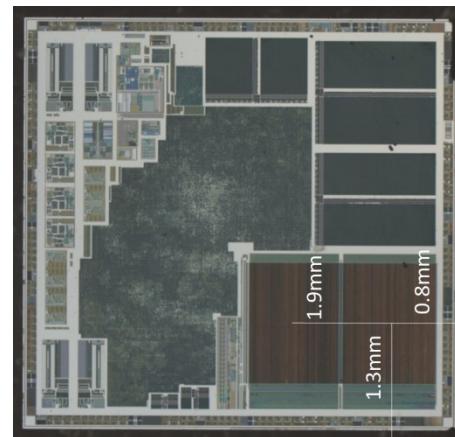
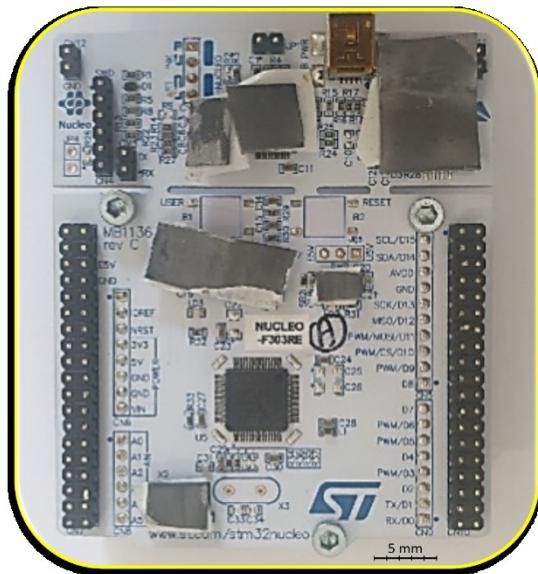
Trou 3 µm / Spot ~1 µm



Transmission X

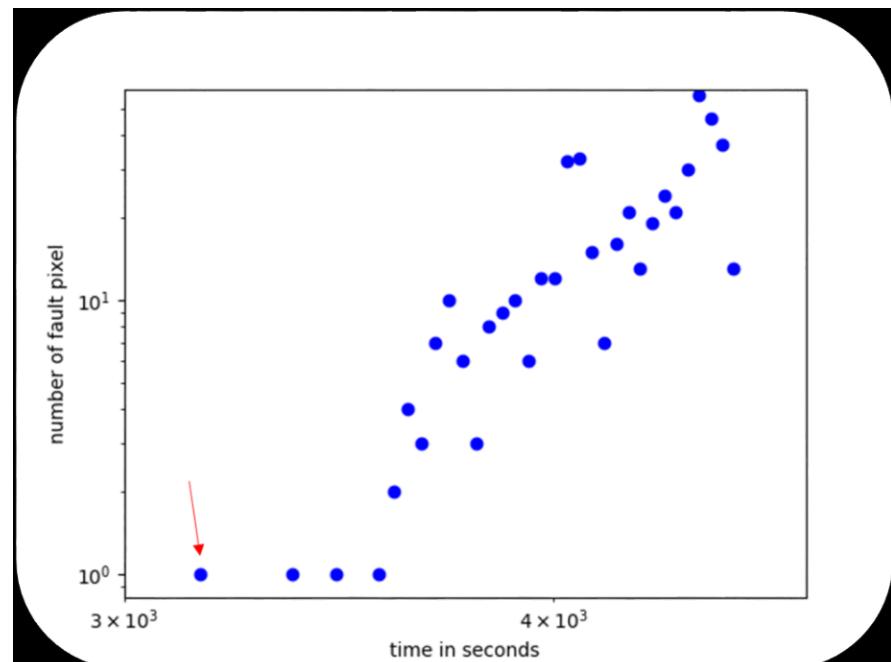
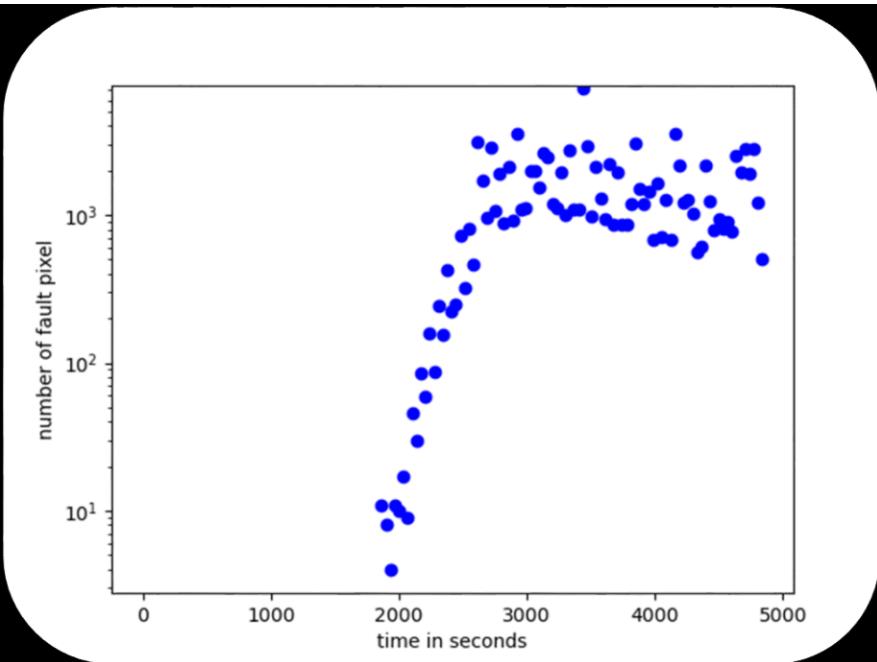


Tilt ⇔ Intensité maximale



Attaque avec Cache Trou $10 \mu\text{m} \times 10\mu\text{m}$
11 fautes au bout de 30 minutes

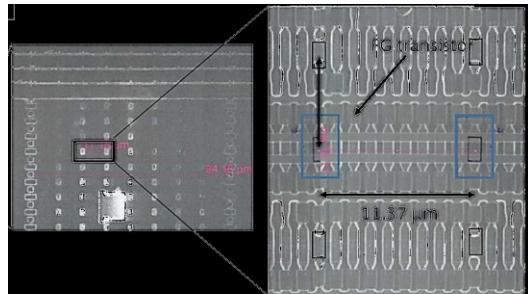
Attaque avec Cache Trou $\varnothing 3 \mu\text{m}$
Faute random single Bit au bout de ~ 50 minutes



Facile à l'ESRF => images de fluorescence à bas flux !

Tomo X =>

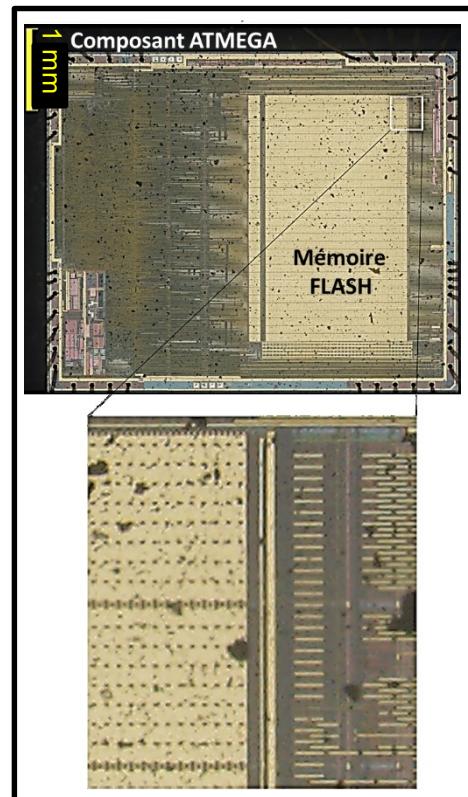
MEB



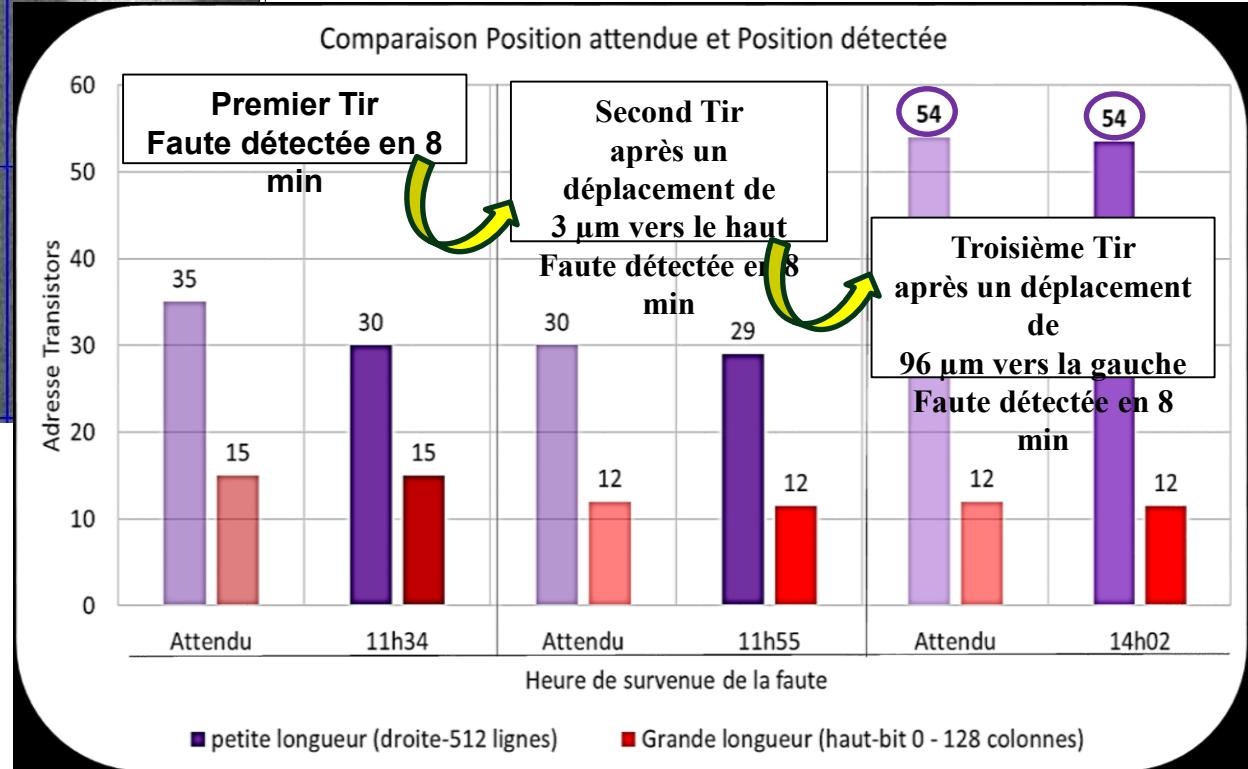
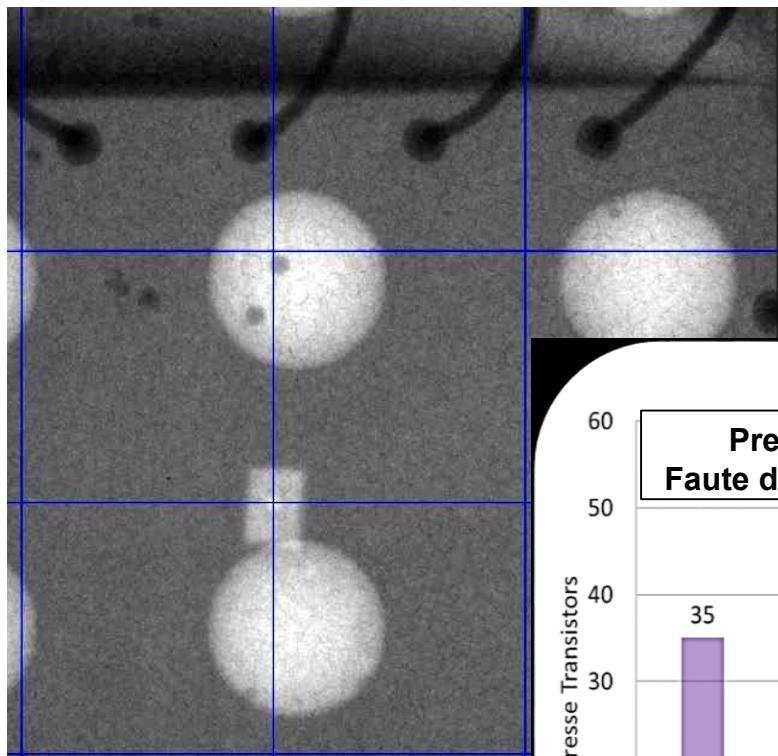
Distance entre centre carré : 11.37 μm
On peut repérer n'importe quel transistor
Par rapport au centre d'un carré

Optique

Transmission X



POSITIONNEMENT PRECIS RESULTATS



- Single bit obtained on 90 nm MCU
- Difficult to target specific cells
- Fault takes time (10s minutes)

Future works :

- Impact if several transistors are perturbed ?
- Mechanical aspects : Better alignment / Smaller masks

- **With a synchrotron => clearly yes, with a high attack potential**
 - Expensive (but not so much indeed)
 - Access not easy
 - Lot of knowledge on the TOE
- **W/o synchrotron => not sure...**
 - Still work to do to obtain at least the same control as for laser fault injections
- **Questions ?**