AN 896: Multi-Rail Power Sequencer and Monitor Reference Design

Contents

683778 | 2024.03.15

Send Feedback

1. Overview of the Multi-Rail Power Sequencer and Monitor Reference Design

The Multi-Rail Power Sequencer and Monitor reference design is a set of highly parameterizable IPs and components that you can customize to suit your power sequencing requirements.

1.1. Features of the Reference Design

The Multi-Rail Power Sequencer and Monitor reference design has the following features:

- The design can control the enable sequence of up to 143 output rails.
- The design can draw from a mix of power good input signals (POK) and monitored voltage rails.
- You can base the power sequencing on voltages reaching a threshold or on timed events.
- You can distribute the design across multiple MAX® 10 devices to increase the number of monitored voltage rails.

These are some of the options, among many others, that the reference design provides:

- Parameterizable levels of glitch filtering on power good or voltage inputs
- Customizable retry responses
- Comprehensive PMBus* interface

To download the Multi-Rail Power Sequencer and Monitor reference design, refer to the related information.

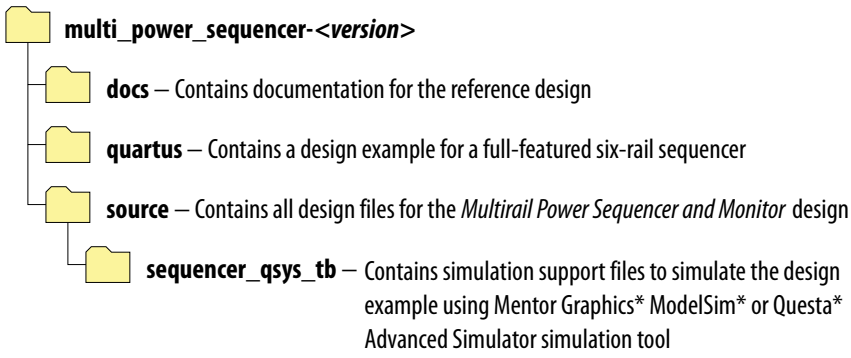
Related Information

Multi-Rail Power Sequencer and Monitor
Provides the Multi-Rail Power Sequencer and Monitor archive file for download.

1.2. Structure of the Reference Design Archive

The Multi-Rail Power Sequencer and Monitor reference design comes in a design archive file—`Power_Sequencer.zip`. To download the reference design archive, refer to the related information.

Figure 1. Multi-Rail Power Sequencer and Monitor Directory Structure



Related Information

- Multi-Rail Power Sequencer and Monitor
  Provides the Multi-Rail Power Sequencer and Monitor archive file for download.
- Implementation and Simulation of the Multi-Rail Power Sequencer and Monitor Reference Design on page 23

2. Architecture and Operation of the Multi-Rail Power Sequencer and Monitor Reference Design

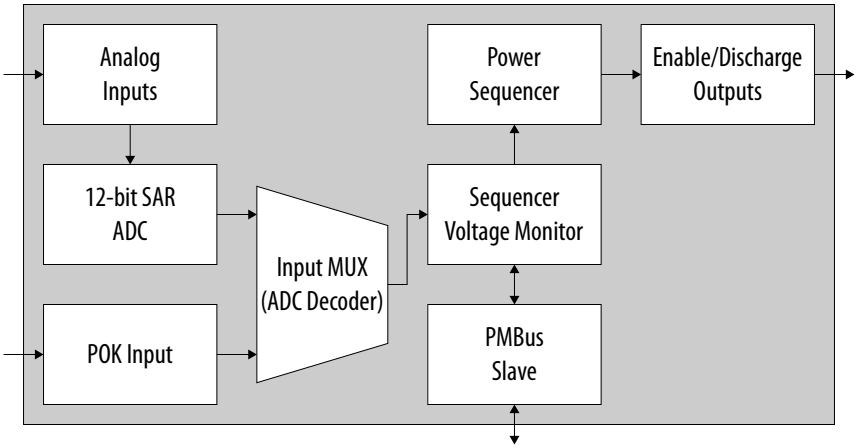
Electronic systems that contain FPGAs, CPUs, digital signal processing (DSP) blocks, and ASICs require specific sequences for applying and removing power.

The Multi-Rail Power Sequencer and Monitor reference design provides you the ability to monitor and correctly sequence up to 144 rails—including monitoring VIN—through normal operations, as well as error conditions:

- Accepts any combination of analog voltage and digital power good input signals.
- Maps any analog-to-digital converter (ADC) input or power good signal to any monitored VOUT or VIN rail.

2.1. Reference Design Architecture

Figure 2. Multi-Rail Power Sequencer and Monitor Top Level Block Diagram



The reference design passes the remapped and decoded inputs to the Sequencer Voltage Monitor component. The Sequencer Voltage Monitor component checks and reports the statuses, among others, for the power good signal, undervoltage, overvoltage, alarms, and present voltage levels.

The reference design provides information about the state of the various rails to the PMBus slave interface, a protocol that operates on the I^2C physical interface. The design is compliant to the PMBus 1.3.1 specification and can operate in 100 KHz and 400 KHz modes.

The Power Sequencer component implements a sequential approach when powering up the rails and powers them down in the reverse order. The Power Sequencer component uses the output of the Sequencer Voltage Monitor component to enable and disable the various power rails.

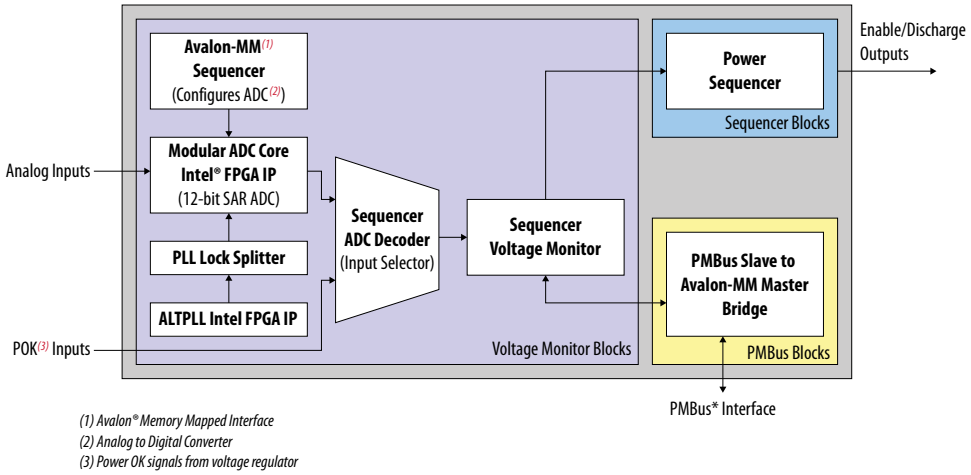
Related Information

PMBus website
Provides more information about the PMBus 1.3.1 specification.

2.2. Reference Design Component Blocks

The reference design partitions the functions into multiple component blocks.

Figure 3. Multi-Rail Power Sequencer and Monitor Design Blocks



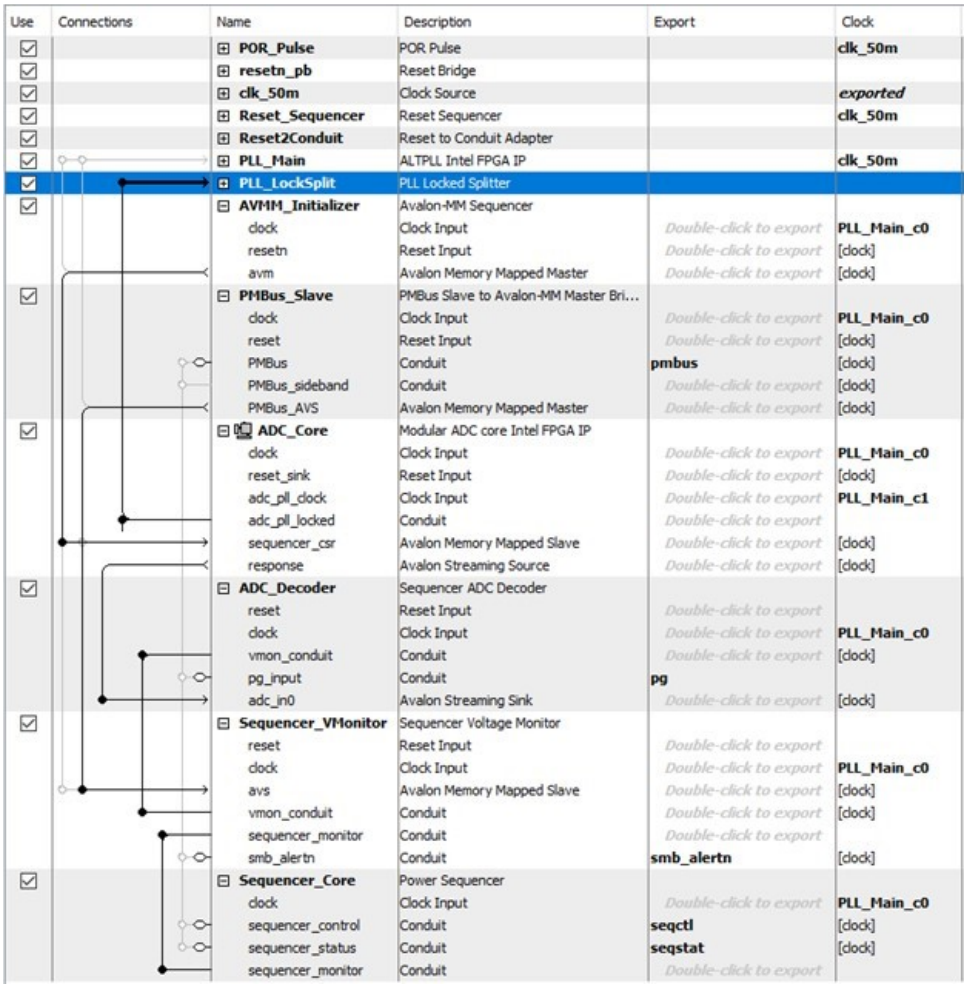
You can remove any blocks you do not need and customize the sequencer for the most cost-effective implementation:

- If you need only a simple sequencer that bases its control on the state of the POK signals, you can use the Power Sequencer component alone.
- If you want to monitor voltage rails but do not require PMBus support, you can remove the PMBus Slave to Avalon®-MM Master Bridge component.

2.3. Design Components and Parameter Options

The reference design consists of several components. Many of the components provide customizable parameter settings.

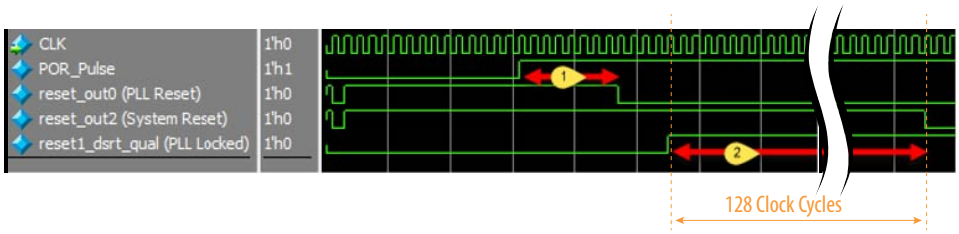
Figure 4. Full-featured Multi-Rail Power Sequencer and Monitor Implementation in the Platform Designer



2.3.1. Reset Sequencer (Reset_Sequencer)

This block provides a controlled reset sequence to the power sequencer design. After configuration and upon entering user mode, a programmable reset pulse is generated by POR_Pulse to the Reset_Sequencer. The Reset_Sequencer re-synchronizes the pulse and asserts reset_out0 (refer to the following figure at time interval 1), which is used to reset the PLL. It waits for the PLL to lock, debouncing it for 128 clock cycles (refer to the following figure at time interval 2) after which it asserts the system reset.

Figure 5. Reset Sequencer



2.3.2. Modular ADC Core Intel® FPGA IP (ADC_Core)

The MAX 10 analog to digital converter (ADC) block is a 12-bit successive approximation register (SAR) ADC with a one million samples per second (MSPS) sampling rate. The Modular ADC Core Intel® FPGA IP is a standard MAX 10 IP that sequences through the various analog input channels, providing you with a 12-bit representation of the input voltage level.

Figure 6. ADC Channel Configuration

The configuration of the Modular ADC Core IP in the reference design uses the **Standard sequencer with external sample storage** core variant. In this core variant, the IP passes the sampled input directly to a streaming output interface instead of buffering the data internally.

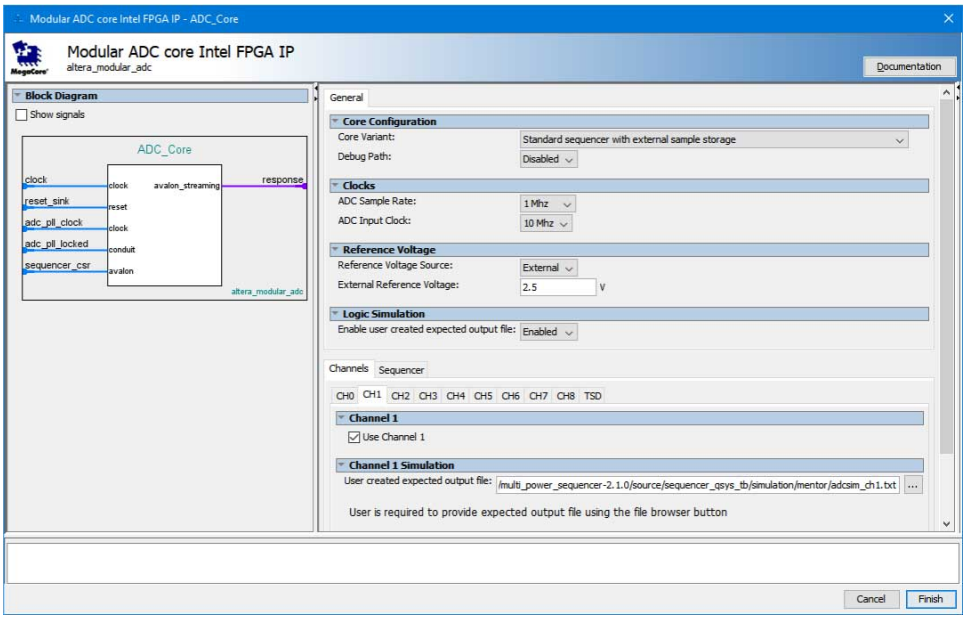
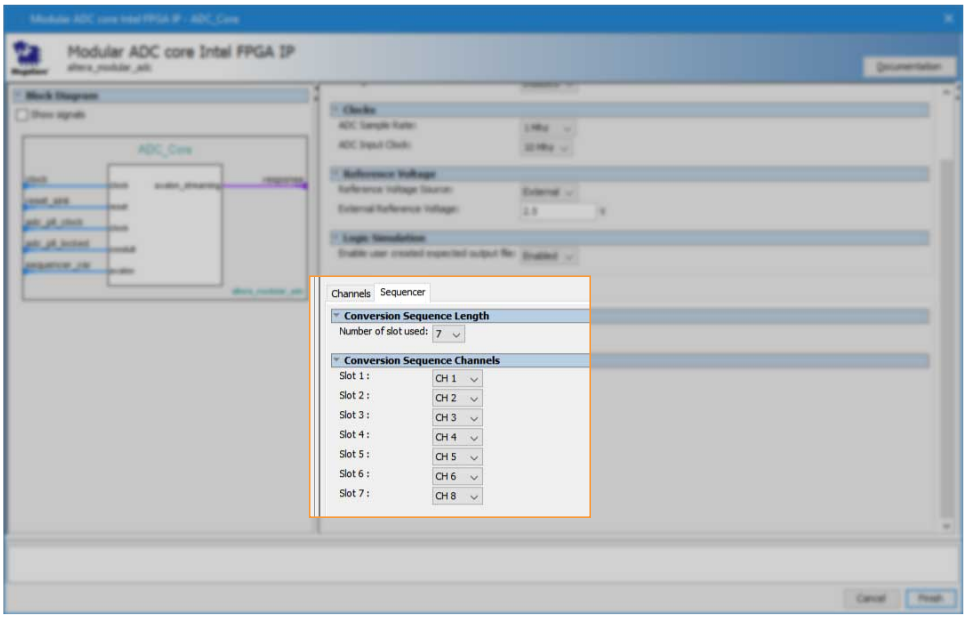


Figure 7. ADC Sequencer Configuration

The configuration of the Modular ADC Core IP in the reference design sets the programmable ADC sequencer to operate in a round-robin fashion, sequencing through each of the analog inputs.



For higher accuracy, always use an external reference voltage:

- For dual-supply MAX 10 devices, use a 2.5 V external reference voltage.
- For single-supply MAX 10 devices, use a 3.0 V or 3.3 V external reference voltage.

To ensure that the maximum value of the power rail is within the measurable range of the ADC, use external voltage dividers on the monitored rails:

- Keep thresholds such as the overvoltage fault less than the reference voltage.
- Use resistor values that maximize the measurement accuracy by not dividing lower than necessary.

Related Information

- Configuration 3: Standard Sequencer with External Sample Storage, MAX 10 Analog to Digital Converter User Guide
  Provides more information about the **Standard sequencer with external sample storage** core variant.
- Modular ADC Core Parameters Settings, MAX 10 Analog to Digital Converter User Guide
  Describes the available parameters of the Modular ADC Core Intel FPGA IP.

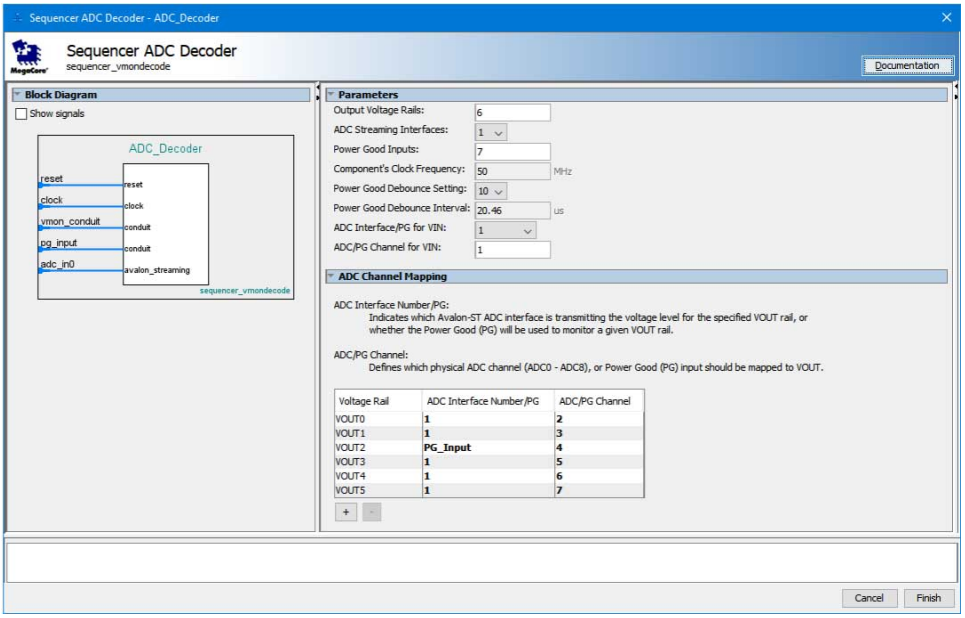
2.3.3. Sequencer ADC Decoder (ADC_Decoder)

The Sequencer ADC Decoder component decodes up to 16 Avalon Streaming (Avalon-ST) ADC interfaces to sets of voltage level busses. Depending on which device you choose, each Avalon-ST ADC interface can contain voltage levels of up to nine or 17 analog input channels. The sequencer allows a total of 144 monitored voltage levels.

Additionally, the Sequencer ADC Decoder component allows you to map any of the voltage level busses or external POK signals to any monitored VOUT or VIN rail. The configurable options allow you to specify the number of VOUT rails, the number of ADC interfaces, the number of power good inputs (POK signals), and how long to debounce the power good inputs.

The debouncer passes through the POK signal only after it has been stable for the duration of the debounce interval. You can select from 28 levels of debounce. The duration of the interval depends on the clock frequency that you provide to the component.

Figure 8. Sequencer ADC Decoder Parameter Editor



The progression of the debounce level is exponential in time. The parameter editor of the Sequencer ADC Decoder component calculates the debounce duration only after the clock of the component connects to the system clock in Platform Designer. Otherwise, the parameter editor does not make any calculation and the **Component's Clock Frequency** box displays 0 MHz.

For every VIN and VOUT rail, you can select the source for the **ADC Interface/PG** input and the **ADC/PG Channel**. Typically, select a unique interface and channel combination for each rail. If you set multiple rails to the same combination, the parameter editor displays a warning message. However, the Quartus® Prime software still allows you to generate the system if that is what you want.

2.3.3.1. Sequencer ADC Decoder Parameter Settings

There are two groups of options: **Parameters** and **ADC Channel Mapping**.

Table 1. Sequencer ADC Decoder Parameters - Parameters

Parameter	Description
Output Voltage Rails	Specify the number of output voltage rails to sequence.

continued...

Parameter	Description
	The number must match the value you specify in the other components of the system. Otherwise, the interface bus widths between components will not match.
ADC Streaming Interfaces	Select the number of Avalon-ST interfaces from the Sequencer ADC Decoder to the Modular ADC Core IP. • A single-ADC MAX 10 device has one interface while a dual-ADC MAX 10 device has two Avalon-ST interfaces. • If you use several MAX 10 devices to monitor voltage inputs, you can increase the number of streaming interfaces. To allow external interconnect, export the interfaces from the system.
Power Good Inputs	Specify the number of power good inputs to monitor. The number must match the value you specify in the other components of the system. Otherwise, the interface bus widths between components will not match.
Component's Clock Frequency	Read-only parameter that specifies the component's input clock frequency. • The number depends on which clock you connect to the component in the Platform Designer. • Ensure that this frequency is correct. Otherwise, the system cannot derive the correct debounce values.
Power Good Debounce Setting	Select the number of clock cycles (2^n) that the power good input signal must be stable before the component forwards the signal downstream.
Power Good Debounce Interval	Calculated parameter that specifies the duration (in µs) for which the power good input must be stable • The number is based on the **Power Good Debounce Setting** that you select. • The parameter editor cannot calculate this value if the input clock is not connected to a clock signal or if the rate is unknown.
ADC Interface/PG for VIN	Select the interface that transmits the voltage level to the VIN rail: • **PG_Input**—use a power good signal from the VRAIL_PWRGD[] input bus to control the VIN rail. • **1** to **16**—the Avalon-ST ADC interface that transmits the voltage level. The available interface numbers depend on the number of **ADC Streaming Interfaces** you select.
ADC/PG Channel for VIN	Specify the physical ADC channel (ADC0 to ADC8) or power good input bit to map to the VIN rail.

Table 2. Sequencer ADC Decoder Parameters - ADC Channel Mapping

Parameter	Description
ADC Interface Number/PG	Select the interface that transmits the voltage level to the VOUT rail: • **PG_Input**—use a power good signal from the VRAIL_PWRGD[] input bus to control the VOUT rail. • **1** to **16**—the Avalon-ST ADC interface that transmits the voltage level. The available interface numbers depend on the number of **ADC Streaming Interfaces** you select.
ADC/PG Channel	Specify the physical ADC channel (ADC0 to ADC8) or power good input bit to map to the VOUT rail.

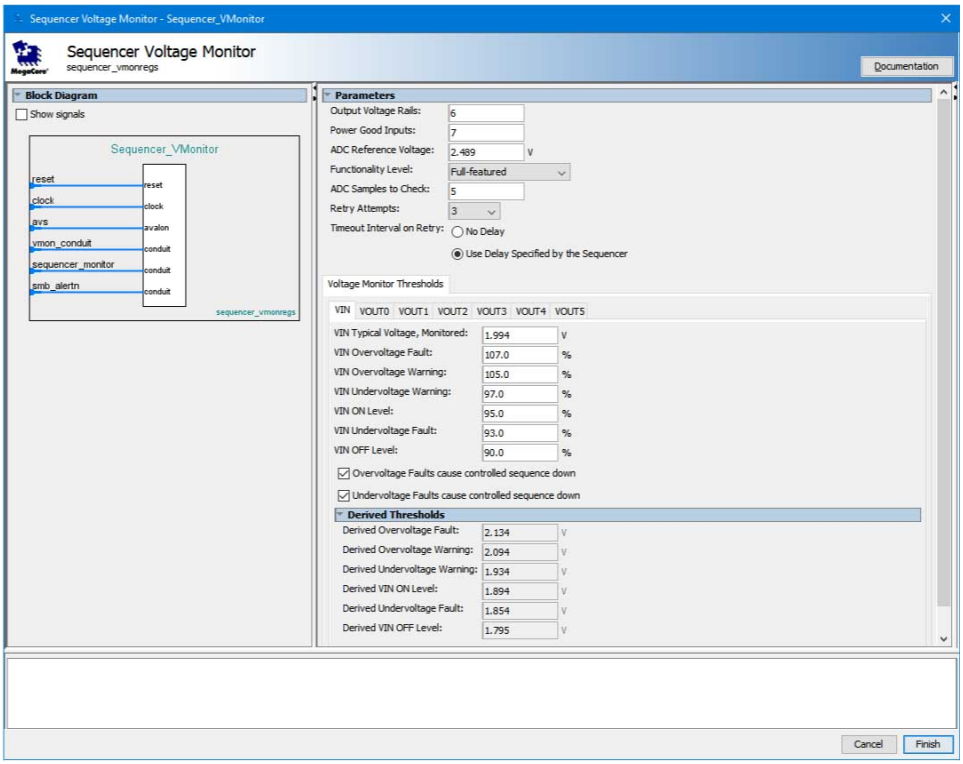
2.3.4. Sequencer Voltage Monitor (Sequencer_VMonitor)

The Sequencer Voltage Monitor component performs two primary functions:

- Monitors the voltage levels provided by the ADC inputs, providing status and alerts via PMBus communication
- Creates internal power good status levels (POK signals) that the Power Sequencer component uses to appropriately power up and down the various VOUT rails.

You can configure several parameters for the Sequencer Voltage Monitor component. For a proper interface to the Sequencer ADC Decoder component, you must accurately specify the number of **Output Voltage Rails** and **Power Good Inputs** parameters.

Figure 9. Sequencer Voltage Monitor Parameter Editor



To prevent false errors or warnings that may be caused by noise on monitored voltage rails, specify the **ADC Samples to Check** parameter. The design only reports an error or warning condition if the condition is present for the number of samples you specify in this parameter.

The interval duration depends on the sample rate and sequencer configuration in the ADC. For example, assume that you configure the Modular ADC Core IP sequencer to process the inputs in a round-robin fashion, reporting the voltage levels for each channel in sequence over seven time slots. If the sample rate is 1 MSPS and you configure the Sequencer Voltage Monitor component to check that five samples exceed the threshold before declaring a warning or error, then the warning or error must be present for $1\ \mu s \times 7\ \text{time slots} \times 5\ \text{samples} = 35\ \mu s$.

Note: The **Retry Attempts** and **Timeout Interval on Retry** parameters are global settings. You can dynamically control these settings through the subset of PMBus commands that affect any of the VIN or VOUT error responses. Changing the response behavior of one command affects all commands that have these parameters.

If an ADC VIN pin monitors a rail, either one of these settings determines the rail's power good status:

- The levels set in the default configuration of the Sequencer Voltage Monitor within the Platform Designer.
- The dynamically modified levels set through the PMBus interface.

The Power Sequencer component uses the power good status outputs to sequence the power regulators on or off.

The following PMBus commands dynamically adjust the levels to assert or deassert the internal power good signal:

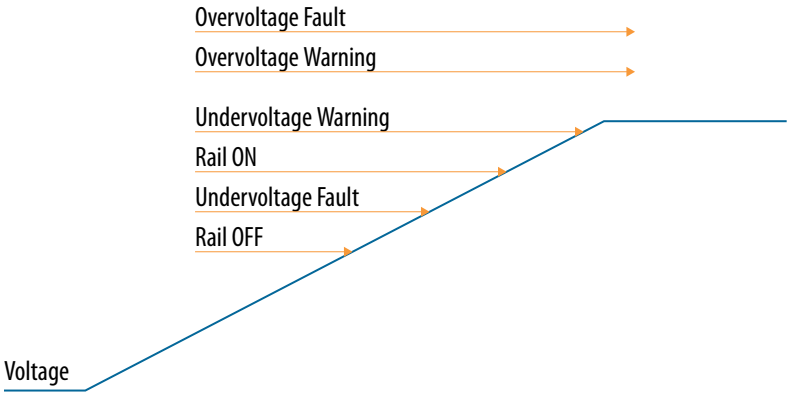
- VIN_ON and VIN_OFF commands dynamically adjust the levels at which the internal power good status is asserted or removed for VIN.
- POWER_GOOD_ON and POWER_GOOD_OFF commands dynamically adjust the levels at which the internal power good status is asserted or removed for VOUT.

The following thresholds provide you with a comprehensive monitoring approach to safely track all input and output voltages and allow you to automatically or manually sequence a power down of the rails in case of an error:

- Undervoltage warning
- Undervoltage fault
- Overvoltage warning
- Overvoltage fault

Figure 10. Voltage Thresholds

In this figure, as the rail's voltage ramps up, the voltage can pass through one of the six possible voltage thresholds.



After the system enables the voltage rail and its level rises, the rail transitions through the undervoltage fault region and into the power good region. While power good is not asserted, the design masks all voltage faults for a given rail so that this portion of the ramp up cycle is not marked as a fault.

After the system reaches the power good level, the rail is still in a state that causes undervoltage warning reports. This behavior is normal and expected. The PMBus may report undervoltage warnings for some of the rails depending on ADC sample rates and the rise time of the rail.

Once the rail reaches its nominal voltage, send the CLEAR_FAULTS command to clear out any latched warnings in the VOUT status registers. You can safely ignore these latched warnings. At this point, the system should be in a normal operation state.

If the rail drifts outside the typical operating range for longer than the duration set in the **ADC Samples to Check** parameter, the design reports overvoltage or undervoltage warnings. The warning causes assertion of the SMB_ALERTN pin. If no other devices are asserting SMB_ALERTN at this time, the page associated with the warning also asserts STATUS_OTHER bit `0: First to Assert SMBALERT#`. You can use this status to indicate which rail was the first to experience an error. If the rail exceeds the levels for an overvoltage or undervoltage fault for longer than the duration specified in the **ADC Samples to Check** parameter, the system behaves according to the programmed response.

In the Sequencer Voltage Monitor component, there are independent checkboxes for each rail. These independent settings allow you to specify a controlled automatic power down sequence in case of overvoltage or undervoltage faults. You can adjust these responses dynamically with the PMBus commands VIN_OV_FAULT_RESP, VIN_UV_FAULT_RESP, VOUT_OV_FAULT_RESP, and VOUT_UV_FAULT_RESP.

The sequencer supports four different behaviors for a fault:

- Ignore that fault and continue operation
- Sequence an immediate power down
- Retry for a selectable number of times from one to six attempts
- Retry indefinitely

The Power Sequencer component does not retry power sequencing until all power good signals for the VOUT rails are deasserted. To specify the duration between retry attempts, set the **Delay Time Between Restarts** parameter in the Power Sequencer component parameter editor. The timer starts after the power good signals deassert.

If a rail uses an external power good signal—typically, a POK output from a power supply—and the ADC VIN does not monitor the rail, the design passes the external power good signal directly to the sequencer. In this case, you cannot perform any PMBus-accessible monitoring or adjustments for that rail.

Related Information

Power Sequencer (Sequencer_Core) on page 17

2.3.4.1. Sequencer Voltage Monitor Parameter Settings

There are two groups of options: **Parameters** and **Voltage Monitor Thresholds**, with a calculated **Derived Thresholds** section for each voltage rail.

Table 3. Sequencer Voltage Monitor Parameters - Parameters

Parameter	Description
Output Voltage Rails	Specify the number of output voltage rails to sequence. The number must match the value you specify in the other components of the system. Otherwise, the interface bus widths between components will not match.
Power Good Inputs	Specify the number of power good inputs to monitor.

continued...

Parameter	Description
	The number must match the value you specify in the other components of the system. Otherwise, the interface bus widths between components will not match.
ADC Reference Voltage	Specify the reference voltage value. The component uses this value to calculate the various power good, undervoltage, and overvoltage thresholds to compare to the ADC output.
Functionality Level	Select the functionality level of the Sequencer Voltage Monitor component: • **No PMBus**—the design uses the hardcoded levels specified in the parameter editor. Dynamic adjustment or monitoring via the PMBus is not available. • **Hard-Coded Thresholds**—you can use the PMBus Slave to Avalon-MM Master Bridge to monitor fault and status but you cannot dynamically adjust the voltage level thresholds. • **Full-featured**—the design contains the full PMBus command set for dynamic adjustment, status, and error monitoring. For more information, refer to the related information. This option allows you to optimize the design and reduce its overall logic footprint. For the logic utilization estimates, refer to the related information.
ADC Samples to Check	Specify the number of contiguous ADC samples to check per input before declaring a warning or a fault such as overvoltage, undervoltage, and power good on or off.
Retry Attempts	Specify the number of attempts the Power Sequencer component should make to sequence power up—following a complete, controlled sequence down—after detecting an error condition.
Timeout Interval on Retry	Select the delay interval the Power Sequencer component waits before retrying the power up sequence: • **No Delay**—retries the power up sequence immediately after all rails have sequenced down • **Use Delay Specified by the Sequencer**—delays the retry attempts according to the **Delay Time Between Restarts** setting in the Power Sequencer component

Table 4. Sequencer Voltage Monitor Parameters - Voltage Monitor Thresholds

Specify the VIN and VOUT thresholds in their respective tabs:

- The **Derived Thresholds** section displays the calculated voltage thresholds.
- Ensure that each calculated threshold does not exceed the **ADC Reference Voltage** setting in the **Parameters** section.
- The default thresholds are based on the typical expected voltage for that rail, after any voltage dividers.
- The component converts all voltage settings in this table to the PMBus DIRECT format. For information about translating to and from the DIRECT format, refer to the related information.

Parameter	Description	Default Threshold
VIN/VOUT*N* Typical Voltage, Monitored	Specify the typical voltage level that you expect to observe at the ADC analog input. In your expectation, include the effect of all voltage divider circuitries on the board.	—
VIN/VOUT*N* Overvoltage Fault	Specify the percentage of the **VIN/VOUT*N* Typical Voltage, Monitored** at which to declare an overvoltage fault.	107%
VIN/VOUT*N* Overvoltage Warning	Specify the percentage of the **VIN/VOUT*N* Typical Voltage, Monitored** at which to declare an overvoltage warning.	105%
VIN/VOUT*N* Undervoltage Warning	Specify the percentage of the **VIN/VOUT*N* Typical Voltage, Monitored** at which to declare an undervoltage warning.	97%
VIN ON Level (VIN tab only)	Specify the percentage of the **VIN Typical Voltage, Monitored** at which to consider the monitored input rail as good and start the power up sequencing of the output rails.	97%

continued...

Parameter	Description	Default Threshold
VOUT Power Good Assertion Level (VOUT*N* tabs only)	Specify the percentage of the **VOUT*N* Typical Voltage, Monitored** at which to consider the output voltage of the rail as good and start the power up sequencing of the next output rail.	97%
VIN/VOUT*N* Undervoltage Fault	Specify the percentage of the **VIN/VOUT*N* Typical Voltage, Monitored** at which to declare an undervoltage fault.	93%
VIN OFF Level (VIN tab only)	Specify the percentage of the **VIN Typical Voltage, Monitored** at which to consider the monitored input rail as bad and start the power down sequencing of all rails.	90%
VOUT*N* Power Good Deassertion Level (VOUT*N* tabs only)	Specify the percentage of the **VOUT*N* Typical Voltage, Monitored** at which to consider the output voltage of the rail as bad and start the power down sequencing of all rails.	90%
Overvoltage Faults cause controlled sequence down	Turn this on to sequence power down for all rails, based on the fault response, if the component detects an overvoltage fault in the VIN or VOUT*N* rail.	—
Undervoltage Faults cause controlled sequence down	Turn this on to sequence power down for all rails, based on the fault response, if the component detects an undervoltage fault in the VIN or VOUT*N* rail.	—

Related Information

- Resource Utilization of the Multi-Rail Power Sequencer and Monitor Reference Design on page 38
  Lists approximate resources estimates to implement different configurations of the reference design.
- PMBus Commands Implementation on page 33
- Output Voltage Data Formats and Related Parameters on page 21
  Provides information about translating to and from the PMBus DIRECT format.

2.3.5. PMBus Slave to Avalon-MM Master Bridge (PMBus_Slave)

The PMBus Slave to Avalon-MM Master Bridge component is optional. You can remove the component from the design if you do not need it.

If you enable the PMBus interface, each power rail that is monitored by one of the ADC VIN pins are on its own page:

- The page numbers of the VOUT rails are sequential and start from zero. For example, in a six-rail sequencer with rails VOUT0 through VOUT5, page zero shows rail zero (VOUT0), page one shows rail one (VOUT1), and so forth.
- The registers associated with VIN are visible across all pages. If you clear an input fault on one page, the design clears the fault on all pages.

The PMBus interface does not support a page setting of 0xFF (broadcasting commands to all pages). The interface only allows for pages that correspond to a monitored VIN rail (page zero), or monitored VOUT rails.

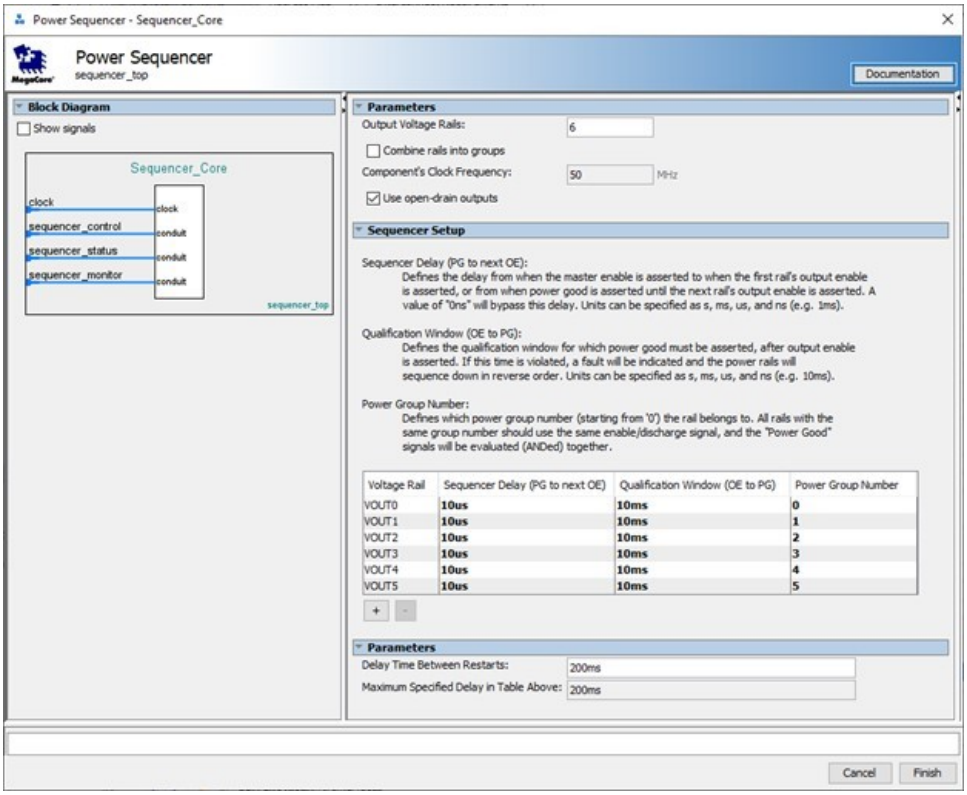
- If an ADC pin does not monitor a rail—the rail uses an external power good signal such as the POK signal from the regulator—the page for the rail is invalid. Any attempt to change to that page causes a PMBus error `bit 6 (Invalid or unsupported data received)` report to the STATUS_CML register.
- If your system monitors only the VIN rail while all VOUT rails use external power good indicators, VIN exists on page zero. All VOUT-related commands result in a PMBus error `bit 7 (Invalid or unsupported command received)` report to the STATUS_CML register.
- If your system does not monitor the VIN rail, all VIN-related commands result in a PMBus error `bit 7 (Invalid or unsupported command received)` report the STATUS_CML register.

2.3.6. Power Sequencer (Sequencer_Core)

The Power Sequencer component implements the decision-making state machine and delay timer for sequencing the output rails. This component is a standalone block that will provide the most minimal design implementation if you do not need voltage rail monitoring and PMBus control.

The Power Sequencer component determines when to sequence the power regulators up or down based on the power good input levels. It provides the enable and discharge output signals to the power regulators.

Figure 11. Power Sequencer Parameter Editor



If you want to enable or disable multiple rails simultaneously, you can combine the rails into a single group. The design conjoins (logically ANDs) the power good signals of groups with the same **Power Group Number** setting. These groups also share the same enable output and discharge output. Power rails within the same group must have the same values for the **Sequencer Delay** and **Qualification Window** parameters. Otherwise, the Platform Designer displays a warning message.

If you disable power groups, the **Power Group Number** column in the table is read-only and each VOUT rail has its own unique power group number.

For example, using the settings in the preceding figure, the sequencer behaves in the following manner:

- The rails for VOUT0, VOUT2, and VOUT3 share the same enable signal and the rails ramp up together.
- After the power good inputs for all those rails go high—occuring within the 10 ms qualification window—the enable signal for VOUT1 asserts following a 10 µs delay.
- After the power good input for VOUT1 goes high—occuring within the 10 ms qualification window—the enable signals for VOUT4 and VOUT5 assert following a 10 µs delay.
- After the power good inputs for both VOUT4 and VOUT5 go high—within the 10 ms qualification window—the sequencer completes ramping up all six rails in the three power groups.

Note: The delay between a power good input going high and the next enable being asserted does not depend only on the value of the **Sequencer Delay** parameter. The total delay also includes the additional delay caused by debouncing power good inputs and the delay caused by the number of ADC samples the Sequencer Voltage Monitor component checks.

While the Multi-Rail Power Sequencer and Monitor design is in a normal operational state and all of the rails are enabled, if a power good signal from one of the VOUT rails deasserts, the sequencer immediately asserts the nFAULT signal and gracefully enters a power down sequence.

If you enable retries in the Sequencer Voltage Monitor component, the Power Sequencer component performs the following steps:

1. Waits for all power good signals to deassert
2. Waits for the duration of the specified delay time between retries
3. Attempts a power up sequence

When the Power Sequencer component attempts a power up sequence, the nFAULT signal automatically clears. If the failure persists and you do not set **Retry Attempts** parameter in Sequencer Voltage Monitor component to **Infinite**, the nFAULT signal continues to toggle until it reaches the maximum number of retries. If the failure still persists after that, the nFAULT signal remains asserted, unless you reset the sequencer in one of these ways:

- Toggle the ENABLE signal
- Use a PMBus command to increase the number of retries

Related Information

Sequencer Voltage Monitor (Sequencer_VMonitor) on page 11

2.3.6.1. Power Sequencer Parameter Settings

There are three groups of options: **Parameters**, **Sequencer Setup**, and **Parameters** (delay settings).

Table 5. Power Sequencer Parameters

Parameter	Description
Output Voltage Rails	Specify the number of output voltage rails to sequence. The number must match the value you specify in the other components of the system. Otherwise, the interface bus widths between components will not match.
Combine rails into groups	Turn on to group power rails with common enable signals and logically AND the individual power good status signals.
Number of Power Groups	Specify the number of power groups for the sequencer to implement. The sequencer creates one set of enable/discharge outputs per group.

continued...

Parameter	Description
	Note: This option is available if you turn on **Combine rails into groups**.
Component's Clock Frequency	Read-only parameter that specifies the component's input clock frequency. • The number depends on which clock you connect to the component in the Platform Designer. • Ensure that this frequency is correct. Otherwise, the system cannot derive the correct delay values.
Use Open-drain Outputs	Controls whether open-drain or push-pull drivers are used for nFAULT, VRAIL_ENA, and VRAIL_DCHG. The default is to use open-drain outputs which drive to the VCCIO rail when active and tri-state (with external pull-down) when inactive. Using open-drain eliminates the potential of glitching these outputs during configuration and before they are actively driven by the CPLD. For standard push-pull outputs or to utilize a different output type, uncheck this box.

Table 6. Power Sequencer Parameters - Sequencer Setup

You can specify the time units in s, ms, us (for µs), and ns. For example, specify 10us for a 10 µs delay.

Parameter	Description
Sequencer Delay (PG to next OE)	Specify the delay: • From the moment the master enable signal asserts before the output enable signal asserts; or • From the moment power good asserts until the next rail's or group's output enable signal asserts. Specify 0ns to bypass the delay.
Qualification Window (OE to PG)	Specify the qualification window for which power good must assert after output enable is asserted. If the qualification time violation occurs, the component indicates a fault and sequences the power rails down (in reverse order of the power up).
Power Group Number	Specify which power group (starting from 0) to assign the rail. • For all rails with the same group number, use the same enable/discharge signal. • The design evaluates the power good signals of the rails in the same group together (ANDed).

Table 7. Power Sequencer Parameters - Parameters (Delay Settings)

You can specify the time units in s, ms, us (for µs), and ns. For example, specify 10us for a 10 µs delay.

Parameter	Description
Delay Time Between Restarts	Specify the delay interval between restart attempts for the sequencer. All power good signals must be low before the delay counter is started.
Maximum Specified Delay in Table Above	Read-only value that displays the derived maximum delay from all parameters. The component passes the value to the design to size the counters accurately .

2.3.7. Other Design Components

The Multi-Rail Power Sequencer and Monitor reference design includes other custom blocks that serve supporting roles and do not need parameterization.

2.3.7.1. POR Pulse (POR_Pulse)

Creates a reset pulse immediately after configuration for 16 clock cycles. This can be set to any value from 2 to 64 clock cycles.

2.3.7.2. Reset to Conduit Adapter (Reset2Conduit)

Converts the reset output "role" from a "Reset Output" to a "Conduit", enabling it to drive the areset_conduit of the MAX 10 PLL.

2.3.7.3. pll_lock_splitter (PLL_LockSplit)

The pll_lock_splitter component receives the `pll_locked` signal from the phaselocked loop (PLL), and fans the signal out to the reset sequencer and the `adc_pll_locked` input of the Modular ADC Core IP. The Multi-Rail Power Sequencer and Monitor design holds all blocks within it in reset until after the PLL locks and becomes stable.

2.3.7.4. Avalon-MM Sequencer (AVMM_Initializer)

The Avalon-MM Sequencer component generates the required control-plane commands to initialize the ADC for usage. These commands are required if you want to use the ADC to monitor voltage rail levels. You do not need these commands if you use a power-sequencer only design that uses POK signals from the power regulators.

Note: The Avalon-MM Sequencer component expects the ADC interface to reside at base address `0x00`. If the base address is not `0x00`, edit the `avmm_sequencer_pkg.sv` file to write the initialization command to the proper address offset.

2.4. Output Voltage Data Formats and Related Parameters

The reference design uses the DIRECT format—defined in the PMBus Specification—to store all data for the input or output voltages for current status, warning levels, or error levels.

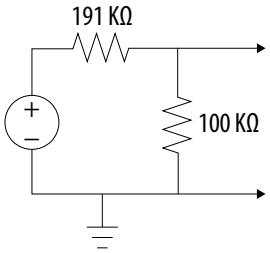
The power coefficients are:

- Determined by you
- Specific to each voltage rail for every page
- Based on the voltage scaling resistors in the design

The ADC in dual supply MAX 10 devices can measure from 0 V to 2.5 V with 12-bits resolution. In single supply MAX 10 devices, the ADC can measure up to 3.0 V or 3.3 V depending on your power supply voltage. To provide a sufficiently large scale that retains enough resolution for accurate measurements, select appropriate values for the voltage divider.

For example, on a 3.3 V input, if you set your `OV_Fail` at 115%, you would need to be able to measure a range from 0 V to 3.8 V. This example assumes that you use a 2.5 V external reference voltage (ADC_VREF) and you apply a voltage divider, as shown in the following figure, to the monitored voltage rail.

Figure 12. Voltage Divider Example on a 3.3 V Rail



In the Platform Designer, the parameter editors automatically calculates the values for you. You just need to ensure that the output of the voltage divider does not exceed ADC_VREF for an overvoltage condition. The calculations show you how the settings and reported values relate to the PMBus specification.

Example 1. Calculations Related to PMBus Specifications

Given the DIRECT format definition of $X = \frac{1}{m\left(Y \times 10^{-R} - b\right)}$:

Where:

- *X* is the calculated "real world" value in the appropriate units such as A, V, and °C
- *m* is the slope coefficient—a two-byte, two's complement integer
- *Y* is a two-byte, two's complement integer received from the PMBus device
- *b* is the offset—a two-byte, two's complement integer
- *R* is the exponent—a one-byte, two's complement integer

You can determine the coefficients knowing that:

$$X = \frac{Y}{4096} \times 2.5\text{V} \times \frac{(191\text{K}\Omega + 100\text{K}\Omega)}{191\text{K}\Omega}$$

$$X = Y \times 9.29907 \times 10^{-4}$$

$$X = \frac{1}{1075.375945} \times Y$$

Using the 16-bits resolution available for *m*, you get these constants:

$$m = 10753$$

$$b = 0$$

$$R = -1$$

Therefore, if you read back a value of 3549 after sending the READ_VOUT command, you can apply the constants to the formula and solve:

$$X = \frac{1}{10753}\left(3549 \times 10^{1} - 0\right)$$

$$X = 3.300$$

3. Implementation and Simulation of the Multi-Rail Power Sequencer and Monitor Reference Design

The Multi-Rail Power Sequencer and Monitor archive file (`Power_Sequencer.zip`) contains a design example project, reference design components, and a simulation testbench system.

The design example is a full-featured configuration:

- Configured to control six ADC-monitored voltage rails
- Includes PMBus support
- Includes an additional seven unused power good inputs, one for each VOUT rail and VIN
- Uses the ADC voltage monitors to control the sequencer
- Customizable to fit your system design requirements

Related Information

- Multi-Rail Power Sequencer and Monitor
  Provides the Multi-Rail Power Sequencer and Monitor archive file for download.
- Structure of the Reference Design Archive on page 3

3.1. Customizing and Generating the Design Example

1. From the Quartus Prime main menu, click **File ➤ Open Project**.
2. Select the <*installation directory*>\quartus\Sequencer.qpf file and click **Open**.

   Note: Ignore the warning message about the missing `sequencer_qsys.qip` file. The Platform Designer will generate this file when you generate the system later.
3. From the Quartus Prime main menu, click **File ➤ Open**.
4. Select the <*installation directory*>\source\sequencer_qsys.qsys file and click **Open**.

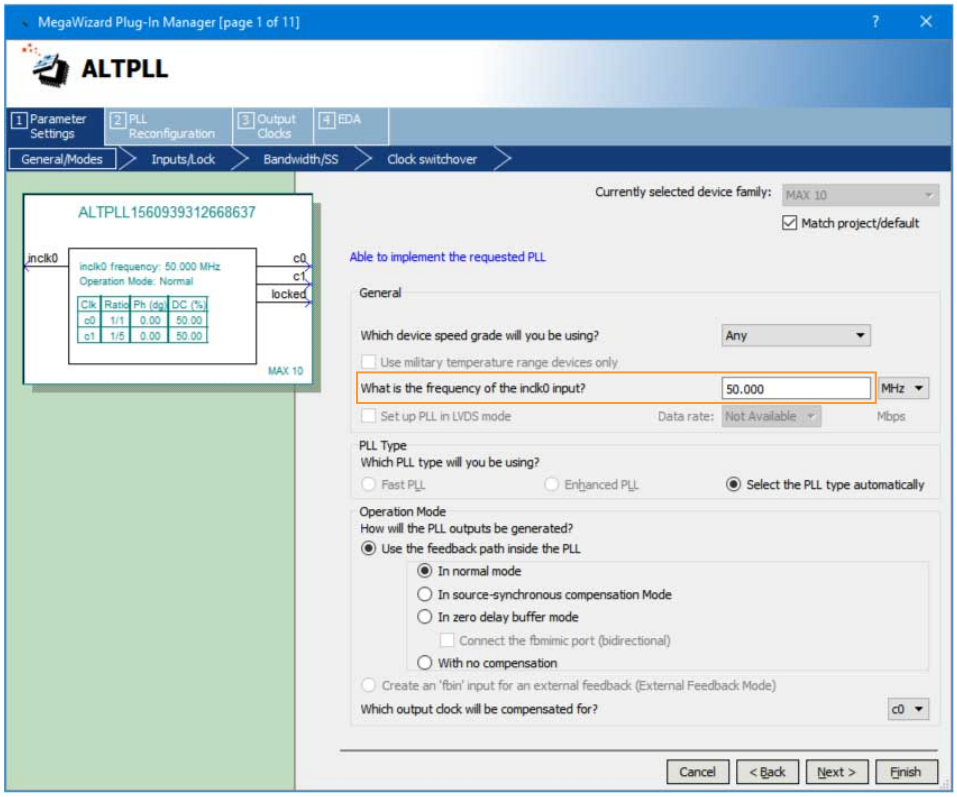
   Note: Do not select the `sequencer_qsys_tb.qsys` file, which is the simulation testbench system.

   The **Platform Designer** opens with the reference design system.
5. Customize the parameters of the components according to your system requirements.

   Many of the components have built-in error checks to prevent you from generating invalid code. Check the **Messages** pane for interface mismatches between components or potentially incorrect settings.

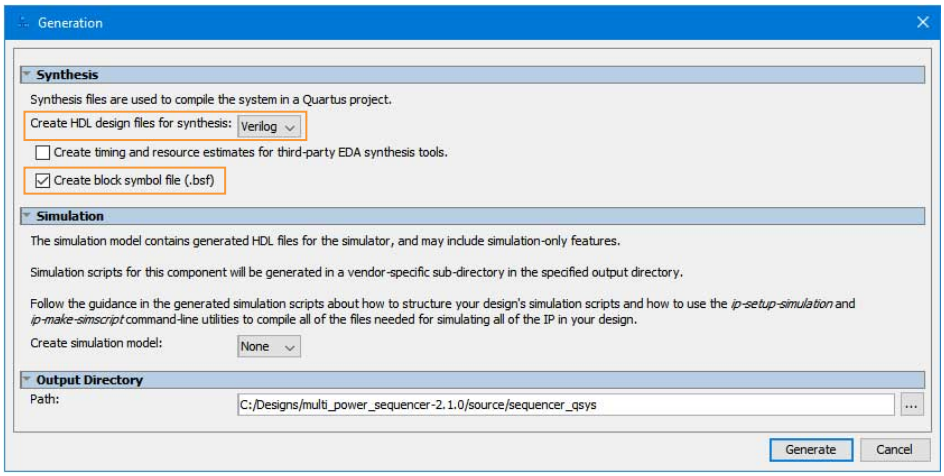
6. The example project defines the reference clock frequency as 50 MHz. If this frequency changes, edit the ALTPLL IP (PLL_Main) to specify the new reference clock frequency in the **What is the frequency of the inclk0 input?** box.

Figure 13. PLL_Main Parameter Editor in the Platform Designer



7. After you have completed all customizations, click **Generate HDL** in the **Platform Designer** window.
8. In the **Generation** window:
   a. Select **Verilog** or **VHDL** in the **Create HDL design files for synthesis** box.
   b. Turn on **Create block symbol file (.bsf)**.
   c. Click **Generate**.

Figure 14. Platform Designer Generation Window



9. In the **Generate Completed** window, click **Close**.

If you make any changes to the design after generating the sequencer code, you must update the top-level schematic to match the customizations.

Note: The Platform Designer regenerates the following files automatically with the parameter settings you specify. Ensure that these files in the source directory are writable. Do not place them under version control. If these files are not writable, the generated design cannot parameterize them accurately:

- `sequencer_params_pkg.sv`
- `sequencer_vmon_pkg.sv`
- `sequencer_vmondecode_pkg.sv`

Related Information

- Assigning Pins and Compiling the Design Example on page 27
- Updating the Schematic After Customizing the Design on page 25

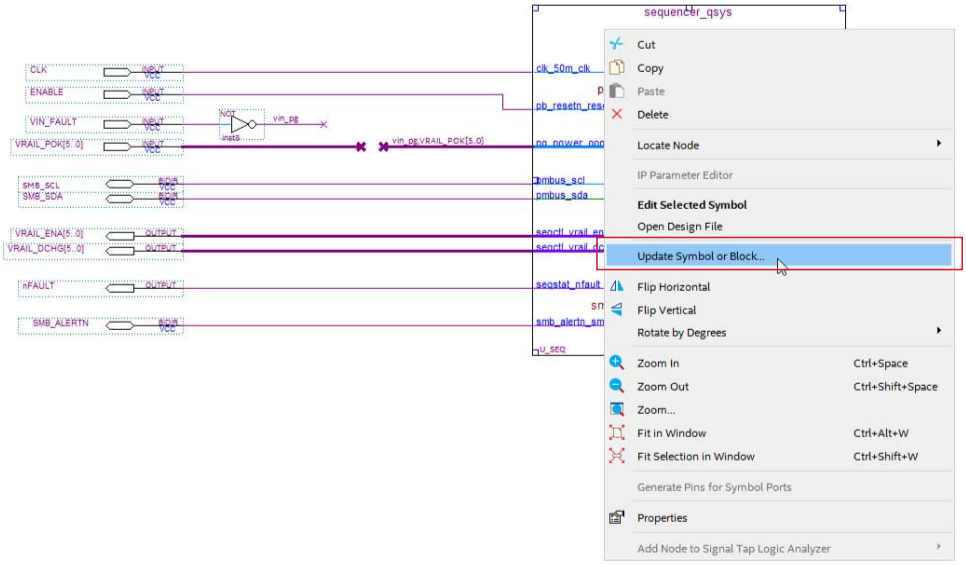
3.2. Updating the Schematic After Customizing the Design

After sequencer code generation, if you make changes that affect the top level design, you must update the top-level schematic accordingly to match the customizations.

For example:

- If you remove the PMBus Slave to Avalon-MM Master Bridge component, you must remove the SMB_SCL and SMB_SDA signals too.
- If you increase or decrease the number of rails, you must change the widths of the VRAIL_POK, VRAIL_ENA, and VRAIL_DCHG signals accordingly.

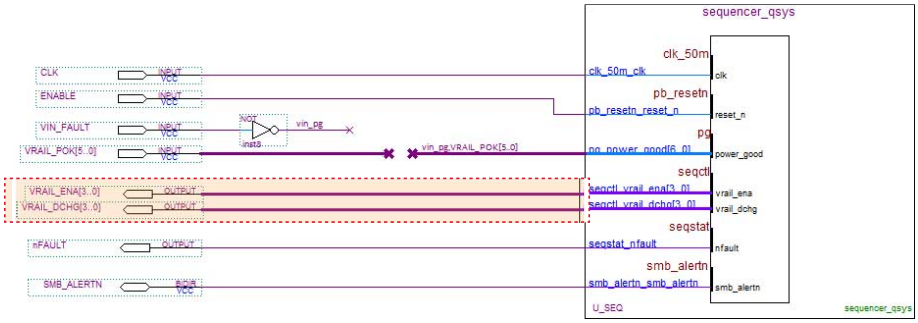
Figure 15. Updating Symbol in Top-Level Schematic of the Sequencer Component



1. In the **Project Navigator**, double click the **sequencer** block diagram file to open it in the **Block Editor** window.
2. In the sequencer schematic, right-click on the **sequencer_qsys** block and select **Update Symbol or Block**.
   The **sequencer_qsys** block updates. For example, the update removes the PMBus ports and decreases the bus widths of the `vrail_ena` and `vrail_dchg` ports from six bits to four bits.
3. Edit the connections from the I/O signals to the **sequencer_qsys** block.

   For example, remove the SMB_SCL and SMB_SDA signals that are not used anymore. Then, edit the bus widths of the VRAIL_ENA and VRAIL_DCHG signals and reconnect them back to the `vrail_ena` and `vrail_dchg` ports.

Figure 16. Correcting the I/O Connections in the Top Level Schematic



4. Save the sequencer schematic and close the **Block Editor** window.

Related Information

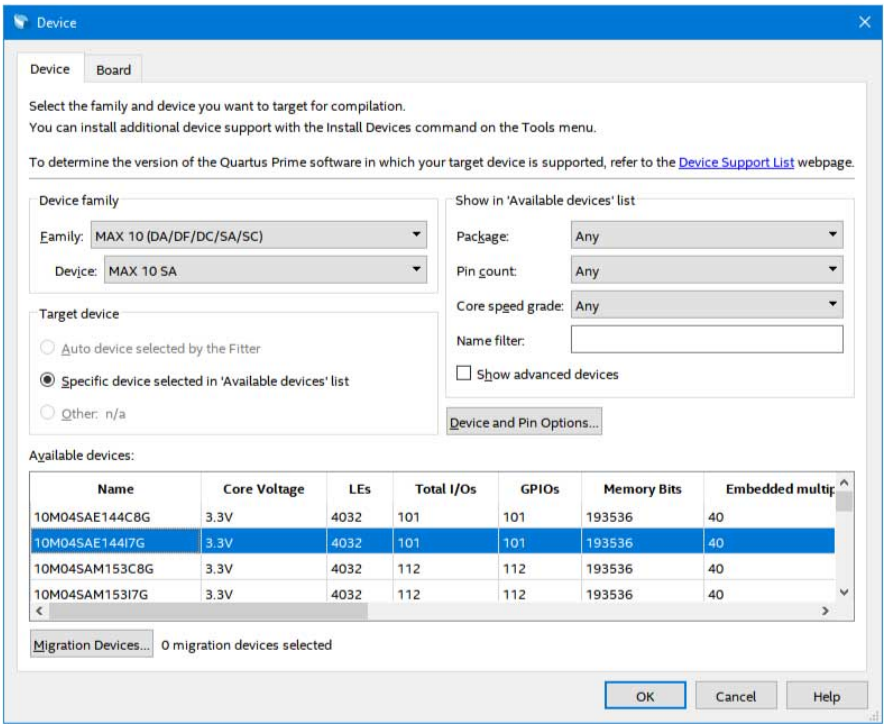
Customizing and Generating the Design Example on page 23

3.3. Assigning Pins and Compiling the Design Example

After customizing the design and generating the HDL files in the Platform Designer, you can prepare and compile the design example.

1. In the main Quartus Prime window, with the design example project opened, click **Assignments ➤ Device** from the main menu.

Figure 17. Select the Target Device in Quartus Prime



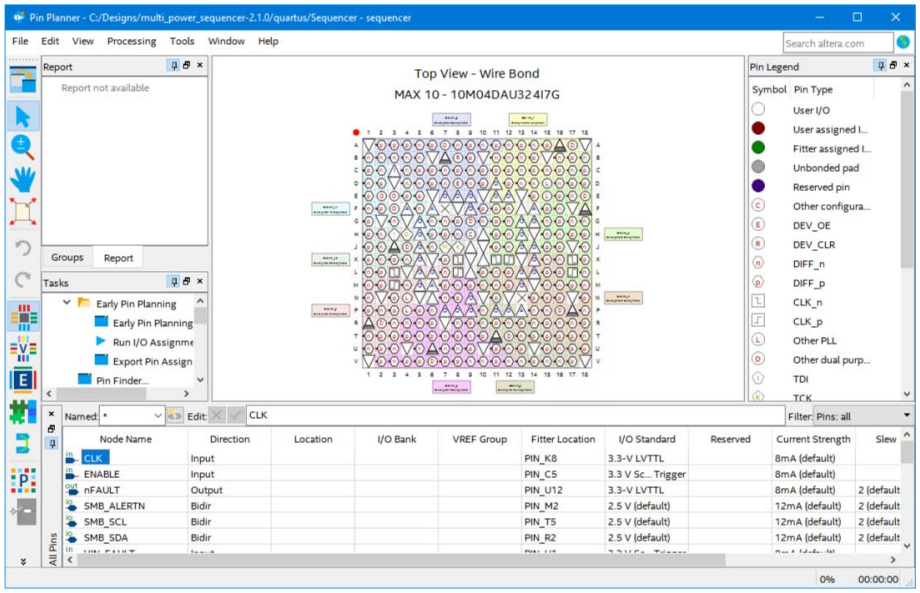
2. In the **Device** window, select the appropriate MAX 10 device for your system and click **OK**.

   If you want the sequencer to perform voltage monitoring, the device you select must have ADC support.

3. Click **Assignments ➤ Pin Planner**.
4. In the **Pin Planner** window, drag pin names from the **All Pins** pane to the pin location on the physical representation of the device in the center of the **Pin Planner** window.

   Alternatively, type the pin number in the **Location** column of the **All Pins** pane.

Figure 18. Assigning Pins in the Pin Planner Window



5. If you change the frequency of the reference clock to the PLL in Platform Designer, adjust the timing constraint for the reference clock input in the <*installation directory*>\quartus\sequencer.sdc file. Search for this line:

```
create_clock -name clk_ref -period 50.0MHz [get_ports {clk}]
```

   For example, if you change the reference clock from 50 MHz to 25 MHz, change the line to:

```
create_clock -name clk_ref -period 25.0MHz [get_ports {clk}]
```

6. In the main Quartus Prime window, click **Processing ➤ Start Compilation**.

   Alternatively, click the **Start Compilation** icon in the main Quartus Prime toolbar.

After the compilation completes, use the <*installation directory*>\quartus\output_files\sequencer.pof to program the targeted MAX 10 device.

Related Information

Customizing and Generating the Design Example on page 23

3.3.1. Pin Description

Table 8. Power Sequencer Signals

Name	Direction	Type	Description
CLOCK	Input	3.3 V LVTTL	Free-running global clock that the design uses as a timing reference for calculated delays.
ENABLE	Input	3.3 V Schmitt Trigger	Master enable signal: • When asserted—allows power up sequencing • When deasserted—sequences all power regulators down

continued...

Name	Direction	Type	Description
VIN_FAULT	Input	3.3 V Schmitt Trigger	Indicates an external fault has occurred. When asserted, the design sequences all power regulators down.
VRAIL_PWRGD[*N*:0]	Input	3.3 V Schmitt Trigger with WEAK_PULL_UP	Power good indication from the power supply of each rail.
VRAIL_ENA[*N*:0]	Output	Configurable: Open-Drain / 3.3 V LVTTL	Enable signal for the power supply of each rail. When configured as open-drain, it requires an external pull-down resistor.
VRAIL_DCHG[*N*:0]	Output	Configurable: Open-Drain / 3.3 V LVTTL	Discharge signal for the discharge Field-Effect Transistor (FET) on each rail. When configured as open-drain, it requires an external pull-down resistor.
nFAULT	Output	Configurable: Open-Drain / 3.3 V LVTTL	Indicates that the sequencer has detected a fault and is sequencing all power rails down. When configured as open-drain, it requires an external pull-down resistor.
VRAIL_MON[*N*:0]	Input	3.3 V LVTTL	Externally scaled voltage monitor for VOUT power supplies. This input is not present at the top level but the ADC directly connects it.
VIN_MON	Input	3.3 V LVTTL	Externally scaled voltage monitor for VIN power supplies. This input is not present at the top level but the ADC directly connects it.
SMB_SCL	Input	3.3 V Open-Drain	PMBus serial clock line generated by the PMBus master. Requires an external pull-up resistor.
SMB_SDA	Bidir	3.3 V Open-Drain	PMBus serial data line. In transmit mode, this pin is open drain. The design acquires data on the positive edge, and delivers data on the negative edge of the PMBus serial clock line. Requires an external pull-up resistor.
SMB_ALERTN	Output	3.3 V Open-Drain	PMBus Alarm Indication. Requires an external pull-up resistor.

3.4. Testbench Simulation to Understand Design Behavior

The Multi-Rail Power Sequencer and Monitor reference design includes a simple testbench that you can use as a springboard to understand design behavior. The testbench implements a six-rail voltage-monitored sequencer design with full functionality.

Important Caveats for the Simulation

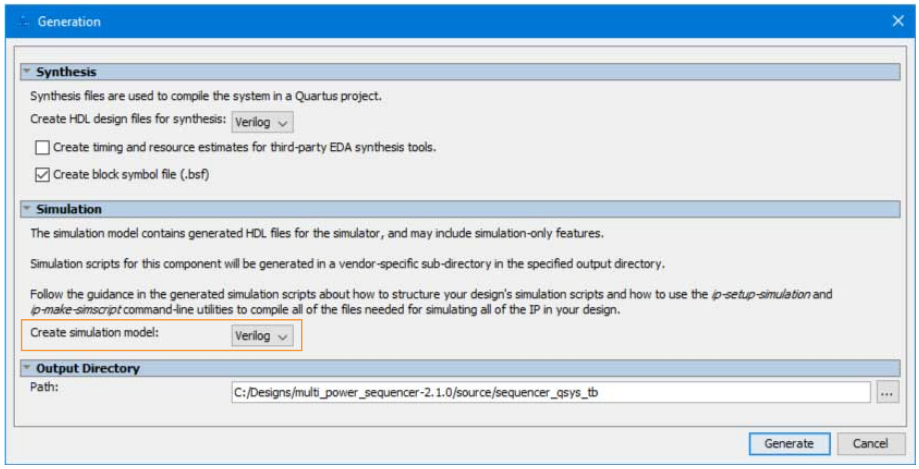
- The analog inputs for the ADC come from voltage levels listed in text files. The simulation continuously loops through these text files. Therefore, the VRAIL_EN signal has no effect on the simulated analog input.
- The analog input does not rise or fall when VRAIL_EN asserts and deasserts. If you modify the simulation behavior, create simulation voltage files—adcsim_ch#.txt files—that match the intent of the simulation test.
- If you configure the design to use external POWER_GOOD signals for simulation, you must incorporate a design block—as simple as a loopback—that adjusts the POWER_GOOD status based on the VRAIL_EN level.

3.4.1. Generating the Testbench Simulation

The testbench system instantiates the sequencer_qsys.qsys subsystem and simple bus functional models (BFMs) for clock and reset.

1. From the Quartus Prime menu, click **File ➤ Open**
2. Select the <*installation directory*>\source\sequencer_qsys_tb.qsys file and click **Open**.
3. Click **Generate HDL** in the **Platform Designer** window.
4. In the **Generation** window:
   a. Select **Verilog** or **VHDL** in the **Create simulation model** box.
   b. Click **Generate**.

Figure 19. Platform Designer Generation Window



5. In the **Generate Completed** window, click **Close**.

The Platform Designer generates the simulation files in the <*installation directory*>\source\sequencer_qsys_tb\simulation directory.

Related Information

Running the Testbench Simulation on page 31

3.4.2. Running the Testbench Simulation

After generating the testbench simulation files in the Platform Designer, you can run the simulation in ModelSim® or Questa* Advanced Simulator.

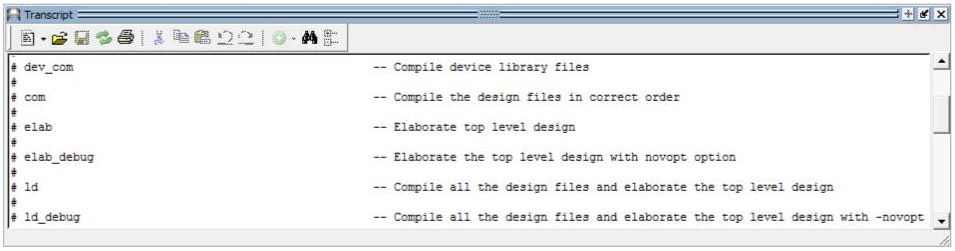
The following procedure describes the steps to run the simulation using the ModelSim - Intel FPGA Starter Edition software.

1. From the ModelSim - Intel FPGA Starter Edition main menu, click **File ➤ Change Directory**.
2. In the **Browse For Folder** window, select the <*installation directory*>`\source\sequencer_qsys_tb\simulation\mentor` directory and click **OK**.
3. At the prompt in the **Transcript** window, enter the following command:

   ```
   source msim_setup.tcl
   ```

   The **Transcript** window lists the command aliases.

Figure 20. Command Aliases in the Transcript Window



4. At the prompt in the **Transcript** window, enter the following command to compile the device and design libraries, and load the simulation:

   ```
   ld_debug
   ```

5. After the simulation loads, enter the following command at the **Transcript** prompt to display the the key signals within the design in the **Wave** window:

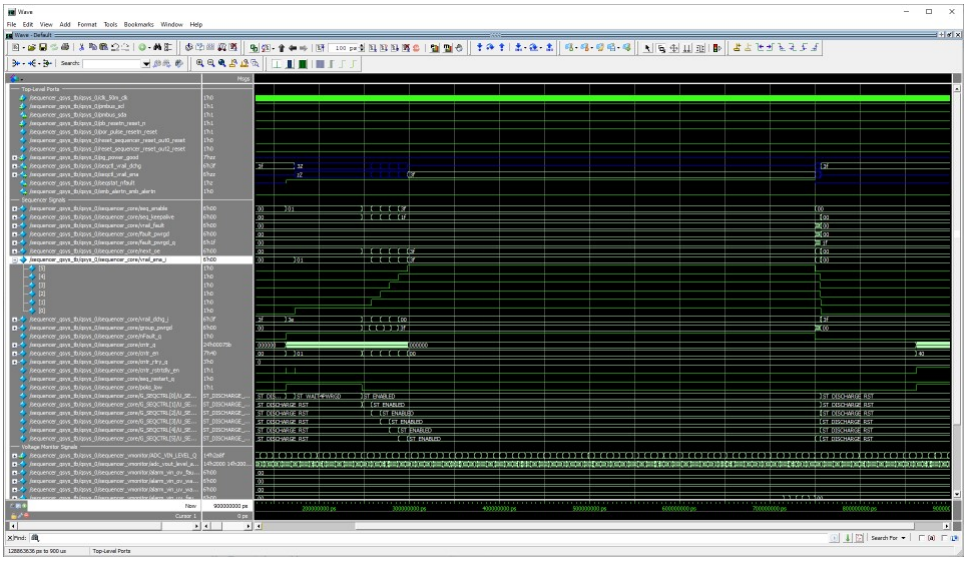
   ```
   do wave.do
   ```

6. At the **Transcript** prompt, enter the following command provide the appropriate stimulus and run the simulation:

   ```
   do force.do
   ```

The simulation runs and the waveforms display in the **Wave** window.

Figure 21. Multi-Rail Power Sequencer and Monitor Testbench Simulation Waveforms



Related Information

Generating the Testbench Simulation on page 30

4. Functionality Level and Resource Utilization Estimates

The Multi-Rail Power Sequencer and Monitor reference design allows you to customize the functionality levels. The various functionality levels affect the PMBus command implementation and use different numbers of resources.

4.1. PMBus Commands Implementation

The design implements different register control and status commands, depending on the functionality level you select in the Sequencer Voltage Monitor component. The commands can address one or two bytes of data. The design stores all data for the output voltage and related parameters in the DIRECT format.

Table 9. Power Sequencer PMBus Commands Description

This table lists the supported PMBus commands. The design implements commands marked with * only if you select the **Full-featured** option for the **Functionality Level** parameter of the Sequencer Voltage Monitor component.

Command Code (Address)	Bit	Name		SMBus Transaction	Description
0x00	[7:0]	PAGE		Read Byte Write Byte	Selects the page of commands for the voltage rail being accessed. Range of valid page values is 0x00 to 0x8F (143) and relates to each VOUT rail.
0x03		CLEAR_FAULTS		Send Byte	Clears all warnings and faults in the write-to-clear status bits.
0x35	[15:0]	VIN_ON(1)	*	Read Word Write Word	Sets the value of the input voltage at which it is sufficiently high for the design to begin sequencing the output rails on.
0x36	[15:0]	VIN_OFF(1)	*	Read Word Write Word	Sets the value of the input voltage at which it has dropped low enough that the design must sequence the output rails off.
0x40	[15:0]	VOUT_OV_FAULT_LIMIT(1)	*	Read Word Write Word	Sets the value of the output voltage that causes an output overvoltage fault.
0x41	—	VOUT_OV_FAULT_RESP		Read Byte Write Byte	Instructs the device on the action to take when there is an output overvoltage fault.

continued...

(1) The levels are specified in the PMBus DIRECT format. For information about translating to and from the DIRECT format, refer to the related information.

Command Code (Address)	Bit	Name		SMBus Transaction	Description
	[7:6]	Response		—	• 00—Continue operation without interruption • 01—Invalid • 10—Sequence a power down in reverse order and respond according to the retry setting in bits [5:3] • 11—Invalid
	[5:3]	Retry Setting(2)		—	Indicates the number of times the device attempts to restart from a fault. • 0—Do not attempt a restart and remain disabled until the fault clears and ENABLE input toggles • 1 to 6—Retry for the specified number of attempts, then stop and remain disabled until the fault clears and the ENABLE input toggles • 7—Retry infinitely
	[2:0]	Delay Time(3)		—	Specifies the delay interval between attempts to restart. • 0—No delay • 1 to 7—Use the **Delay Time Between Restarts** parameter setting in the Power Sequencer component
0x42	[15:0]	VOUT_OV_WARN_LIMIT(1)	*	Read Word Write Word	Sets the value of the output voltage that causes an output overvoltage warning.
0x43	[15:0]	VOUT_UV_WARN_LIMIT(1)	*	Read Word Write Word	Sets the value of the output voltage that causes an output undervoltage warning.
0x44	[15:0]	VOUT_UV_FAULT_LIMIT(1)	*	Read Word Write Word	Sets the value of the output voltage that causes an output undervoltage fault.
0x45	—	VOUT_UV_FAULT_RESP		Read Byte Write Byte	Instructs the device on the action to take when there is an output undervoltage fault.
	[7:6]	Response		—	• 00—Continue operation without interruption • 01—Invalid • 10—Sequence a power down in reverse order and respond according to the retry setting in bits [5:3] • 11—Invalid

continued...

(2) The Retry Setting value is common across all pages, and warnings or faults. The controller attempts to recover after a fault until it reaches the global number of times to retry. The retry counter resets whenever the ENABLE input toggles low. The Response setting for this same command is unique to each warning or fault.

(3) The Delay Time setting is common across all pages, and warnings or faults. After all power good signals deasserts, the controller waits between retry attempts for the specified time before power sequencing the rails back up. The Response setting for this same command is unique to each warning or fault.

Command Code (Address)	Bit	Name		SMBus Transaction	Description
	[5:3]	Retry Setting[2]		—	Indicates the number of times the device attempts to restart from a fault. • 0—Do not attempt a restart and remain disabled until the fault clears and ENABLE input toggles • 1 to 6—Retry for the specified number of attempts, then stop and remain disabled until the fault clears and the ENABLE input toggles • 7—Retry infinitely
	[2:0]	Delay Time[3]		—	Specifies the delay interval between attempts to restart. • 0—No delay • 1 to 7—Use the **Delay Time Between Restarts** parameter setting in the Power Sequencer component
0x55	[15:0]	VIN_OV_FAULT_LIMIT[1]	*	Read Word Write Word	Sets the value of the input voltage that causes an input overvoltage fault.
0x56	—	VIN_OV_FAULT_RESP		Read Byte Write Byte	Instructs the device on the action to take when there is an input overvoltage fault.
	[7:6]	Response		—	• 00—Continue operation without interruption • 01—Invalid • 10—Sequence a power down in reverse order and respond according to the retry setting in bits [5:3] • 11—Invalid
	[5:3]	Retry Setting[2]		—	Indicates the number of times the device attempts to restart from a fault. • 0—Do not attempt a restart and remain disabled until the fault clears and ENABLE input toggles • 1 to 6—Retry for the specified number of attempts, then stop and remain disabled until the fault clears and the ENABLE input toggles • 7—Retry infinitely
	[2:0]	Delay Time[3]		—	Specifies the delay interval between attempts to restart. • 0—No delay • 1 to 7—Use the **Delay Time Between Restarts** parameter setting in the Power Sequencer component
0x57	[15:0]	VIN_OV_WARN_LIMIT[1]	*	Read Word Write Word	Sets the value of the input voltage that causes an input overvoltage warning.
0x58	[15:0]	VIN_UV_WARN_LIMIT[1]	*	Read Word Write Word	Sets the value of the input voltage that causes an input undervoltage warning.
0x59	[15:0]	VIN_UV_FAULT_LIMIT[1]	*	Read Word Write Word	Sets the value of the input voltage that causes an input undervoltage fault.
0x5A	—	VIN_UV_FAULT_RESP		Read Byte Write Byte	Instructs the device on the action to take when there is an input undervoltage fault.

continued...

Command Code (Address)	Bit	Name		SMBus Transaction	Description
	[7:6]	Response		—	• 00—Continue operation without interruption • 01—Invalid • 10—Sequence a power down in reverse order and respond according to the retry setting in bits [5:3] • 11—Invalid
	[5:3]	Retry Setting(2)		—	Indicates the number of times the device attempts to restart from a fault. • 0—Do not attempt a restart and remain disabled until the fault clears and ENABLE input toggles • 1 to 6—Retry for the specified number of attempts, then stop and remain disabled until the fault clears and the ENABLE input toggles • 7—Retry infinitely
	[2:0]	Delay Time(3)		—	Specifies the delay interval between attempts to restart. • 0—No delay • 1 to 7—Use the **Delay Time Between Restarts** parameter setting in the Power Sequencer component
0x5E	[15:0]	POWER_GOOD_ON(1)	*	Read Word Write Word	Sets the value of the output voltage at which it is sufficiently high for the design to assert the POWER_GOOD signal to the Power Sequencer component, indicating that the output voltage is valid.
0x5F	[15:0]	POWER_GOOD_OFF(1)	*	Read Word Write Word	Sets the value of the output voltage at which it has dropped low enough for the design to deassert the POWER_GOOD signal to the Power Sequencer component, indicating that the output voltage is not valid.
0x78	[7:0]	STATUS_BYTE • [7]: BUSY • [6]: OFF • [5]: VOUT_OV_FAULT • [4]: Reserved • [3]: VIN_UV_FAULT • [2]: Reserved • [1]: CML • [0]: NONE_OF_THE_ABOVE		Read Byte	A value of 1 for any bit indicates that a fault or warning has occurred in the associated status registers.
0x79	[15:0]	STATUS_WORD • [15]: VOUT • [14]: Reserved • [13]: INPUT • [12]: MFRSPECIFIC • [11]: PG_STATUS# • [10]: Reserved • [9]: OTHER • [8]: UNKNOWN		Read Word	A value of 1 for any bit indicates that a fault or warning has occurred in the associated status registers. Bits [7:0] are duplicate of STATUS_BYTE.

continued...

Command Code (Address)	Bit	Name	SMBus Transaction	Description
		• [7]: BUSY • [6]: OFF • [5]: VOUT_OV_FAULT • [4]: Reserved • [3]: VIN_UV_FAULT • [2]: Reserved • [1]: CML • [0]: NONE_OF_THE_ABOVE		
0x7A	[7:0]	STATUS_VOUT • [7]: VOUT_OV_FAULT • [6]: VOUT_OV_Warning • [5]: VOUT_UV_Warning • [4]: VOUT_UV_FAULT • [3]: Reserved • [2]: Reserved • [1]: Reserved • [0]: Reserved	Read Byte Write Byte	A value of 1 for any bit indicates that a fault or warning has occurred and flagged for the various conditions. To clear the flag, write 1 to the particular bit in the register.
0x7C	[7:0]	STATUS_INPUT • [7]: VIN_OV_FAULT • [6]: VIN_OV_Warning • [5]: VIN_UV_Warning • [4]: VIN_UV_FAULT • [3]: Unit Off for Low VIN • [2]: Reserved • [1]: Reserved • [0]: Reserved	Read Byte Write Byte	A value of 1 for any bit indicates that a fault or warning has occurred and flagged for the various conditions. To clear the flag, write 1 to the particular bit in the register.
0x7E	[7:0]	STATUS_CML • [7]: Invalid/Unsupported Command • [6]: Invalid/Unsupported Data • [5]: Reserved • [4]: Reserved • [3]: Reserved • [2]: Reserved • [1]: Reserved • [0]: Reserved	Read Byte Write Byte	A value of 1 for any bit indicates that a fault or warning has occurred and flagged for the various conditions. To clear the flag, write 1 to the particular bit in the register.
0x7F	[7:0]	STATUS_OTHER • [7]: Reserved • [6]: Reserved • [5]: Reserved • [4]: Reserved • [3]: Reserved	Read Byte Write Byte	A value of 1 for any bit indicates that a fault or warning has occurred and flagged for the various conditions. To clear the flag, write 1 to the particular bit in the register.

continued...

Command Code (Address)	Bit	Name	SMBus Transaction	Description
		• [2]: Reserved • [1]: Reserved • [0]: First to Assert SMBALERT#		
0x88	[15:0]	READ_VIN(1)	Read Word	Indicates the present input voltage level.
0x8B	[15:0]	READ_VOUT(1)	Read Word	Indicates the present output voltage level.

Related Information

Output Voltage Data Formats and Related Parameters on page 21
Provides information about translating to and from the PMBus DIRECT format.

4.2. Resource Utilization of the Multi-Rail Power Sequencer and Monitor Reference Design

Table 10. Approximate Resource Estimate for MAX 10 Device

Configuration	Component	Logic Elements	Flip-Flops
Six-rail sequencer with all rails monitored and full PMBus support	Modular ADC Core	120	90
	Sequencer ADC Decoder	300	100
	Sequencer Voltage Monitor	2125	1000
	PMBus Slave to Avalon-MM Master Bridge	150	100
	Power Sequencer	175	80
	Total Resources	**2870**	**1370**
Six-rail sequencer with all rails monitored and hardcoded PMBus thresholds	Modular ADC Core	120	90
	Sequencer ADC Decoder	300	100
	Sequencer Voltage Monitor	1025	500
	PMBus Slave to Avalon-MM Master Bridge	150	100
	Power Sequencer	175	80
	Total Resources	**1770**	**870**
Six-rail sequencer with all rails monitored but no PMBus support	Modular ADC Core	120	90
	Sequencer ADC Decoder	300	100
	Sequencer Voltage Monitor	225	130
	Power Sequencer	175	80
	Total Resources	**820**	**400**
Three-rail sequencer with all rails monitored and full PMBus support	Modular ADC Core	120	90
	Sequencer ADC Decoder	200	60
	Sequencer Voltage Monitor	1300	575
	PMBus Slave to Avalon-MM Master Bridge	150	100

continued...

Configuration	Component	Logic Elements	Flip-Flops
	Power Sequencer	120	60
	Total Resources	**1870**	**885**
Six-rail sequencer with no rails monitored and no PMBus support	Power Sequencer	160	80
	Total Resources	**160**	**80**

5. PCB Implementation for the Multi-Rail Power Sequencer and Monitor Reference Design

These block diagrams show how to connect MAX 10 devices programmed with the reference design on the PCB.

Figure 22. PCB Connection for MAX 10 Power Sequencer with Power Good (POK or PG)

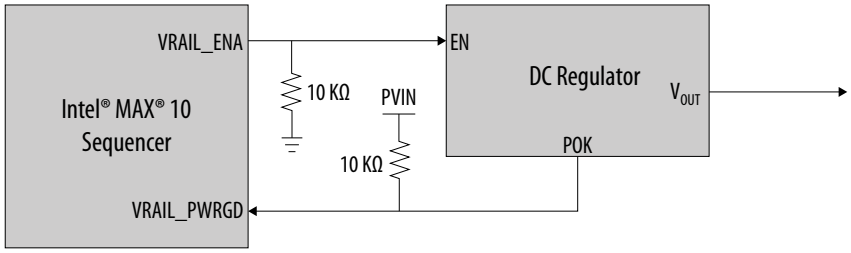


Figure 23. PCB Connection for MAX 10 Power Sequencer with Voltage Monitoring

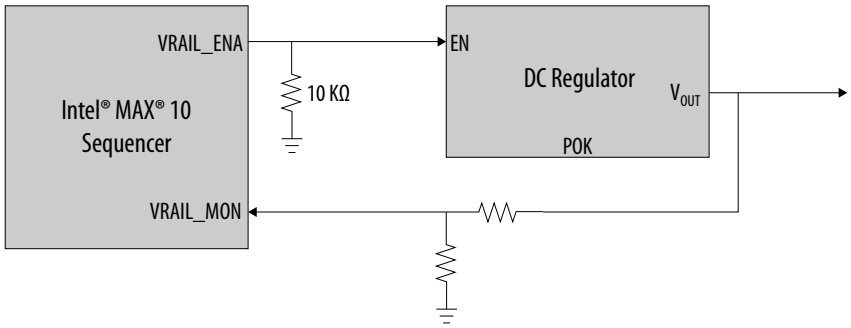


Figure 24. PCB Connection for MAX 10 Power Sequencer with Fast Discharge FET Circuit

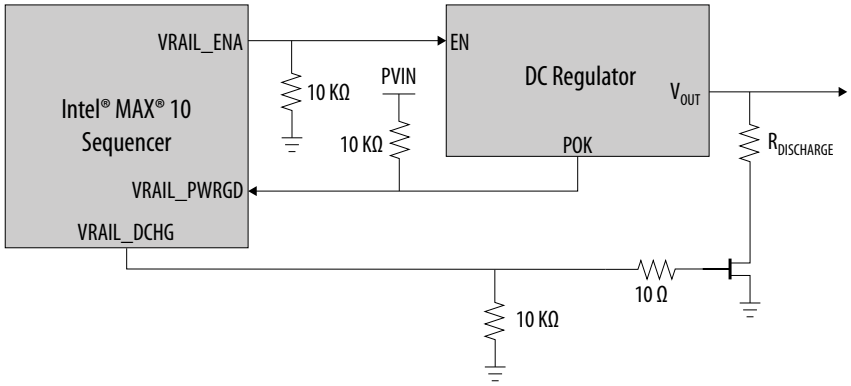


Figure 25. PCB Connection for MAX 10 Power Sequencer with Sequence Groups

- One EN signal per group fans out to multiple regulators.
- A separate POK signal or voltage monitor feedback is used per rail.
- You can tie multiple POK signals together for a single input (not shown in this figure).

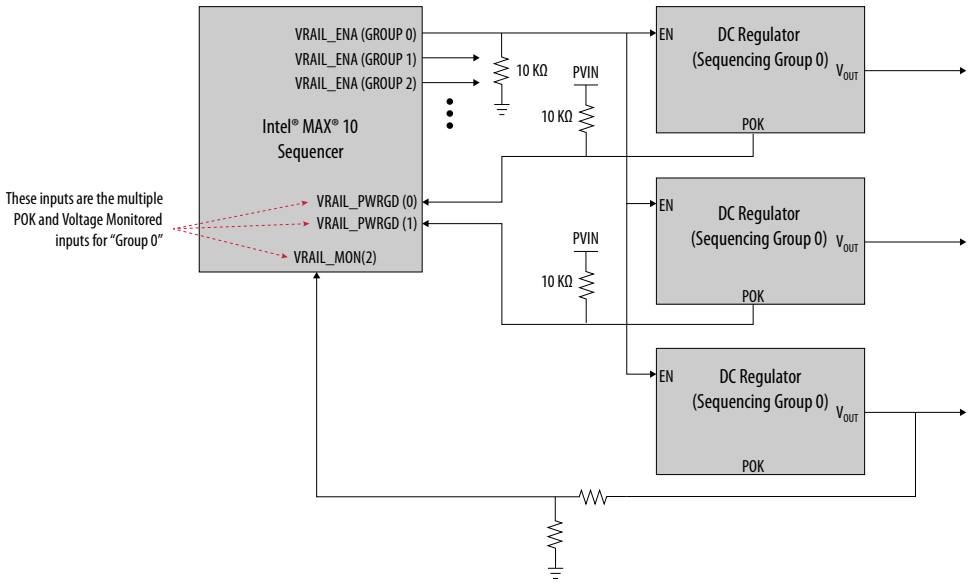
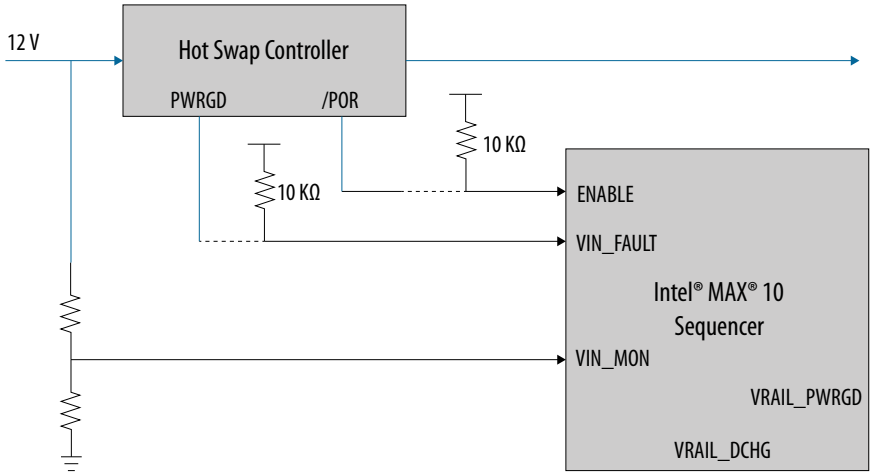


Figure 26. PCB Connection for MAX 10 Power Sequencer with VIN Monitoring and Enable

- Option to monitor VIN_FAULT or VIN_MON.
- The sequencer uses only one input or the other.
- Whichever input the sequencer uses determines if the input rail is within specification.



6. Document Revision History for the AN 896: Multi-Rail Power Sequencer and Monitor Reference Design

Document Version	Changes
2024.03.15	• Added *Reset Sequencer (Reset_Sequencer)* section. • Updated *Power Sequencer Parameter Editor* figure in *Power Sequencer (Sequencer_Core)*. • Added *POR Pulse (POR_Pulse)* section. • Added *Reset to Conduit Adapter (Reset2Conduit)* section. • Updated *pll_lock_splitter (PLL_LockSplit)* section. • Updated *Power Sequencer Signals* table in *Pin Description* section. • Updated *Multi-Rail Power Sequencer and Monitor Testbench Simulation Waveforms* figure in *Running the Testbench Simulation* section. • Updated instances of Intel Enpirion® PowerSoC to *DC Regulator*.
2019.09.30	Initial release.