AXI Streaming Intel® FPGA IP for PCI Express* IP Core Release Notes

Online Version

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815304

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1. AXI Streaming Intel® FPGA IP for PCI Express* IP Core Release Notes

The IP version (X.Y.Z) number may change from one Intel® Quartus® Prime software version to another. A change in:

- X indicates a major revision of the IP. If you update your Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

1.1. AXI Streaming Intel FPGA IP for PCI Express* IP Core v1.0.0

AXI Streaming Intel FPGA IP for PCI Express* IP Core v1.0.0

Table 1. v1.0.0 2024.01.19

Intel Quartus Prime Version	IP Version	Description
23.4	1.0.0 (P-Tile) 1.0.0 (F-Tile) 1.0.0 (R-Tile)	Initial release.

Table 2. AXI Streaming Intel FPGA IP for PCI Express IP Support Matrix for P-Tile in Intel Quartus Prime v23.4

EP = Endpoint, RP = Root Port, BP = TLP Bypass. Support level keys: S = Simulation, C = Compilation, T = Timing, H = Hardware, N/A = Configuration not supported.

Configuration	PCIe* IP Support			Design Example Support		
	EP	RP	BP	EP	RP	BP
Gen 4 x16	S C T	N/A	N/A	SCT	N/A	N/A
Gen4 x8/x8	S C T	N/A	N/A	N/A	N/A	N/A
Gen 3 x16	S C T	N/A	N/A	N/A	N/A	N/A
Gen3 x8/x8	S C T	N/A	N/A	N/A	N/A	N/A

Table 3. AXI Streaming Intel FPGA IP for PCI Express IP Support Matrix for F-Tile in Intel Quartus Prime v23.4

EP = Endpoint, RP = Root Port, BP = TLP Bypass. Support level keys: S = Simulation, C = Compilation, T = Timing, H = Hardware, N/A = Configuration not supported.

Configuration	PCIe IP Support			Design Example Support		
	EP	RP	BP	EP	RP	BP
Gen 4 x16	S C T	N/A	N/A	N/A	N/A	N/A
Gen4 x8/x8	S C T	N/A	N/A	N/A	N/A	N/A
Gen 3 x16	S C T	N/A	N/A	N/A	N/A	N/A
Gen3 x8/x8	S C T	N/A	N/A	N/A	N/A	N/A

Table 4. AXI Streaming Intel FPGA IP for PCI Express IP Support Matrix for R-Tile in Intel Quartus Prime v23.4

EP = Endpoint, RP = Root Port, BP = TLP Bypass. Support level keys: S = Simulation, C = Compilation, T = Timing, H = Hardware, N/A = Configuration not supported.

Configuration	PCIe IP Support			Design Example Support		
	EP	RP	BP	EP	RP	BP
Gen 5 x16	S C T	N/A	N/A	N/A	N/A	N/A
Gen5 x8/x8	S C T	N/A	N/A	N/A	N/A	N/A
Gen 4 x16	S C T	N/A	N/A	N/A	N/A	N/A
Gen4 x8/x8	S C T	N/A	N/A	N/A	N/A	N/A
Gen 3 x16	S C T	N/A	N/A	N/A	N/A	N/A
Gen3 x8/x8	S C T	N/A	N/A	N/A	N/A	N/A