END SEMESTER ASSESSMENT (ESA)
B.TECH. (CSE)
III SEMESTER

UE22CS251A – DIGITAL DESIGN & COMPUTER ORGANIZATION LABORATORY

PROJECT REPORT

ON

"VENDING MACHINE"

SUBMITTED BY

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ABSTRACT OF THE PROJECT:

This is like the brain of the vending machine.
It has a clock (clk), a reset (rst), and an input (in) that represents the money inserted (2 bits: 00 for 0 rs, 01 for 5 rs, 10 for 10 rs).
It has two outputs: out (whether a product should be dispensed) and change (the change to be returned, 2 bits).
States:

The vending machine has three states: s0, s1, and s2.
s0 is the initial state when nothing is happening.
s1 is when there's 5 rs inserted.` 1111111111111111

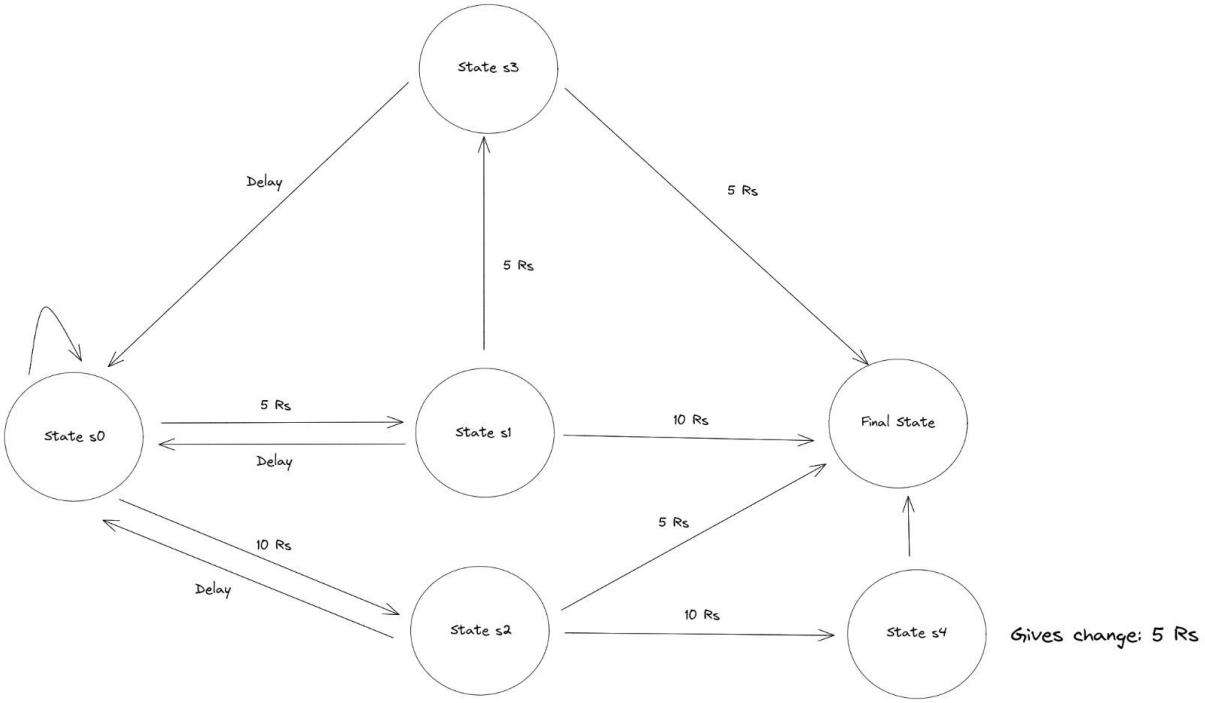
s2 is when there's 10 rs inserted.
State Transitions:

It starts in s0 when you turn it on (rst is pressed).
If you insert 5 rs (in is 01), it moves to s1.
If you insert 10 rs (in is 10), it moves to s2.
It goes back to s0 if you insert 0 rs (in is 00).
Product Dispensing and Change:

In s1, if you insert more money (in is 10), it goes to s2.
If you select a product (in is 10), it dispenses the product (out is set).
If you insert more money in s2 (in is 01), it goes back to s0.
Testbench:

The testbench is like a simulation of a person interacting with the vending machine.
It creates a clock (clk) and inputs money (in) to see how the vending machine reacts.
It generates a VCD file to visualize what's happening over time.
The simulation prints out messages to show the state of the vending machine and the values of inputs and outputs.
In summary, it's like a vending machine that goes through different states (like when you insert money, select a product, etc.) based on the inputs it receives. The testbench simulates this interaction to check if the vending machine is working as expected.

CIRCUIT DIAGRAM:



MAIN VERILOG CODE:

```
module vending_machine_18105070 (
    input clk,
    input rst,
    input [1:0] in, // 01 = 5 rs, 10 = 10 rs
    output reg out,
    output reg [1:0] change
);

parameter s0 = 2'b00;
parameter s1 = 2'b01;
parameter s2 = 2'b10;

reg [1:0] c_state, n_state;

always @(posedge clk or posedge rst)
begin
    if (rst)
    begin
        c_state <= s0;
```

```
        n_state <= s0;
        change <= 2'b00;
        out <= 0;
    end
    else
        c_state <= n_state;

    case (c_state)
        s0: // state 0 : 0 rs
            if (in == 2'b00)
            begin
                n_state = s0;
                out = 0;
                change = 2'b00;
            end
            else if (in == 2'b01)
            begin
                n_state = s1;
                out = 0;
                change = 2'b00;
            end
            else if (in == 2'b10)
            begin
                n_state = s2;
                out = 0;
                change = 2'b00;
            end

        s1: // state 1 : 5 rs
            if (in == 2'b00)
            begin
                n_state = s0;
                out = 0;
                change = 2'b01; // change returned 5 rs
            end
            else if (in == 2'b01)
            begin
                n_state = s2;
                out = 0;
                change = 2'b00;
            end
            else if (in == 2'b10)
            begin
```

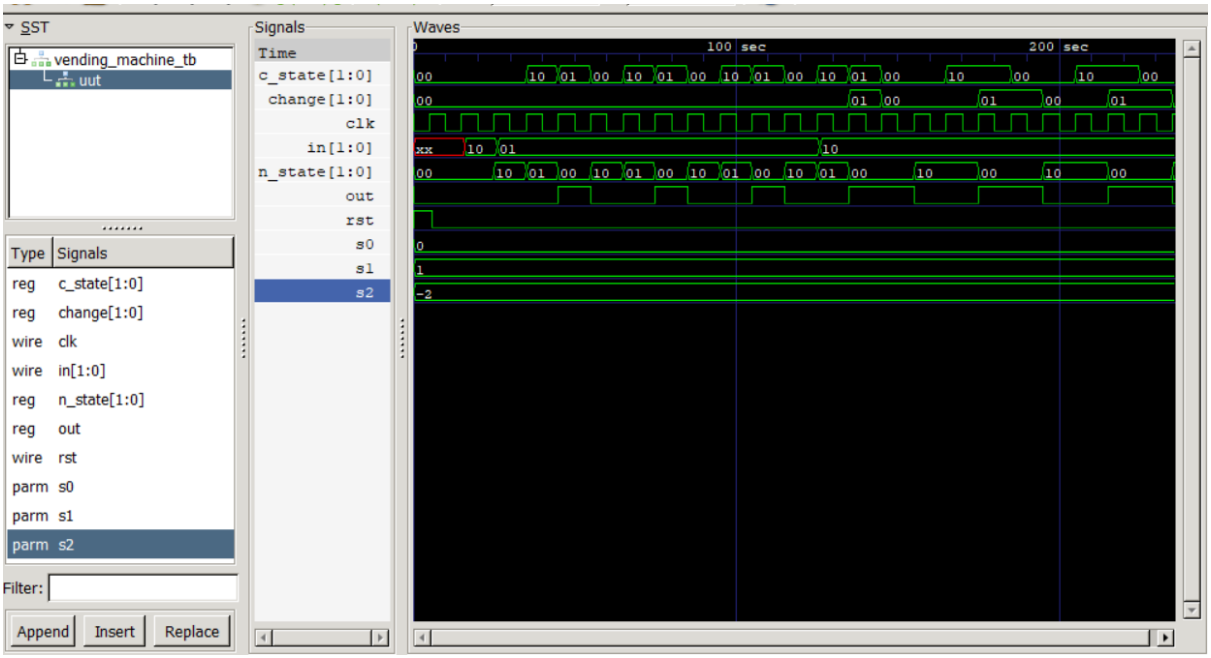
```
                n_state = s0;
                out = 1;
                change = 2'b00;
            end

        s2: // state 2 : 10 rs
            if (in == 2'b00)
            begin
                n_state = s0;
                out = 0;
                change = 2'b10;
            end
            else if (in == 2'b01)
            begin
                n_state = s0;
                out = 1;
                change = 2'b00;
            end
            else if (in == 2'b10)
            begin
                n_state = s0;
                out = 1;
                change = 2'b01; // change returned 5 rs and 1 bottle
            end
    endcase
end

endmodule
```

TEST BENCH FILE:

```
//TESTBENCH
module vending_machine_tb;

    reg clk;
    reg [1:0] in;
    reg rst;

    wire out;
    wire [1:0] change;
```

```
    vending_machine_18105070 uut(
    .clk(clk),
    .rst(rst),
    .in(in),
    .out(out),
    .change(change)
);

always #5 clk = ~clk;

initial begin
    $dumpfile("vending_machine_18105070.vcd");
    $dumpvars(0, vending_machine_tb);

    rst = 1;
    clk = 0;
    #6 rst = 0;

    #10;
    in = 2;
    #10 in = 1;

    #100;

    in = 2;
    #10 in = 2;

    #100;

    $finish;
end

always @(posedge clk) begin
    $display("Time %0t: in = %b, out = %b, change = %b", $time, in,
out, change);
end

endmodule
```

SCREENSHOT OF THE OUTPUT:



```
VCD info: dumpfile vending_machine_18105070.vcd opened for outp
Time 5: in = xx, out = 0, change = 00
Time 15: in = xx, out = 0, change = 00
Time 25: in = 10, out = 0, change = 00
Time 35: in = 01, out = 0, change = 00
Time 45: in = 01, out = 0, change = 00
Time 55: in = 01, out = 1, change = 00
Time 65: in = 01, out = 0, change = 00
Time 75: in = 01, out = 0, change = 00
Time 85: in = 01, out = 1, change = 00
Time 95: in = 01, out = 0, change = 00
Time 105: in = 01, out = 0, change = 00
Time 115: in = 01, out = 1, change = 00
Time 125: in = 01, out = 0, change = 00
Time 135: in = 10, out = 0, change = 00
Time 145: in = 10, out = 1, change = 01
Time 155: in = 10, out = 1, change = 00
Time 165: in = 10, out = 0, change = 00
Time 175: in = 10, out = 0, change = 00
Time 185: in = 10, out = 1, change = 01
Time 195: in = 10, out = 1, change = 01
Time 205: in = 10, out = 0, change = 00
Time 215: in = 10, out = 0, change = 00
Time 225: in = 10, out = 1, change = 01
Time 235: in = 10, out = 1, change = 01
project6_tb.v:134: $finish called at 236 (1s)
```