# Efficient Processing Time with Carry-lookahead Adder Memristor Rationed Logic

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***Abstract*— This paper presents a novel approach to the design of full adder circuits, leveraging the unique properties of memristors and CMOS logic in a hybrid system. This paper explores the design and operation of memristor-based logic gates, including AND, OR, NAND, and NOR gates, realized through CMOS inverters. This paper further proposes a full adder circuit using Hybrid Memristor-CMOS logic and a carry look-ahead adder (CLA). Our simulations demonstrate that the proposed full adder circuit outperforms traditional RCA-based circuits in terms of speed. This work contributes to the ongoing discourse in digital electronics, offering fresh perspectives and potential solutions to existing challenges, and hope it will inspire further research in the field of memristor-based digital electronics.**

***Keywords—memristor, full adder, carry look ahead adder***

## I. INTRODUCTION

In the dynamic field of digital electronics, the pursuit of efficient, high-speed logic circuits is a critical research objective. This paper presents a pioneering approach to full adder circuit design, harnessing the unique properties of memristors in combination with CMOS logic, a hybrid system that offers promising potential for significant advancements in digital circuit design.

Memristors, or memory resistors, are non-volatile resistive devices [1] that retain their state even when powered off. Their unique ability to remember their resistance state makes them an ideal candidate for various applications, including logic gates and adder circuits. The structure of a memristor is simple yet powerful, consisting of a thin film of titanium dioxide sandwiched between two electrodes. This structure allows for the control of resistance, and hence, the flow of electric current.

This paper delves into the intricacies of memristor-based logic gates, including AND, OR, NAND, and NOR gates [2], and their realization through CMOS inverters. The exploration extends to the design of a full adder circuit using Hybrid Memristor-CMOS logic.

Recognizing the inherent limitations of the Ripple Carry Adder (RCA), particularly its carry propagation delay, we propose an innovative solution: the carry look-ahead adder. This method calculates carry signals in advance based on input signals, significantly reducing carry propagation time, and enhancing the overall efficiency of the adder circuit.

Through rigorous simulations, we demonstrate that our proposed full adder circuit, which employs a carry look-ahead adder and memristor-based logic, outperforms traditional full adder circuits that use RCA in terms of speed.

## II. CONSTRUCTION LOGIC GATES UTILIZING MEMRISTORS

This paper, we delve into the design and operation of various memristor-based logic gates. These include the fundamental AND, OR, NAND, and NOR gates. Each of these gates plays a crucial role in digital circuit design, and their realization through memristors can lead to enhanced performance and efficiency.

The design process involves the use of CMOS inverters, specifically using 180 nm technology, which are integral to the operation of these logic gates. By harnessing the properties of memristors in combination with CMOS inverters. For measure the efficiency of each circuit, we use LTSPICE [4] to calculate the delay time. This provides a reliable metric for evaluating the performance and efficiency of the designed logic gates.

### *A. Construction Of NAND And OR Gates Utilizing Hybrid Memristor-CMOS Logic*

Leveraging the unique properties of memristors, we have designed AND and OR gates. The design of the AND gate is achieved by connecting the positive polarities of two memristors together and then feeding the positive voltage input into the negative polarity, as illustrated in Fig. 1(a) results in an increase in resistance, a key characteristic of the AND gate operation.

Similarly, the OR gate is designed by connecting the negative polarities of two memristors together and then feeding the input into the positive polarity, as depicted in Fig. 1(b). The positive input that feeds into the positive polarity leads to a decrease in resistance, which is fundamental to the operation of the OR gate.

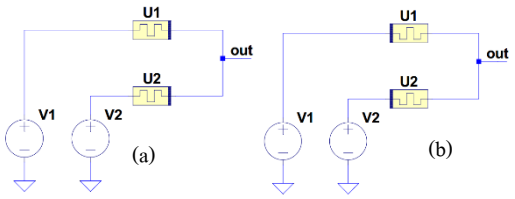


Fig.1(a) AND gate(b)OR gate [5]

The operation of these gates can be further understood through equation (1), where we define the input V1=VDD and V2=0V. This method yields the desired results for the AND and OR gates respectively.

$$V_{out} = V_1 \frac{R_1}{R_1 + R_2} \quad (1)$$

In equation (1), R1 represents the resistance of memristor U1, and R2 represents the resistance of memristor U2.

To design the NAND and NOR gates, we augment this setup with a CMOS inverter, as shown in Fig. 2. This hybrid approach combines the unique properties of memristors with the robustness of CMOS technology, creating efficient and high-speed logic gates.

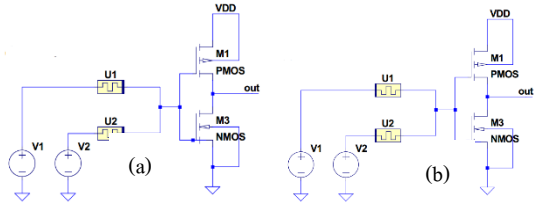


Fig. 2(a) NAND gate(b)NOR gate [5]

### *B. Construction Of Full Adder Circuit Utilizing Hybrid Memtistor-CMOS Logic*

The design of a full adder circuit using Hybrid Memristor-CMOS logic involves the integration of various logic circuits [6]. This approach allows for the creation of a full adder that benefits from the unique properties of memristors.

The XOR circuit, a fundamental component of the full adder, is defined by Equation (2) and is depicted in Fig. 5. Similarly, the Carry Out circuit, another crucial component of the full adder, is represented by Equation (3) and is shown in Fig. 6.

$$sum = \overline{A}B + A\overline{B} \quad (2)$$

$$C_{out} = AB \quad (3)$$

The full adder circuit itself, using Hybrid Memristor-CMOS logic, is defined by Equations (4) and (5). This full adder circuit comprises 18 memristors and 20 CMOS components, demonstrating the complexity and precision required in its design.

$$sum = C_{in}\left(AB + \overline{A}\overline{B}\right) + C_{in}\left(\overline{A}B + A\overline{B}\right) \quad (4)$$

$$C_{out} = AB + BC_{in} + AC_{in} \quad (5)$$

### *C. Limitations Of Ripple Carry Adder (RCA)*

As Figure 3, the operation of an RCA involves a sequential propagation of carry signals, which can result in significant delays. In an RCA, the generation of the first sum bit is contingent on the input carry signal. Subsequent sum bits, in turn, must wait for the propagation of the previous carry signal. This sequential dependency continues until the final output sum, which cannot be generated until all previous carry signals have been propagated.

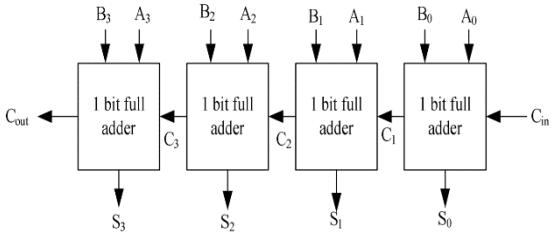


Fig.3 Example of 4-bit full adder by Ripple Carry Adder

## III. Construction Of Proposed Full Adder Circuit Utilizing Carry Look-ahead Adder

The ripple-carry adder, its limiting factor is the time it takes to propagate the carry. The carry look-ahead adder solves this problem by calculating the carry signals in advance, based on the input signals. The result is a reduced carry propagation time.

To be able to understand how the carry look-ahead adder works, we must manipulate the Boolean expression dealing with the full adder. The Propagate P and generate G in a full-adder, is following by Equation (6)-(7) and figure 4-6

$$P_i = A_i \oplus B_i \quad (6)$$

$$G_i = A_i B_i \quad (7)$$

Where $i$ is number of sequences

Notice that both propagate and generate signals depend only on the input bits and thus will be valid after one gate delay. The new expressions for the output sum and the carryout are given by Equation (8)-(9) and figure 7-8

$$S_i = P_i \oplus C_i \quad (8)$$

$$C_{i+1} = G_i + P_i C_i \quad (9)$$

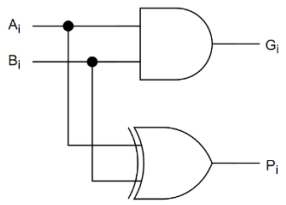


Fig.4 Logic Diagram of $G_i$ and $P_i$ of proposed circuit

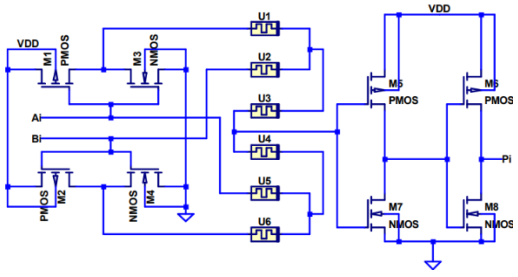


Fig.5 Circuit Diagram $P_i$ of proposed circuit

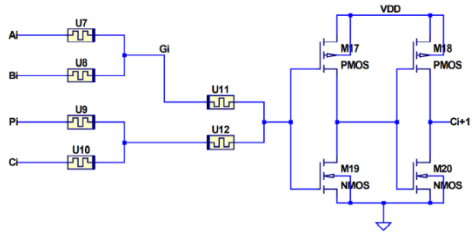


Fig.6 Circuit Diagram of $G_i$ and $C_{i+1}$ of proposed circuit

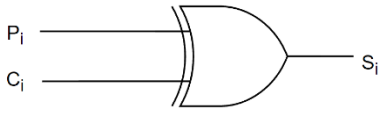


Fig.7 Logic Diagram of $S_i$ of proposed circuit

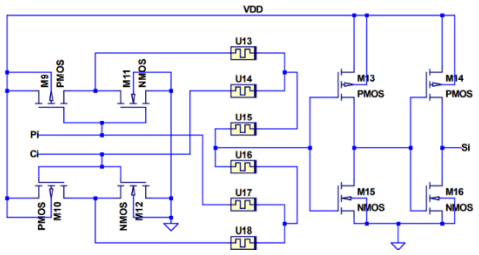


Fig.8 Circuit Diagram of $S_i$ of proposed circuit

In Equation (9) and figure 6 can be replace *i* by sample number 0-3 that effect circuit following by Equation (10)-(13) and figure 9-12 respectively

$$C_1 = G_0 + P_0 C_0 \tag{10}$$

$$C_2 = G_1 + G_0 P_1 + P_0 P_1 C_0 \tag{11}$$

$$C_3 = G_2 + G_1 P_2 + G_0 P_1 P_2 + P_0 P_1 P_2 C_0 \tag{12}$$

$$C_4 = G_3 + G_2 P_3 + G_1 P_2 P_1 + G_0 P_0 P_1 P_2 + P_0 P_1 P_2 P_3 C_0 \tag{13}$$

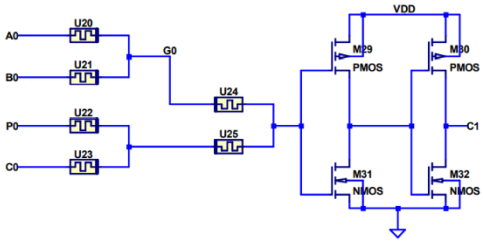


Fig.9 Circuit Diagram of $C_1$ of proposed circuit

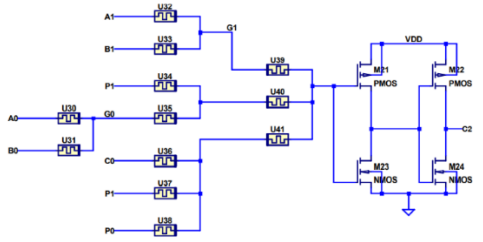


Fig.10 Circuit Diagram of $C_2$ of proposed circuit

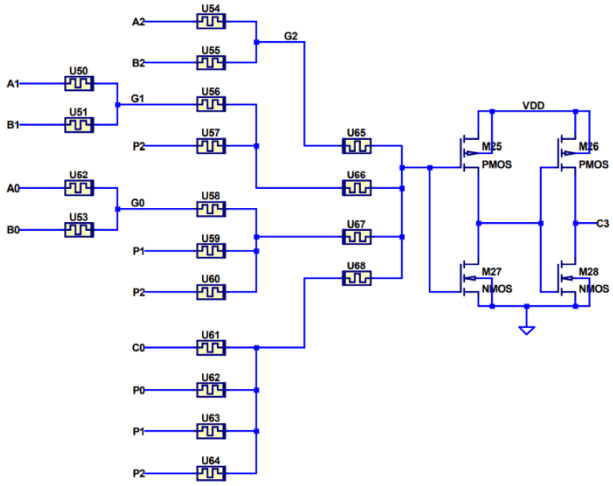


Fig.11 Circuit Diagram of $C_3$ of proposed circuit

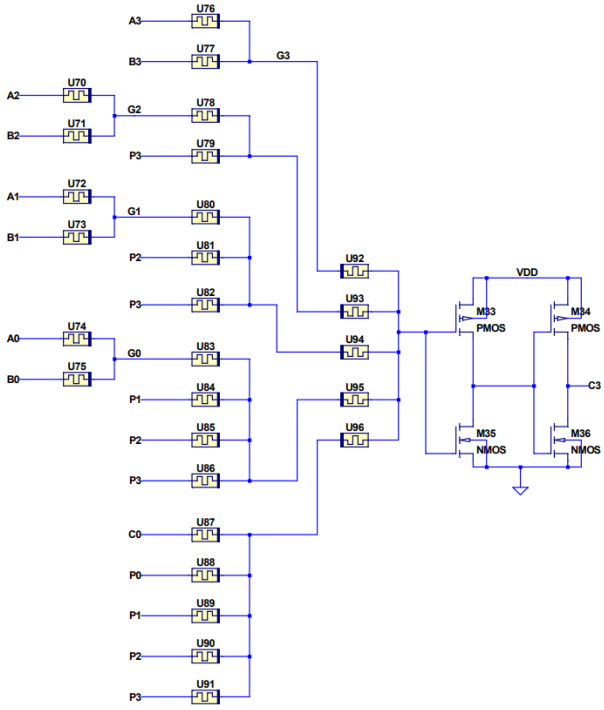


Fig.12 Circuit Diagram of $C_4$ of proposed circuit

Table 1 tabulates sample of the voltage input ($A_0$, $B_0$, $A_1$, $B_1$, $C_0$), $P_0$, $P_1$, $P_2$, $P_3$, $R_{on}$, and voltage output of proposed Carry-lookahead Adder Memristor Rationed Logic (Fig. 8 and 10). For example, 1, given $A_0$= LOW, $B_0$= LOW, $A_1$= LOW, $B_1$= LOW, $C_0$= HIGH (i.e., scenario 1), that effect output $S_0$= HIGH, $S_1$= LOW, $C_1$= LOW, $C_2$= LOW. For example, 2, given $A_0$= HIGH, $B_0$= LOW, $A_1$= HIGH, $B_1$= HIGH, $C_0$= HIGH (i.e., scenario 6), that effect output $S_0$= LOW, $S_1$= LOW, $C_1$= HIGH, $C_2$= HIGH

Table 1 sample of the voltage input $A_0$, $B_0$, $A_1$, $B_1$, $C_0$ , process voltage $G_0$, $G_1$, $P_0$, $P_1$ and voltage output of the proposed MRL 2-bit full adder

| Voltage Input | | | | | | | | | Voltage Output | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $A_0$ | $B_0$ | $A_1$ | $B_1$ | $C_0$ | $G_0$ | $G_1$ | $P_0$ | $P_1$ | $S_0$ | $S_1$ | $C_1$ | $C_2$ |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |

## IV. SIMULATION RESULTS

The proposed circuit high-speed full adder circuit using carry look ahead adder was simulated the rise time ( $T_r$ ), fall time ( $T_f$ ), and delay time ( $T_{pd}$ ) by LTspice simulation software, given the threshold memristor model [18] and 180 nm CMOS transistors.

Table 2 Comparison processing time of Conventional multi-stage MRL full adder, Multi-stage NAND gate full adder and Proposed circuit. Nevertheless, the realization of proposed circuit no need required 4 CMOS transistors in each 1-bit full adder block for cascade block because look ahead adder mothed is parallel processing.

Table 2. Comparison processing time of Conventional multi-stage MRL full adder, Multi-stage NAND gate full adder and Proposed circuit

| | $T_r$ (ps) | $T_f$ (ps) | $T_{pd}$ (ps) |
|---|---|---|---|
| Conventional multi-stage MRL full adder | 84.12 | 31.34 | 122.55 |
| Multi-stage NAND gate-based full adder | 69.41 | 13.37 | 129.39 |
| Proposed circuit | 32.509 | 12.45 | 36.34 |

## V. CONCLUSION

This research proposes the high-speed full adder circuit using carry look ahead adder. It is an alternative full adder which is mostly high speed because parallel processing. The performance of proposed circuit faster than other full adder circuit with RCA around 4 times by using LTspice simulator. Nonetheless, due to speed, the proposed full adder requires a higher number of components and energy consumption.

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