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A Comparative Analysis of 8-Bit Parallel Prefix Adder Architectures

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***Abstract* — Digital adders are crucial parts of contemporary computer systems that influence the efficiency of specific arithmetic processes. Parallel prefix adders, like Sparse Kogge, Hancarlson and Brent Kung enhance performance by calculating results leading to faster and more efficient arithmetic operations compared to traditional adders that process data sequentially. This paper thoroughly compares four 8 bit designs; Sparse Kogge, Han Carlson, Brent Kung and Binary Coded Decimal (BCD) adder. Evaluation criteria include propagation latency (ns) power consumption (W) and area utilization (LUTS). When comparing the Brent Kung adder with the BCD adder there is a 18.33% increase in propagation delay but a significant 83.87% decrease in power consumption and a fifty percent reduction in area usage. The primary focus of the Hancarlson adder is power efficiency leading to an 87.10% drop in power usage but a substantial 93.49% increase in propagation latency. The Sparse Kogge adder strikes a balance with a 58.06% decrease in power consumption and a moderate 18.75% reduction in area utilization while maintaining a propagation delay, as the BCD adder.These results illustrate trade-offs between various adder architectures in terms of power, latency, and area utilization. These designs are designed and simulated using Xilinx Vivado 2022.2 software.**

Keywords— Digital adders, parallel prefix adders, Sparse Kogge, Hancarlson, Brent Kung, Binary-Coded Decimal (BCD) adder.

I. Introduction

Adders play a role, in circuits as they facilitate arithmetic functions in modern computer systems. The functionality of processors, memory units and various arithmetic logic components relies on these circuits which're responsible, for adding values. Historically adders were constructed using an approach handling each bit individually. However, a paradigm change has resulted in the investigation of parallel prefix adders as computing demands have increased. The significance of prefix adders, especially their innovative variations such as carry-select and carry-lookahead adders, becomes evident in the field of digital circuit design when juxtaposed with their more traditional equivalents such as ripple-carry adders. One important feature that increases their significance is the noticeable increase in parallelism and speed. Prefix adders are really good, at speeding up addition tasks by handling bits. This is an advantage for programs that value computing speed. Also these adders have a path latency, which reduces the time it takes for carry propagation, in the adders structure. When cutting down on latency is important this feature proves to be quite useful. Another interesting trait of prefix adders is their ability to scale up; as the number of bits goes up their latency increases in a manner. One interesting aspect of prefix adders is their ability to scale up naturally; as the number of bits grows their delay increases in a manner. This scalability proves useful for tasks demanding adders. Moreover prefix adders can help reduce power consumption making them an attractive option, for energy efficient solutions, in certain scenarios. While it is understood that these adders may require hardware and occupy more physical space these considerations are often justified in situations where high performance computing relies heavily on fast arithmetic operations. Prefix adders are crucial because they are able to balance speed, scalability, and customisation, which makes them highly suitable for a variety of digital computation applications.

II. Literature Review

In [1], innovative approaches to adder design are provided for two new types of adders: Single Exact Dual Approximate Adders and Single Exact Single Approximate Adders. Some research studies worked on enhancing the speed and effectiveness of output carry look adders [2][3]. This investigation delves into design strategies for parallel prefix adders, which are crucial components of modern VLSI systems. The search for fast arithmetic operations in computer applications [4] drives the development of new strategies capable of effectively managing the difficulties involved in parallel-prefix addition. It is possible that the article will look at how to use parallelism to speed up arithmetic processes. Parallel-prefix adders are known to reduce the critical path latency associated with standard ripple-carry adders, since they can calculate the carry values

in parallel. Delay reduction leads to faster multi-bit number addition, which is important for optimizing the overall performance of digital systems. The main focus of this study is to develop an 8-bit Arithmetic Logic Unit (ALU) using Sparse Tree Superconductor Rapid Single Flux Quantum (RSFQ) technology [5][7]. Unlike architectures asynchronous ALU designs offer potential benefits in terms of improved power efficiency and system performance. The implementation and comparison of VLSI architectures for a 16-bit carry-select adder are examined by the research team. In particular, [6] makes use of the Brent Kung adder, a well-known parallel prefix structure that is highly effective in VLSI design.

It focuses on exploring designs in the unique QCA paradigm, which is a potential technology, for nano scale computing. By contrasting the Ripple Carry and Brent Kung adders the authors contribute to our understanding of how different adder architectures operate within the QCA framework. This comparison sheds light on the balance, between performance and complexity in this advancing minuscule computing environment. In the special context of QCA, Paper [8] investigates the low complexity design features of Brent-Kung and Ripple Carry adders. By analyzing these adder architectures, it is intended to provide insights on efficient nanoscale computer systems. By comparing the two adder types, the performance and complexity trade-offs are made clear in the context of QCA, which offers crucial information for designing dependable circuits in this new technology. In [9], a new design strategy for parallel prefix adders is presented with an emphasis on approximation methods. This research investigates the trade-offs between computational efficiency and precision, providing light on the possible uses of approximate adders.

The study contributes to the evolving field of adder architectures by addressing the growing interest in approximation computing for enhanced performance and energy efficiency in many applications [10]. A new approach, for applications that require real time processing is put forward with a focus on the developments, in designs discussed in the research [11],[12][13]. The study recommends exploring Binary Coded Decimal (BCD) Brent Kung, Hancarlson. Sparse Kogge adders to address limitations identified in studies. Every adder tackles a different set of problems; BCD provides accuracy in decimal arithmetic, Brent-Kung uses parallelism to speed up operations, Hancarlson [14] introduces a variety of design techniques, and Sparse Kogge simplifies hardware. The goal of this strategy is to get beyond the drawbacks of current techniques and advance the development of effective and high-performing adder designs for real-time computing [15].

III. Proposed Method

Parallel prefix adders are circuits that have been designed for efficient binary addition, making them essential in digital systems such as microprocessors. These adders are especially valuable for applications that need fast arithmetic operations, offering significant performance advantages compared to simpler adder designs like ripple-carry adders.

Performing addition with binary integers requires careful control of carry values as they propagate from one-bit location to the next. Effectively managing these carries is crucial for achieving rapid addition. Binary addition involves determining the perform of each bit based on the carry-in from the previous bit and the bits being added at that specific place. Parallel prefix adders are designed to optimize the propagation of carry process to minimize delays.

A digital circuit intended for the addition of numbers expressed in Binary-Coded Decimal (BCD) form is called a BCD adder. Applications requiring exact decimal arithmetic, such financial and scientific computations, benefit greatly from the usage of BCD adders. They provide a simple approach to add decimal numbers in a binary environment, guaranteeing precise outcomes with little in the way of complexity.

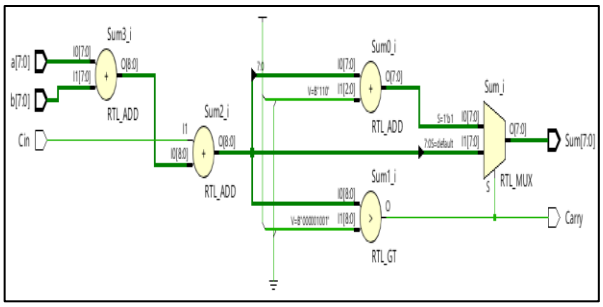

Figure 1. RTL Schematic of 8 bit BCD Adder

Adder is a basic part of digital systems and is essential to many different applications, including image processing, digital signal processing [16], digital filtering [17] and a variety of mathematical calculations. Figure 1 shows the RTL schematic of BCD adder & figure 2 is about power calculation for the above schematic. The Brent-Kung adder speeds up binary addition by breaking the process up into two stages: final sum selection through a carry-select network and partial sum production in parallel using group-specific carry-lookahead adders. When comparing the traditional ripple-carry adders to our parallelized approach [18], speed is boosted by lowering critical path delays. Despite its efficiency, the Brent-Kung adder could require more space due to the additional hardware required for parallel processing.

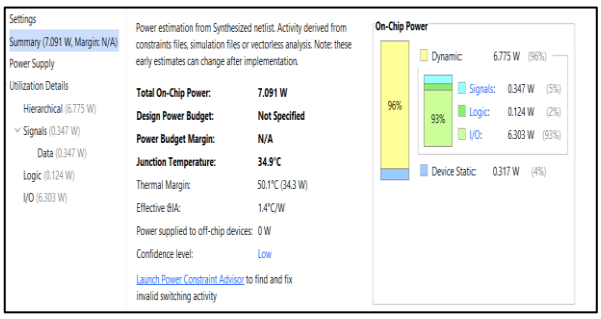

Figure 2. Power Calculation of 8 bit BCD adder

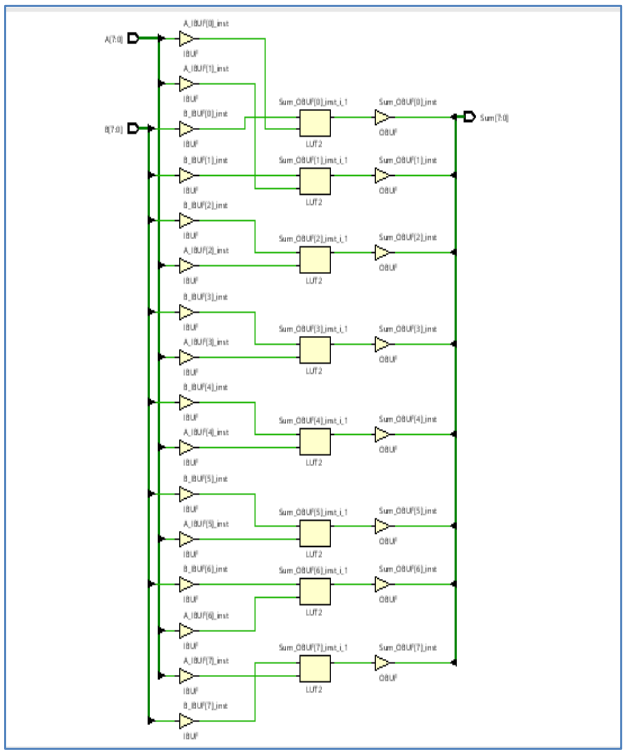

Figure 3. RTL Schematic of 8 bit Brent Kung Adder

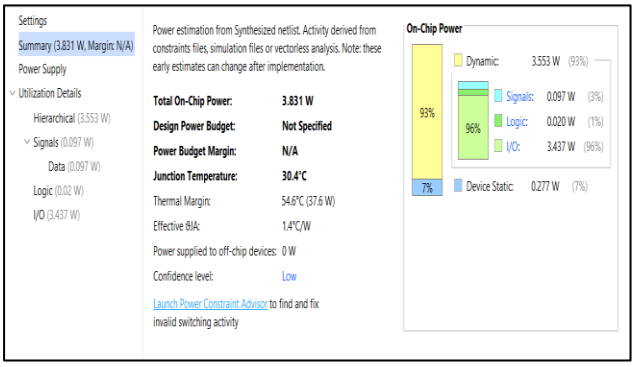

Figure 4. Power Calculation of 8 bit Brent Kung adder

Figures 3 and 4 shows the RTL schematic and power calculations of Brent Kung adder. Practical uses for the Brent-Kung adder include embedded systems, high-performance computers, digital signal processors, processors, graphics processing units, communication systems, and cryptographic processes. Because of its quick addition speed, it can be used in situations where processing binary numbers quickly and effectively is necessary [19].

A parallel-prefix adder called the Han-Carlson adder was created to accelerate binary addition. This adder uses a tree-like structure and a divide-and-conquer strategy to calculate sum and carry values in parallel are shown in figure 5 and its power calculations are shown in figure 6. It seeks to increase the use of parallelism and, as a result, lower the critical path latency by dividing jobs among several phases. The Han-Carlson adder is a parallel-prefix adder that works well in applications where quick binary addition is essential, much like the Brent-Kung adder. Depending on certain design needs, adder designs [20] can be chosen based on things like speed, area overhead, and power consumption.

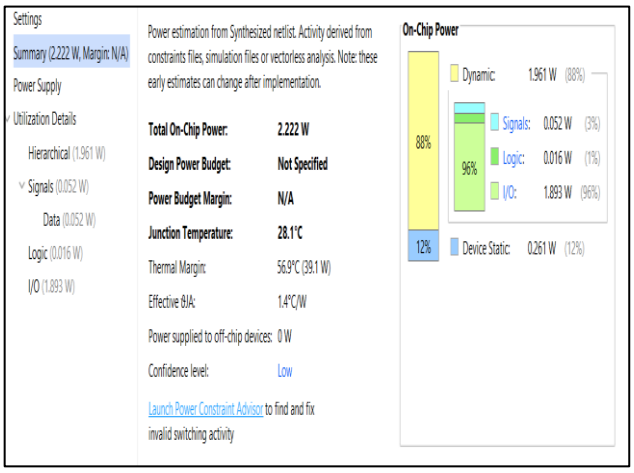

Figure 5. RTL Schematic of 8 bit Hancarlson Adder

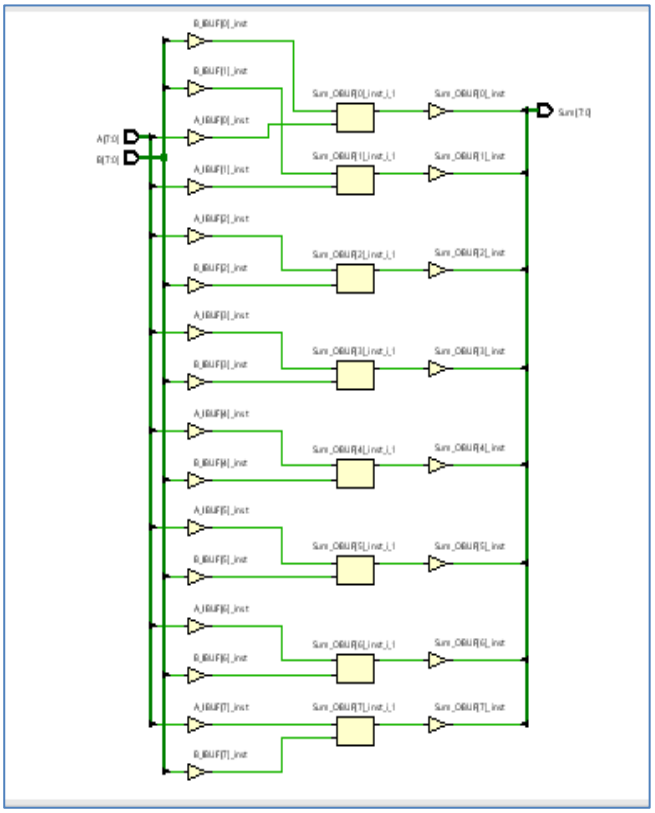

Figure 6. Power Calculation of 8 bit Hancarlson adder

A number of versions that aim to minimize hardware complexity and maximize resources have been inspired by the Kogge-Stone adder, a parallel-prefix adder that is well-known for its effective binary number summing via a tree structure. Among these variations is the "sparse Kogge-Stone adder," which denotes a design strategy intended to reduce the number of parts or connections while maintaining the Kogge-Stone architecture's inherent parallelism and speed advantages. "Sparse" refers, in the context of adders, to designs that make intelligent use of resources according to the properties of the input data; these designs are especially useful in situations when certain bits of the input data are anticipated to be zero.

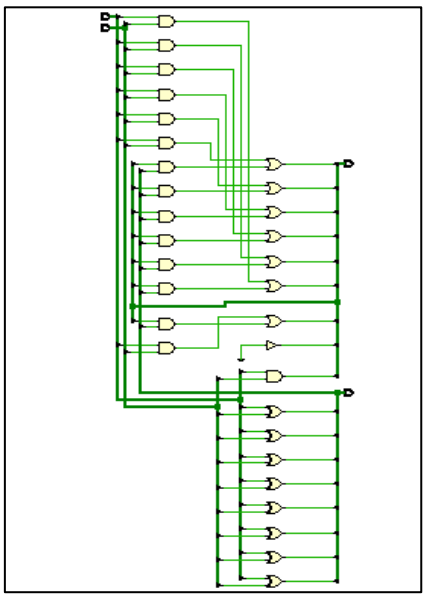

Figure 7. RTL Schematic of 8 bit Sparse Kogge stone Adder

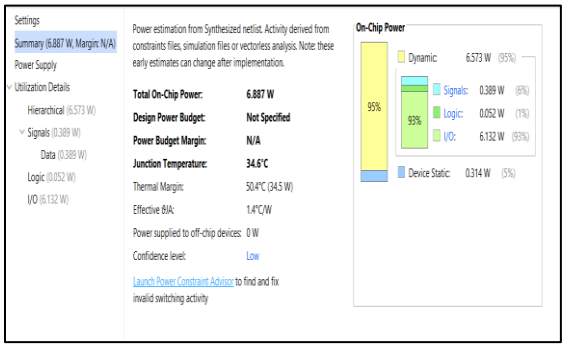

Figure 8. Power Calculation of 8 bit Sparse Koggestone Adder

A sparse Kogge-Stone adder can be used in low-power embedded systems, sparse matrix operations, signal processing in communication systems, custom hardware accelerators for machine learning, and environments with limited hardware are shown in figure 7 resources. Its purpose is to maximize computational efficiency in situations where there are a lot of zero bits and its power calculations are shown in figure 8. Its advantages are especially pertinent when sparse characteristics are present in the input data.

IV. Results and Discussion

Figure 9 shows the results of a BCD ADDER simulation. It shows inputs labeled 'a' and 'b,' and outputs labeled ‘sum' and 'carry.'

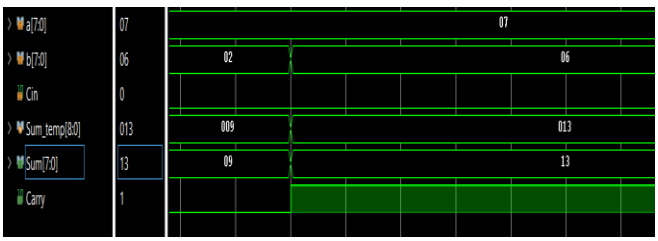

Figure 9. Simulation Results of 8 bit BCD Adder

Figure 10 displays the results of a Brent kung ADDER simulation. It includes inputs denoted as 'a' and 'b,' and outputs denoted as’ sum' and 'carry.'

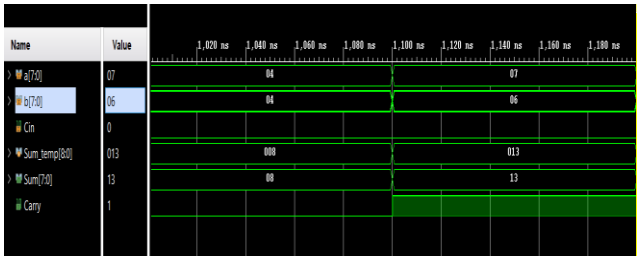

Figure 10. Simulation Results of 8 bit Brent Kung Adder

Figure 11 displays the results of a 8 bit Hancarlson ADDER simulation. It includes inputs denoted as 'a' and 'b,' and outputs denoted as ‘sum' and 'carry.'

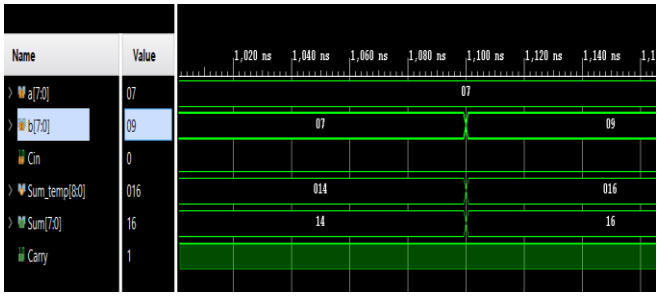

Figure 11. Simulation Results of 8 bit Hancarlson Adder

Figure 12 shows the results of a Sparse Kogge ADDER simulation. It includes inputs labelled 'a' and 'b,' and outputs labeled 'sum' and 'carry.'

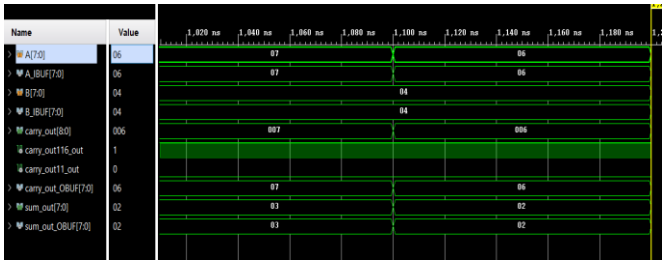

Figure 12. Simulation Results of 8 bit Sparse Kogge Adder

Table 1: Comparison of performance(Area, Logic Power and Delay) analysis of various adders of 8 bit.

ADDER Design (8 bit)	Performance parameters		
	AREA(LUT's)	LOGIC POWER(W)	Delay(ns)
BCD	16	0.124	5.960
Brent Kung	8	0.020	2.876
Hancarlson	8	0.016	2.874
Sparse Kogge	13	0.052	5.960

Table 1 displays the various qualitative qualities displayed by the four 8-bit adder architectures, namely BCD, Brent Kung, Hancarlson, and Sparse Kogge, based on their performance metrics. Delay analysis figure 15 illustrates how the BCD adder, which has 16 LUTs and a 5.960 ns delay, appears to be built for Binary-Coded Decimal representation and may have very complex architecture.

The Brent Kung adder, on the other hand, demonstrates efficiency in both area utilization and speed, making it appropriate for a wide range of applications. It has 8 LUTs, 0.020 W logic power, and a 2.876 ns latency. The Hancarlson adder, which has the lowest logic power (0.016

W) with a similar latency of 2.874 ns, highlights power efficiency even further are shown in figure 14. With 13 LUTs and a 5.960 ns delay, the Sparse Kogge adder prioritizes area utilization, are shown in figure13. which makes it a viable option in situations where latency compromise is not as important as efficient resource handling. Finally, the qualitative study shows how important it is to consider application-specific needs when selecting the optimal adder design, including things like speed, power consumption, and resource utilization.

The Sparse Kogge adder, which has 13 LUTs and a 5.960 ns delay, is a good choice when controlling resources efficiently is more crucial than sacrificing latency. Ultimately, the qualitative study shows how important it is to consider application-specific needs when selecting the optimal adder design, including things like speed, power consumption, and resource utilization.

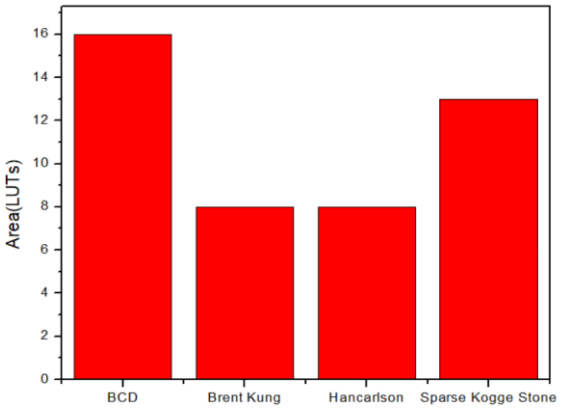

Figure 13. Area Analysis of 8 bit adders

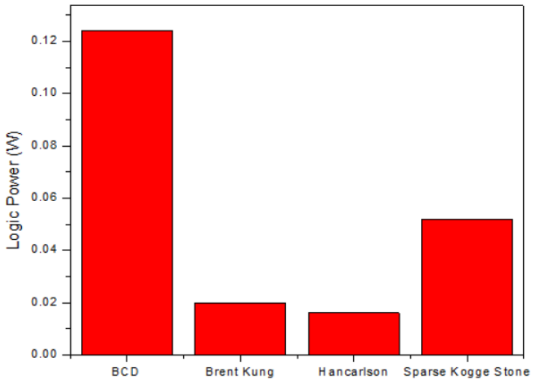

Figure 14. PowerAnalysis of of 8 bit adders

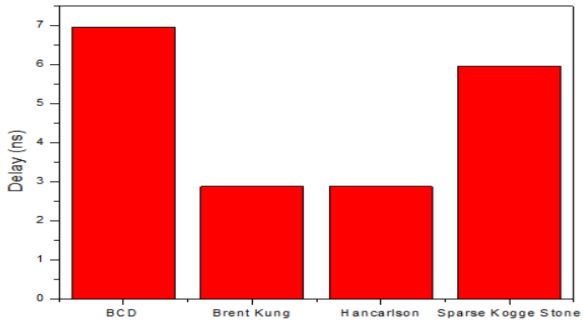

Figure 15. Delay Analysis of of 8 bit adders

The particular requirements of the application should guide the choice of adder design. BCD adders are better for decimal arithmetic. Hancarlson and Brent Kung adders work well in low-power applications. Sparse Kogge adders are adaptable for a range of applications because they provide a trade-off between area efficiency and delay.

V. CONCLUSION

Four different 8-bit adder designs are compared: Sparse Kogge, Brent Kung, Hancarlson, and BCD. This comparison provides important information about the performance trade-offs of each architecture. Despite a little increase in propagation delay, the Brent Kung adder performs well in power economy and compactness, making it a good choice for situations where energy consumption and space constraints are critical. The Hancarlson adder, on the other hand, is the best option in situations when low power consumption trumps processing speed since it prioritizes power savings at the cost of higher latency. The Sparse Kogge adder is a flexible solution for applications that require a trade-off between resource utilization and power efficiency because it achieves a harmonious balance between large power reduction and minimal area utilization decline. These results highlight how complex adder selection is and how important it is to carefully weigh application-specific factors including latency, power consumption, and area utilization. This research offers valuable insights that will help academics and engineers make well-informed decisions when optimizing arithmetic processes for various computational requirements in contemporary computer systems.

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