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Designing Carry Look Ahead Adder to Enrich Performance using One Bit Hybrid Full Adder

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Abstract- ***Digital circuits also known for logic circuits ,logic circuits mainly operate on addition, subtraction, division multiplication etc.. here ,Adders are the circuits which has copious ways of smearing for todays digital era, the main grail of our design is to extrapolate and whip up low power Carry look ahead adder by taking prerequisite of one bit hybrid Full Adder circuit and comparing it with numerous adders design styles like a Full Adder designed using 10 transistors, full adder using 13 Transistors , full adder using 28 Transistors , Ripple -Carry Adder using one bit hybrid adder ,looking within of details make comparative study where in, one bit hybrid full adder is considered because of its Less Power consumption ,delay and power delay product these parameters were studied them as performance metrics , and designed Carry Look Ahead adder using one bit hybrid full adder, as Carry Look Ahead is considered it is knows as fastest adder circuits which upgrades the speed by reducing the time by determining the carry bits. calibrates each and every digit's position either it will be propagating and generate a carry bit. Carry Look Ahead is designed and implemented in Cadence virtuoso 90nm technology with 1.0v of supply voltage.***

Keywords— Delay, Power, Power Delay Product, Full Adder, Carry Look Ahead

I.INTRODUCTION

Adders had became one of the important circuit in electronics. It performs the addition of numbers. Adders circuits are used in designing of Arithmetic Logic Unit (ALU) which is the major component of computer. It does operations like increment and decrement and also calculate table indices, addresses. Adders are The major concern nowadays in devices that are portable like cell phones, laptops etc. is about battery life and performance the devices with huge battery life and good performance having high demand so, many of the researchers working on new technologies of Very Large Scale Integration (VLSI) [3].

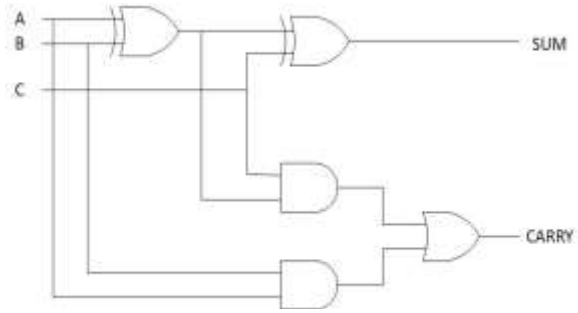

Fig 1: Schematics full adder

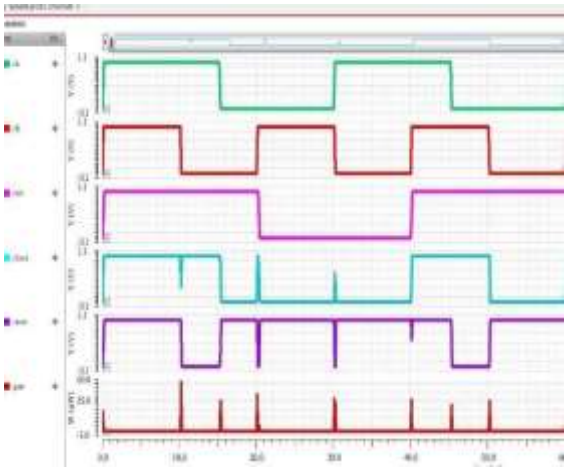

Fig 2: Wave form of full adder

II. ONE BIT HYBRID FULL ADDER

By relating normal static full adder with hybrid, Hybrid one has more efficiency. Hybrid adder means designing the circuit by incorporating profuse logic styles such as transmission gate and PTL in one circuit[2]. The main aim of the proposed design is to bring down the PDP, delay and power and make the circuit optimized[1]. The design is split into 3 parts, part1 and part2 are used for generating SUM and part3 generates CARRY (Cout). So every part is designed to get the desired output with low power and delay values[2].

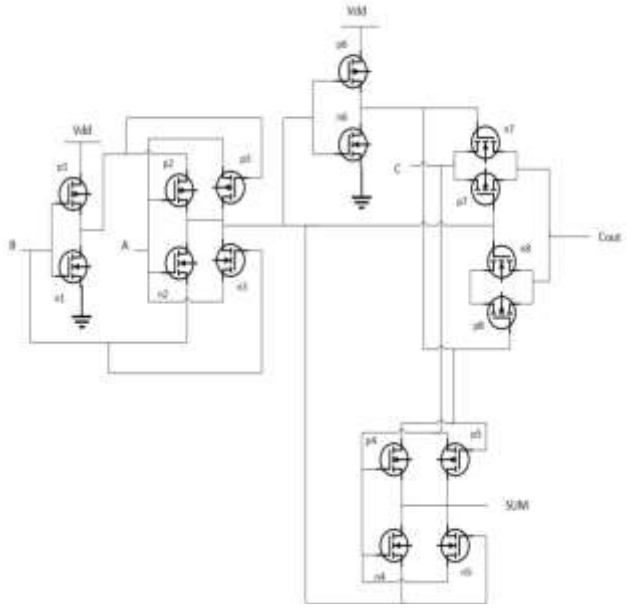

Fig 3:Schematics of one Bit hybrid full adder

By observing the above diagram XNOR part generate SUM transistors p1 and n1 produces B and p3 and n3 pass transistors are used to eliminate voltage declining caused by the not gate . To complete the entire SUM transistors p4, n4, p5, n5, p6, n6 are used[6]. Hence SUM is analyzed and next comes carry, carry Cout is obtained with the help of n7, p7, n8, p8 transistors which acts transmission gate and therefore carry also obtained[10].

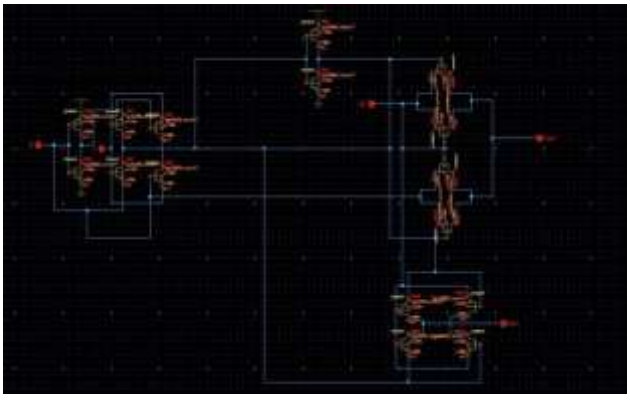

Fig 4: Schematics of one Bit hybrid full adder

III. APPLICATION OF ONE BIT HYBRID FULL ADDER AS CARRY LOOK AHEAD (CLA)ADDER

The carry-look ahead adder (CLA) or fast adder is one of the best application of one bit hybrid full adder . A carry lookahead adder is more efficient because of its speed and reduced delay while calculating carry bits[4]. But when it is related to ripple carry adder with carry look ahead adder the delay is high in ripple carry adder because the carry has to pass through every stage so it obviously increases the delay[7]. So, to overcome this problem carry look adder is preferred over ripple carry adder. The carry look ahead adder produces the sum without waiting for the carry in this way delay is reduced. Carry-Look Ahead Adder (CLA) is constructed by cascading the one bit hybrid full adder circuit in parallel form.

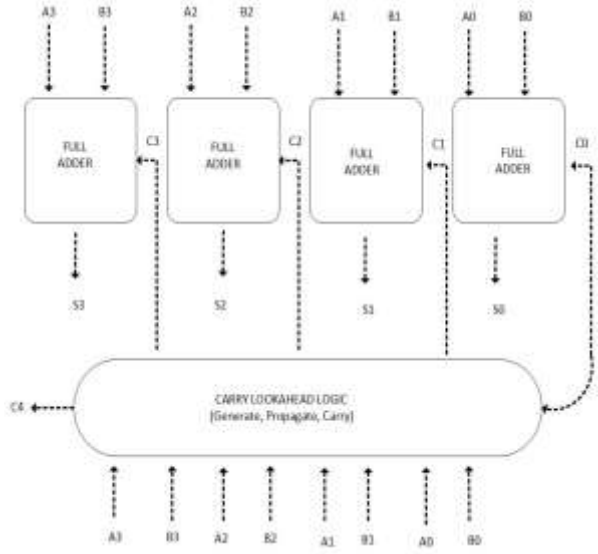

Fig 5: Block diagram of Carry Look Ahead (CLA) logic

Working : The above diagram is used to calculate addition of any 4 bit number initially the carry is 0 (grounded) the diagram also consist of combinational circuit .It uses the concept of carry propagator and carry generator .irrespective of the values carry input (0 and 1) if a carry is generated then those values of A and B are called as carry generators[. As a result the addition of two numbers A and B is done very fast without waiting for the previous carry

$$Pi = Ai \text{ XOR } Bi$$

$$Gi = Ai \text{ AND } Bi$$

$$SUM = Ai \text{ XOR } Bi \text{ XOR } Cin$$

$$Ci+1 = Pi\,Ci + Gi$$

By the help of above equations, the remaining values are calculated. So finally the addition of two numbers of 4 bits is done with the proposed circuit and it is observed that carry look ahead adder produces the output very fast when related with existing ripple carry adder[9].

IV. SIMULATION RESULTS

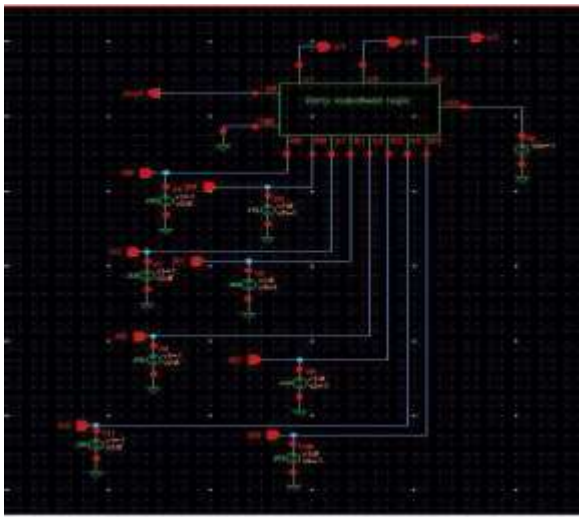

Fig 6. Schematics of Carry Look Ahead (CLA) Logic Circuit

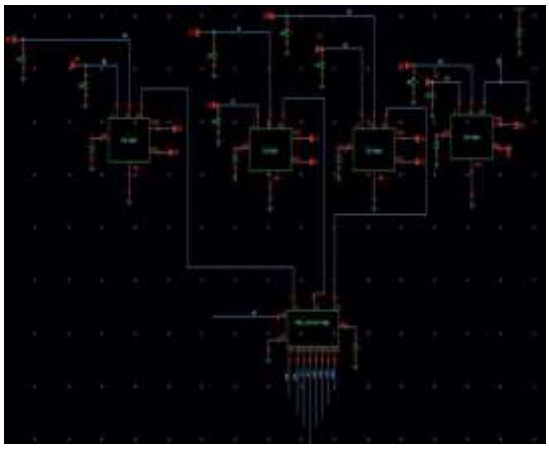

Fig 7. Schematics of Carry Look Ahead (CLA) Logic Circuit

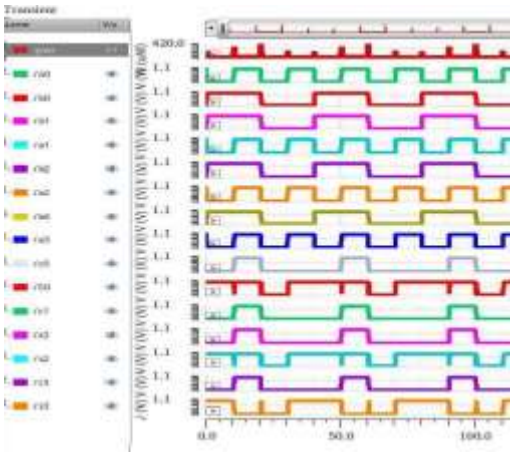

Fig 8. Wave forms of Carry Look Ahead (CLA)

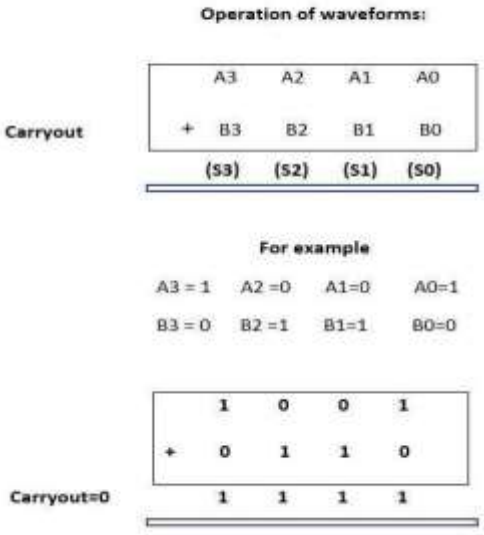

Fig 9 : Operations of Waveforms

V. PROPOSED CALCULATIONS

TABLE I. CARRY LOOK AHEAD ADDER(CLA)

Parameters	Results
Power	1.26uW
Delay	51.6ps
Power Delay Product	$65.01x10^{-18}$

TABLE II. FULL ADDER USING 28 TRANSISTORS

Parameters	Results
Power	442nW
Delay	171ps
Power Delay Product	$31.3x10^{-13}$

TABLE III. FULL ADDER USING 13 TRANSISTORS

Parameters	Results
Power	523uW
Delay	130ps
Power Delay Product	$6.79x10^{-11}$

TABLE IV. FULL ADDER USING 10 TRANSISTORS

Parameters	Results
Power	162uW
Delay	51.3ps
Power Delay Product	$8.31x10^{-13}$

TABLE V. HYBRID ONE BIT FULL ADDER

Parameters	Results
Power	400nW
Delay	5ps
Power Delay Product	$2.11x10^{-15}$

TABLE VI. RCA USING HYBRID ONE BIT FULL ADDER

Parameters	Results
Power	13.8uW
Delay	100ps
Power Delay Product	$13.8x_{10^{-13}}$

VI. CONCLUSIONS

The design of Carry look Ahead adder (CLA) was designed and implemented in cadence virtuoso tool in 90nm technology and simulated with 1.0v power supply ,the main moto of this design of Carry look Ahead adder(CLA) is to analyze and understand the performance metrics by comparative study of adders with different design styles or different logic styles like full adder using 28 transistors, full adder using 13 transistors, full adder using 10 transistors, 1 bit hybrid full adder and Ripple carry adder using 1 bit hybrid full adder. Also calculated power, delay and power delay product for all the above designs, hence the power, delay and power delay product are very less for carry look ahead adder.

VII. REFERENCES

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