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FPGA IMPLEMENTATION OF HYBRID ADDER

K. Bala Sindhuri
G. Challa Ram[1]
M. Venkata Subbarao
M. Aravind kumar
B. Kalivaraprasad
P.S. Brahmanandam

A B S T R A C T

In applications of Digital Electronics, the primary aim is precision, emphasizing accurate outcomes while concurrently minimizing power dissipation and latency. This precision is especially crucial in arithmetic operations, notably addition and multiplication, where the critical path plays a substantial role in influencing the delay of electronic devices. To enhance the speed of these operations, various adder architectures such as Linear Carry Select Adder (CSELA), Square Root CSELA (SQRT CSELA), Ling, Hancarlson, and Weinberger adders are surveyed. This survey serves as motivation for the development of a hybrid adder, which combines different addition techniques to optimize the speed of addition. The proposed hybrid adder architecture is synthesized and simulated using the Xilinx Vivado 2017.2 ISIM tool, with subsequent hardware implementation on the Zedboard. Experimental findings indicate that the introduced hybrid adder exhibits improved speed compared to other conventional adders.

1. INTRODUCTION

The fundamental building block extensively employed in computer arithmetic, originating from Digital Signal Processing (DSP) Filters to Ultra Low Power Biomedical Frequency Low Pass Filters, is the binary adder (Anil Kumar et al., 2023) The Ripple Carry Adder (RCA) (Koyada et al., 2017) is recognized as the most fundamental and straightforward binary adder. Nevertheless, a significant drawback of ripple carry adders lies in their speed dependence on the time needed to propagate a carry throughout the entire adder. Consequently, the Carry Select Adder (CSLA) finds extensive use due to its enhanced computational speed, particularly in integrated systems (Sreevani et al., 2021). CSLA incorporates both adders and multiplexers in its structure. Describing CSLA as an alternative to regular adders, it emphasizes the simultaneous computation of multiple intermediate values, leading to a more rapid addition process. The Carry Select Adder (CSLA), while effective in its function, is noted for its inefficiency in terms of area utilization. This inefficiency arises from the use of multiple Ripple Carry Adder (RCA) pairs, which generate partial sum and carry data by considering carry information. The final sum and carry are then selected using multiplexers (mux) (Balasubramanian and Mastorakis, 2018). To address this issue and

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[1] Corresponding author: G. Challa Ram
  Email: challaram.grandhi@svecw.edu.in

enhance area efficiency while minimizing power consumption, the conventional RCA is replaced with a Binary to Excess-1 Converter (BEC) in the regular CSLA. This substitution achieved a more streamlined and resource-efficient design, optimizing the overall performance of the adder. The integration of a BEC reduced the area usage and power consumption compared to the traditional approach employing multiple RCAs (Gudala et al., 2021; Patil et al., 2015).

Another most precisely used adder is parallel-prefix adder designed for efficient binary number addition. Unlike traditional ripple-carry adders that process carries sequentially, parallel-prefix adders compute carries signals in parallel, thereby decreasing overall delay and enhancing performance. These adders play a crucial role in high-performance computing applications like microprocessors and digital signal processors, where rapid arithmetic operations are indispensable. They bring advantages in terms of speed, efficiency, and reduced carry propagation delay when compared to conventional adders such as ripple-carry adders. The selection of a specific parallel-prefix adder depends on the application's needs and the desired trade-offs between speed, area, and power efficiency.

The Ling adder (Guo et al., 2023), Han-Carlson adder (Rao et al., 2018), Brent-Kung adder, and Kogge-Stone adder (Penchalaiah and Siva Kumar 2018) belong to the category of parallel-prefix adders, designed to enhance binary addition in digital circuits. The Ling adder utilizes a network of binary full adders and carry-select adders, prioritizing efficiency in terms of speed and minimized carry propagation delay. The Han-Carlson adder excels in high-speed carry propagation through a tree-based structure. The Brent-Kung adder adopts a hierarchical tree structure, emphasizing low fan-out and a balance between speed and area efficiency. In contrast, the Kogge-Stone adder features a balanced binary tree structure, known for its simplicity, regularity, and a well-balanced combination of speed and area efficiency. The Weinberger adder integrates the concept of parallel carry computation (Varshney and Arya 2019), (Gaur et al., 2019) to boost circuit speed. Each adder provides distinct advantages, catering to various preferences in digital circuit design based on specific application requirements (Priya and Kumar 2013). Until now, several adders (Suganya and Meganathan 2015; Thamizharasan and Kasthuri 2021) have been designed to enhance the performance of the adder. This paper introduces a hybrid adder that is meticulously designed by integrating diverse addition techniques, with the goal of improving the speed of the addition process.

In this paper, Section 2 focuses on detailing the design of the proposed VLSI architecture for the adder. Sections 3 and 4 delve into the presentation of results, discussions, and conclusions.

2. PROPOSED HYBRID ADDER

Designing an energy-efficient hybrid adder involves integrating basic components like Half Adder and Full Adder, Ripple Carry Adder and the latest adders exploring low-power adder designs, and optimizing with techniques such as clock gating, power gating, and pipeline staging. The choice of semiconductor technology and dynamic voltage scaling are critical, and parallelism, bit-level optimizations, and data-dependent power management contribute to efficiency. Considering error tolerance and employing simulation tools for power analysis are essential, followed by rigorous testing and continuous optimization based on real-world performance feedback. The proposed hybrid adder is designed based on Power efficient adders such as different adders such as Hancarlson Adder (Lakshmanan et al., 2006), Ling and Weinberger adder (Sudhakar et al., 2012) at different stages (Ram et al., 2023), (Raju et al., 2023). Considering the major constraints, architecture of the 16-bit hybrid adder is proposed which is depicted in Figure1, is built upon the SQRT CSELA architecture and is organized into five distinct groups, each with a designated function in the addition process:

First and Second Groups:

The inputs for these groups encompass bits 0-1, a carry input (cin), and bits 2-3. Utilizing 2-bit Ripple Carry Adders (RCA), these groups perform the addition operation on their respective inputs.

Third Group:

Comprising a 3-bit Weinberger adder, a Binary to Excess-1 Converter (BEC) for input carry 'one' to reduce the area and a Multiplexer (MUX) unit to select the final output. Responsible for handling inputs from bits 4-6, the MUX unit selects the output from either the Weinberger adder or the BEC based on the specific requirements of the addition process.

Fourth Group:

Similar to the third group in structure, with a 4-bit Hancarlson adder replacing the Weinberger adder. This group is designed to add inputs from bits 7-10.

Fifth Group:

Resembling the structure of the third and fourth groups, the fifth group integrates a 5-bit Ling adder, a Binary to Excess-1 Converter (BEC) for input carry 'one' to reduce the area and a Multiplexer (MUX) unit to select the final output. It is specifically configured to add inputs from bits 11-15.
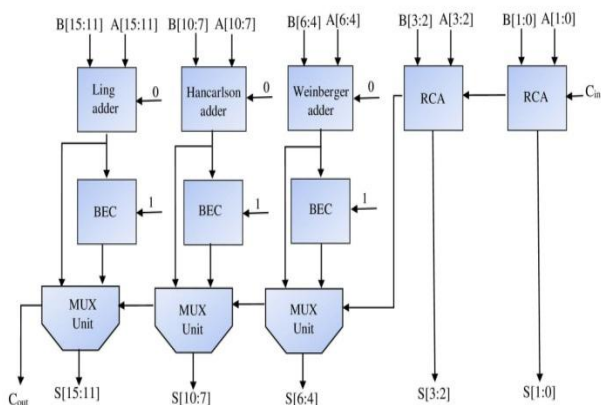
Figure 1. Architecture of Proposed 16-bit Hybrid Adder

In summary, the hybrid adder employs a combination of various adder types, including 2-bit RCA, 3-bit Weinberger, 4-bit Hancarlson, and 5-bit Ling adders. Each group is strategically designed to handle a specific range of input bits, optimizing the addition process for different segments of the 16-bit input (Parvathi 2020). This approach is intended to enhance efficiency and speed in binary addition within the context of a 16-bit computational system.

3. ANALYSIS OF ADDER ARCHITECTURE USING THEORITICAL APPROACH

The analysis of the various adder architectures using a theoretical approach is tabulated in Table1 which involves assessing the estimated delay and area metrics provided for each design. Here's a summary of the analysis based on the theoretical approach:

i. **Ripple Carry Adder (RCA):**
High delay may become impractical for large bit-widths due to carry propagation.

ii. **Linear CSELA:**
Speed is improved compared to RCA due to parallelism. The area is higher than RCA due to additional components.

iii. **Modified Linear CSELA:**
Slight reduction in area compared to Linear CSELA due to incorporation of BEC.

iv. **SQRT CSELA:**
Improved performance in terms of area and delay compared to Linear CSELA.

v. **Modified SQRT CSELA with BEC:**
Similar to SQRT CSELA, potentially modified for optimizations which balances delay and area considerations.

vi. **Ling Based Linear CSELA:**
Incorporates Ling adder for potentially faster linear

addition with moderate increase compared to Linear CSELA.

vii. **Ling Based SQRT CSELA:**
Utilizes Ling adder in square root carry select architecture with balanced approach between delay and area.

viii. **Hancarlson Based Linear CSELA:**
Utilizes Hancarlson adder for potential improvement in linear addition. With slight increase in area due to additional components.

ix. **Hancarlson Based SQRT CSELA:**
Utilizes Hancarlson adder in square root carry select architecture aims for a balance between delay reduction and moderate area increase.

x. **Weinberger Based Linear CSELA:**
Incorporates Weinberger adder for linear addition with relatively higher area due to additional components.

xi. **Weinberger Based SQRT CSELA:**
Uses Weinberger adder in square root carry select architecture for Potential trade-off between delay, area, and additional features.

The Proposed Hybrid Adder aims for a balance between delay reduction and moderate area increase.

Table. 1. Theoretical Delay and Area of Adders

Adder	Theoretical Delay	Theoretical Area
Ripple Carry Adder (RCA)	$T_{XOR} + 30T_{OR} + 15T_{AND}$	$32A_{XOR} + 48A_{AND} + 32A_{OR}$
Linear CSELA	$3T_{MUX} + 4T_{AND} + 8T_{OR}$	$15A_{MUX} + 47A_{XOR} + 3A_{XNOR} + 69A_{AND} + 47A_{OR}$
Modified Linear CSELA	$3T_{MUX} + 2T_{XOR} + 4T_{AND} + 5T_{OR}$	$15A_{MUX} + 38A_{XOR} + 51A_{AND} + 29A_{OR} + 3A_{NOT}$
SQRT CSELA	$T_{MUX} + 2T_{XOR} + 4T_{AND} + 6T_{OR}$	$18A_{MUX} + 48A_{XOR} + 4A_{XNOR} + 70A_{AND} + 48A_{OR}$
Modified SQRT CSELA	$T_{MUX} + 3T_{XOR} + 4T_{AND} + 6T_{OR}$	$18A_{MUX} + 38A_{XOR} + 50A_{AND} + 28A_{OR} + 4A_{NOT}$
Ling Based Linear CSELA	$4T_{MUX} + 2T_{XOR} + 4T_{AND} + T_{OR}$	$25A_{MUX} + 38A_{XOR} + 50A_{AND} + 45A_{OR} + 3A_{NOT}$
Ling Based SQRT CSELA	$3T_{MUX} + 2T_{XOR} + T_{AND} + T_{OR}$	$26A_{MUX} + 38A_{XOR} + 48A_{AND} + 43A_{OR} + 4A_{NOT}$

Hancarlson Based Linear CSELA	$3T_{MUX} + 2T_{XOR} + 3T_{AND} + 3T_{OR}$	$15A_{MUX} + 38A_{XOR} + 58A_{AND} + 20A_{OR} + 3A_{NOT}$
Hancarlson Based SQRT CSELA	$4T_{MUX} + 2T_{XOR} + T_{AND} + T_{OR}$	$18A_{MUX} + 38A_{XOR} + 53A_{AND} + 18A_{OR} + 4A_{NOT}$
Weinberger Based Linear CSELA	$4T_{MUX} + 2T_{XOR} + 2T_{AND} + T_{OR}$	$33A_{MUX} + 33A_{XOR} + 14A_{AND} + 8A_{OR} + 20A_{NAND} + 24A_{NOR} + 3A_{NOT}$
Weinberger Based SQRT CSELA	$5T_{MUX} + T_{XOR} + T_{AND} + T_{OR} + T_{NOT}$	$33A_{MUX} + 32A_{XOR} + 16A_{AND} + 10A_{OR} + 17A_{NAND} + 18A_{NOR} + 41A_{NOT}$
Proposed Hybrid adder	$3T_{MUX} + 4T_{AND} + 5T_{OR}$	$20A_{MUX} + 37A_{XOR} + 50A_{AND} + 31A_{OR} + 3A_{NAND} + 3A_{NOR} + 8A_{NOT}$

4. PERFORMANCE ANALYSIS OF SENSOR

The Table 2 provides a comparison of different adder designs based on LUT count and power consumption. The proposed hybrid adder seems to have relatively lower power consumption (11.532W) compared to some other designs.

Table. 2. Practical Comparative analysis of Power, LUT'S for various adders.

Adder	LUTs	Power(W)
Ripple Carry Adder (RCA)	16	11.014
Linear CSELA	30	11.615
Modified Linear CSELA	28	11.644
SQRT CSELA	33	12.017
Modified SQRT CSELA	36	11.680
Ling Based Linear CSELA	29	11.629
Ling Based SQRT CSELA	30	11.400
Hancarlson Based Linear CSELA	29	11.659
Hancarlson Based SQRT CSELA	32	11.683
Weinberger Based Linear CSELA	28	11.553
Weinberger Based SQRT CSELA	33	11.634
Proposed Hybrid adder	29	11.532

From Table 3, the proposed hybrid adder outperforms the other designs in terms of setup delay, hold delay, and PDP, indicating superior performance and energy efficiency. Lower setup and hold delays suggest faster and more stable operation. The lower PDP for

the proposed hybrid adder implies a more efficient use of power resources compared to the other adders in the list. In practical terms, the proposed hybrid adder seems to be a promising design if the goal is to achieve a balance between speed and power efficiency in adder circuits.

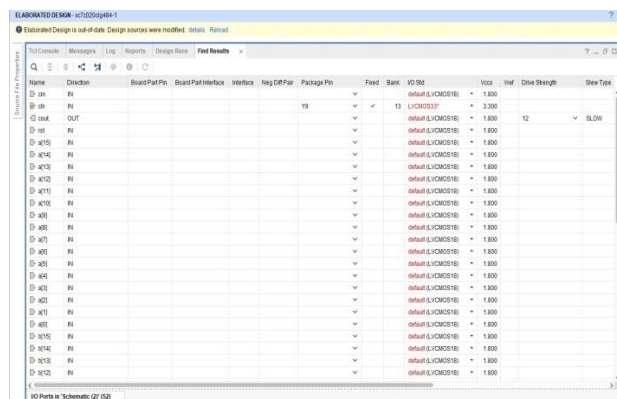**Table. 3.** Practical Comparative analysis of Delay and PDP for various adders.

Adder	Setup Delay(ns)	Hold Delay(ns)	PDP
Ripple Carry Adder (RCA)	11.359	2.448	125.108
Linear CSELA	9.662	2.511	112.224
Modified Linear CSELA	10.144	2.498	118.117
SQRT CSELA	9.339	2.511	112.227
Modified SQRT CSELA	9.227	2.417	107.771
Ling Based Linear CSELA	9.997	2.474	116.255
Ling Based SQRT CSELA	9.987	2.477	113.852
Hancarlson Based Linear CSELA	10.140	2.514	118.222
Hancarlson Based SQRT CSELA	9.222	2.484	107.741
Weinberger Based Linear CSELA	10.166	2.496	117.448
Weinberger Based SQRT CSELA	9.230	2.512	107.382
Proposed Hybrid adder	9.096	2.467	104.895

5. HARDWARE IMPLEMENTATION

The process of implementing and validating a hybrid adder design is outlined with meticulous detail, involving the use of Verilog Hardware Description Language (HDL) and the Vivado 2017.2 toolset. Simulation is conducted using Vivado ISIM, and synthesis takes place on a system equipped with an INTEL Core i5 processor boasting a 64-bit operating system, 16GB of RAM, and a clock frequency of 2.50GHz.

For the validation of the proposed design on the ZedBoard Zynq Evaluation and Development Kit (xc7z020clg484-1), crucial components from the IP Catalog, namely the Virtual Input Output (VIO) and Integrated Logic Analyzer (ILA) packages, are employed. The VIO package plays a pivotal role in configuring inputs and outputs, establishing a virtual environment conducive to configuration. On the other hand, the ILA package designates all probes as inputs, facilitating the capture and subsequent analysis of internal signals within the adder during the verification process.

The ZedBoard is selected as a robust platform for the implementation and validation of the hybrid adder design. Leveraging the VIO and ILA packages enhances the verification process by providing the capability to analyze input-output relationships and internal signals that are critical for the proper functioning of the adder. In the implementation phase, a Verilog file undergoes meticulous creation and modification for the purpose of port mapping. This involves the selection of the clock pin as a Y9 package pin, with I/O standards set to LVCMOS33 as shown in Figure 2.

Figure 2. Clock pin selection

Successful Bitstream generation follows this stage. The ZedBoard is then powered on, and the connection is established through hardware management. The implemented hybrid adder architecture is visually represented in Fig. 3.
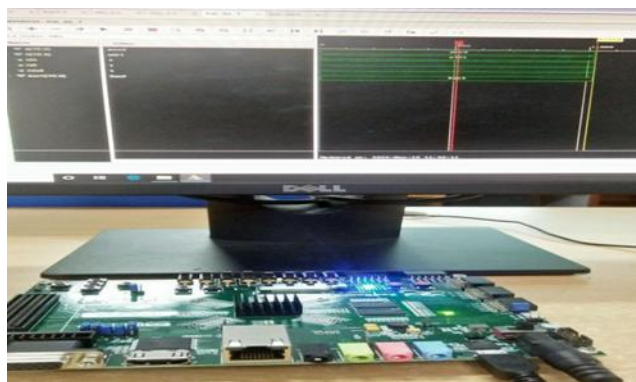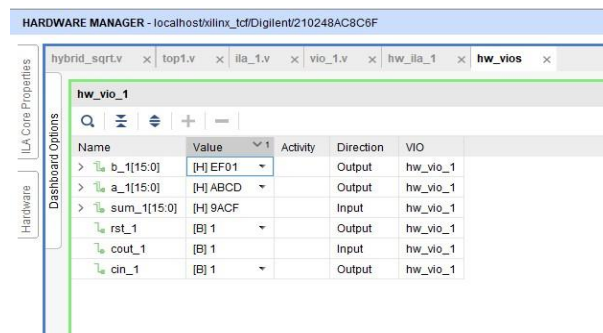
Figure 3. Implementation of hybrid adder on Zedboard

Figure 4. Hardware manager to provide inputs

Subsequently, in Fig. 4, all pins are selected, inputs are modified, and the run trigger is activated, leading to the presentation of simulation results in Fig. 3. This comprehensive process ensures a thorough evaluation and validation of the proposed hybrid adder design.

6. CONCLUSION

In this research, an energy-efficient hybrid adder is proposed, designed utilizing Ling, Hancarlson, Weinberger Adders, and BEC Circuit. The resultant hybrid adder demonstrates reduced delay and power delay product. The architecture of the hybrid adder is synthesized and simulated using Xilinx Vivado 2017.2 isim tool, with subsequent hardware implementation on zedboard. Experimental results reveal a speed enhancement of 19.92%, 5.86%, 10.33%, 2.60%, 1.42%, 9.01%, 8.92%, 10.29%, 1.37%, 10.52%, and 1.45% when compared To Ripple Carry Adder, Linear Csela, Modified Linear CSELA, SQRT CSELA, Modified SQRT CSELA, Ling-Based Linear CSELA, Ling-Based SQRT CSELA, Hancarlson-Based Linear CSELA, Hancarlson-Based SQRT CSELA, Weinberger-Based Linear CSELA, And Weinberger-Based SQRT CSELA respectively.

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K. Bala Sindhuri
Department of ECE
S. R. K. R Engineering College,
Bhimavaram, India.
kbsindhuri@srkrec.ac.in
ORCID 0000-0001-7892-2062

M. Aravind kumar
Department of ECE,
West Godavari Institute of Science
and Engineering,
Tadepalligudem,India.
drmaravindkumar@gmail.com
ORCID 0000-0003-4718-5738

G. Challa Ram
Department of ECE
Shri Vishnu Engineering College for
Women, Bhimavaram, India.
challaram.grandhi@svecw.edu.in
ORCID 0000-0002-3790-1318

B. Kalivaraprasad
Department of ECE,
Koneru Lakshmaiah Education
Foundation (KLEF),Vaddeswaram,
India
baditakali@gmail.com
ORCID 0000-0001-7817-2062

M. Venkata Subbarao
Department of ECE,
Shri Vishnu Engineering College for
Women, Bhimavaram, India.
mvsubbarao@svecw.edu.in
ORCID 0000-0001-5840-2190

P.S. Brahmanandam
Dept . of Physics,
Shri Vishnu Engineering College for
Women, Bhimavaram, India
dranandpotula@svecw.edu.in
ORCID 0000-0001-9777-3496