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COEN 21 Lab

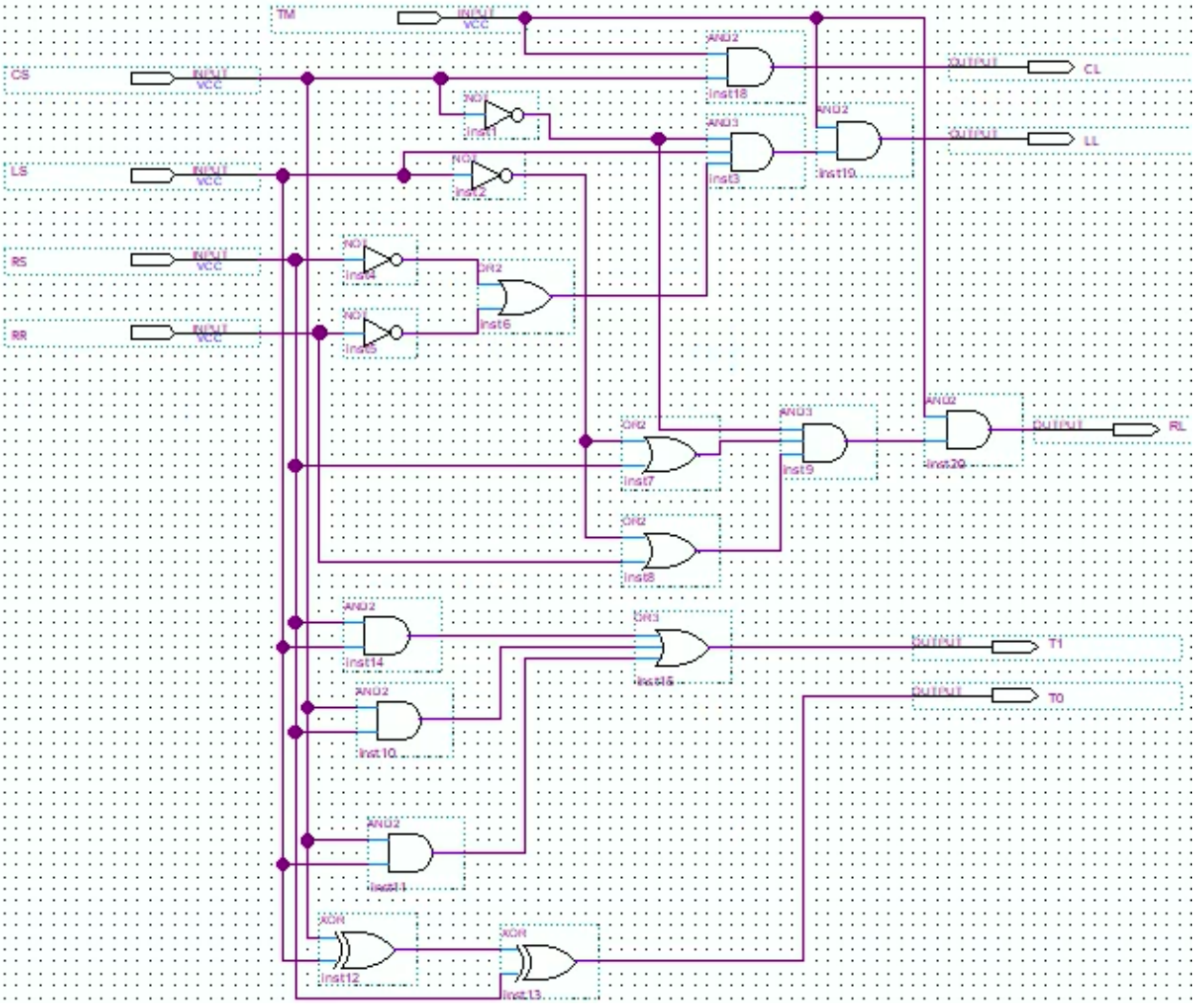
Lab 3

We designed a highway entrance ramp light system that controlled which lights were enabled at different times according to the requirements specified. There were four controller inputs: CS, LS, RS, and RR detecting if a car is present. There were also three controller outputs: CL, LL, and RL that indicated the lights lit up on the different lanes. There were also 7 controller specifications:

1. If there is a car in the carpool lane, CL is 1.
2. If there are no cars in the carpool lane and the right lane, and there is a car in the left lane, LL is 1.
3. If there are no cars in the carpool lane and in the left lane, and there is a car in the right lane, RL is 1.
4. If there is no car in the carpool lane and there are no cars in the left and right lanes, then RL is 1.
5. If there is no car in the carpool lane, there are cars in both the left and right lanes, and RR is 0, then LL = 1.
6. If there is no car in the carpool lane, there are cars in both the left and right lanes, and RR is 1, then RL is 1.
7. If any of CL, LL, or RL is not specified to be 1 in conditions 1 to 6 above, then it has value 0 for that condition.

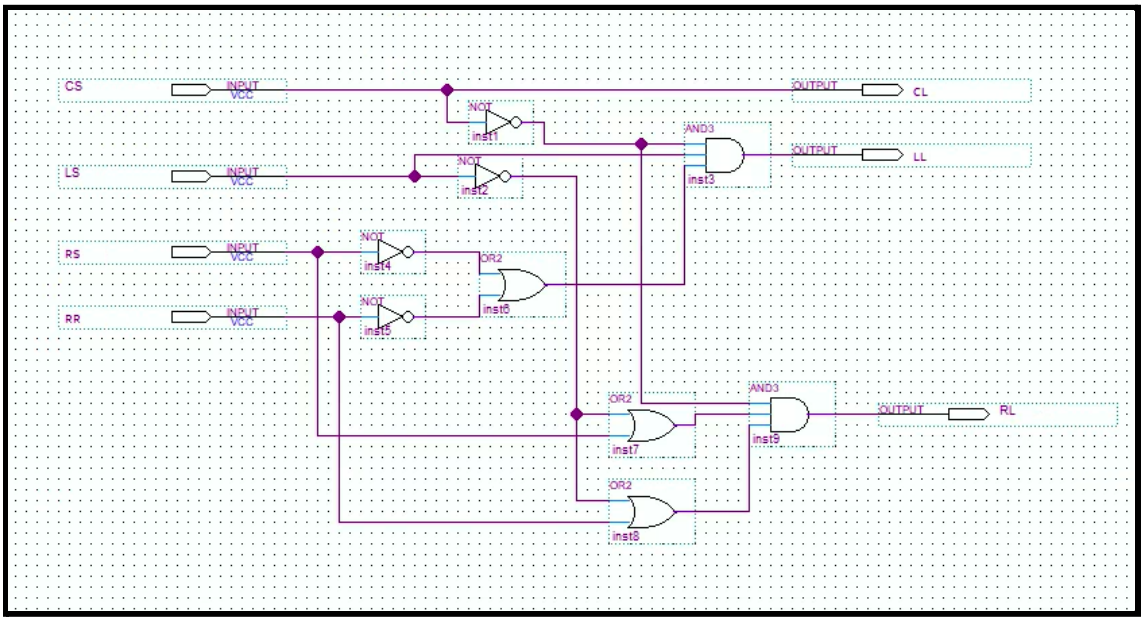
In order to design this circuit, we created a truth table with all of the inputs and outputs and then drew K-maps to get the SOP and POS form for all of the outputs. We then realized that the POS form for all of the outputs was the lowest cost so we chose that for all three outputs. After compiling the circuit, we started the simulation and compared values of the original outputs with the truth table to see if our logic was correct. We only had an error in the simulation diagram because our outputs were ordered wrong so they didn't quite match up with our truth table. This was easily fixed by reordering the outputs. We think this simulation strategy detected all design errors because it matched every output on the diagram with the truth table we created before the lab started.

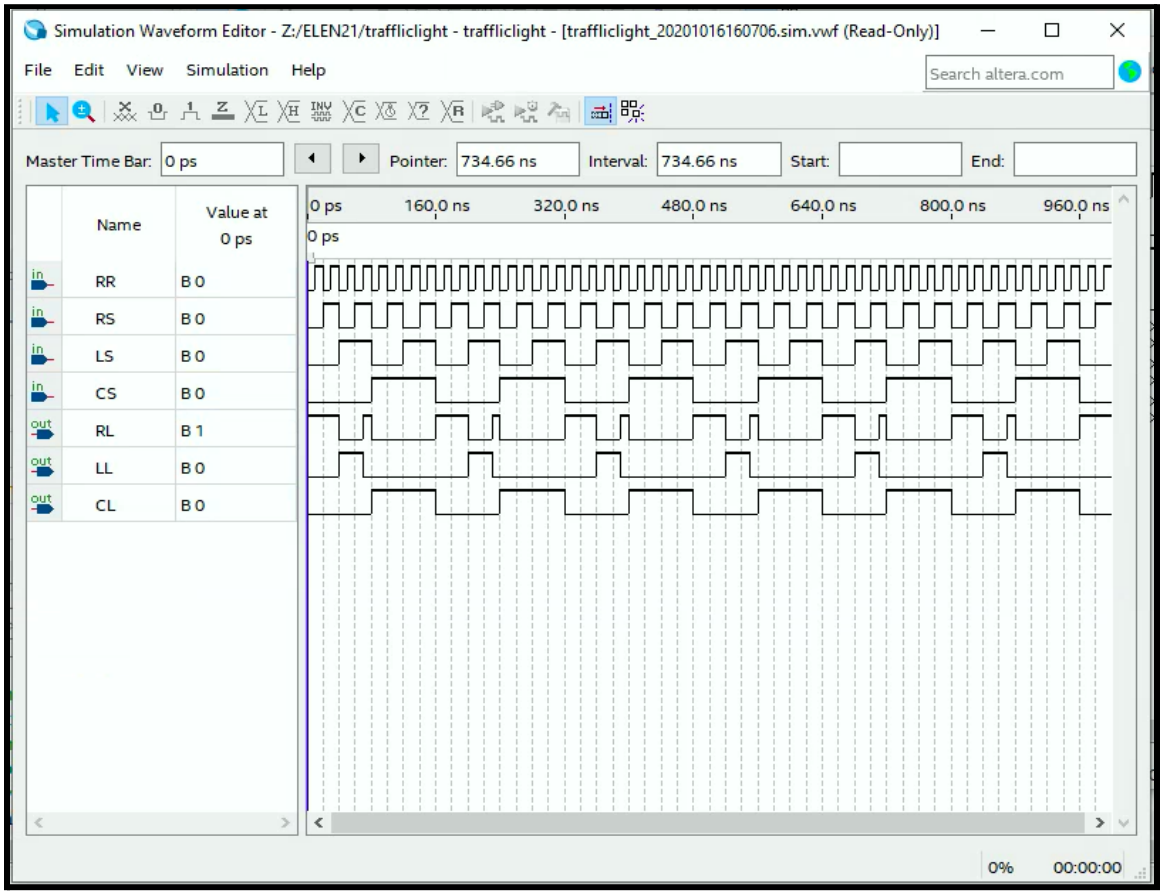
In order to add ERR1 we would use the same logic as T1 with the And and Or gates to see if two or more sensors are on at the same time. The outputs on the truth table for ERR1 will be the same as T1. Modifying the circuit, we would AND the new fifth input, TM, with every original output: CL, LL, RL. One possible strategy to implement in order to prevent a blockage of cars in the non-carpool lanes is to alternate between LS and RS for every 2 CS. This will ensure that the carpool lane still has priority but there will not be a blockage in the non-carpool lanes.



Additional TM input

Basic Circuit in POS form





Extended Circuit with T1 and T0 outputs