Jason Vu
COEN 21 Lab

Introduction:

In this lab, we model some functionality used in a simple game to test an individual's physical reactions. By using two counters that'll move in opposite directions - one counting up and one counting down - we'll imagine that there is a scoreboard that the person views during gameplay. We'll make a Start button when the button is pressed to start the counters. Also, we'll make a Stop button , which simulates when a user releases the button to stop the counters from counting and generate results as follows:

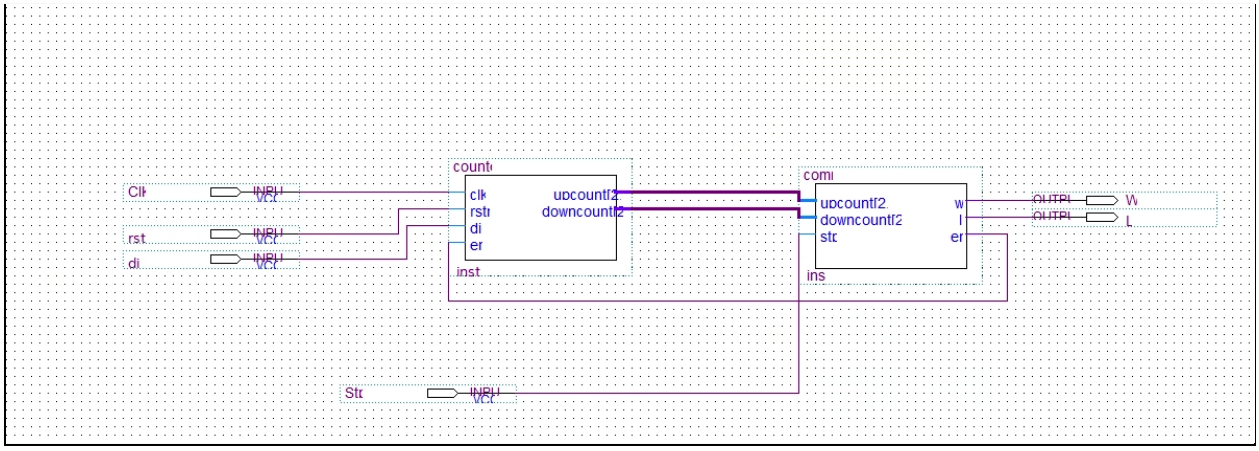
- “win” signal is asserted if the two counter values match when Stop is asserted.
- A “lose” signal is asserted if the two counter values do not match when Stop is asserted.
- While Stop is not asserted, and the counters are counting, neither the “win” nor the “lose”signal is asserted.

Though the game simulation could allow the use of increasing speed to further the difficulty, we won’t be concerned about the speed of the circuit’s runtime.

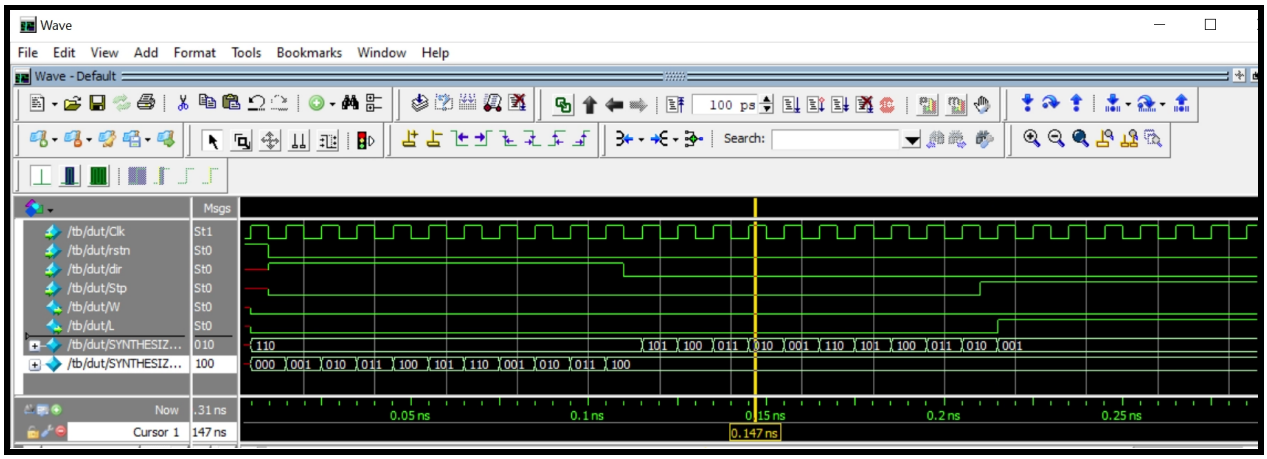
Verilog Code:

Verilog Code
Here is the Verilog code which is pasted in here.

Design Schematics:



Waveform:



Questions:

If you were to change your design to have the counters count from 1 to 8 (or 8 to 1) instead of only 1 to 6, list all the things you would need to change.

- It will need 4 bits to count to 8 meaning you need a wider bus
- Verilog needs to be changed so that it counts to 8 in binary instead of 6
- Edit the stop to stop at 8 so the counter won't count past that number.

Conclusion:

- By using the testbench module, we were able to generate the clock and reset signals and control the value of the Stop signal over time. By testing our design, we were able to verify that the counters stop counting when Stop is asserted and vice versa. Also, we made sure that both counters cycled through the correct values in opposite positions. Thus, this allows us to confirm whether the win or lose outputs work properly as expected.

Stop = 0, and once we go down, it'll stop counting and then the Lose asserts

The Lose signal turns on because the counters cycle and determines the downcount 1 .

WIn-Lose module is a game of some sort. When Stop is asserted and two counters match, we lose the game. Otherwise, we keep winning for the time being.