CS 343, SPRING2019

Laboratory Exercise: Simple Circuit Design and Testing (REVIEW, TUTORIAL)

Instructor: Professor Izidor Gertner
Due February 20,2019 by 12:00 PM

Objective:

This introductory lab allows you to apply everything you learned about Quartus II in the tutorials. You will build a circuit, verify correctness using waveform simulation. Write a testbench file in VHDL to test the correctness of your design. In addition, you will also have to use Quartus Library of Parameterized Modules and compare the functional performance with your own design.

This lab consists of 6 parts:
Part 1: Please describe a simple digital circuit from AND, OR and NOT gate primitives using VHDL, and verify its correctness in simulation using waveforms (i.e. compare simulation results with TRUTH table specification).
Part 2: Please describe a digital circuit for 2-to-1 multiplexer using gate primitive functions using VHDL.
Part 3: Please describe the same multiplexer (described in Part 2) in VHDL using the Library of Parameterized Modules (LPM) available within Quartus to create circuits using the MegaWizard Plug-In Manager.
Part4 : Please write testbench file in VHDL to test designs in Part 2 and Part 3.
Part 5: Please repeat Part 2, Part 3, Part 4 using VHDL for:

- 1 bit half adder
- 1 bit Full adder using 1 bit half adder as a component
- 3 to 8 Decoder
- 8 to 3 Encoder

Part 6: Create Lab report – and 2 min video showing your design and verification in simulation using waveforms.

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PART 1: A Simple Circuit

Before you begin, you should already be familiar with circuit design creation by adding gate symbols and input/output pins using block diagram design. You should also know how to create waveform files to simulate your implementations and loading your design onto the DE2 board.

YOUR TASK

1. WE show you how to design digital circuit using schematic capture.
2. You have to redesign the same circuit using VHDL.

Steps:

1. Open Quartus and create a new project. Call it lab1part1.
   When creating your projects, remember to always use the following settings:
   Device family: **Cyclone II**
   Available devices: **EP2C35F672C6**
   EDA Tool Settings: Set everything to **None**

2. Go to **File > New**, then create a new Block Diagram/Schematic file. Hit **OK**.

3. Design a circuit similar to the one described in the figure 1 below. Add your input pins, call them a and b; add your output pin, call it f.

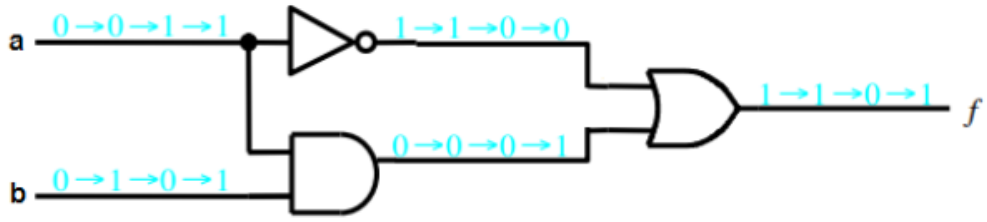

Figure 1. Simple Circuit to be implemented

4. Save your changes. Give your file a meaningful name, you may want to call it **simpleCircuit.bdf**

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5. Create a new waveform simulation file, add your input and output pins. Create your waveforms and check the correctness of the output. You should obtain a waveform similar to figure 2 (Note: When you simulate your circuit, you may obtain your inputs and outputs in a different order from the one shown in the figure, you can just click and drag your pins to reorder).

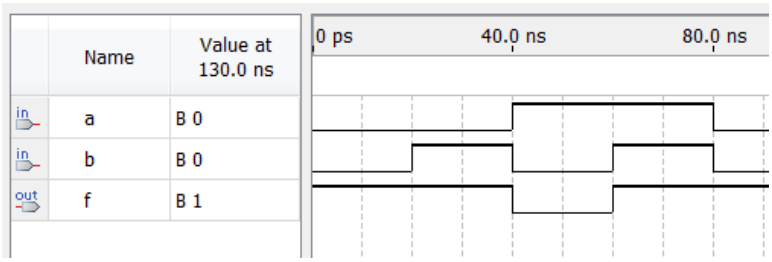

Figure 2. Waveform simulation result for simple circuit.

How do you check for correctness?
From figure 1, see the following sequences:
for input a: 0 -> 0 -> 1 -> 1
for input b: 0 -> 1 -> 0 -> 1
for output f: 1 -> 1 -> 0 -> 1

If you take the first value from each of these sequences (a=0, b=0), you should see the output in f to be equal to 1. Now if you check these values in the waveform of figure 2, you see that for the time period 0ns to 20ns you have a=0 and b=0, which produce the output f=1, as expected.
Check in a similar way for the rest of input combinations, for example when a=0,b=1, then f=1 during time period 20ns to 40ns, etc.

6. Save your files and take screenshots of your circuit and waveform; you will need them for your report.

7. Pin Assignment:
   Click here for pin assignment manual

   Create a new text file to add your pin assignments:
   - a: Assign to SW[0]
   - b: Assign to SW[1]
   - f: Assign to LEDR[0]

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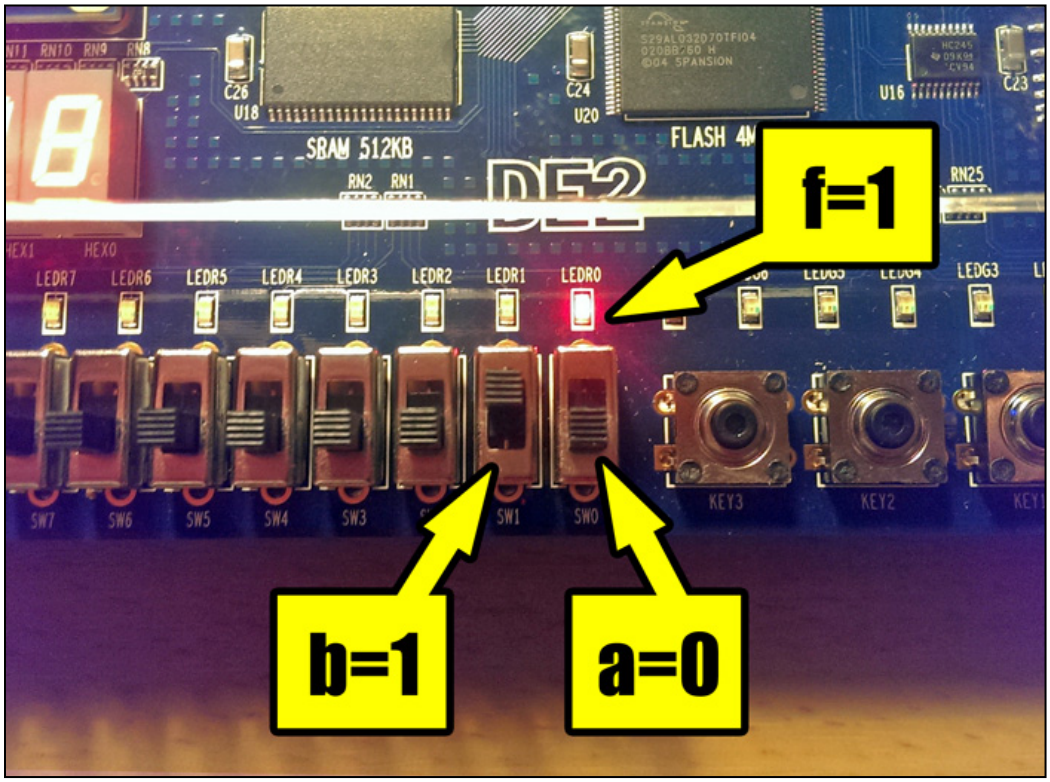
Because this is your very first lab assignment, we will show you how the pin assignment text file should actually look like.
For the remaining parts of this lab and future projects, you should use the pin assignment manual from the link above. For now just copy this assignment onto a text file and import to your project:

To, Location
a, PIN_N25
b, PIN_N26
f, PIN_AE23

8. You should be now ready to load and test this circuit onto DE2 board. Make sure you test all possible cases/combinations for a and b you simulated in your waveform. For example when a=0, b=1, then f=1, this is exemplified in the picture below:



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PART 2: 2-to-1 Multiplexer

YOUR TASK

1. WE show you how to design digital circuit using schematic capture.
2. You have to redesign the same circuit using VHDL.

Figure 3 shows a digital circuit that implements a 2-to-1 multiplexer (generally abbreviated as MUX) with select input ***s***. If ***s=0***, then the output ***m*** of the multiplexer is equal to whatever value is passed by the input ***x***. Conversely, if ***s=1***, then the value of output ***m*** of the multiplexer is equal to the value of ***y***. Figure 4 gives the truth table for this multiplexer and figure 5 shows the circuit symbol.

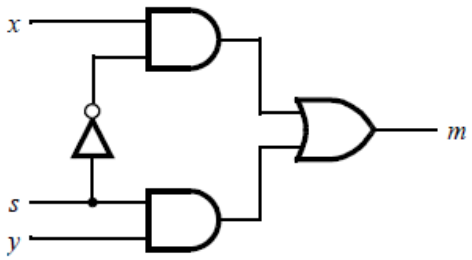

Figure 3. The 2-to-1 multiplexer circuit design

s	*m*
0	*x*
1	*y*

Figure 4. The 2-to-1 multiplexer's truth table

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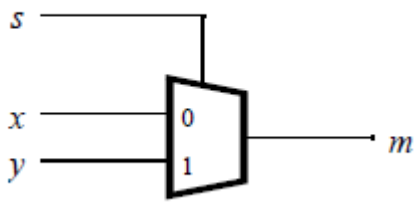

Figure 5. Multiplexer circuit symbol

YOUR TASK

1. Create a new project. Call it ***lab1part2***.

2. Create a new Block Diagram/Schematic file. Call it ***mux2to1.bdf***. Design your circuit following the representation of the multiplexer shown in figure 3. Give your circuit input and output pins and name them accordingly (x, y, s and m). Note: If you need to rotate a symbol, just right click it and choose **Rotate by Degrees**.

3. Set this circuit as your Top Level Entity and compile.

4. Create a new simulation file. Simulate and verify the correctness of your digital circuit. A resulting waveform is shown in figure 6.

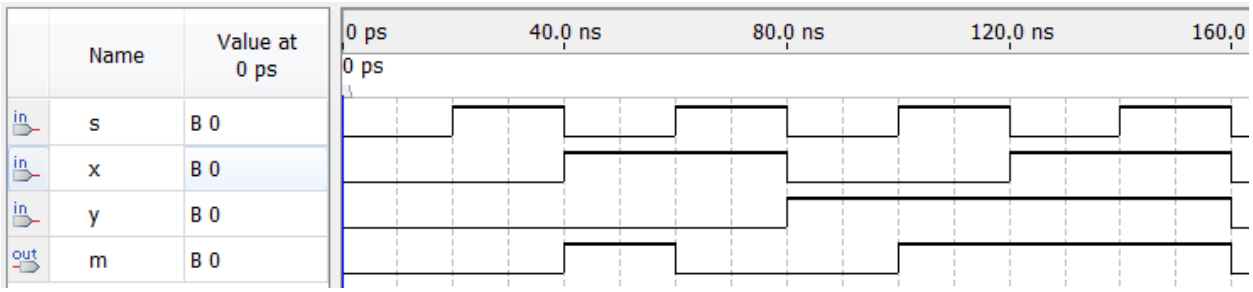

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Figure 6. Output Waveform for 2-to-1 multiplexer

How do we check the correctness of our multiplexer?
Remember that when s=0, then the output m should reflect the value of x and when s=1, then m should reflect whatever value is in y. Let's check some cases using figure 6:

- For the time period 40ns to 60ns:
  The value of s=0, so we should see the value of x passed down to m. This is correct, we see that during this time period x=1, and then output m=1.

- For the time period 60ns to 80ns:
  The value of s=1, so we should see the value of y passed down to m. This is correct, we see that during this time period y=0, and then output m=0.

5. Save your files and take screenshots of your circuit and waveform; you will need them for your report.

6. Pin Assignment:
   Click here for pin assignment manual

   Create a new text file to add your pin assignments:

   x: Assign to SW[0]
   y: Assign to SW[1]
   s: Assign to SW[2]
   m: Assign to LEDR[0]

7. You should be now ready to load and test this circuit onto DE2 board. The behavior should reflect the truth table of figure 4 and the results obtained in the waveform of figure 6.

   Two examples of circuit behavior are described below:

- The following picture shows the behavior of the multiplexer when s=1, meaning that it should take whatever value is stored in y. Since y=1, then output m will also be 1, therefore the light of the LED[0] will be on.

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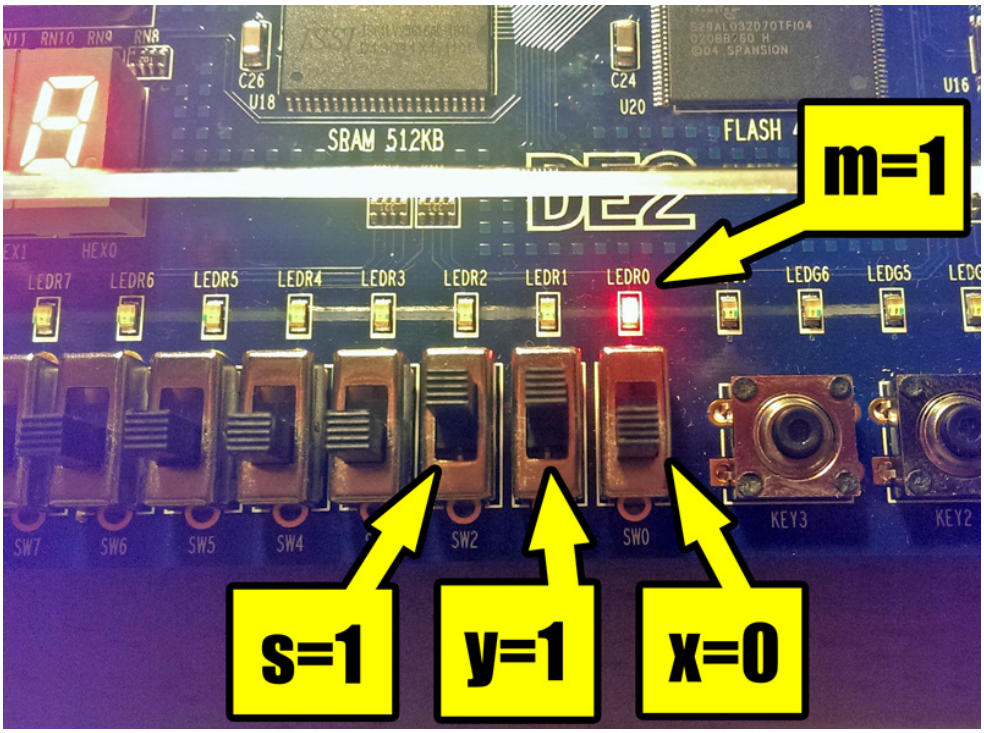

Figure 7. Sample behavior of 2-to-1 multiplexer from part2

- The following picture shows the behavior of the multiplexer when s=0, meaning that it should take whatever value is stored in x (regardless of the value in y). Since x=0, then output m will also be 0, therefore the light of the LED[0] will be off.

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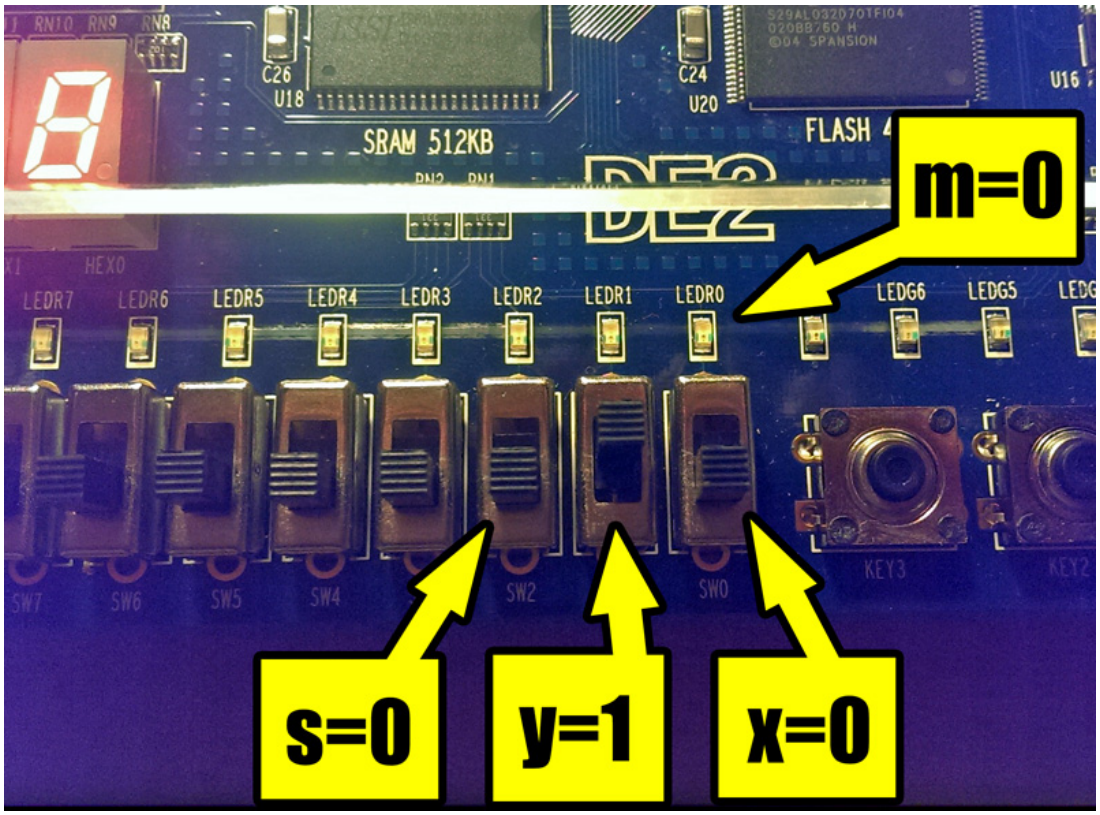

Figure 8. Sample behavior of 2-to-1 multiplexer from part2

PART 3: 2-to-1 Multiplexer using LPM

YOUR TASK

1. WE show you how to design digital circuit using schematic capture.
2. You have to redesign the same circuit using VHDL.

When you design your circuits, you will realize that there are certain circuit blocks that you need to use over and over, such as adders, subtractors, multipliers, decoders, shifters, and counters. To save you time, these blocks are provided by Altera in the form of library modules that can be inserted into your

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Verilog designs. In Quartus, this library of modules is referred to as LPM (Library of parameterized modules).

For this part, we will implement the same 2-to1 multiplexer you designed in part2; however, this time we will implement it from the MegaWizard Plug-In available in Quartus.

YOUR TASK

1. Create a new project. Call it **lab1part3**.

2. Go to **Tools > MegaWizard Plug-In Manager**

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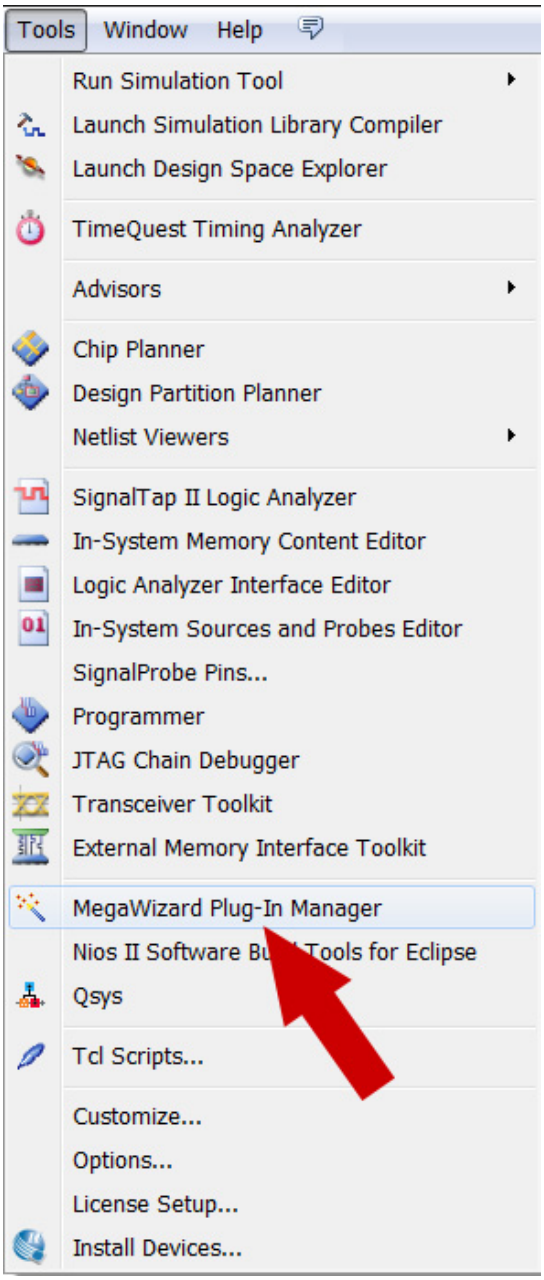

3. The following screen shows up. Click **Next**

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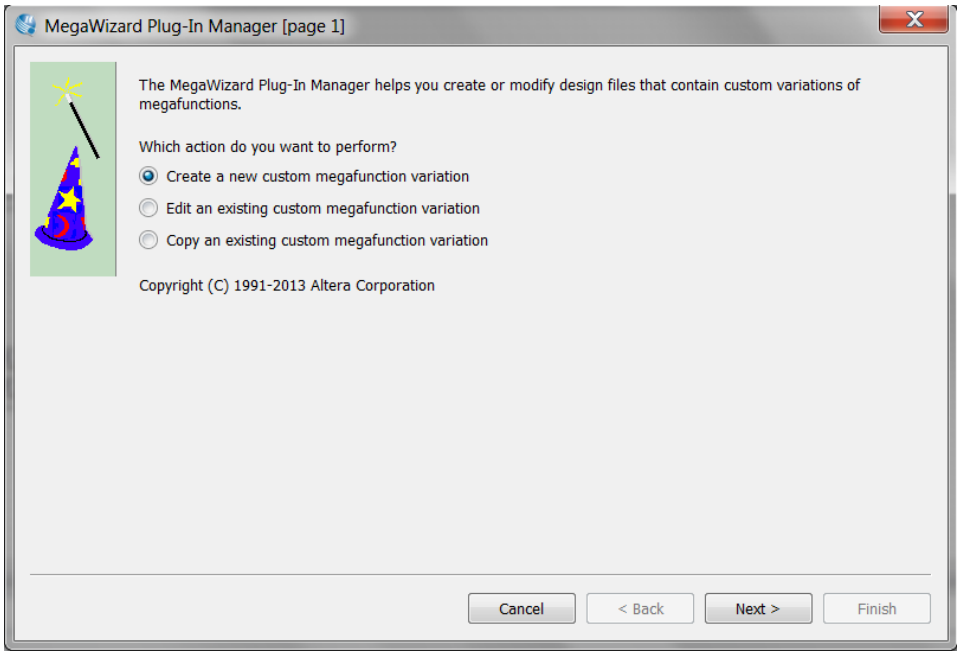

4. In the screen that appears, browse for LPM_MUX under the Gates folder. Alternatively, you can also type “mux” in the search box on the left, as shown in the figure below. Now click to select LPM_MUX. Then on the right give a name to the output file, you might want to call it muxLPM or something similar. Click **Next**

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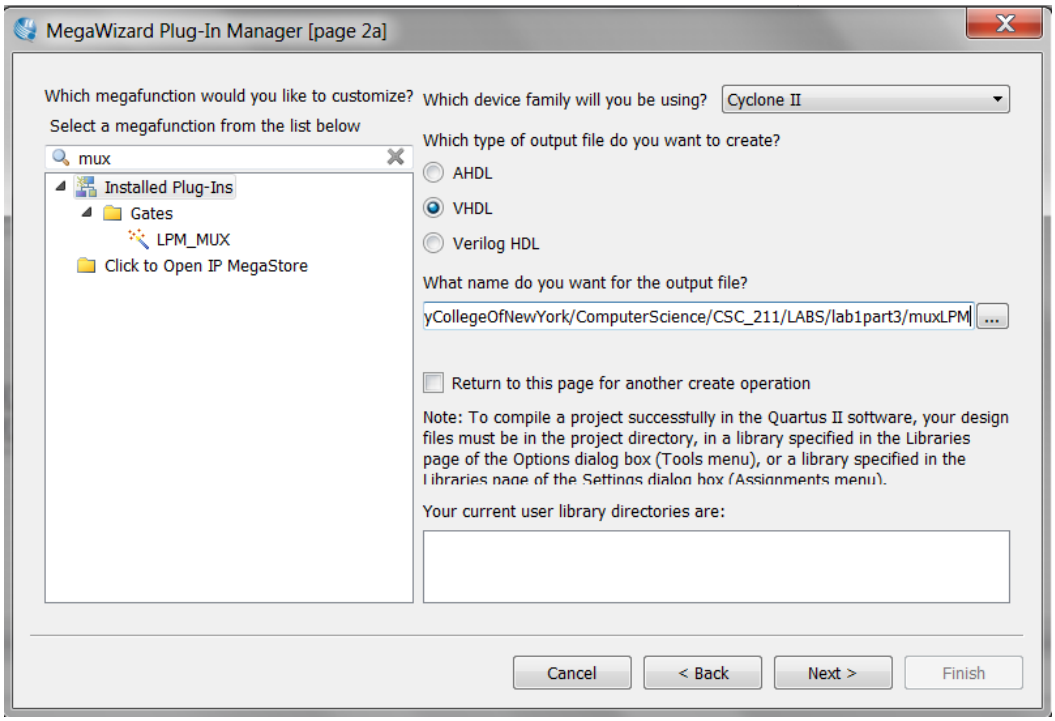

5. In the next screen make sure that you specify 2 inputs and 1 output bit as shown in the figure below.
   Note that the symbol for the resulting LPM is shown in the top left corner and any changes you make through the wizard will be reflected in the top left corner image.
   Click **Next** twice.

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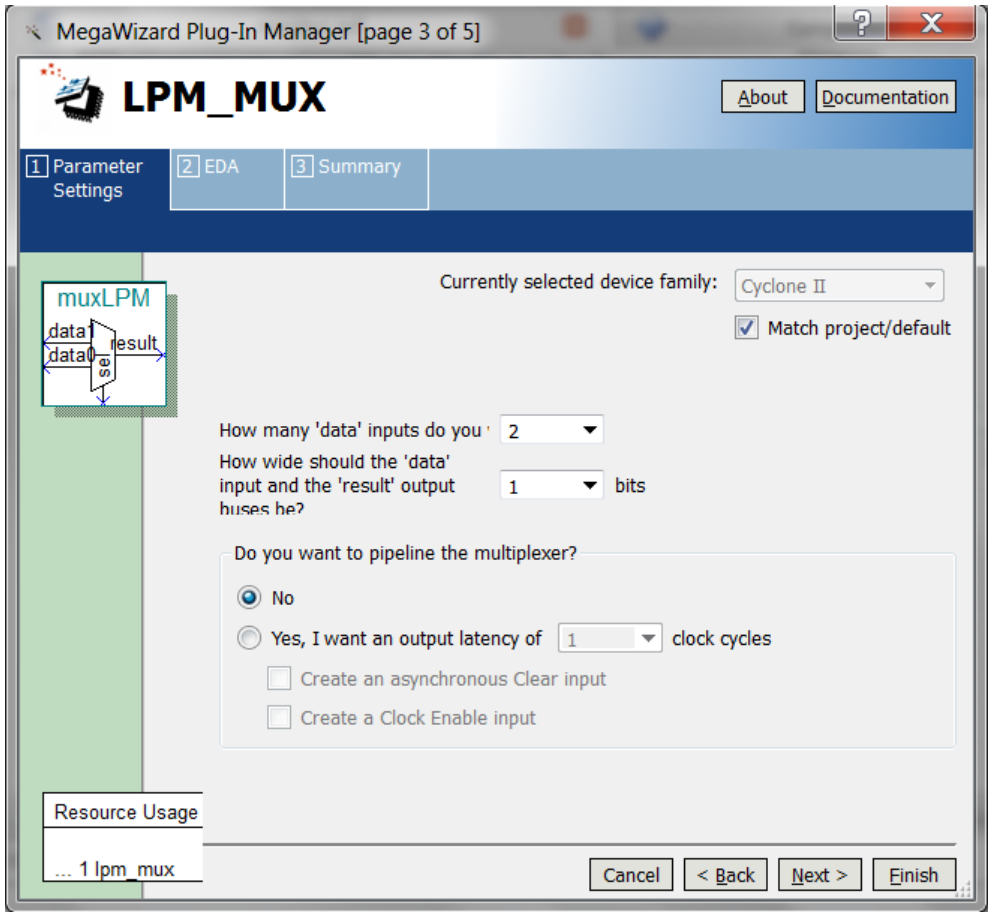

6. This is the final screen, you should simply click **Finish**

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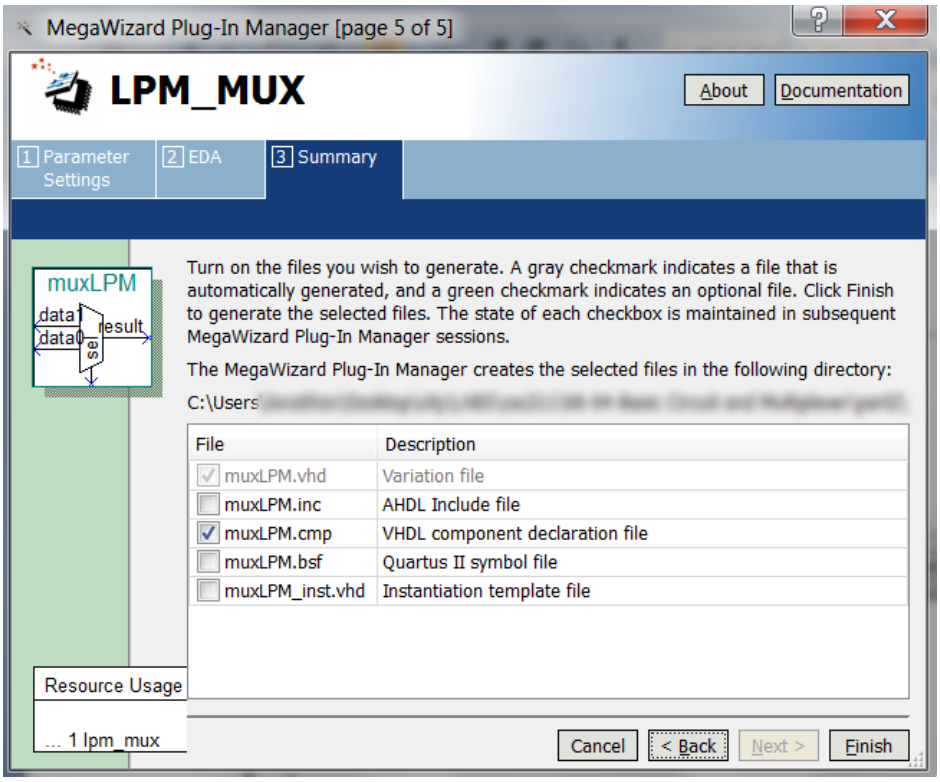

7. If you are asked whether you want to add the circuit you just created to the project, click **Yes**.

8. Quartus automatically generated a VHDL file, you can verify in the navigation panel as shown below:

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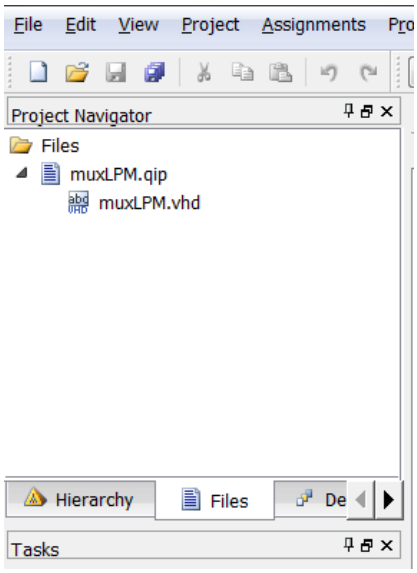
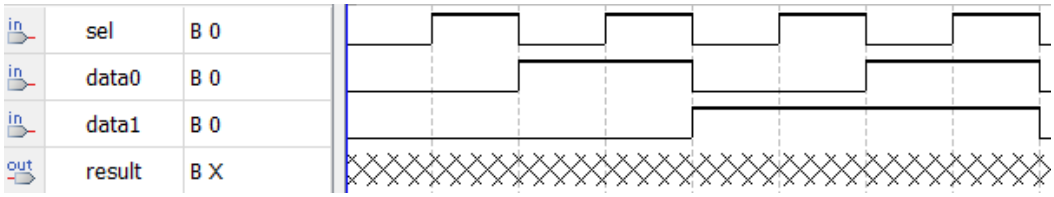


9. You don't need to make any changes to this VHDL file. Simply right click the vhd file and set it as your top level entity, then compile.

10. Create a waveform simulation file. Note that Quartus will give some default names to your inputs and outputs, in this case *sel*, *data0*, *data1* for inputs, and *result* for output.
Your setup before simulation may look something like this:



11. Run your waveform simulation, you should obtain the same output behavior described in part 2 of this lab.

12. Pin Assignment:
[Click here for pin assignment manual]

Create a new text file to add your pin assignments:
data0: Assign to SW[0]

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data1: Assign to SW[1]
sel: Assign to SW[2]
result: Assign to LEDR[0]

13. You should be now ready to load and test this circuit onto DE2 board. The behavior should be the same as the multiplexer designed manually in part 2.

PART 4: Lab Report

YOUR TASK

After finishing the above steps, write a report following the format below. Be sure to answer all the questions in the report. You should use Microsoft Word to write the report; **no handwritten reports will be accepted**.

Objective:

- What is the goal of this lab?

Functionality and Specifications:

- What are the inputs and outputs for each circuit and what are they assigned to on the DE2 board?
- Include a screenshot of the circuit diagrams you designed (in this case from part 1 and part 2).

Simulation:

- Include a screenshot of the vector waveform from every part of the lab after producing the output.
- Explain the functionality/behavior of the circuits from each part of the lab, referring to the waveforms obtained.

Conclusion:

- What did you learn from this lab?

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Appendix:

- Include the text of the pin assignments. Also, whenever you write your own VHDL code in future labs, you should also include your code here.