ARCHITECTURE AND DESIGN OF A ROOM-TEMPERATURE FEEDBACK LOOP BETWEEN CRYOGENIC QUBITS MEASUREMENTS AND CONTROLS

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Quantum computing has the potential to beat classical computing…

classical register

0010

$\downarrow$

0101

one operation = 1 state changed

quantum register

$\alpha_1|0000> + \alpha_2|0001> + \cdots + \alpha_{2^4}|1111>$

$\downarrow$

$\alpha'_1|0000> + \alpha'_2|0001> + \cdots + \alpha'_{2^4}|1111>$

one operation = 2^n states changed

factoring algorithms

GNFS

$O(e^{1.9*\log(N)^{\frac{1}{3}}*\log\log(N)^{2/3}})$

Shor's algorithm

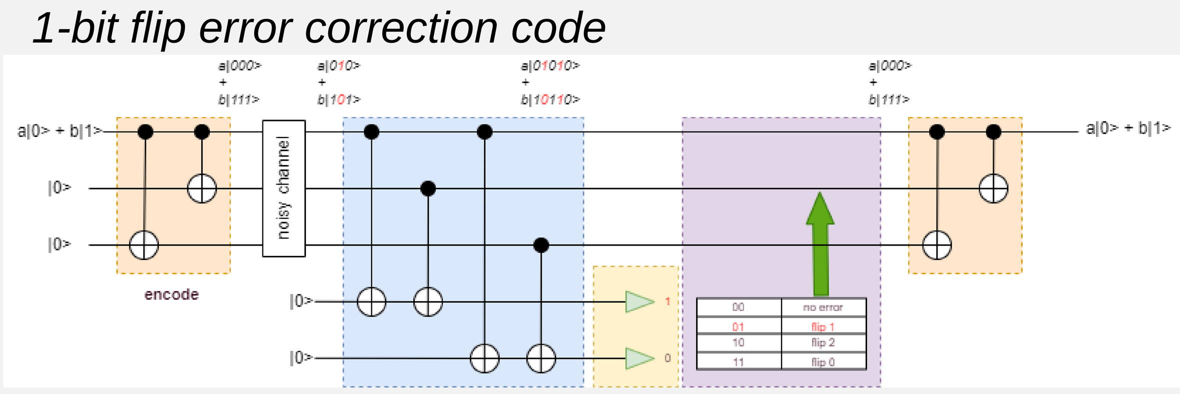
$O((\log N)^2(\log\log N)(\log\log\log N))$

…but **error correction** is needed to exploit quantum advantage...

Use of redundancy

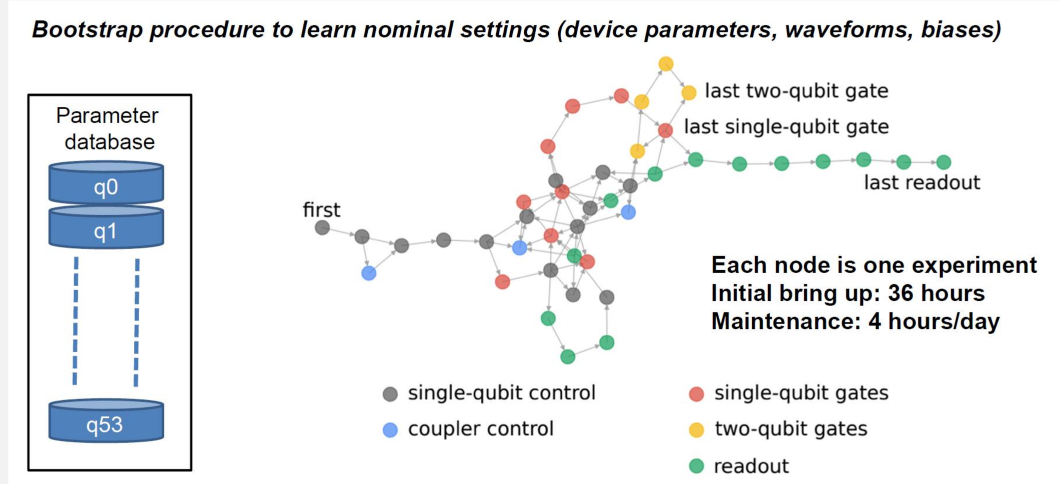
10^3 Physical qubits ≈ 1 logical qubit

1-bit flip error correction code



Need fast (~1 µs) and scalable **feedback**

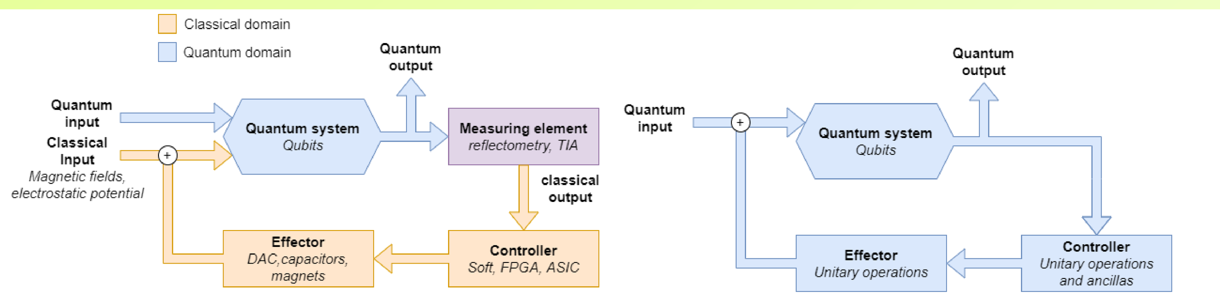
… and fine tuning of parameters with **calibration**



Calibration protocol of Google Sycamore, Each node is an experiment aiming at calibrating one or several parameters. For example those parameters can be Rabbi frequencies, pulse shapes and timings, biases etc… [1]

Need flexible and scalable **feedback**

Two main kind of quantum feedback [2]



Typical Bayesian feedback

Typical Markovian feedback

Based on classical technology

- Uses measurements

+ Can implement any kind of loop control

Based on physics

+ No need for measurement

- May not implement complex feedbacks

- Quantum correction

Goal : **implementing a FPGA architecture for Bayesian feedback**

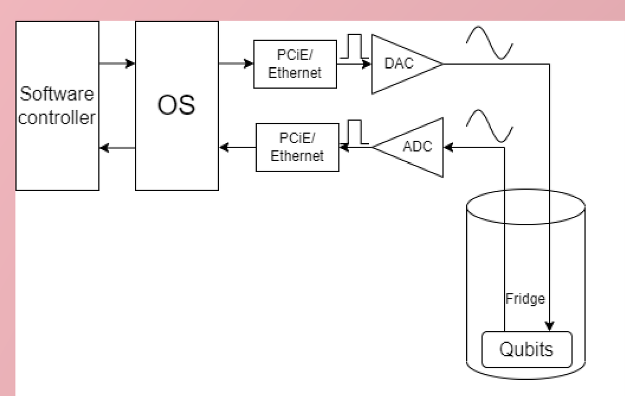
- Need to scale to thousands of Qubits (multi-board synchronization, distributed control)
- Need latencies below 1 µs
- Real-time constraints for control and measurements
- Implementation on RFSoC ZCU111 (and ZCU208)

Four ways of controlling, measuring and implementing Bayesian feedback on spin qubits [3]

Software based

+ Fast and easy to develop
+ High flexibility
+ Almost free

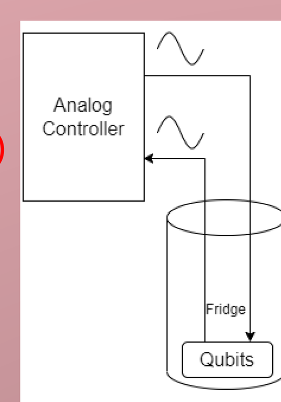
- Very high latency (~1 µs)
- More points of failure



Analog devices

+ Very low latency (~100 ns)

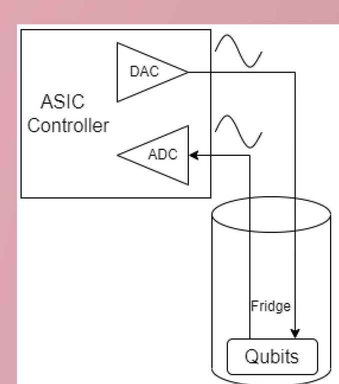
- Complex to design (especially in RF)
- Can't implement complex algorithms
- No memory and no parallelization
- Extremely sensitive to noise
- Prone to failure



ASICs

+ Low latency (~100 ns*)
+ Can implement complex algorithms
+ Easy interface with computer

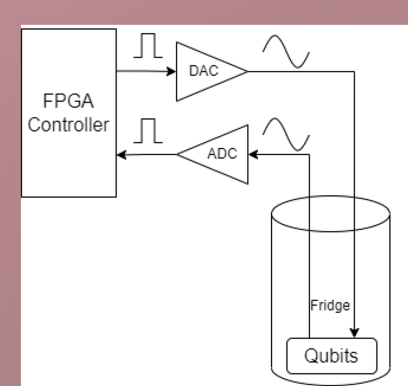
- Costly
- Design is frozen after tape-out
- Very long design process



FPGAs

+ Low latency (~200 ns)
+ Can implement complex algorithms
+ Easy interface with computer
+ Prepare ASIC transition
+ Flexibility

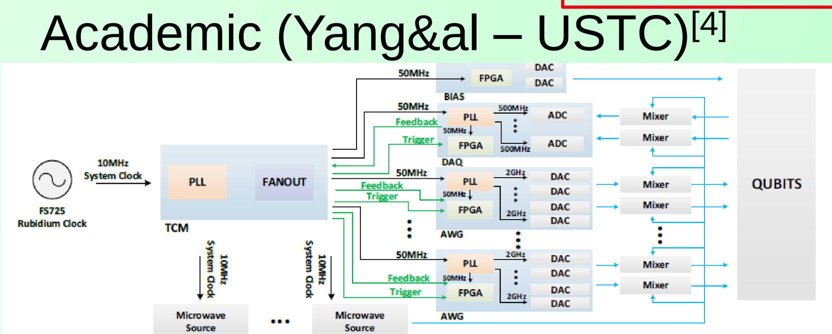
- Less optimal than ASIC



**no actual implementation, this latency is an estimation based on FPGA latencies*

State of the art

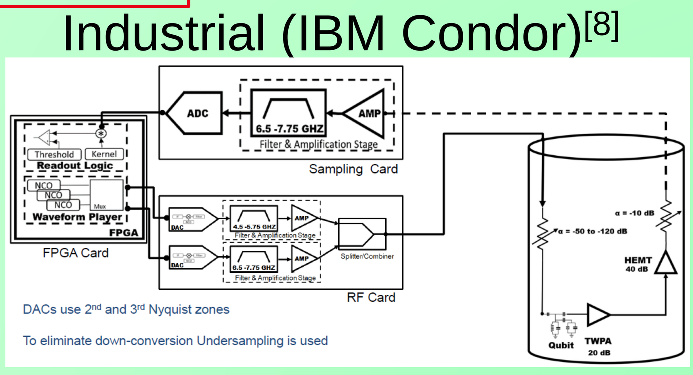
Academic (Yang&al – USTC)[4]



125 ns feedback scales to 100 qubits

Also open-source projects[5], specialized in fast switching[6] or scalability[7]…

Industrial (IBM Condor)[8]



100 ns feedback scales to 1121 qubits

Also control architectures[9] , start-ups projects[10]…

Conclusion

- Objective is a high-performance FPGA architecture, ready for future ASIC implementation
- Similar work on supra-conducting qubits is more advanced
- Focus on the specificities of semiconducting qubits
- Currently working on a low-memory footprint real-time ramp generator

[1] J. Bardin, "Beyond-Classical Computing Using Superconducting Quantum Processors," *2022 IEEE International Solid- State Circuits Conference (ISSCC)*, 2022, pp. 422-424
[2] J. Zhang, Y. Liu, R.-B. Wu, K. Jacobs, et F. Nori, « Quantum feedback: theory, experiments, and applications », *Physics Reports*, vol. 679, p. 1-60, mars 2017
[3] Y. Salathé *et al.*, « Low-Latency Digital Signal Processing for Feedback and Feedforward in Quantum Computing and Communication », *Phys. Rev. Applied*, vol. 9, nº 3, p. 034011, mars 2018
[4] Y. Yang *et al.*, « FPGA-based electronic system for the control and readout of superconducting quantum processors », *arXiv:2110.07965 [physics, physics:quant-ph]*, févr. 2022
[5] L. Stefanazzi *et al.*, « The QICK (Quantum Instrumentation Control Kit): Readout and control for qubits and detectors », *arXiv:2110.00557 [physics, physics:quant-ph]*, oct. 2021
[6] K. H. Park *et al.*, « ICARUS-Q: A scalable RFSoC-based control system for superconducting quantum computers », *arXiv:2112.02933 [physics, physics:quant-ph]*, déc. 2021
[7] N. Messaoudi, C. Crocker, et M. Almendros, « A Hardware-Accelerated Qubit Control System for Quantum Information Processing », in *2020 XXXV Conference on Design of Circuits and Integrated Systems (DCIS)*, nov. 2020, p. 1-5.
[8] Zettles et al., "Design Considerations for Superconducting Quantum Systems," *Proc. 2022 IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 424-425, feb. 2022.
[9] N. Khammassi *et al.*, « A Scalable Microarchitecture for Efficient Instruction- Driven Signal Synthesis and Coherent Qubit Control », p. 10.
[10] QBLOX https://www.qblox.com/

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