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Scratchy - An open-source generator of lightweight scratchpad-based multi-RISC-V architectures

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Résumé
Due to the successive technological limitations named "power wall", memory wall", and "instruction-level parallelism wall", processing performance is now obtained by employing domain-specific architectures or general-purpose multi-core architectures [4]. These technologies have introduced system-level complexity, making architectures difficult and costly to evolve and adapt to novel application requirements. System-level design complexity is mitigated by combining well-validated hardware intellectual properties (IPs) interconnected by standard interfaces. To go beyond architectural conservatism and propose diverse and adaptable architectures needed to improve performance [2], system design methods are needed to raise the abstraction level while providing efficient integration and verification. Open-source hardware (OSH) is rapidly spreading as a good practice that delivers the functional description of hardware blocks such as central processing units (CPUs), accelerators, and networks-on-chip under an open-source license. With OSH, a designer can freely study, build and manufacture custom architectures for processing applications with advanced customization. Open source tools for prototyping architectures on Field-Programmable Gate Arrays (FPGA) are increasingly adopted, such as the Open ESP System-on-a-Chip (SoC) Development tool [5] and the OpenPiton open source manycore platform [1]. These tools focus on high-performance cores and require high-end FPGAs to implement a prototype. This work introduces Scratchy, an open-source generator of lightweight scratchpad-based multi-RISC-V architectures. The interconnect and storage of the generated platforms are strongly customizable, and a 4-core Scratchy architecture can fit on a small Intel MAX10 FPGA [1]. The Scratchy generator is built upon the S-LAM quasi-MoA [7] implemented in the PREESM [6] rapid prototyping tool and the LiteX SoC Composer tool [3]. The generator produces a cluster of cores communicating through hierarchical scratchpad memories. Our work considers scratchpads as private memories as in Rouxel et al [8].

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