JOSHUA BAS

704.978.9370 | joshua.n.bas@gmail.com | Charlotte, NC

EDUCATION

Carnegie Mellon University, Pittsburgh, PA *May 2020*
B.S. in Electrical & Computer Engineering

RELEVANT COURSEWORK

Logic Design & Verification	Introduction to Computer Architecture
Introduction to Embedded Systems	Structure & Design of Digital Systems

WORK EXPERIENCE

Audition Technology *June 2019 - May 2020*
Analog Engineer Intern *Pittsburgh, PA*

- Researched digital hearing aid design and multiple hearing aid-specific DSP chips, including patents
- Scouted an electrical device assembly facility as a potential manufacturing partner
- Contributed to meetings with the startup's stakeholders and medical advisor
- Proposed and designed a modular, 2-layer evaluation board
- Created and maintained EagleCAD parts library

PROJECTS

RISCV Processor (SystemVerilog & C) *January 2020 - May 2020*
Introduction to Computer Architecture

- Designed and implemented a 6-stage dual-core processor for the RISCV ISA, particularly the RV32I base. Both cores are capable of the usual logical and arithmetical operations, as well as branches and unconditional jumps; the primary core can also access memory.

Real-Time Kernel (C & ARM Assembly) *August 2019 - December 2019*
Introduction to Embedded Systems

- Implemented a simple real-time kernel on the STM32F microcontroller capable of executing SVCs and interrupt service routines; communicating via polled/interrupt UART, I2C, and SPI; receiving ADC inputs; and context swapping between different threads. Built on Ubuntu Linux.

CMU Mars Ice (C/C++ & Python) *October 2018 - June 2019*
2019 Moon to Mars Ice & Prospecting Challenge

- Created design blocks for PCB using EagleCAD for a drilling robot. Implemented a network with client dropped protocol, as well as the server-side controls system for the robot. Traveled to Langley Research Center to operate the robot.

SDRAM Controller (SystemVerilog) *October 2018 - June 2019*
Logic Design and Verification

- Designed a memory controller for a 64MB, 4-banked SDRAM, using VCS (Verilog Compiler Simulator) and Altera Quartus to debug and upload onto the Cyclone V FPGA.

PUBLICATIONS

- Development of Hearing Technology with Personalized Safe Listening Features. Gupta, S.; Xu, X.; Liu, H.; Zhang, J.; **Bas, J.**; Kelly, S. 2019 ITU Kaleidoscope Conference Proceedings.

SKILLS

Programming Languages	C/C++, SystemVerilog, Python, ARM Assembly, MatLab
Hardware	PCB design, circuit analysis, soldering
Software & Tools	GDB, VCS, Valgrind, EagleCAD, Git, SolidWorks, MS Office