MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

DSP56001A

24-bit Digital Signal Processor

The DSP56001A is an MPU-style general purpose Digital Signal Processor (DSP) composed of an efficient 24-bit digital signal processor engine, program and data memories, various peripherals, and support circuitry. The 56000-Family-compatible DSP engine is fed by on-chip program RAM, two independent data RAMs, and two data ROMs with sine, A-law, and m-law tables. The DSP56001A contains a Serial Communication Interface (SCI), Synchronous Serial Interface (SSI), and parallel Host Interface (HI). This combination of features, illustrated in Figure 1, makes the DSP56001A a cost-effective, high-performance solution for high-precision general-purpose digital signal processing. The DSP56001A is intended as a replacement to the DSP56001. The DSP56002 should be considered for new designs.

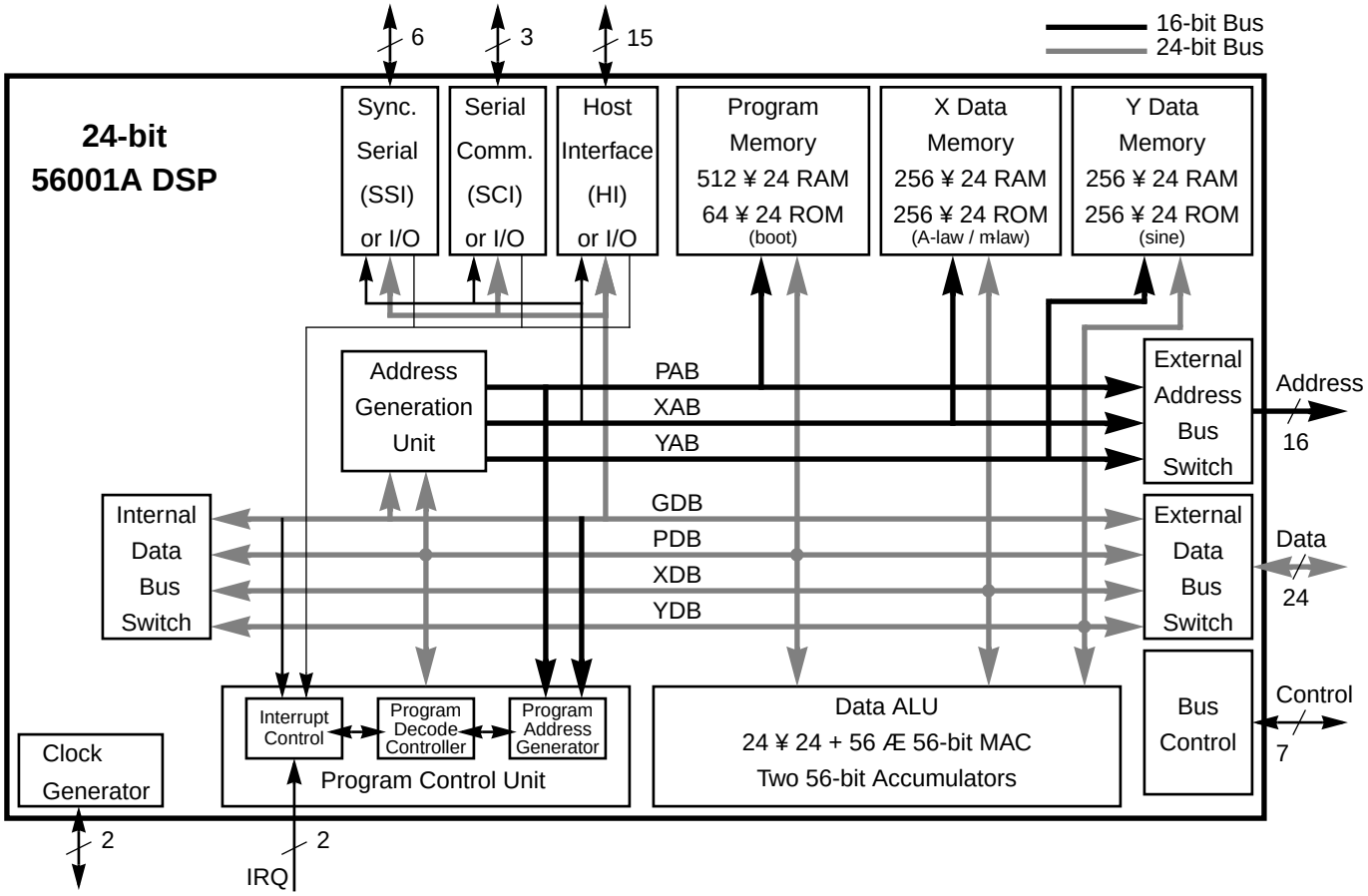


Figure 1 DSP56001A Block Diagram

DSP56001A Features

Digital Signal Processing Engine

- Efficient, object code compatible, 24-bit 56000-Family DSP engine
  - — Up to 16.5 Million Instructions Per Second (MIPS) – 60.6 ns instruction cycle at 33 MHz
  - — Up to 99 Million Operations Per Second (MOPS) at 33 MHz
  - — Executes a 1024-point complex Fast Fourier Transform (FFT) in 59,898 clocks
  - — Highly parallel instruction set with unique DSP addressing modes
  - — Two 56-bit accumulators including extension byte
  - — Parallel 24×24-bit multiply-accumulate in 1 instruction cycle (2 clock cycles)
  - — Double precision 48×48-bit multiply with 96-bit result in 6 instruction cycles
  - — 56-bit Addition / Subtraction in 1 instruction cycle
  - — Fractional arithmetic with support for multiprecision arithmetic
  - — Hardware support for block-floating point FFT
  - — Hardware nested DO loops
  - — Zero-overhead fast interrupts (2 instruction cycles)
  - — Four 24-bit internal data buses and three 16-bit internal address buses for maximum information transfer on-chip

Memory

- On-chip Harvard architecture permitting simultaneous accesses to program and two data memories
- 512×24-bit on-chip program RAM and 64×24-bit bootstrap ROM
- Two 256×24-bit on-chip data RAMs
- Two 256×24-bit on-chip data ROMs containing sine, A-law and μ-law tables
- External memory expansion with 16-bit address and 24-bit data buses
- Bootstrap loading from external data bus or Host Interface

Peripheral and Support Circuits

- Byte-wide Host Interface (HI) with Direct Memory Access (DMA) support
- Synchronous Serial Interface (SSI) to communicate with codecs and synchronous serial devices
  - — 8-, 12-, 16-, and 24-bit word sizes
  - — Up to 32 software-selectable time slots in network mode
- Serial Communication Interface (SCI) for full-duplex asynchronous communications
- On-chip peripheral registers memory mapped in data memory space
- Double buffered peripherals

- Up to 24 general-purpose I/O (GPIO) pins
- Two external interrupt request pins

Miscellaneous Features

- Power-saving Wait and Stop modes
- Fully static, HCMOS design for operating frequencies from 33 MHz down to 4 MHz
- 88-pin Ceramic Pin Grid Array (PGA) package; 13×13 array
- 132-pin Plastic Quad Flat Pack (PQFP) surface-mount package; $24 \times 24 \times 4$ mm
- 132-pin Ceramic Quad Flat Pack (CQFP) surface-mount package; $22 \times 22 \times 4$ mm
- 5 V power supply

Product Documentation

This data sheet plus the two manuals listed in Table 1 are required for a complete description of the DSP56001A and are necessary to properly design with the part. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, or through a Motorola Literature Distribution Center.

Table 1 DSP56001A Documentation

Topic	Description	Order Number
DSP56001 User's Manual	Detailed description of the 56001 architecture, 24-bit DSP processor, memory, peripherals, and instruction set	DSP56001UM/AD
DSP56000 Family Manual	Detailed description of the 56000-family architecture and the 24-bit core processor and instruction set	DSP56KFAMUM/AD
DSP56001A Data Sheet	Pin and package descriptions, and electrical and timing specifications	DSP56001A/D

Related Documentation

Table 2 lists additional documentation relevant to the DSP56001A.

Table 2 DSP56001A Related Documentation

Document Name	Description	Order Number
Motorola's 16-, 24-, and 32-bit Digital Signal Processing Families	Overview of all of the DSP product families.	BR1105/D
Digital Sine-Wave Synthesis	Application Report. Uses the DSP56001 look-up table.	APR1/D
Digital Stereo 10-band Graphic Equalizer	Application Report. Includes code and circuitry; features the DSP56001.	APR2/D
Fractional and Integer Arithmetic	Application Report. Includes code.	APR3/D
Implementation of Fast Fourier Transforms	Application Report. Comprehensive FFT algorithms and code for DSP56001, DSP56156, and DSP96002.	APR4/D
Implementation of PID Controllers	Application Report. PWM using the SCI timer and three phase output using modulo addressing.	APR5/D
Convolutional Encoding and Viterbi Decoding with a V.32 Modem Trellis Example	Application Report. Theory and code; features the DSP56001.	APR6/D
Implementing IIR/FIR Filters	Application Report. Comprehensive example using the DSP56001.	APR7/D
Principles of Sigma-Delta Modulation for A-to-D Converters	Application Report. Features the DSP56ADC16; improving resolution with half-band filters	APR8/D
Full-Duplex 32-kbit/s CCITT ADPCM Speech Coding	Application Report. Features the DSP56001	APR9/D
DSP56001 Interface Techniques and Examples	Application Report. Interfaces for pseudo static RAM, dynamic RAM, ISA bus, Host	APR11/D
Twin CODEC Expansion Board for the DSP56000 ADS	Application Report. Circuit, code, FIR filter design for two voice band CODECs connecting to the SSI	APR12/D
Conference Bridging in the Digital Telecommunications Environment	Application Report. Theory and code; features the DSP56001/002	APR14/D
Implementation of Adaptive Controllers	Application Report. Adaptive control using reference models; generalized predictive control; includes code	APR15/D

Table 2 DSP56001A Related Documentation (Continued)

Document Name	Description	Order Number
Calculating Timing Requirements of External SRAM	Application Report. Determination of SRAM speed for optimum performance	APR16/D
Low Cost Controller for DSP56001	Application Report. Circuit and code to connect two DSP56001s to an MC68008	APR402/D
G.722 Audio Processing	Application Report. Theory and code using SB-ADPCM	APR404/D
Minimal Logic DRAM Interface	Application Report. 1M x 480 ns DRAM, 1 PAL, code	APR405/D
Logarithmic/Linear Conversion Routines	Application Report. μ-law and A-law companding routines for PCM mono-circuits	ANE408/D
Dr. BuB Bulletin Board	Flyer. Motorola's electronic bulletin board where free DSP software is available	BR297/D
DSP Development Tools	Overview of Motorola's hardware and software development tools	DSPTOOLSP/D
Third Party Compendium	Brochures from companies selling hardware and software that supports Motorola DSPs	DSP3RDPTYPAK/D
University Support Program	Flyer. Motorola's program supporting Universities in DSP research and education	BR382/D
Technical Training Schedule	Technical Training Schedule	BR348AD/D
Audio Course Information	Audio Course Information	BR928/D
Real Time Signal Processing Applications with Motorola's DSP56000 Family	Textbook by Mohamed El-Sharkawy; 398+ pages. (This is a charge item.)	Prentice-Hall, 1990; ISBN 0-13-767138-5

Data Sheet Contents

This data sheet contains:

Data Sheet Conventions

This data sheet uses the following conventions:

- $\overline{\text{OVERBARS}}$ are used to indicate a signal that is active when pulled to ground (see Table 3) e.g. the $\overline{\text{HREQ}}$ pin is active when pulled to ground. Therefore, references to the $\overline{\text{HREQ}}$ pin will always have an overbar.
- The word “assert” (see Table 3) means that a high true (active high) signal is pulled high to V_{CC} or that a low true (active low) signal is pulled low to ground.
- The word “deassert” (see Table 3) means that a high true signal is pulled low to ground or that a low true signal is pulled high to V_{CC}.

Table 3 High True / Low True Signal Conventions

Signal/Symbol	Logic State	Signal State	Voltage
$\overline{\text{PIN}}$	True	Asserted	Ground
$\overline{\text{PIN}}$	False	Deasserted	V_{CC}
PIN	True	Asserted	V_{CC}
PIN	False	Deasserted	Ground

NOTES:

1. PIN is a generic term for any pin on the chip.
2. Ground is an acceptable low voltage level. See the DC electrical specifications for the range of acceptable low voltage levels (typically a TTL logic low).
3. V_{CC} is an acceptable high voltage level. See the DC electrical specifications for the range of acceptable high voltage levels (typically a TTL logic high).

Pin Groupings

The input and output signals of the DSP56001A are organized into functional groups as shown in Table 4 and as illustrated in Figure 2.

Table 4 DSP56001A Functional Pin Groupings

Functional Group	Number of Pins
Address Bus	16
Data Bus	24
Bus Control	7
Host Interface (HI) *	15
Serial Communication Interface (SCI) *	3
Synchronous Serial Interface (SSI) *	6
Interrupt and Mode Control	3
Clock	2
Power (V_{CC})	5 / 10
Ground (GND)	7 / 14
Reserved (no connect)	0 / 32 **
Total Number of Pins	88 / 132 **

* alternately, general purpose I/O pins
** package dependent

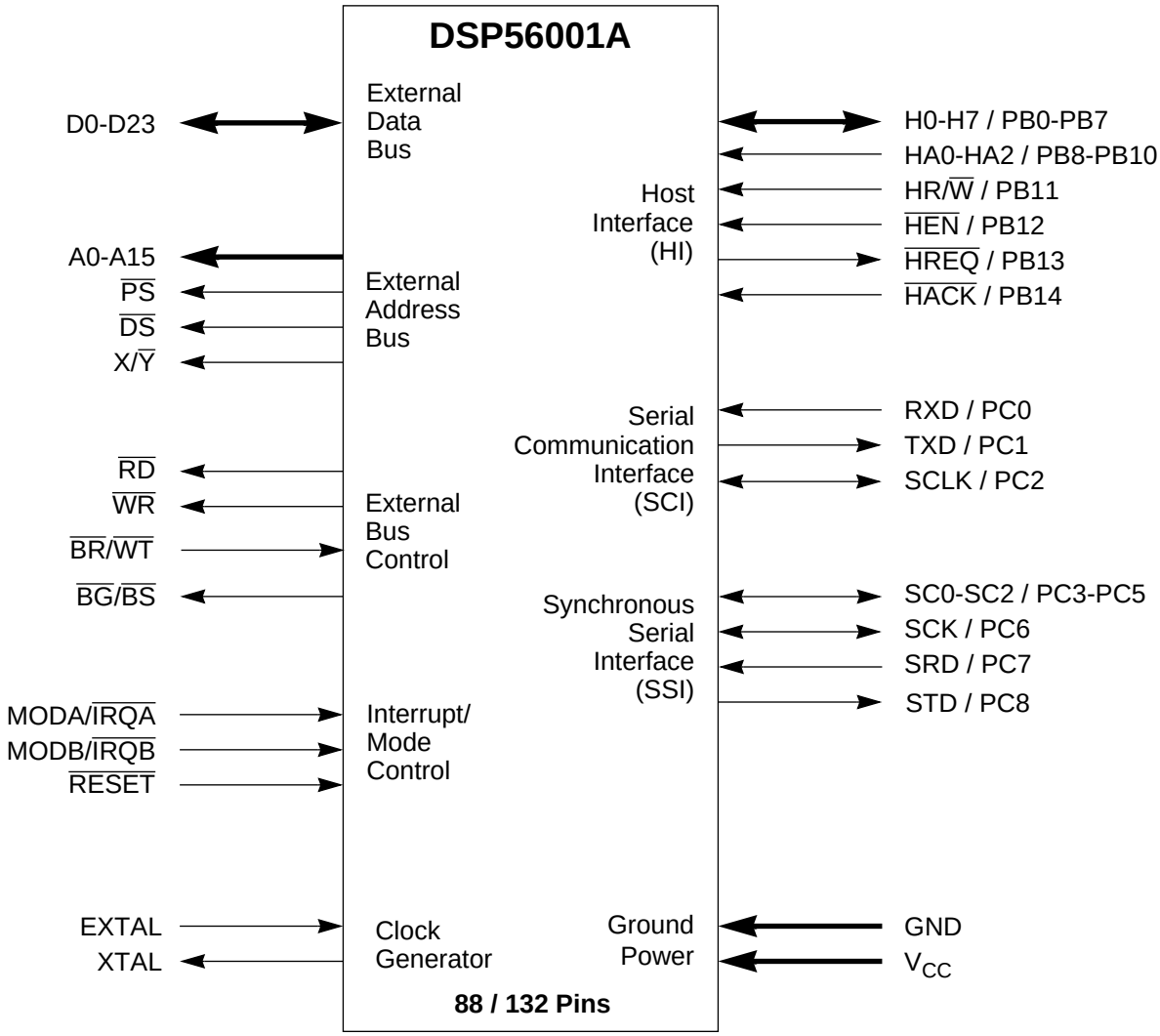


Figure 2 DSP56001A Pin Functions

Pin Descriptions

All unused inputs should have pull-up resistors for two reasons:

1. floating inputs draw excessive power
2. floating inputs can cause erroneous operation

For example, during reset, all signals are three-stated unless noted otherwise. Without pull-up resistors, the $\overline{PS}$ and $\overline{DS}$ signals may be interpreted by peripheral circuitry as being asserted, causing two or more memory chips to try to simultaneously drive the external bus, which can damage the memory chips. A pull-up resistor in the 50 K-ohm range should be sufficient.

Address and Data Bus

The Port A address and data bus signals control the access to external memory. They are three-stated during hardware reset.

A0-A15 (Address Bus) — three-state, active high outputs. These pins specify the address for external program and data memory accesses. If there is no external bus activity, A0-A15 remain at their previous values to reduce power consumption. A0-A15 are three-stated when the bus grant signal is asserted.

D0–D23 (Data Bus) — three-state, active high, bidirectional input/outputs. These pins provide the bidirectional data bus for external program and data memory accesses. D0–D23 are three-stated when the bus grant signal is asserted.

Bus Control

The bus control signals provide a means to connect additional bus masters (which may be additional DSPs, microprocessors, Direct Memory Access (DMA) controllers, etc.), control external memory, and force wait states through Port A to the DSP56001A. These pins are three-stated during reset unless noted otherwise and may require pull-up resistors to assure expected operation.

$\overline{PS}$ (Program Memory Select) — three-state, active low output. This output is asserted only when external program memory is referenced.

$\overline{DS}$ (Data Memory Select) — three-state, active low output. This output is asserted only when external data memory is referenced.

X/$\overline{Y}$ (X/$\overline{Y}$ Select) — three-state output. This output is driven low during external Y data memory accesses. It is also driven low during external exception vector fetches when operating in the development mode.

$\overline{RD}$ (Read Enable) — three-state output. This output is asserted to read external memory on the data bus (D0–D23).

$\overline{WR}$ (Write Enable) — three-state output. This output is asserted to write external memory on the data bus (D0–D23).

$\overline{BR}$/$\overline{WT}$ (Bus Request/Wait) — three-state, active low, bidirectional input/outputs. The bus request input $\overline{BR}$ allows another device such as a processor or DMA controller to become the master of external data bus D0-D23 and external address bus A0-A15. When operating mode register (OMR) bit 7 is clear

and $\overline{BR}$ is asserted, the DSP56001 will always release the external data bus D0-D23, address bus A0-A15, and bus control pins $\overline{PS}$, $\overline{DS}$, X/$\overline{Y}$, $\overline{RD}$, and $\overline{WR}$ (i. e., Port A), by placing these pins in the high-impedance state after execution of the current instruction has been completed. The $\overline{BR}$ pin should be pulled up when not in use.

If OMR bit 7 is set, this pin is an input that allows an external device to force wait states during an external Port A operation for as long as $\overline{WT}$ is asserted.

$\overline{BG}$/$\overline{BS}$ (Bus Grant/Bus Strobe) — three-state, active low, bidirectional input/outputs. If OMR bit 7 is clear, this output is asserted to acknowledge an external bus request after Port A has been released. If OMR bit 7 is set, this pin is bus strobe and is asserted when the DSP accesses Port A. This pin is three-stated during $\overline{RESET}$.

Interrupt and Mode Control

The interrupt and mode control pins select the chip's operating mode as it comes out of hardware reset, and then receive interrupt requests from external sources.

MODA/ $\overline{IRQA}$ (Mode Select A/External Interrupt Request A/STOP Recovery) — input. This input pin has three functions:

- to work with the MODB pin to select the chip's operating mode
- to receive an interrupt request from an external source
- to turn on the internal clock generator, causing the chip to recover from the stop processing state. Reset causes this input to act as MODA.

As the chip comes out of reset, it reads the states of MODA and MODB, writes the information to the Operating Mode Register, and thus sets the chip's operating mode. (For more information, see the *DSP56001 User's Manual* (DSP56001UM/AD).) Therefore, during reset, this pin should be forced to the desired state. After the chip has left the reset state, the MODA pin automatically changes to external interrupt request $\overline{IRQA}$.

$\overline{IRQA}$ receives external interrupt requests. It can be programmed to be level sensitive or negative edge triggered. When the signal is edge triggered, triggering occurs at a voltage level, V_{ILM}, and is not directly related to the fall time of the interrupt signal. However, as the fall time of the interrupt signal increases, the probability that noise on $\overline{IRQA}$ will generate multiple interrupts also increases.

MODB/ $\overline{IRQB}$ (Mode Select B/External Interrupt Request B) — input. This input pin works with the MODA pin to select the chip's operating mode, and it receives an interrupt request from an external source. Reset causes this input to act as MODB.

During reset, this pin should be forced to the desired state, because as the chip comes out of reset, it reads the states of the mode pins and writes the information to the Operating Mode Register, and thus sets the chip's operating mode. After the chip has left the reset state, the

MODB pin automatically changes to external interrupt request $\overline{\text{IRQB}}$.

$\overline{\text{IRQB}}$ receives external interrupt requests. It can also be programmed to be level sensitive or negative edge triggered. When the signal is edge triggered, triggering occurs at a voltage level, V_{ILM}, and is not directly related to the fall time of the interrupt signal. However, as the fall time of the interrupt signal increases, the probability that noise on $\overline{\text{IRQB}}$ will generate multiple interrupts also increases.

WARNING

A Non-Maskable Interrupt (NMI) function was previously accessible on the DSP56001 by applying 10 Volts to the MODB/$\overline{\text{IRQB}}$ pin. The DSP56001A does not support a non-maskable interrupt (NMI).

DO NOT APPLY 10 VOLTS TO ANY PIN OF THE DSP56001A (including MODB)! *Subjecting any pin of the DSP56001A to voltages in excess of the specified TTL/CMOS levels will permanently damage the device.*

$\overline{\text{RESET}}$ (Reset) — input. This Schmitt trigger input pin resets the DSP56001A. When $\overline{\text{RESET}}$ is asserted, the DSP56001A is initialized and placed in the reset state. When $\overline{\text{RESET}}$ is deasserted, the chip writes the mode pin (MODA, MODB) information to the operating mode register, setting the chip's operating mode. When coming out of the reset state, deassertion occurs at a voltage level, V_{IL}, that is not directly related to the rise time of the $\overline{\text{RESET}}$ signal. The probability that noise on $\overline{\text{RESET}}$ will generate multiple resets increases with increasing rise time of the $\overline{\text{RESET}}$ signal.

Host Interface (HI)

The host interface signals provide a convenient connection to another processor through Port B on the DSP56001A.

H0–H7 (Host Data Bus) — bidirectional. This data bus transfers data between the host processor and the DSP56001A. It acts as an input unless HR/$\overline{\text{W}}$ is high and $\overline{\text{HEN}}$ is asserted, making H0–H7 become outputs and allowing the host processor to read DSP56001A data. It is high impedance when $\overline{\text{HEN}}$ is deasserted. H0-H7 become outputs when $\overline{\text{HACK}}$ is asserted during $\overline{\text{HREQ}}$ assertion. H0–H7 can be programmed as general-purpose I/O pins (PB0–PB7) when the host interface is not selected. These pins are configured as GPIO input pins during hardware reset.

HA0–HA2(Host Address) — input*. These inputs provide the address selection for each host interface register. HA0–HA2 can be programmed as general-purpose I/O pins (PB8–PB10) when the host interface is not selected. These pins are configured as GPIO input pins during hardware reset.

HR/$\overline{\text{W}}$ (Host Read/Write) — input*. This input selects the direction of data transfer for each host processor access. If HR/$\overline{\text{W}}$ is high and $\overline{\text{HEN}}$ is asserted, H0-H7 are outputs and DSP data is transferred to the host processor. If HR/$\overline{\text{W}}$ is low and $\overline{\text{HEN}}$ is asserted, H0-H7 are inputs and host data is transferred to the DSP. HR/$\overline{\text{W}}$ must be stable when $\overline{\text{HEN}}$ is asserted. It can be programmed as a general-purpose I/O pin (PB11) when the host interface is not selected. This pin is configured as a GPIO input pin during hardware reset.

* These pins can be input or output when programmed as general purpose I/O.

$\overline{\text{HEN}}$ (Host Enable) — input*. This input enables a data transfer on the host data bus. When $\overline{\text{HEN}}$ is asserted and HR/$\overline{\text{W}}$ is high, H0–H7 become outputs and the host processor may read DSP56001A data. When $\overline{\text{HEN}}$ is asserted and HR/$\overline{\text{W}}$ is low, H0–H7 become inputs. Host data is latched inside the DSP on the rising edge of $\overline{\text{HEN}}$. Normally, a chip select signal derived from host address decoding and an enable strobe are used to generate $\overline{\text{HEN}}$. $\overline{\text{HEN}}$ can be programmed as a general-purpose I/O pin (PB12) when the host interface is not selected. This pin is configured as a GPIO input pin during hardware reset.

$\overline{\text{HREQ}}$ (Host Request) — open drain output*. This signal is used by the host interface to request service from the host processor, DMA controller, or a simple external controller. $\overline{\text{HREQ}}$ can be programmed as a general-purpose (not open-drain) I/O pin (PB13) when the host interface is not selected. This pin is configured as a GPIO input pin during hardware reset.

NOTE: $\overline{\text{HREQ}}$ should always be pulled high when it is not in use.

$\overline{\text{HACK}}$ (Host Acknowledge) — input*. This input has two functions. It provides a host acknowledge handshake signal for DMA transfers and it receives a host interrupt acknowledge compatible with MC68000 Family processors. When the port is defined as the host interface, the user may program this input as either a general-purpose I/O pin, or as the $\overline{\text{HACK}}$ pin. This pin is configured as a GPIO input pin during hardware reset.

NOTE: $\overline{\text{HACK}}$ should always be pulled high when it is not in use.

Serial Communications Interface (SCI)

RXD (Receive Data) — input*. This input receives byte-oriented data and transfers the data to the SCI receive shift register. Input data can be sampled on either the positive edge or on the negative edge of the receive clock, depending on how the SCI control register is programmed. RXD can be programmed as a general-purpose I/O pin (PC0) when it is not needed as an SCI pin. This pin is configured as a GPIO input pin during hardware reset.

TXD (Transmit Data) — output*. This output transmits serial data from the SCI transmit shift register. In the default configuration, the data changes on the positive clock edge and is valid on the negative clock edge. The user can reverse this clock polarity by programming the SCI control register appropriately. TXD can be programmed as a general-purpose I/O pin (PC1) when the SCI TXD function is not being used. This pin is configured as a GPIO input pin during hardware reset.

SCLK (SCI Serial Clock) — bidirectional. This pin provides an input or output clock from which the transmit and/or receive baud rate is derived in the asynchronous mode, and from which data is transferred in the synchronous mode. SCLK can be programmed as a general-purpose I/O pin (PC2) when the SCI SCLK function is not being used. This pin is configured as a GPIO input pin during hardware reset.

* These pins can be input or output when programmed as general purpose I/O.

Synchronous Serial Interface (SSI)

The SSI operating mode affects the definition and function of the SC0, SC1 and SC2 control pins.

SC0 (Serial Clock 0) — bidirectional. This pin's function is determined by whether the SCLK is in synchronous or asynchronous mode. In synchronous mode, this pin is used for serial flag I/O. In asynchronous mode, this pin receives clock I/O. SC0 can be programmed as a general-purpose I/O pin (PC3) when the SSI SC0 function is not being used. This pin is configured as a GPIO input pin during hardware reset.

SC1 (Serial Control 1) — bidirectional. The SSI uses this bidirectional pin to control flag or frame synchronization. This pin's function is determined by whether the SCLK is in synchronous or asynchronous mode. In asynchronous mode, this pin is frame sync I/O. For synchronous mode with continuous clock, this pin is serial flag SC1 and operates like the SC0. SC0 and SC1 are independent serial I/O flags but may be used together for multiple serial device selection. SC1 can be programmed as a general-purpose I/O pin (PC4) when the SSI SC1 function is not being used. This pin is configured as a GPIO input pin during hardware reset.

SC2 (Serial Control 2) — bidirectional. The SSI uses this bidirectional pin to control frame synchronization only. As with SC0 and SC1, its function is defined by the SSI operating mode. SC2 can be programmed as a general-purpose I/O pin (PC5) when the SSI SC2 function is not being used. This pin is configured as a GPIO input pin during hardware reset.

SCK (SSI Serial Clock) — bidirectional. This bidirectional pin provides the serial bit rate clock for the SSI when only one clock is being used. SCK can be programmed as a general-purpose I/O pin (PC6) when it is not needed as an SSI pin. This pin is configured as a GPIO input pin during hardware reset.

SRD (SSI Receive Data) — input*. This input pin receives serial data into the SSI receive shift register. SRD can be programmed as a general-purpose I/O pin (PC7) when it is not needed as an SSI pin. This pin is configured as a GPIO input pin during hardware reset.

STD (SSI Transmit Data) — output*. This output pin transmits serial data from the SSI transmit shift register. STD can be programmed as a general-purpose I/O pin (PC8) when it is not needed as an SSI pin. This pin is configured as a GPIO input pin during hardware reset.

Power and Ground

V_{CC} (Power) — Power pins (see Table 22).

GND (Ground) — Ground pins (see Table 22).

Clock Generator

EXTAL (External Clock/Crystal Input) — input. The EXTAL input interfaces the internal oscillator input to an external crystal or an external clock.

***** These pins can be input or output when programmed as general purpose I/O.

XTAL (Crystal) — output. This output connects the internal oscillator output to an external crystal. If an external clock is used, XTAL should be left unconnected.

Electrical Specifications

The DSP56001A is fabricated in high density CMOS with TTL compatible inputs and outputs.

Table 5 Maximum Ratings (GND = 0 Vdc)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	V
All Input Voltages	V_{IN}	GND - 0.5 to V_{CC} + 0.5	V
Current Drain per Pin Excluding V_{CC} and GND	I	10	mA
Operating Temperature Range	T_J	-40 to +105	°C
Storage Temperature	T_{stg}	-55 to +150	°C

Table 6 Thermal Characteristics — PGA Package

Thermal Resistance	Symbol	Value	Unit
Junction to Ambient	Θ_{JA}	27	°C/W
Junction to Case	Θ_{JC}	6.5	°C/W

Table 7 Thermal Characteristics — CQFP/PQFP Packages

Thermal Resistance	Symbol	Value PQFP	Value CQFP	Unit
Junction to Ambient	Θ_{JA}	47	40	°C/W
Junction to Case	Θ_{JC}	13	7.0	°C/W

DC Electrical Characteristics

(V_{CC} = 5.0 Vdc ± 10% for 20.5 MHz and 27 MHz;
V_{CC} = 5.0 Vdc ± 5% for 33 MHz; T_J = -40° to +105° C)

Table 8 DC Electrical Characteristics for the DSP56001A

Characteristics	Symbol	Min	Typ	Max	Units
Supply Voltage 20, 27 MHz 33 MHz	V_{CC}	4.5 4.75	5.0	5.5 5.25	V
Input High Voltage • Except EXTAL, $\overline{RESET}$, MODA, MODB • EXTAL • $\overline{RESET}$ • MODA, MODB	 V_{IH} V_{IHC} V_{IHR} V_{IHM}	 2.0 4.0 2.5 3.5	 — — — —	 V_{CC} V_{CC} V_{CC} V_{CC}	 V V V V
Input Low Voltage • Except EXTAL, MODA, MODB • EXTAL • MODA, MODB	 V_{IL} V_{ILC} V_{ILM}	 -0.5 -0.5 -0.5	 — — —	 0.8 0.6 2.0	 V V V
Input Leakage Current EXTAL, $\overline{RESET}$, MODA/$\overline{IRQA}$, MODB/$\overline{IRQB}$, $\overline{BR}$/$\overline{WT}$	I_{IN}	-1	—	1	µA
Three-State (Off-State) Input Current (@ 2.4 V / 0.4 V)	I_{TSI}	-10	—	10	µA
Output High Voltage (I_{OH} = -0.4 mA)	V_{OH}	2.4	—	—	V
Output Low Voltage (I_{OL} = 1.6 mA; $\overline{HREQ}$ I_{OL} = 6.7 mA, TXD I_{OL} = 6.7 mA)	V_{OL}	—	—	0.4	V
Internal Supply Current at 33MHz (See Note 3) • in Wait Mode (See Note 1) • in Stop Mode (See Note 1)	I_{CCI} I_{CCW} I_{CCS}	— — —	80 10 2	115 25 2000	mA mA µA
Input Capacitance (See Note 2)	C_{IN}	—	10	—	pF

NOTES:

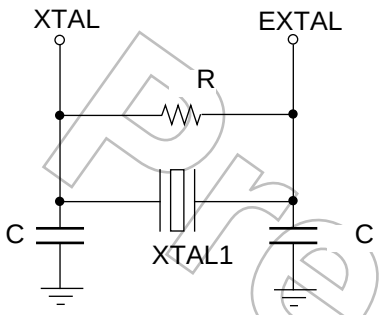
1. In order to obtain these results all inputs must be terminated (i.e., not allowed to float).
2. Periodically sampled and not 100% tested.
3. The “Power Consumption” section describes how to calculate the external supply current.

AC Electrical Characteristics

The timing waveforms for the DSP56001A in the AC Electrical Characteristics are tested with a V_{IL} maximum of 0.5 V and a V_{IH} minimum of 2.4 V for all pins, except EXTAL, $\overline{\text{RESET}}$, MODA, MODB.. These four pins are tested using the input levels set forth in the DC Electrical Characteristics section. AC timing specifications which are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition. DSP56001A output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.8 V and 2.0 V respectively.

Clock Operation

The DSP56001A system clock may be derived from the on-chip crystal oscillator as shown in Figure 3, or it may be externally supplied. An externally supplied square wave voltage source (see Figure 4) should be connected to EXTAL, leaving XTAL physically not connected to the board or socket. The rise and fall time of this external clock should be 4 ns maximum.



Fundamental Frequency Crystal Oscillator

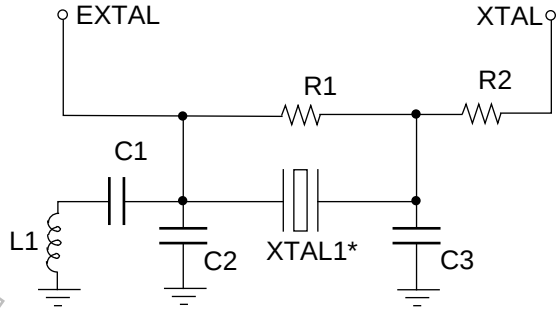
Suggested Component Values

For f_{OSC} = 4 MHz
R = 680 KΩ ± 10%
C = 20 pf ± 20%

For f_{OSC} = 30 MHz
R = 680 KΩ ± 10%
C = 20 pf ± 20%

NOTE:

1. The suggested crystal source is ICM, # 433163 - 4.00 (4MHz fundamental, 20 pf load) or # 436163 - 30.00 (30 MHz fundamental, 20 pf load).



3rd Overtone Crystal Oscillator

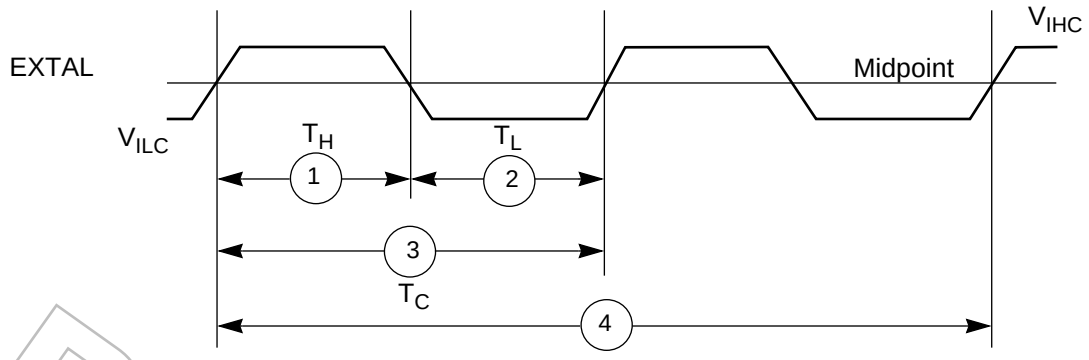
Suggested Component Values

R1 = 470 KΩ ± 10%
R2 = 330 Ω ± 10%
C1 = 0.1 µf ± 20%
C2 = 26 pf ± 20%
C3 = 20 pf ± 10%
L1 = 2.37 µH ± 10%
XTAL = 33 MHz, AT cut, 20 pf load, 50Ω max series resistance

NOTES:

1. *3rd overtone crystal.
2. The suggested crystal source is ICM, # 471163 - 33.00 (33 MHz 3rd overtone, 20 pf load).
3. R2 limits crystal current.
4. Reference Benjamin Parzen, The Design of Crystal and Other Harmonic Oscillators, John Wiley & Sons, 1983.

Figure 3 Crystal Oscillator Circuits



NOTE: The midpoint is $V_{ILC} + 0.5 (V_{IHC} - V_{ILC})$.

Figure 4 External Clock Timing

Table 9 Clock Operation

Num	Characteristics	Symbol	20.5 MHz		27 MHz		33 MHz		Unit
			Min	Max	Min	Max	Min	Max	
	Min Frequency of Operation (EXTAL Pin)	f	4	20.5	4	27.0	4	33.0	MHz
1	Clock Input High (See Note) • 46.7% - 53.3% duty cycle	T_H	22	150	17	150	13.5	150	ns
2	Clock Input Low (See Note) • 46.7% - 53.3% duty cycle	T_L	22	150	17	150	13.5	150	ns
3	Clock Cycle Time	T_C	48.75	250	37	250	30	250	ns
4	Instruction Cycle Time = $I_{CYC} = 2 \times T_C$ (See Note)	I_{CYC}	97.5	500	74	500	60	500	ns

NOTE: External Clock Input High and External Clock Input Low are measured at 50% of the input transition.

Reset, Stop, Mode Select, and Interrupt Timing

V_{CC} = 5.0 Vdc ± 10% for 20.5 MHz and 27 MHz, V_{CC} = 5.0 Vdc ± 5% for 33 MHz, T_J = -40° to +105° C, C_L = 50 pF + 1 TTL Load

WS = Number of wait states (1 WS = T_C) programmed into external bus access using BCR (WS = 0 - 15)

Table 10 Reset, Stop, Mode Select, and Interrupt Timing

Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
9	Delay from $\overline{\text{RESET}}$ Assertion to Address High Impedance (periodically sampled and not 100% tested).	—	50	—	38	—	31	ns
10	Minimum Stabilization Duration • Internal Osc. (See Note 1)	$75000 \times T_C$	—	$75000 \times T_C$	—	$75000 \times T_C$	—	ns
	• External clock (See Note 2)	$25 \times T_C$	—	$25 \times T_C$	—	$25 \times T_C$	—	ns
11	Delay from Asynchronous $\overline{\text{RESET}}$ Deassertion to First External Address Output (Internal Reset Deassertion)	$8 \times T_C$	$9 \times T_C$ + 40	$8 \times T_C$	$9 \times T_C$ + 31	$8 \times T_C$	$9 \times T_C$ + 25	ns
12	Synchronous Reset Setup Time from $\overline{\text{RESET}}$ Deassertion to Falling Edge of External Clock	20	T_C - 10	15	T_C - 8	13	T_C - 7	ns
13	Synchronous Reset Delay Time from the Falling Edge of External Clock to the First External Address Output	$8 \times T_C$ + 5	$8 \times T_C$ + 30	$8 \times T_C$ + 5	$8 \times T_C$ + 23	$8 \times T_C$ + 5	$8 \times T_C$ + 19	ns
14	Mode Select Setup Time	100	—	77	—	62	—	ns
15	Mode Select Hold Time	0	—	0		0		ns
16	Minimum Edge-triggered Interrupt Request Assertion Width	25	—	17	—	16	—	ns
16a	Minimum Edge-triggered Interrupt Request Deassertion Width	15	—	10	—	10	—	ns
17	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, Assertion to External Memory Access Address Out Valid • Caused by First Interrupt Instruction Fetch	$5 \times T_C + T_H$	—	$5 \times T_C + T_H$	—	$5 \times T_C + T_H$	—	ns
	• Caused by First Interrupt Instruction Execution	$9 \times T_C + T_H$	—	$9 \times T_C + T_H$	—	$9 \times T_C + T_H$	—	ns

Table 10 Reset, Stop, Mode Select, and Interrupt Timing (continued)

Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
18	Delay from $\overline{IRQA}$, $\overline{IRQB}$, Assertion to General Purpose Transfer Output Valid caused by First Interrupt Instruction Execution	$11 + T_C + T_H$	—	$11 \times T_C + T_H$	—	$11 \times T_C + T_H$	—	ns
19	Delay from Address Output Valid caused by First Interrupt Instruction Execute to Interrupt Request Deassertion for Level Sensitive Fast Interrupts (See Note 3)	—	$2 \times T_C + T_L + (T_C \times WS) - 44$	—	$2 \times T_C + T_L + (T_C \times WS) - 34$	—	$2 \times T_C + T_L + (T_C \times WS) - 27$	ns
20	Delay from $\overline{RD}$ Assertion to Interrupt Request Deassertion for Level Sensitive Fast Interrupts (See Note 3)	—	$2 \times T_C + (T_C \times WS) - 40$	—	$2 \times T_C + (T_C \times WS) - 31$	—	$2 \times T_C + (T_C \times WS) - 25$	ns
21	Delay from $\overline{WR}$ Assertion to Interrupt Request Deassertion for Level Sensitive-Fast Interrupts							
	• WS = 0	—	$2 \times T_C - 40$	—	$2 \times T_C - 31$	—	$2 \times T_C - 25$	ns
	• WS > 0 (See Note 3)	—	$T_C + T_L + (T_C \times WS) - 40$	—	$T_C + T_L + (T_C \times WS) - 31$	—	$T_C + T_L + (T_C \times WS) - 25$	ns
22	Delay from General-Purpose Output Valid to Interrupt Request Deassertion for Level Sensitive Fast Interrupts - If Second Interrupt Instruction is:							
	• Single cycle	—	$T_L - 60$	—	$T_L - 46$	—	$T_L - 37$	ns
	• Two cycles (See Note 3)	—	$(2 \times T_C) + T_L - 60$	—	$(2 \times T_C) + T_L - 46$	—	$(2 \times T_C) + T_L - 37$	ns
23	Synchronous Interrupt Setup Time from $\overline{IRQA}$, $\overline{IRQB}$, Assertion to the Rising Edge of External Clock	25	$T_C - 10$	19	$T_C - 8$	16	$T_C - 7$	ns
24	Synchronous Interrupt Delay Time from the Rising Edge External Clock to the First External Address Output Valid caused by the First Instruction Fetch after coming out of Wait State	$13 \times T_C + T_H + 7$	$13 \times T_C + T_H + 30$	$13 \times T_C + T_H + 6$	$13 \times T_C + T_H + 23$	$13 \times T_C + T_H + 5$	$13 \times T_C + T_H + 19$	ns
25	Duration for $\overline{IRQA}$ Assertion to Recover from stop state	25	—	19	—	16	—	ns

Table 10 Reset, Stop, Mode Select, and Interrupt Timing (continued)

Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
26	Delay from $\overline{IRQA}$ Assertion to Fetch of First Interrupt Instruction (when exiting 'STOP') • Internal Crystal Oscillator Clock, OMR bit 6 = 0 • Stable External Clock, OMR bit 6 = 1 (See Note 4)	65548 × T_C 20 × T_C	— —	65548 × T_C 20 × T_C	— —	65548 × T_C 20 × T_C	— —	ns ns
27	Duration of Level Sensitive $\overline{IRQA}$ Assertion to ensure interrupt service (when exiting 'STOP') • Internal Crystal Oscillator Clock, OMR bit 6 = 0 • Stable External Clock, OMR bit 6 = 1 (See Note 4)	65534 × T_C + T_L 6 × T_C + T_L	— —	65534 × T_C + T_L 6 × T_C + T_L	— —	65534 × T_C + T_L 6 × T_C + T_L	— —	ns ns
28	Delay from Level Sensitive $\overline{IRQA}$ Assertion to Fetch of First Interrupt Instruction (when exiting 'Stop') • Internal Crystal Oscillator Clock, OMR bit 6 = 0 • Stable External Clock, OMR bit 6 = 1 (See Note 4)	65548 × T_C 20 × T	— —	65548 × T_C 20 × T_C	— —	65548 × T_C 20 × T_C	— —	ns ns

NOTES:

1. A clock stabilization delay is required when using the on-chip crystal oscillator in two cases:
   - after power-on reset, and
   - when recovering from Stop mode.

   During this stabilization period, T_C, T_H and T_L will not be constant. Since this stabilization period varies, a delay of 75,000 × T_C is typically allowed to assure that the oscillator is stable before executing programs. While it is possible to set OMR bit 6 = 1 when using the internal crystal oscillator, it is not recommended and these specifications do not guarantee timings for that case.

2. Circuit stabilization delay is required during reset when using an external clock in two cases:
   - after power-on reset, and
   - when recovering from Stop mode.

3. When using fast interrupts and $\overline{IRQA}$ and $\overline{IRQB}$ are defined as level-sensitive, then timings 19 through 22 apply to prevent multiple interrupt service. To avoid these timing restrictions, the deassertive edge-triggered mode is recommended when using fast interrupt. Long interrupts are recommended when using level-sensitive mode.

4. A clock stabilization delay is required when using the on-chip crystal oscillator in two cases:
   - after power-on reset, and
   - when recovering from Stop mode.

   During this stabilization period, T_C, T_H and T_L will not be constant. Since this stabilization period varies, a delay of 75,000 × T_C is typically allowed to assure that the oscillator is stable before executing programs. While it is possible to set OMR bit 6 = 1 when using the internal crystal oscillator, it is not recommended and these specifications do not guarantee timings for that case.

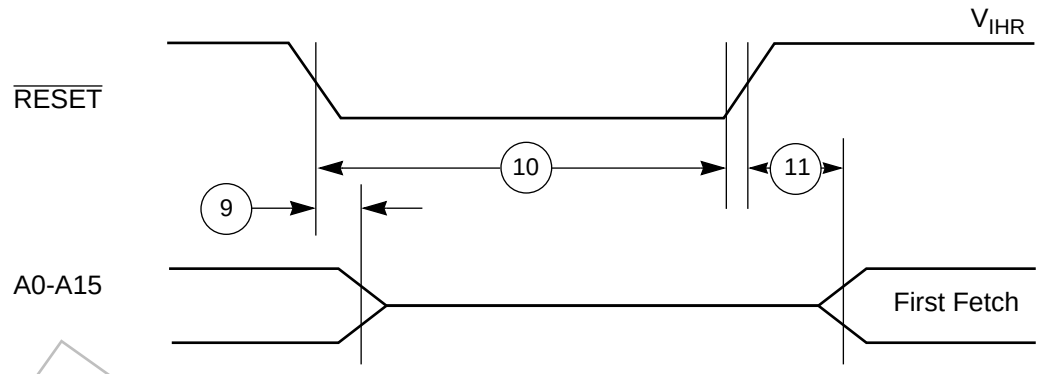


Figure 5 Reset Timing

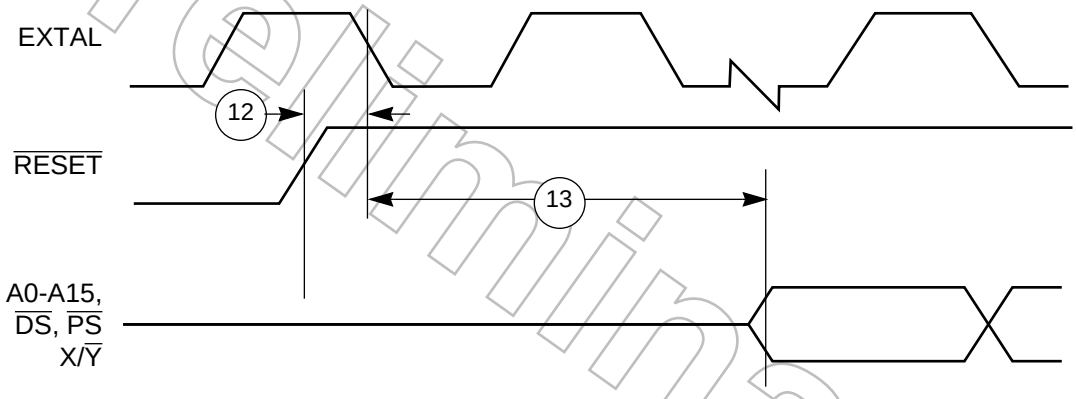


Figure 6 Synchronous Reset Timing

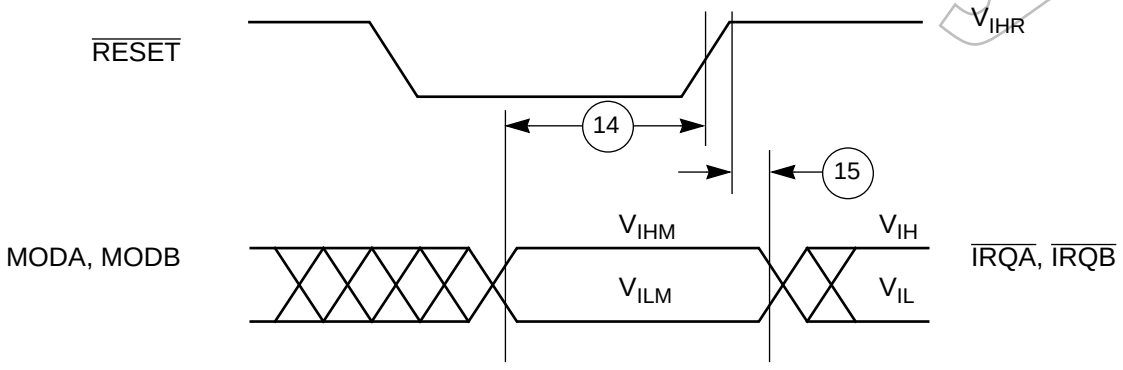


Figure 7 Operating Mode Select Timing

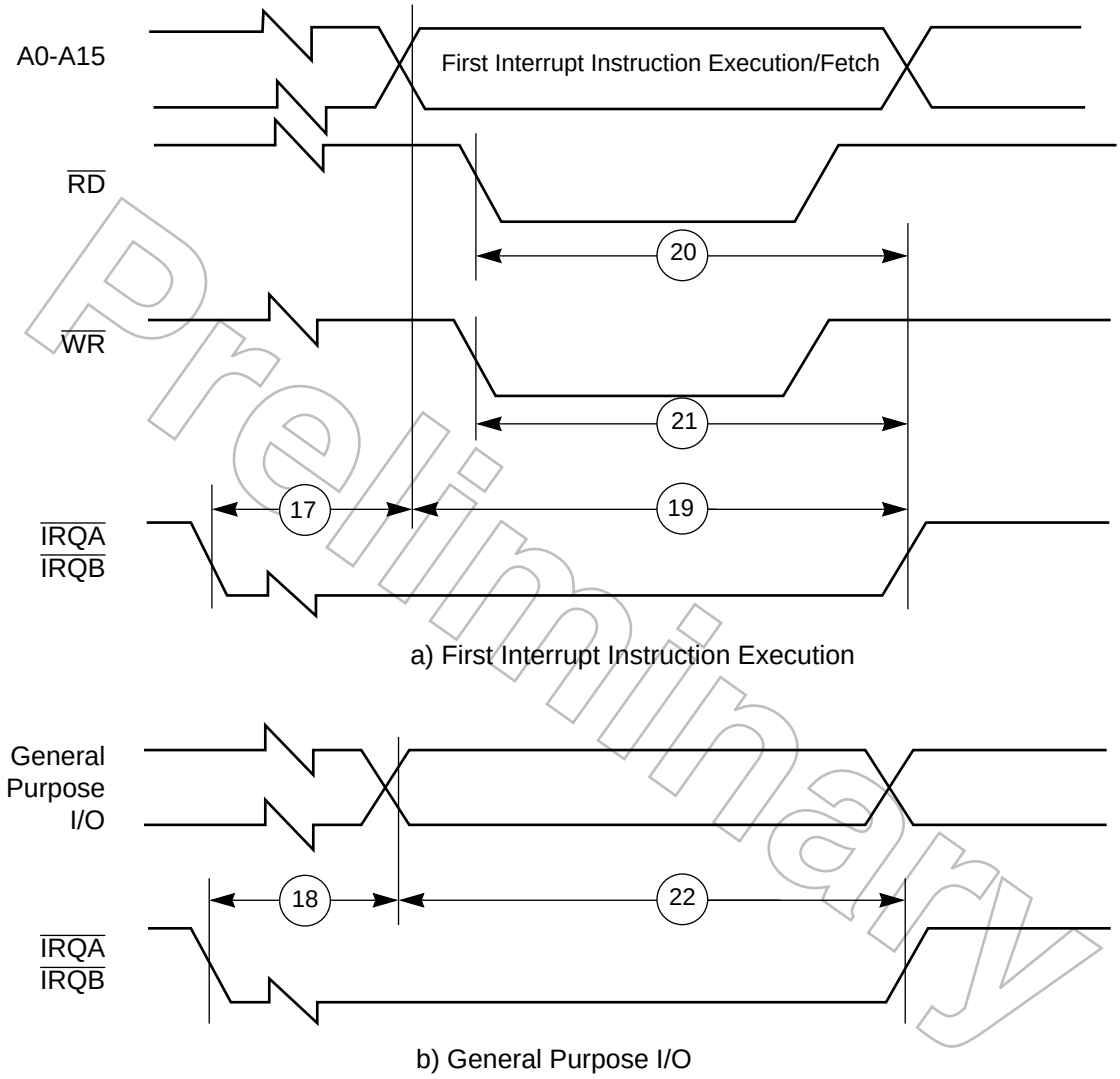


Figure 8 External Level-Sensitive Fast Interrupt Timing

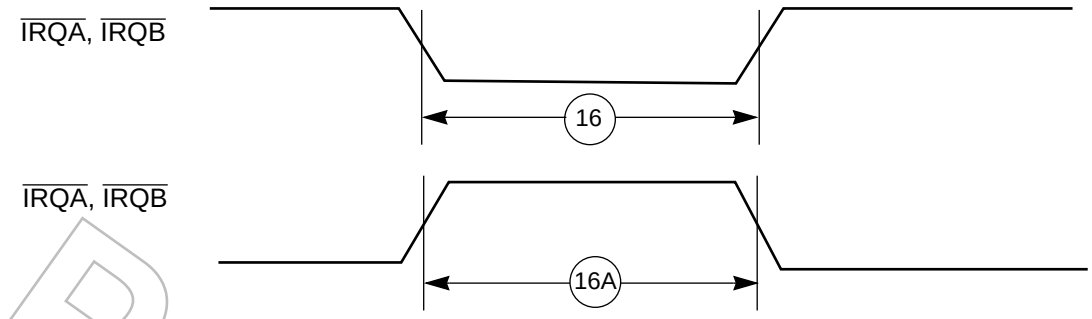


Figure 9 External Interrupt Timing (Negative Edge-Triggered)

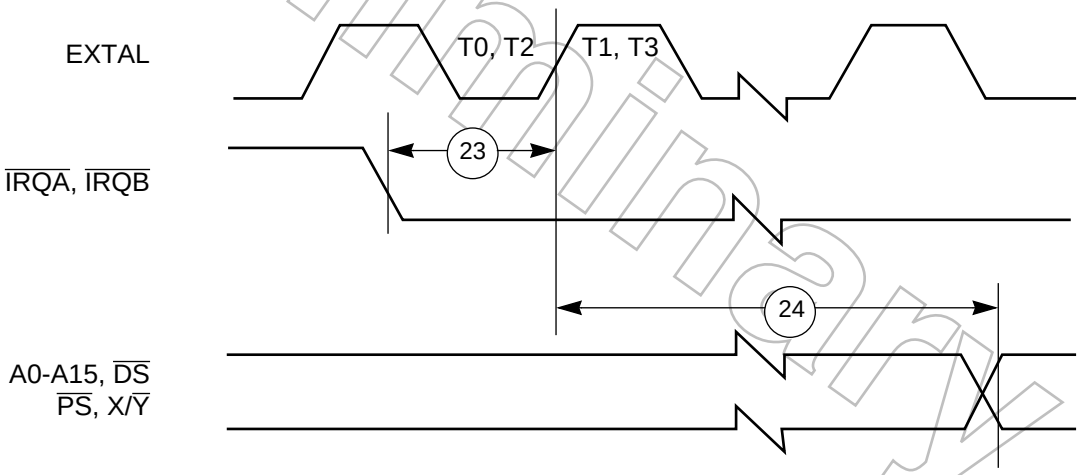


Figure 10 Synchronous Interrupt from Wait State Timing

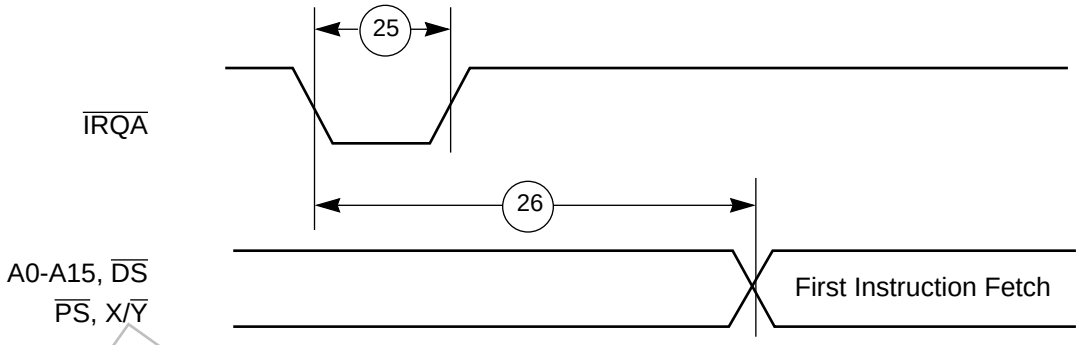


Figure 11 Recovery from Stop State Using IRQA

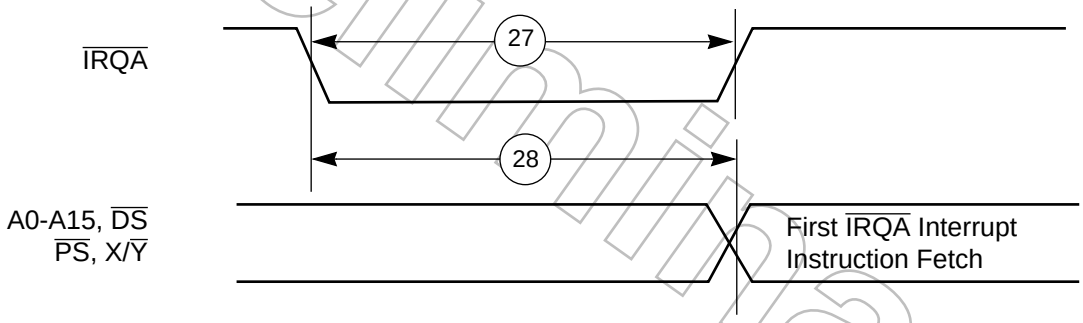


Figure 12 Recovery from Stop State Using IRQA Interrupt Service

Host I/O Timing

V_{CC} = 5.0 Vdc ± 10% for 20.5 MHz and 27 MHz, V_{CC} = 5.0 Vdc ± 5% for 33 MHz,
T_J = -40° to +105° C, C_L = 50 pF + 1 TTL Load

Active low lines should be "pulled up" in a manner consistent with the AC and DC specifications.

Table 11 Host I/O Timing

Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
30	Host Synchronous Delay (see Note 1)	T_L	$T_C + T_L$	T_L	$T_C + T_L$	T_L	$T_C + T_L$	ns
31	$\overline{HEN}/\overline{HACK}$ Assertion Width (See Note 2) • CVR, ICR, ISR, RXL Read	$T_C + 60$	—	$T_C + 46$	—	$T_C + 37$	—	ns
	• VR, RXH/M Read	50	—	39	—	31	—	ns
	• Write	25	—	19	—	16	—	ns
32	$\overline{HEN}/\overline{HACK}$ Deassertion Width (See Note 2)	25	—	19	—	16	—	ns
	• Between Two TXL Writes (See Note 3)	$2 \times T_C + 60$	—	$2 \times T_C + 46$	—	$2 \times T_C + 37$	—	ns
	• Between Two CVR, ICR, ISR, RXL Reads (See Note 4)	$2 \times T_C + 60$	—	$2 \times T_C + 46$	—	$2 \times T_C + 37$	—	ns
33	Host Data Input Setup Time Before $\overline{HEN}/\overline{HACK}$ Deassertion	5	—	4	—	4	—	ns
34	Host Data Input Hold Time After $\overline{HEN}/\overline{HACK}$ Deassertion	5	—	4	—	4	—	ns
35	$\overline{HEN}/\overline{HACK}$ Assertion to Output Data Active from High Impedance	0	—	0	—	0	—	ns
36	$\overline{HEN}/\overline{HACK}$ Assertion to Output Data Valid	—	50	—	39	—	31	ns
37	$\overline{HEN}/\overline{HACK}$ Deassertion to Output Data High Impedance (See Note 6)	—	35	—	27	—	22	ns
38	Output Data Hold Time After $\overline{HEN}/\overline{HACK}$ Deassertion (See Note 7)	5	—	4	—	4	—	ns
39	HR/$\overline{W}$ Low Setup Time Before $\overline{HEN}$ Assertion	0	—	0	—	0	—	ns
40	HR/$\overline{W}$ Low Hold Time After $\overline{HEN}$ Deassertion	5	—	4	—	4	—	ns
41	HR/$\overline{W}$ High Setup Time to $\overline{HEN}$ Assertion	0	—	0	—	0	—	ns

Table 11 Host I/O Timing (continued)

Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
42	HR/$\overline{W}$ High Hold Time After $\overline{HEN}$/$\overline{HACK}$ Deassertion	5	—	4	—	4	—	ns
43	HA0-HA2 Setup Time Before $\overline{HEN}$ Assertion	0	—	0	—	0	—	ns
44	HA0-HA2 Hold Time After $\overline{HEN}$ Deassertion	5	—	4	—	4	—	ns
45	DMA $\overline{HACK}$ Assertion to $\overline{HREQ}$ Deassertion (See Note 5)	5	60	4	46	4	46	ns
46	DMA $\overline{HACK}$ Deassertion to $\overline{HREQ}$ Assertion (See Notes 4, 5)							
	• for DMA RXL Read	$t_{HSDL} + T_C + T_H + 5$	—	$t_{HSDL} + T_C + T_H + 4$	—	$t_{HSDL} + T_C + T_H + 4$	—	ns
	• for DMA TXL Write	$t_{HSDL} + T_C + 5$	—	$t_{HSDL} + T_C + 4$	—	$t_{HSDL} + T_C + 4$	—	ns
	• all other cases	5	—	4	—	4	—	ns
47	Delay from $\overline{HEN}$ Deassertion to $\overline{HREQ}$ Assertion for RXL Read (See Notes 4, 5)	$t_{HSDL} + T_C + T_H + 5$	—	$t_{HSDL} + T_C + T_H + 4$	—	$t_{HSDL} + T_C + T_H + 4$	—	ns
48	Delay from $\overline{HEN}$ Deassertion to $\overline{HREQ}$ Assertion for TXL Write (See Notes 4, 5)	$t_{HSDL} + T_C + 5$	—	$t_{HSDL} + T_C + 4$	—	$t_{HSDL} + T_C + 4$	—	ns
49	Delay from $\overline{HEN}$ Assertion to $\overline{HREQ}$ Deassertion for RXL Read, TXL Write (See Notes 4, 5)	5	75	4	70	4	65	ns

NOTES:

1. Host synchronization delay (t_{HSDL}) is the time period required for the DSP56001 to sample any external asynchronous input signal, determine whether it is high or low, and synchronize it to the DSP56001 internal clock.
2. See **HOST PORT CONSIDERATIONS**.
3. This timing must be adhered to only if two consecutive writes to the TXL are executed without polling TXDE or $\overline{HREQ}$.
4. This timing must be adhered to only if two consecutive reads from one of these registers are executed without polling the corresponding status bits or $\overline{HREQ}$
5. $\overline{HREQ}$ is pulled up by a 1 kΩ resistor.
6. Specifications are periodically sampled and not 100% tested.
7. May decrease to 0 ns for future versions.

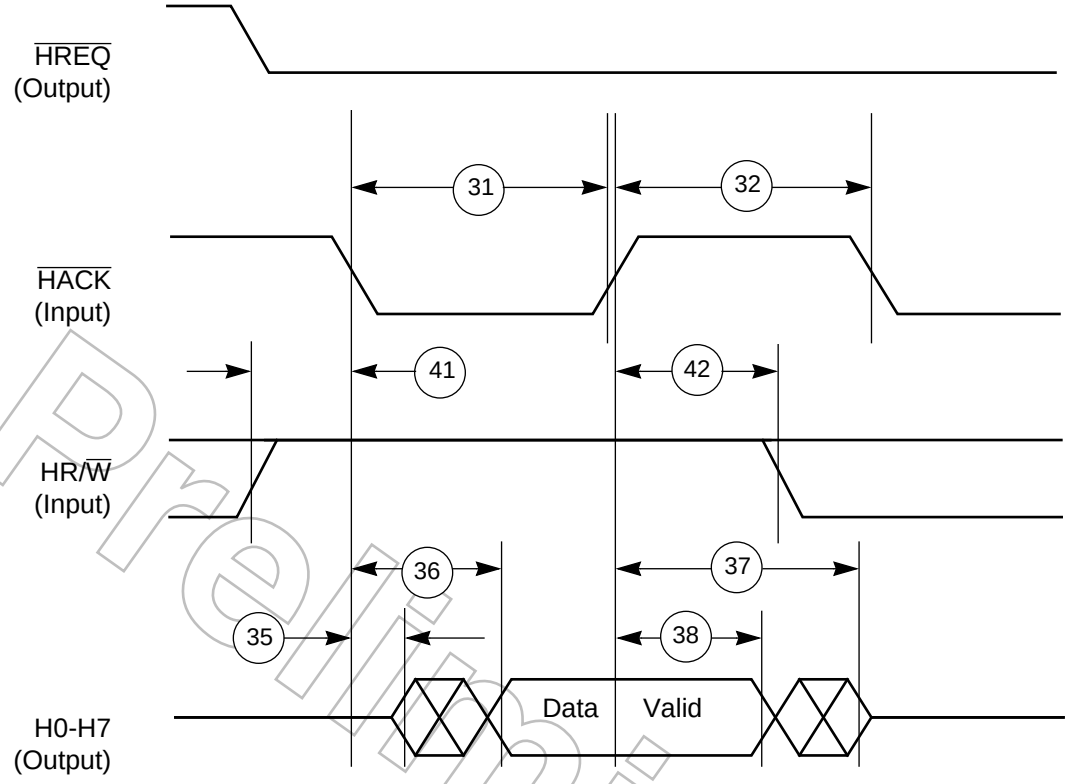


Figure 13 Host Interrupt Vector Register (IVR) Read

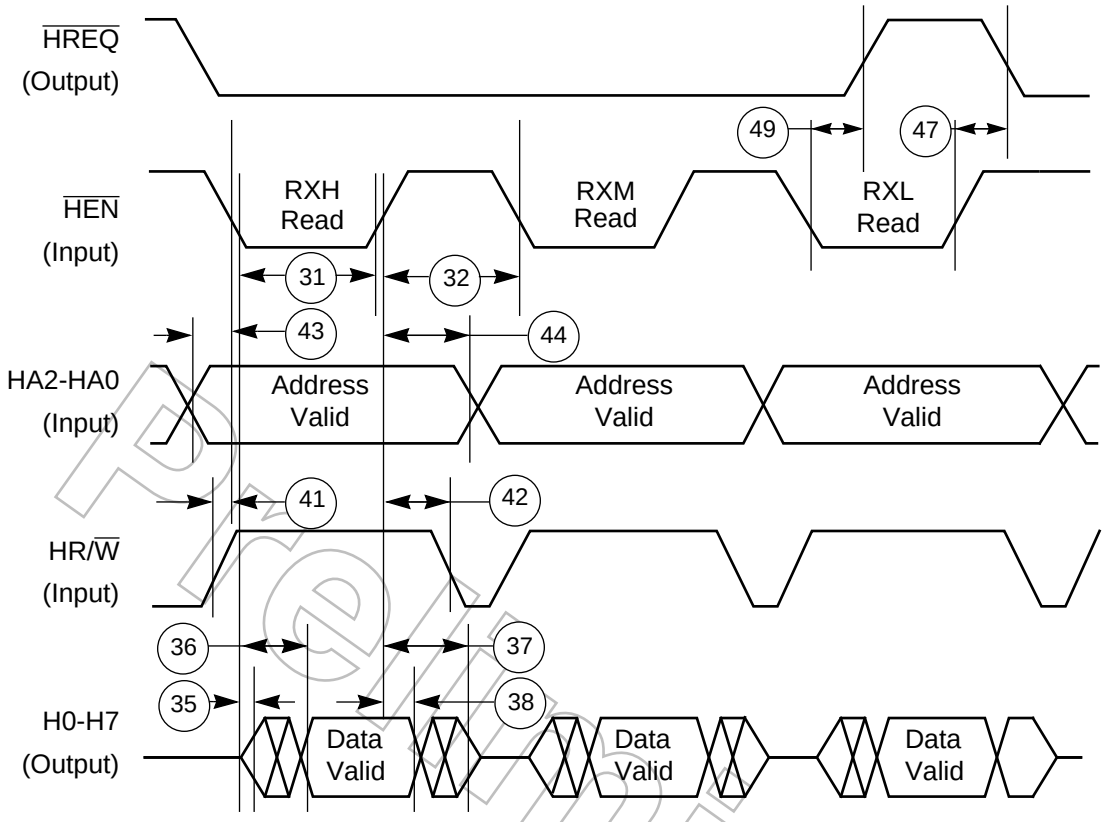


Figure 14 Host Read Cycle (Non-DMA Mode)

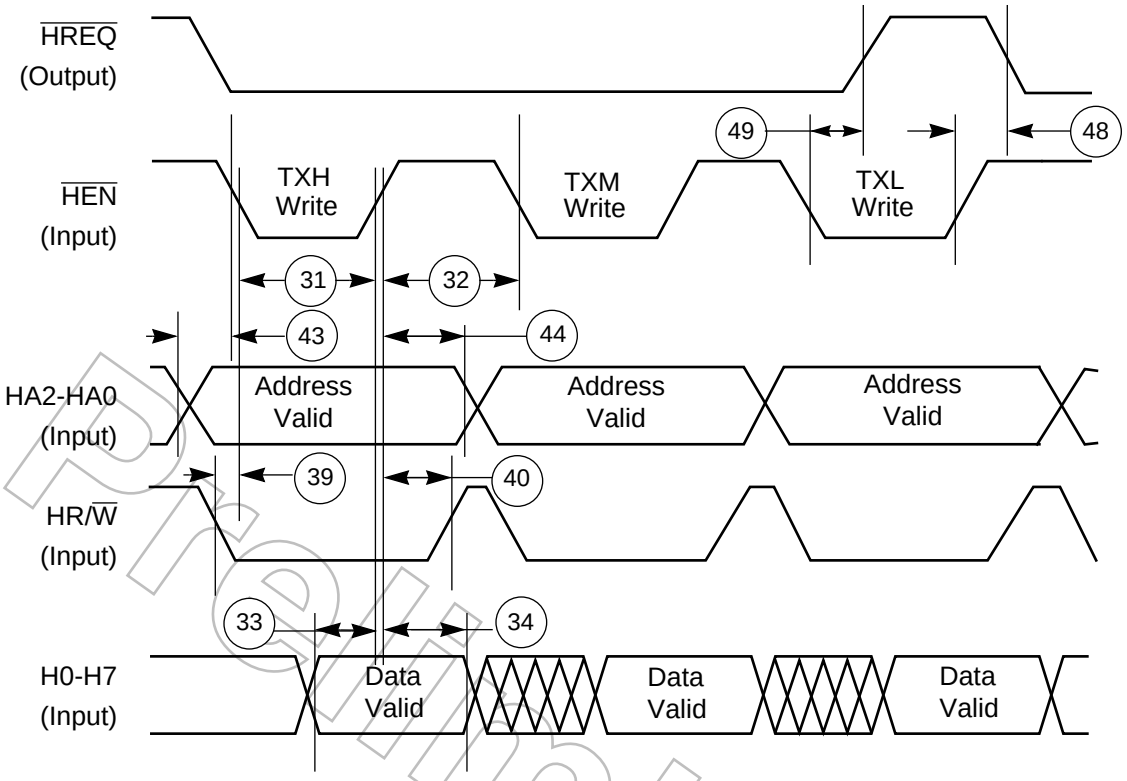


Figure 15 Host Write Cycle (Non-DMA Mode)

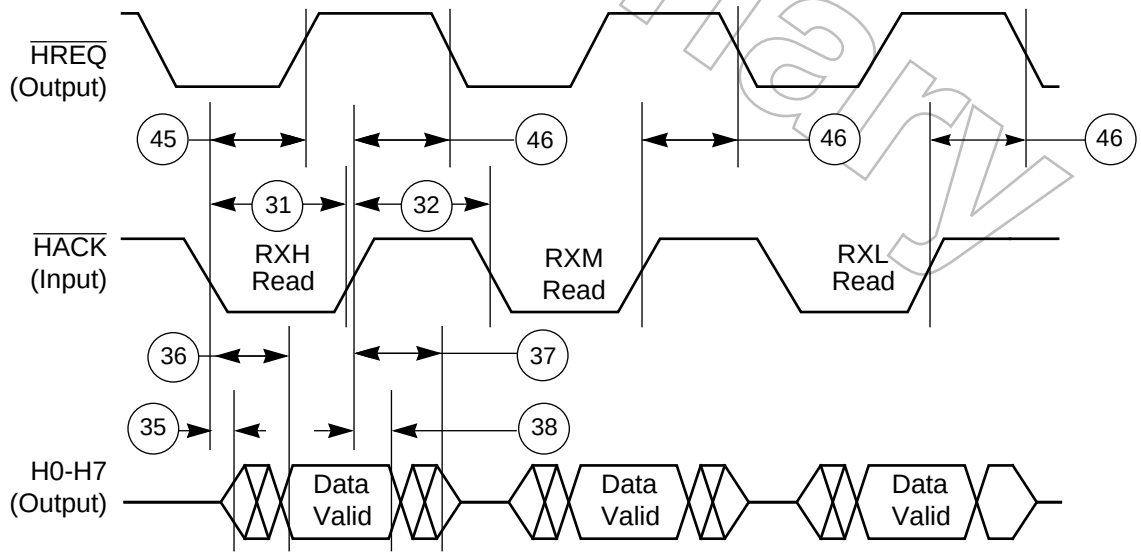


Figure 16 Host DMA Read Cycle

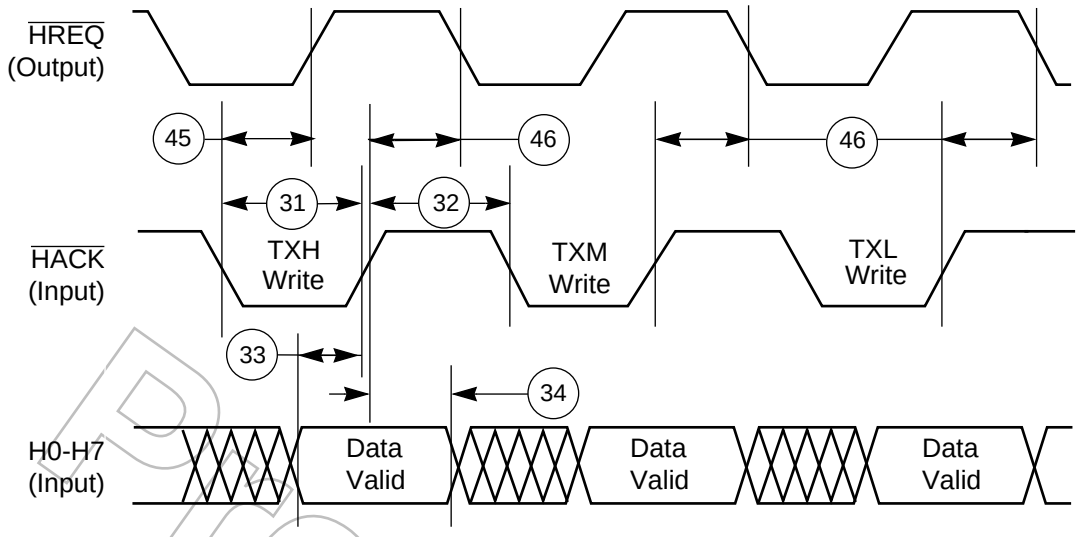


Figure 17 Host DMA Write Cycle

Synchronous Communications Interface (SCI) Timing

V_{CC} = 5.0 Vdc ± 10% for 20.5 MHz and 27 MHz, V_{CC} = 5.0 Vdc ± 5% for 33 MHz,
T_J = -40° to +105° C, C_L = 50 pF + 1 TTL Load

t_{SCC} = Synchronous Clock Cycle Time (for internal clock, t_{SCC} is determined by the SCI clock control register and T_C)

Table 12 SCI Synchronous Mode Timing

Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
55	Synchronous Clock Cycle — t_{SCC}	$8 \times T_C$	—	$8 \times T_C$	—	$8 \times T_C$	—	ns
56	Clock Low Period	$4 \times T_C$ - 20	—	$4 \times T_C$ - 15	—	$4 \times T_C$ - 13	—	ns
57	Clock High Period	$4 \times T_C$ - 20	—	$4 \times T_C$ - 15	—	$4 \times T_C$ - 13	—	ns
58	< intentionally blank >	—	—	—	—	—	—	—
59	Output Data Setup to Clock Falling Edge (Internal Clock)	$2 \times T_C$ + T_L - 50	—	$2 \times T_C$ + T_L - 39	—	$2 \times T_C$ + T_L - 31	—	ns
60	Output Data Hold After Clock Rising Edge (Internal Clock)	$2 \times T_C$ - T_L - 15	—	$2 \times T_C$ - T_L - 11	—	$2 \times T_C$ - T_L - 9	—	ns
61	Input Data Setup Time Before Clock Rising Edge (Internal Clock)	$2 \times T_C$ + T_L + 45	—	$2 \times T_C$ + T_L + 35	—	$2 \times T_C$ + T_L + 28	—	ns
62	Input Data Not Valid Before Clock Rising Edge (Internal Clock)	—	$2 \times T_C$ + T_L - 10	—	$2 \times T_C$ + T_L - 8	—	$2 \times T_C$ + T_L - 6	ns
63	Clock Falling Edge to Output Data Valid (External Clock)	—	63	—	48	—	39	ns
64	Output Data Hold After Clock Rising Edge (External Clock)	T_C + 12	—	T_C + 9	—	T_C + 8	—	ns
65	Input Data Setup Time Before Clock Rising Edge (External Clock)	30	—	23	—	19	—	ns
66	Input Data Hold Time After Clock Rising Edge (External Clock)	40	—	31	—	25	—	ns

Table 13 SCI Asynchronous Mode Timing — 1X Clock

Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
67	Asynchronous Clock Cycle — t_{ACC}	$64 \times T_C$	—	$64 \times T_C$	—	$64 \times T_C$	—	ns
68	Clock Low Period	$32 \times T_C$ - 20	—	$32 \times T_C$ - 15	—	$32 \times T_C$ - 13	—	ns
69	Clock High Period	$32 \times T_C$ - 20	—	$32 \times T_C$ - 15	—	$32 \times T_C$ - 13	—	ns
70	< intentionally blank >	—	—	—	—	—	—	—
71	Output Data Setup to Clock Rising Edge (Internal Clock)	$32 \times T_C$ - 100	—	$32 \times T_C$ - 77	—	$32 \times T_C$ - 61	—	ns
72	Output Data Hold After Clock Rising Edge (Internal Clock)	$32 \times T_C$ - 100	—	$32 \times T_C$ - 77	—	$32 \times T_C$ - 61	—	ns

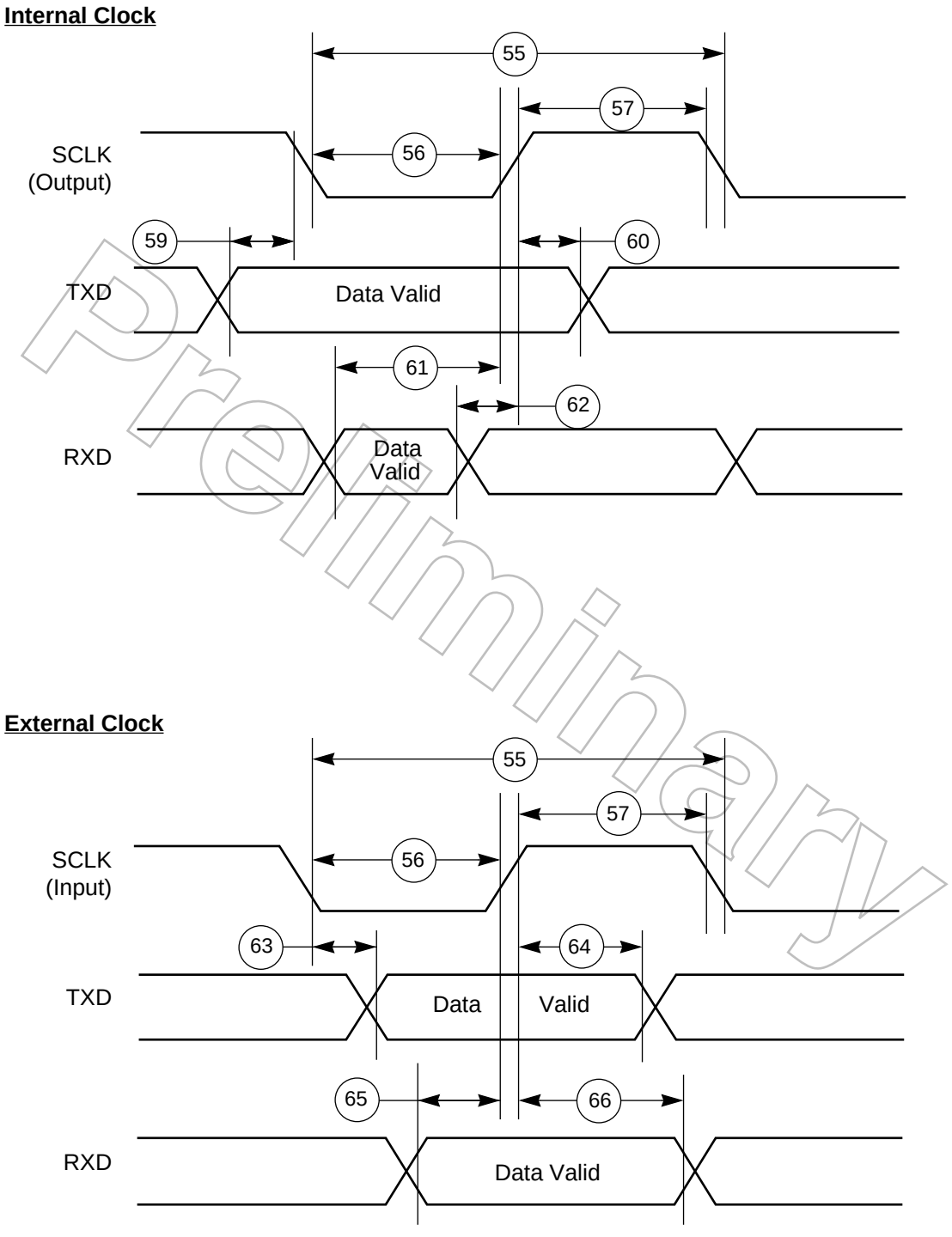
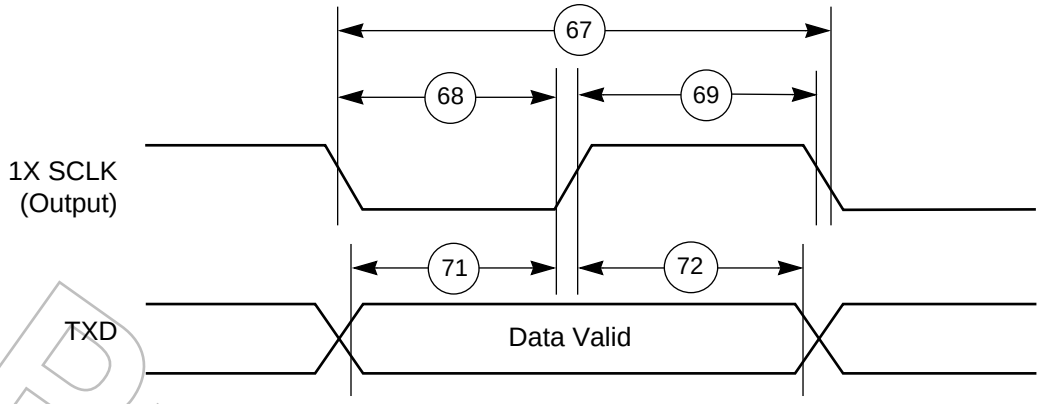


Figure 18 SCI Synchronous Mode Timing



NOTE: In the wire-OR mode, TXD can be pulled up by 1 KΩ

Figure 19 SCI Asynchronous Mode Timing

Synchronous Serial Interface (SSI) Timing

V_{CC} = 5.0 Vdc ± 10% for 20.5 MHz and 27 MHz, V_{CC} = 5.0 Vdc ± 5% for 33 MHz,
T_J = -40° to +105° C, C_L = 50 pF + 1 TTL Load

t_{SSICC} = SSI clock cycle time
TXC (SCK Pin) = Transmit Clock
RXC (SC0 or SCK Pin) = Receive Clock
FST (SC2 Pin) = Transmit Frame Sync
FSR (SC1 or SC2 Pin) = Receive Frame Sync
ick = Internal Clock
xck = External Clock
gck = Gated Clock
icka = Internal Clock, Asynchronous Mode (Asynchronous implies that STD and SRD are two different clocks)
icks = Internal Clock, Synchronous Mode (Synchronous implies that STD and SRD are the same clock)
bl = bit length
wl = word length

Table 14 SSI Timing

Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Case	Unit
		Min	Max	Min	Max	Min	Max		
80	Clock Cycle — t_{SSICC} (See Note 1)	$4 \times T_C$	—	$4 \times T_C$	—	$4 \times T_C$	—	—	ns
81	Clock High Period	$2 \times T_C$ - 20	—	$2 \times T_C$ - 15	—	$2 \times T_C$ - 13	—		ns
82	Clock Low Period	$2 \times T_C$ - 20	—	$2 \times T_C$ - 15	—	$2 \times T_C$ - 13	—	—	ns
83	< intentionally blank >	—	—	—	—	—	—	—	—
84	SRD Rising Edge to FSR Out (bl) High	— —	80 50	— —	61 38	— —	48 31	x ck i ck a	ns ns
85	SRD Rising Edge to FSR Out (bl) Low	— —	70 40	— —	54 31	— —	43 25	x ck i ck a	ns ns
86	SRD Rising Edge to FSR Out (wl) High	— —	70 40	— —	54 31	— —	43 25	x ck i ck a	ns ns
87	RXC Rising Edge to FSR Out (wl) Low	— —	70 40	— —	54 31	— —	43 25	x ck i ck a	ns ns

Table 14 SSI Timing (continued)

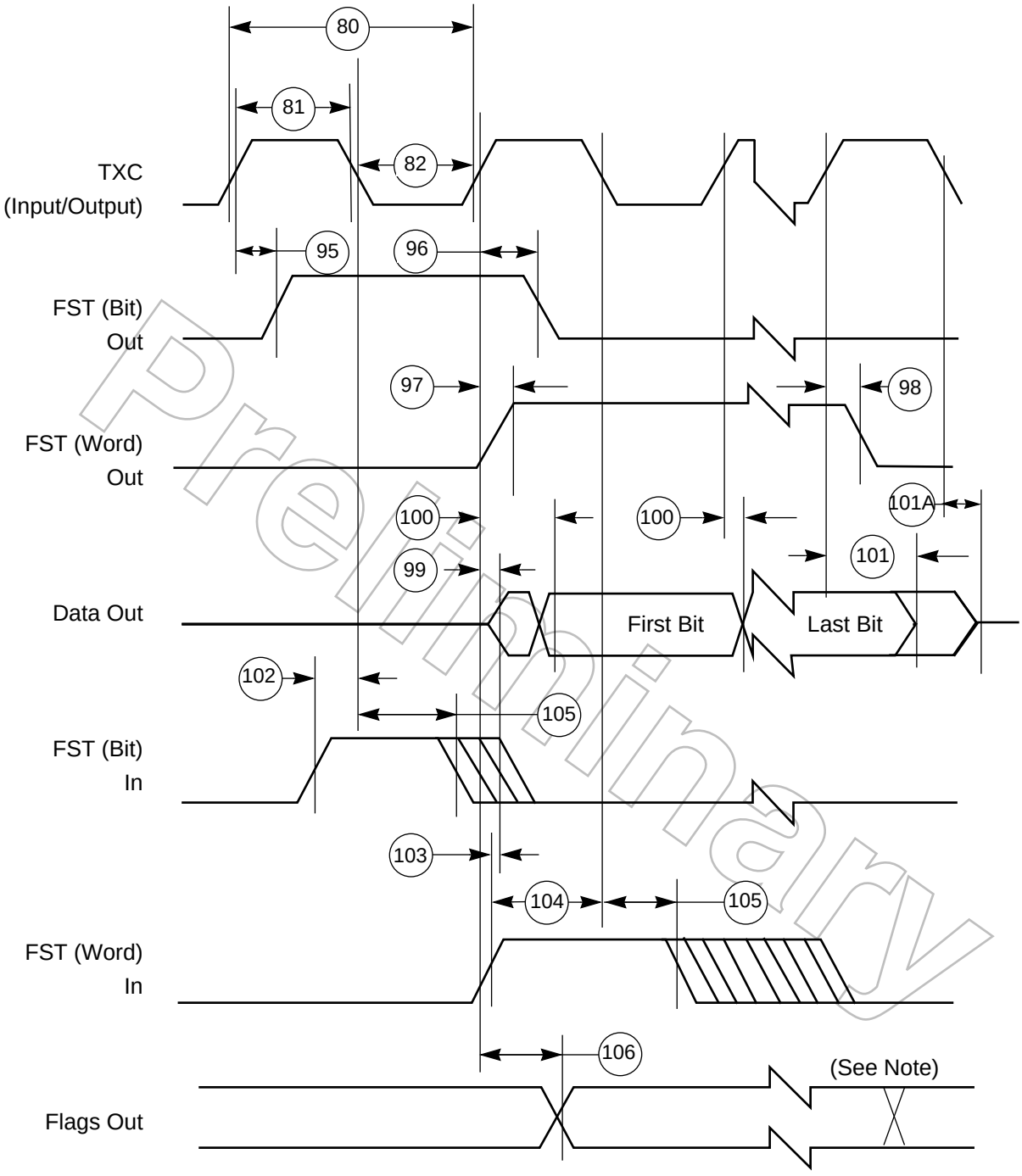
Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Case	Unit
		Min	Max	Min	Max	Min	Max		
88	Data In Setup Time Before RXC (SCK in Synchronous Mode) Falling Edge	15 35 25	— — —	12 27 19	— — —	10 22 16	— — —	x ck i ck a i ck s	ns ns ns
89	Data In Hold Time After RXC Falling Edge	35 5	— —	27 4	— —	22 4	— —	x ck i ck	ns ns
90	FSR Input (bl) High Before RXC Falling Edge	15 35	— —	12 27	— —	10 23	— —	x ck i ck a	ns ns
91	FSR Input (wl) High Before RXC Falling Edge	20 55	— —	15 42	— —	13 34	— —	x ck i ck a	ns ns
92	FSR Input Hold Time After RXC Falling Edge	35 5	— —	27 4	— —	22 4	— —	x ck i ck	ns ns
93	Flags Input Setup Before RXC Falling Edge	30 50	— —	23 39	— —	19 31	— —	x ck i ck s	ns ns
94	Flags Input Hold Time After RXC Falling Edge	35 5	— —	27 4	— —	22 4	— —	x ck i ck s	ns ns
95	TXC Rising Edge to FST Out (bl) High	— —	70 30	— —	54 23	— —	43 19	x ck i ck	ns ns
96	TXC Rising Edge to FST Out (bl) Low	— —	65 35	— —	50 27	— —	40 22	x ck i ck	ns ns
97	TXC Rising Edge to FST Out (wl) High	— —	65 35	— —	50 27	— —	40 22	x ck i ck	ns ns
98	TXC Rising Edge to FST Out (wl) Low	— —	65 35	— —	50 27	— —	40 22	x ck i ck	ns ns
99	TXC Rising Edge to Data Out Enable from High Impedance	— —	65 40	— —	50 31	— —	40 25	x ck i ck	ns ns
100	TXC Rising Edge to Data Out Valid	— —	65 40	— —	50 31	— —	40 25	x ck i ck	ns ns
101	TXC Rising Edge to Data Out High Impedance (See Note 2)	— —	70 40	— —	54 31	— —	43 25	x ck i ck	ns ns
101A	TXC Falling Edge to Data Out High Impedance (See Note 2)	—	$T_C + T_H$	—	$T_C + T_H$	—	$T_C + T_H$	g ck	ns
102	FST Input (bl) Setup Time Before TXC Falling Edge	15 35	— —	12 27	— —	10 23	— —	x ck i ck	ns ns
103	FST Input (wl) to Data Out Enable from High Impedance	—	60	—	46	—	37		ns

Table 14 SSI Timing (continued)

Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Case	Unit
		Min	Max	Min	Max	Min	Max		
104	FST Input (wl) Setup Time Before TXC Falling Edge	20 55	— —	15 42	 — —	13 34	— —	x ck i ck	ns ns
105	FST Input Hold Time After TXC Falling Edge	35 5	— —	27 4	— —	22 4	— —	x ck i ck	ns ns
106	Flag Output Valid After TXC Rising Edge	— —	70 40	— —	54 31	— —	43 25	x ck i ck	ns ns

NOTES:

1. For internal clock, External Clock Cycle is defined by I_{cyc} and SSI control register.
2. Periodically sampled, and not 100% tested



NOTE: In the Network mode, output flag transitions can occur at the start of each time slot within the frame. In the Normal mode, the output flag state is asserted for the entire frame period.

Figure 20 SSI Transmitter Timing

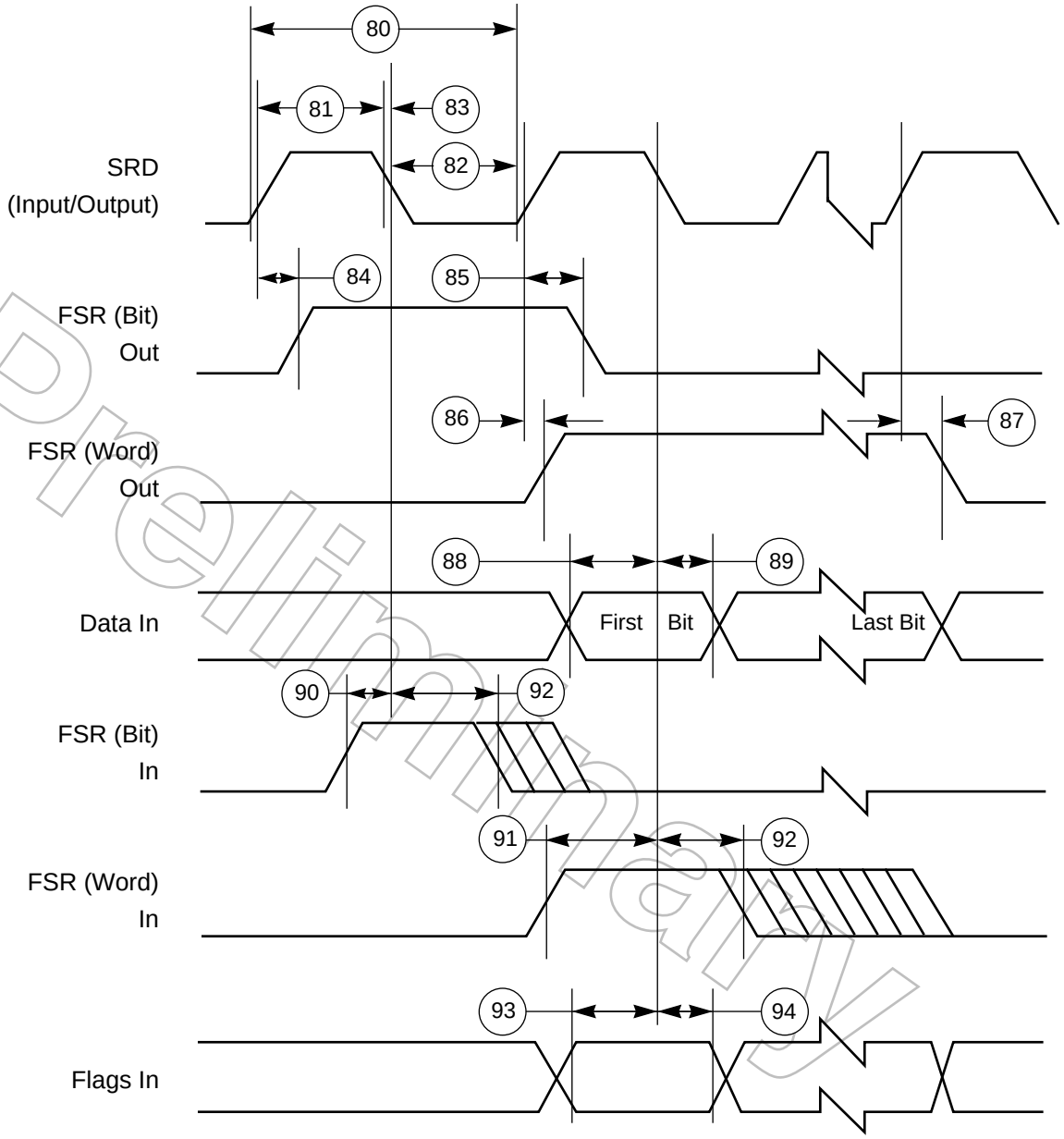


Figure 21 SSI Receiver Timing

External Bus Asynchronous Timing

V_{CC} = 5.0 Vdc ± 10% for 20.5 MHz and 27 MHz, V_{CC} = 5.0 Vdc ± 5% for 33 MHz,
T_J = -40° to +105° C, C_L = 50 pF + 1 TTL Load

WS = Number of Wait States, as determined by BCR register (WS = 0 to 15)

Capacitance Derating

The DSP56001A External Bus Timing Specifications are designed and tested at the maximum capacitive load of 50 pF, including stray capacitance. Typically, the drive capability of the External Bus pins (A0-A15, D0-D23, $\overline{PS}$, $\overline{DS}$, $\overline{RD}$, $\overline{WR}$, X/$\overline{Y}$) derates linearly at 1 ns per 12 pF of additional capacitance from 50 pF to 250 pF of loading. Port B and C pins derate linearly at 1 ns per 5 pF of additional capacitance from 50 pF to 250 pF of loading. Active low lines should be "pulled up" in a manner consistent with the AC and DC specifications.

Table 15 External Bus Asynchronous Timing

Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
115	Delay from $\overline{BR}$ Assertion to $\overline{BG}$ Assertion							
	• With no external access from the DSP	$2 \times T_C + T_H$	$4 \times T_C + T_H + 20$	$2 \times T_C + T_H$	$4 \times T_C + T_H + 15$	$2 \times T_C + T_H$	$4 \times T_C + T_H + 13$	ns
	• During external read or write access	$T_C + T_H$	$4 \times T_C + T_H + T_C \times WS + 20$	$T_C + T_H$	$4 \times T_C + T_H + T_C \times WS + 15$	$T_C + T_H$	$4 \times T_C + T_H + T_C \times WS + 13$	ns
	• During external read-modify-write access	$T_C + T_H$	$6 \times T_C + T_H + 2 \times T_C \times WS + 20$	$T_C + T_H$	$6 \times T_C + T_H + 2 \times T_C \times WS + 15$	$T_C + T_H$	$6 \times T_C + T_H + 2 \times T_C \times WS + 13$	ns
	• During stop mode — external bus will not be released and $\overline{BG}$ will not go low	∞	—	∞	—	∞	—	ns
	• During wait mode	$T_H + 4$	$T_C + T_H + 30$	$T_H + 3$	$T_C + T_H + 23$	$T_H + 3$	$T_C + T_H + 19$	ns
116	Delay from $\overline{BR}$ Deassertion to $\overline{BG}$ Deassertion	$2 \times T_C$	$4 \times T_C + 20$	$2 \times T_C$	$4 \times T_C + 15$	$2 \times T_C$	$4 \times T_C + 13$	ns
117	$\overline{BG}$ Deassertion Duration	$2 \times T_C + T_H - 10$	—	$2 \times T_C + T_H - 8$	—	$2 \times T_C + T_H - 6$	—	ns

Table 15 External Bus Asynchronous Timing (continued)

Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
118	Delay from Address, Data, and Control Bus High Impedance to $\overline{BG}$ Assertion	0	—	0	—	0	—	ns
119	Delay from $\overline{BG}$ Deassertion to Address and Control Bus Enabled	—	T_H - 10	—	T_H - 8	—	T_H - 6	ns
120	Address Valid to $\overline{WR}$ Assertion							
	• WS = 0	T_L - 9	T_L + 5	T_L - 7	T_L + 5	T_L - 5.5	T_L + 5	ns
	• WS > 0	T_C - 9	T_C + 5	T_C - 7	T_C + 5	T_C - 5.5	T_C + 5	ns
121	$\overline{WR}$ Assertion Width							
	• WS = 0	T_C - 9	—	T_C - 7	—	T_C - 5.0	—	ns
	• WS > 0	$WS \times T_C + T_L - 9$	—	$WS \times T_C + T_L - 7$	—	$WS \times T_C + T_L - 5.0$	—	ns
122	$\overline{WR}$ Deassertion to Address Not Valid	T_H - 12	—	T_H - 9	—	T_H - 7.5	—	ns
123	$\overline{WR}$ Assertion to Data Out Active From High Impedance							
	• WS = 0	T_H - 9	T_H + 10	T_H - 7	T_H + 8	T_H - 5.5	T_H + 6.5	ns
	• WS > 0	0	10	0	8	0	6.5	ns
124	Data Out Hold Time from $\overline{WR}$ Deassertion (the maximum specification is periodically sampled, and not 100% tested)	T_H - 9	T_H + 7	T_H - 7	T_H + 6	T_H - 5.5	T_H + 4.5	ns
125	Data Out Setup Time to $\overline{WR}$ Deassertion							
	• WS = 0	T_L - 5	—	T_L - 5	—	T_L - 5	—	ns
	• WS > 0	$WS \times T_C + T_L - 5$	—	$WS \times T_C + T_L - 5$	—	$WS \times T_C + T_L - 5$	—	ns
126	$\overline{RD}$ Deassertion to Address Not Valid	T_H - 9	—	T_H - 7	—	T_H - 5.5	—	ns

Table 15 External Bus Asynchronous Timing (continued)

Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
127	Address Valid to $\overline{RD}$ Deassertion							
	• WS = 0	$T_C + T_L - 8$	—	$T_C + T_L - 6$	—	$T_C + T_L - 6$	—	ns
	• WS > 0	$((WS + 1) \times T_C) + T_L - 8$	—	$((WS + 1) \times T_C) + T_L - 6$	—	$((WS + 1) \times T_C) + T_L - 6$	—	ns
128	Input Data Hold Time to $\overline{RD}$ Deassertion	0	—	0	—	0	—	ns
129	$\overline{RD}$ Assertion Width							
	• WS = 0	$T_C - 9$	—	$T_C - 7$	—	$T_C - 5.5$	—	ns
	• WS > 0	$((WS + 1) \times T_C) - 9$	—	$((WS + 1) \times T_C) - 7$	—	$((WS + 1) \times T_C) - 5.5$	—	ns
130	Address Valid to Input Data Valid							
	• WS = 0	—	$T_C + T_L - 18$	—	$T_C + T_L - 14$	—	$T_C + T_L - 11$	ns
	• WS > 0	—	$((WS + 1) \times T_C) + T_L - 18$	—	$((WS + 1) \times T_C) + T_L - 14$	—	$((WS + 1) \times T_C) + T_L - 11$	ns
131	Address Valid to $\overline{RD}$ Assertion	$T_L - 9$	$T_L + 5$	$T_L - 7$	$T_L + 5$	$T_L - 5.5$	$T_L + 5$	ns
132	$\overline{RD}$ Assertion to Input Data Valid							
	• WS = 0	—	$T_C - 14$	—	$T_C - 11$	—	$T_C - 9$	ns
	• WS > 0	—	$((WS + 1) \times T_C) - 14$	—	$((WS + 1) \times T_C) - 11$	—	$((WS + 1) \times T_C) - 9$	ns
133	$\overline{WR}$ Deassertion to $\overline{RD}$ Assertion	$T_C - 15$	—	$T_C - 12$	—	$T_C - 10$	—	ns
134	$\overline{RD}$ Deassertion to $\overline{RD}$ Assertion	$T_C - 10$	—	$T_C - 8$	—	$T_C - 6.5$	—	ns
135	$\overline{WR}$ Deassertion to $\overline{WR}$ Assertion							
	• WS = 0	$T_C - 15$	—	$T_C - 12$	—	$T_C - 10$	—	ns
	• WS > 0	$T_C + T_H - 15$	—	$T_C + T_H - 12$	—	$T_C + T_H - 10$	—	ns
136	$\overline{RD}$ Deassertion to $\overline{WR}$ Assertion							
	• WS = 0	$T_C - 10$	—	$T_C - 8$	—	$T_C - 6.5$	—	ns
	• WS > 0	$T_C + T_H - 10$	—	$T_C + T_H - 8$	—	$T_C + T_H - 6.5$	—	ns

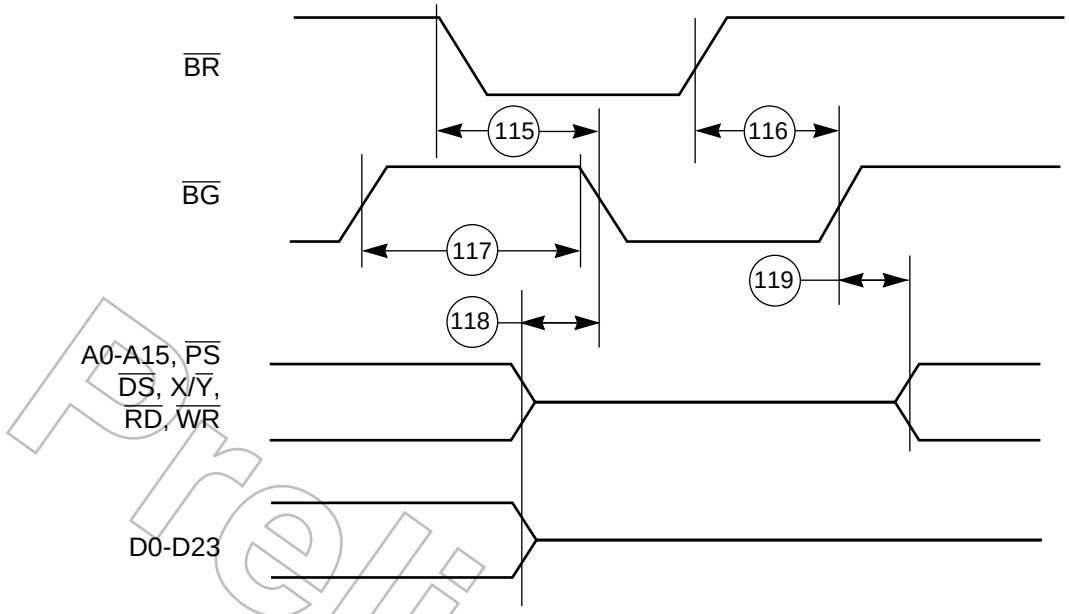
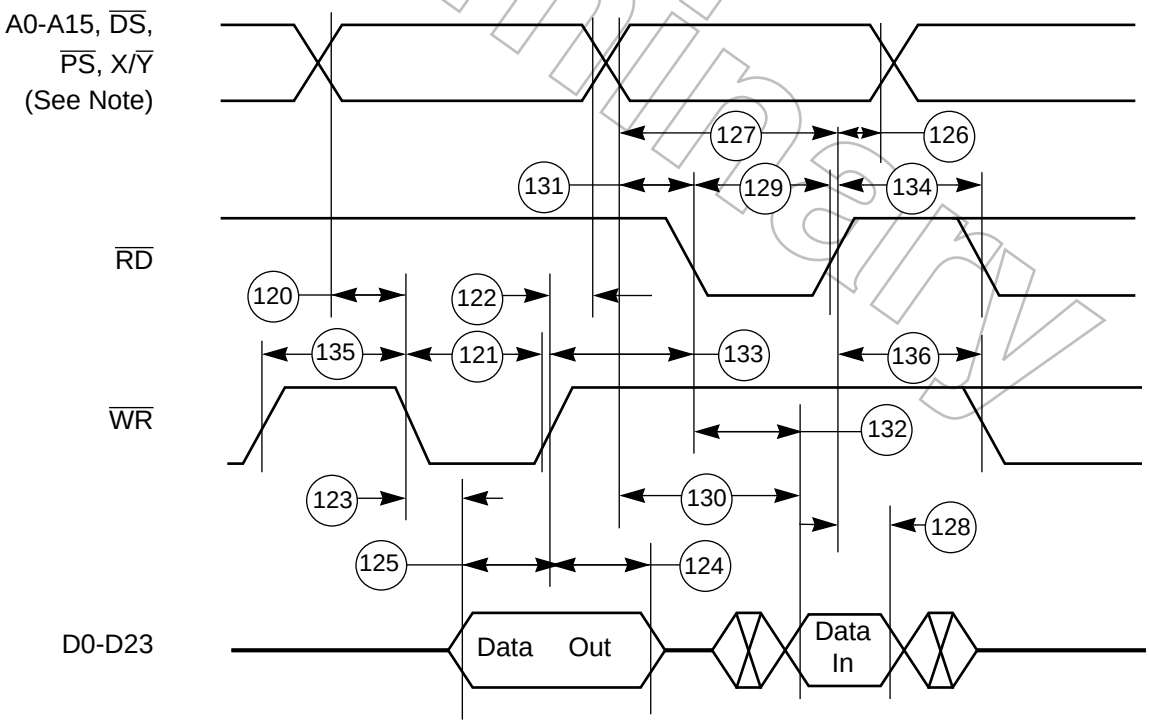


Figure 22 Bus Request / Bus Grant Timing



NOTE: During Read-Modify-Write instructions, the address lines do not change state.

Figure 23 External Bus Asynchronous Timing

External Bus Synchronous Timing

V_{CC} = 5.0 Vdc ± 10% for 20.5 MHz and 27 MHz, V_{CC} = 5.0 Vdc ± 5% for 33 MHz,
T_J = -40° to +105° C, C_L = 50 pF + 1 TTL Load

Capacitance Derating

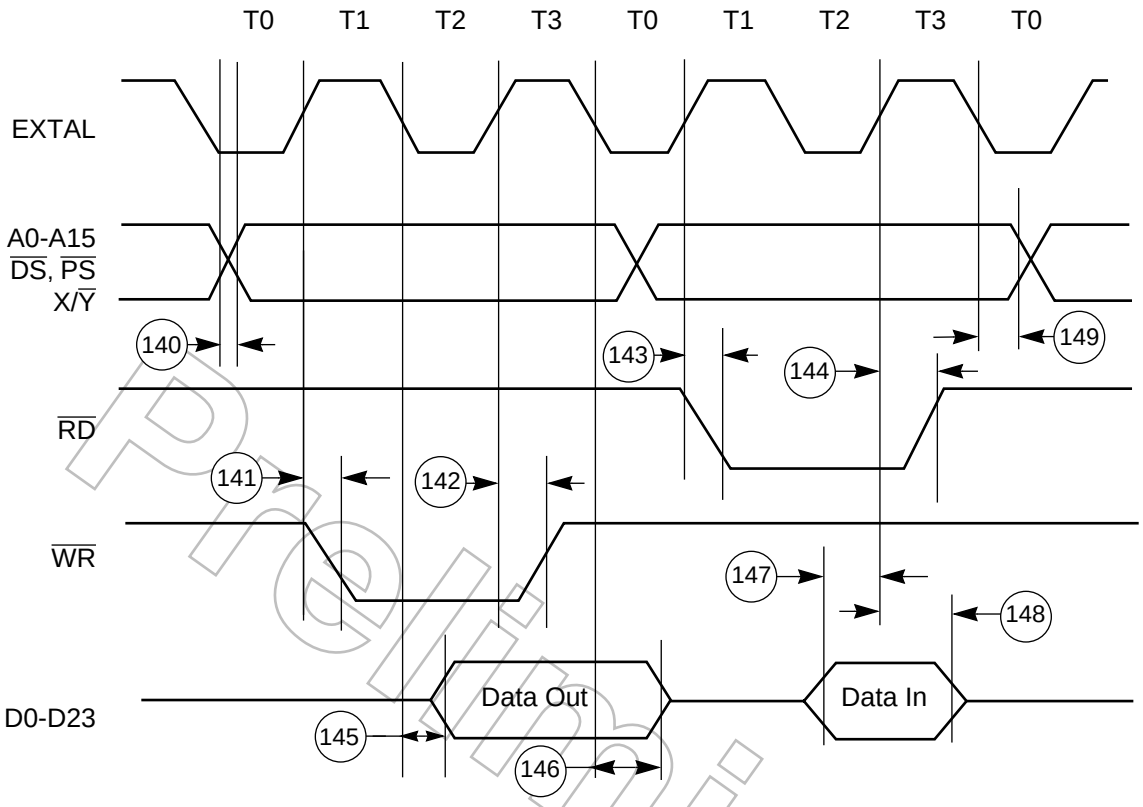
The DSP56001A External Bus Timing Specifications are designed and tested at the maximum capacitive load of 50 pF, including stray capacitance. Typically, the drive capability of the External Bus pins (A0-A15, D0-D23, $\overline{PS}$, $\overline{DS}$, $\overline{RD}$, $\overline{WR}$, X/$\overline{Y}$) derates linearly at 1 ns per 12 pF of additional capacitance from 50 pF to 250 pF of loading. Port B and C pins derate linearly at 1 ns per 5 pF of additional capacitance from 50 pF to 250 pF of loading. Active low lines should be “pulled up” in a manner consistent with the AC and DC specifications.

Table 16 External Bus Synchronous Timing

Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
140	Clk Low transition to Address Valid	—	24	—	19	—	19	ns
141	Clk High transition to $\overline{WR}$ Assertion • WS=0 • WS>0 (See Note 1)	0 0	19 T_H + 19	0 0	17 T_H + 17	0 0	17 T_H + 17	ns ns
142	Clk High transition to $\overline{WR}$ Deassertion	5	21	5	16	5	13	ns
143	Clk High transition to $\overline{RD}$ Assertion	0	19	0	16	0	16	ns
144	Clk High transition to $\overline{RD}$ Deassertion	3	17	3	13	3	10.5	ns
145	Clk Low transition to Data-Out Valid	—	25	—	19	—	19	ns
146	ClkLlow transition to Data-Out Invalid (See Note 3)	5	—	4	—	3.5	—	ns
147	Data-In Valid to Clk High transition (Setup)	4	—	4	—	4	—	ns
148	Clk High transition to Data-In Invalid (Hold)	12	—	12	—	12	—	ns
149	Clk Low transition to Address Invalid (See Note 3)	2	—	2	—	2	—	ns

NOTES:

1. AC timing specifications which are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal’s transition.
2. WS are wait state values specified in the BCR.
3. Clk Low transition to data-out invalid (specification # T146) and Clk Low transition to address invalid (specification # T149) indicate the time after which data/address are no longer guaranteed to be valid.
4. Timings are given from Clk midpoint to V_{OL} or V_{OH} of the corresponding pin(s).



NOTE: During Read-Modify-Write Instructions, the address lines do not change states.

Figure 24 DSP56001A Synchronous Bus Timing

Bus Strobe / Wait Timing

V_{CC} = 5.0 Vdc ± 10% for 20.5 MHz and 27 MHz, V_{CC} = 5.0 Vdc ± 5% for 33 MHz,
T_J = -40° to +105° C, C_L = 50 pF + 1 TTL Load

Table 17 Bus Strobe / Wait Timing

Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
150	Clk Low transition to $\overline{BS}$ Assertion	3	24	3	19	2.5	19	ns
151	$\overline{WT}$ Assertion to Clk Low transition (setup time)	4	—	3	—	2.5	—	ns
152	Clk Low transition to $\overline{WT}$ Deassertion for Minimum Timing	14	T_C - 8	11	T_C - 6	12	T_C - 5	ns
153	$\overline{WT}$ Deassertion to Clk Low transition for Maximum Timing (2 wait states)	8	—	6	—	5	—	ns
154	Clk High transition to $\overline{BS}$ Deassertion	3	26	3	20	3	19	ns
155	$\overline{BS}$ Assertion to Address Valid	-2	10	-2	8	-2	6.5	ns
156	$\overline{BS}$ Assertion to $\overline{WT}$ Assertion (See Note 2)	0	T_C - 15	0	T_C - 11	0	T_C - 10	ns
157	$\overline{BS}$ Assertion to $\overline{WT}$ Deassertion (See Note 2 and Note 4) • WS ≤ 2 • WS ≥ 2	T_C (WS - 1) × T_C	2 × T_C - 15 WS × T_C - 15	T_C (WS - 1) × T_C	2 × T_C - 11 WS × T_C - 11	T_C + 4 (WS - 1) × T_C + 4	2 × T_C - 10 WS × T_C - 10	ns ns
158	$\overline{WT}$ Deassertion to $\overline{BS}$ Deassertion	T_C + T_L	2 × T_C + T_L + 23	T_C + T_L	2 × T_C + T_L + 17	T_C + T_L	2 × T_C + T_L + 15	ns
159	Minimum $\overline{BS}$ Deassertion Width for Consecutive External Accesses	T_H - 7	—	T_H - 6	—	T_H - 4.5	—	ns
160	$\overline{BS}$ Deassertion to Address Invalid (See Note 3)	T_H - 10		T_H - 8		T_H - 6.5		ns
161	Data-In Valid to $\overline{RD}$ Deassertion (Set Up)	16	—	12	—	10	—	ns

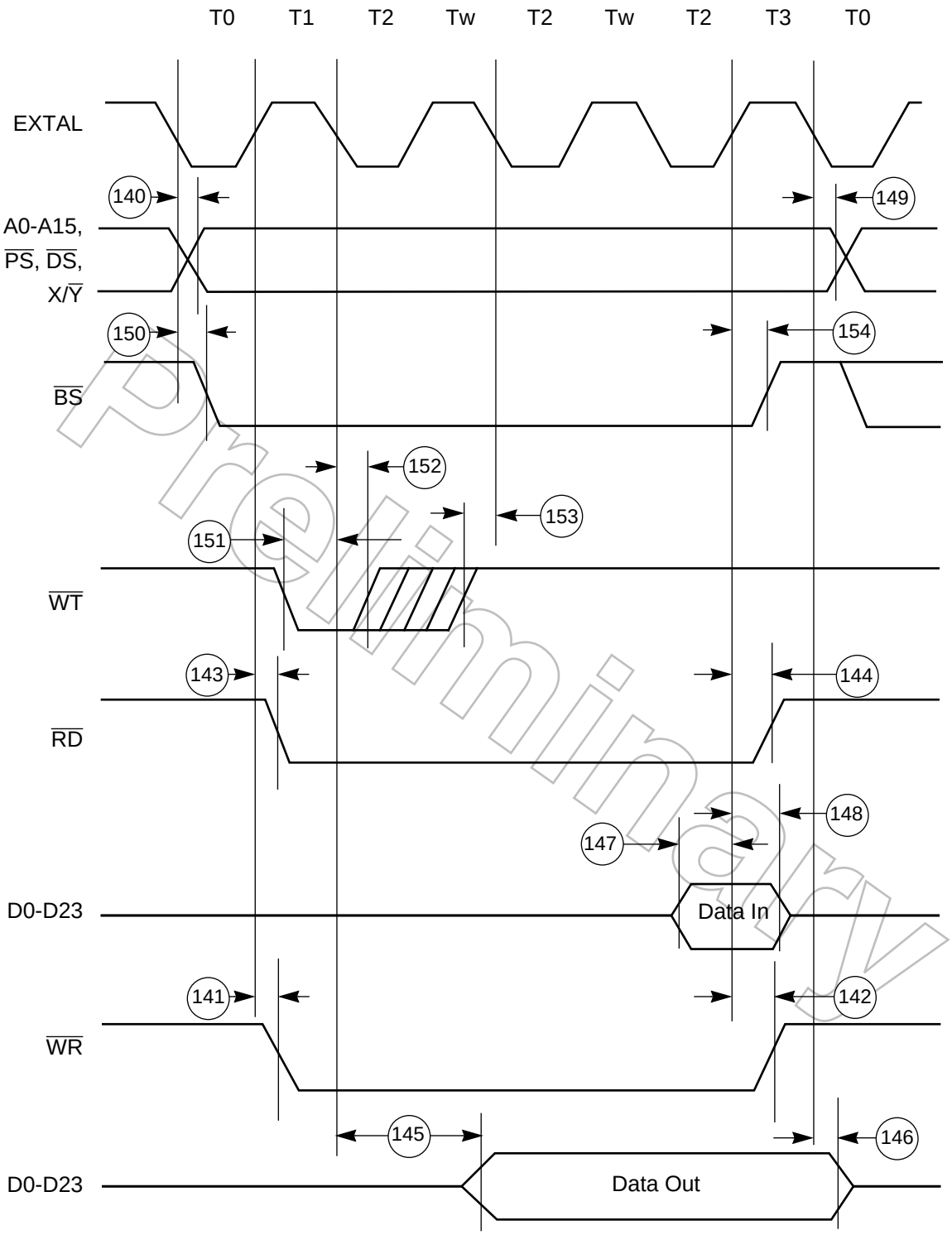
NOTES:

1. AC timing specifications which are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition.
2. If wait states are also inserted using the BCR and if the number of wait states is greater than 2, then specification numbers 156 and 157 can be increased accordingly.
3. $\overline{BS}$ deassertion to address invalid indicates the time after which the address are no longer guaranteed to be valid.
4. The minimum number of wait states when using $\overline{BS}$/$\overline{WT}$ is two (2).
5. For read-modify-write instructions, the address lines will not change states between the read and the write

cycle. However, $\overline{BS}$ will deassert before asserting again for the write cycle. If wait states are desired for each of the read and write cycle, the $\overline{WT}$ pin must be asserted once for each cycle.

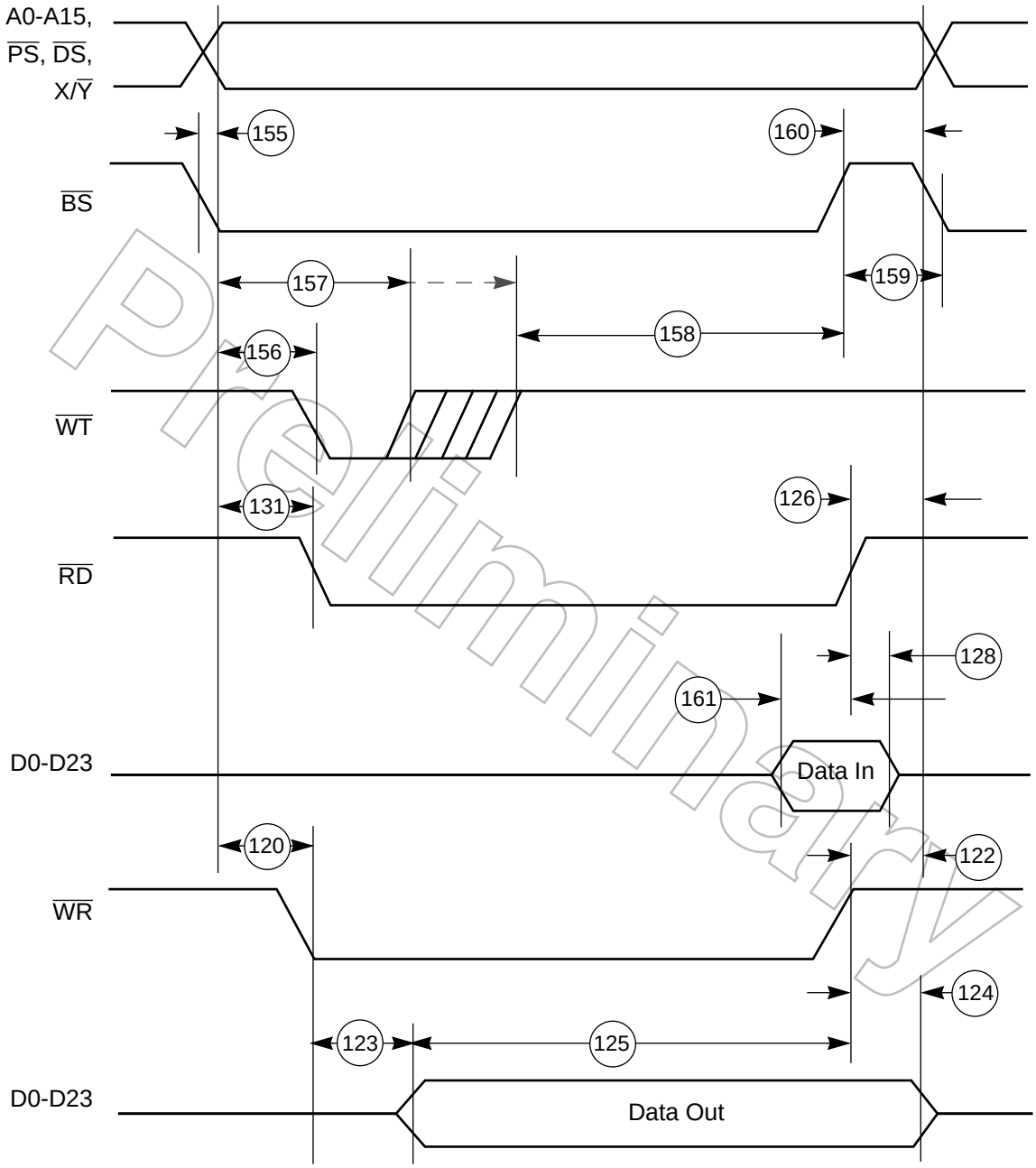
Bus Strobe / Wait Timing

Bus Strobe / Wait Timing



NOTE: During Read-Modify-Write Instructions, the address lines do not change state. However, $\overline{BS}$ will deassert before asserting again for the write cycle.

Figure 25 DSP56001A Synchronous $\overline{BS}$ / $\overline{WT}$ Timings

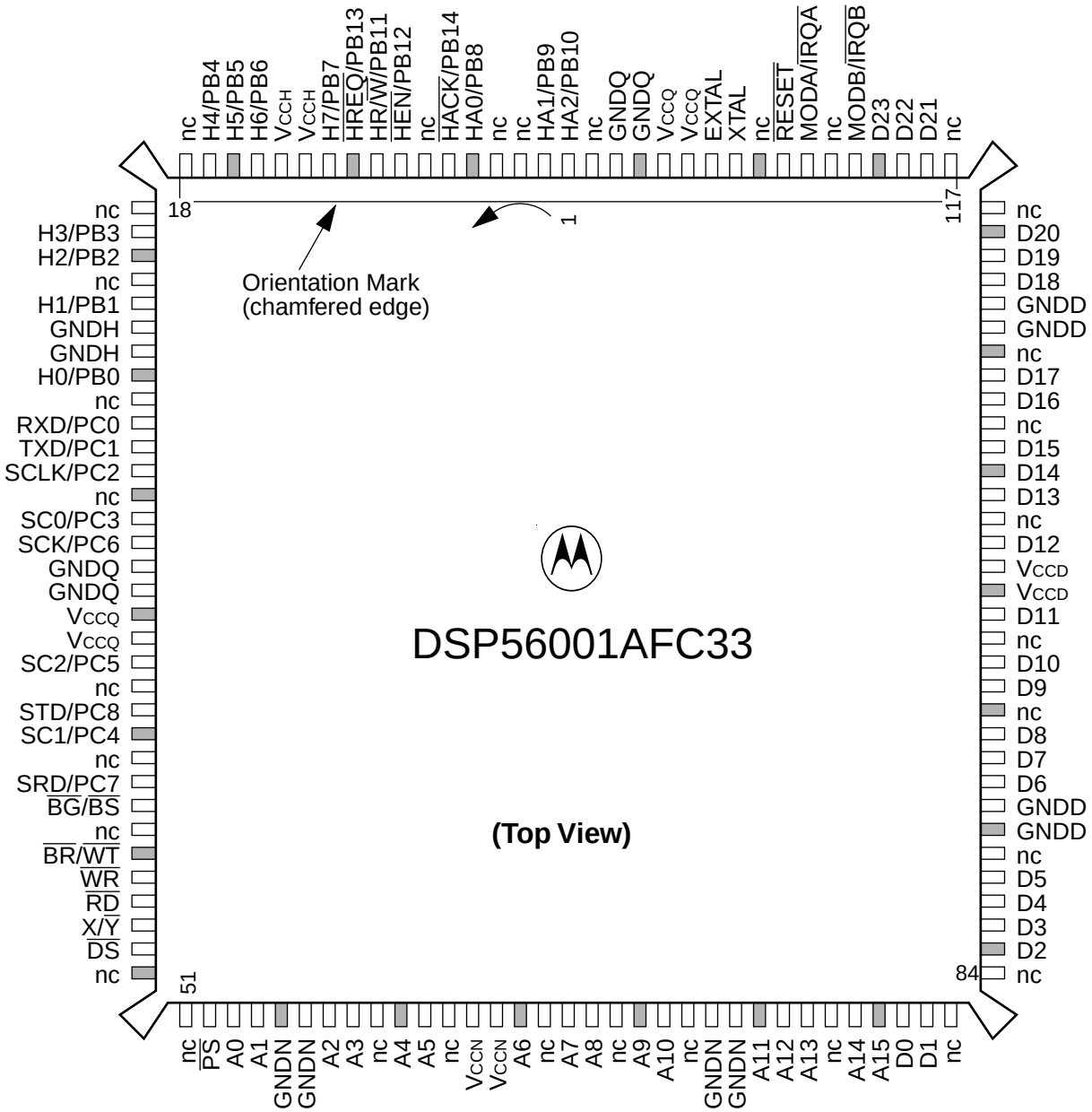


NOTE: During Read-Modify-Write instructions, the address lines do not change state. However, $\overline{BS}$ will deassert before asserting again for the write cycle.

Figure 26 DSP56001A Asynchronous $\overline{BS}$ / $\overline{WT}$ Timings

Package and Tray Descriptions

Top and bottom views of each of the three packages are shown in Figure 27 - Figure 32 with their pin-outs.

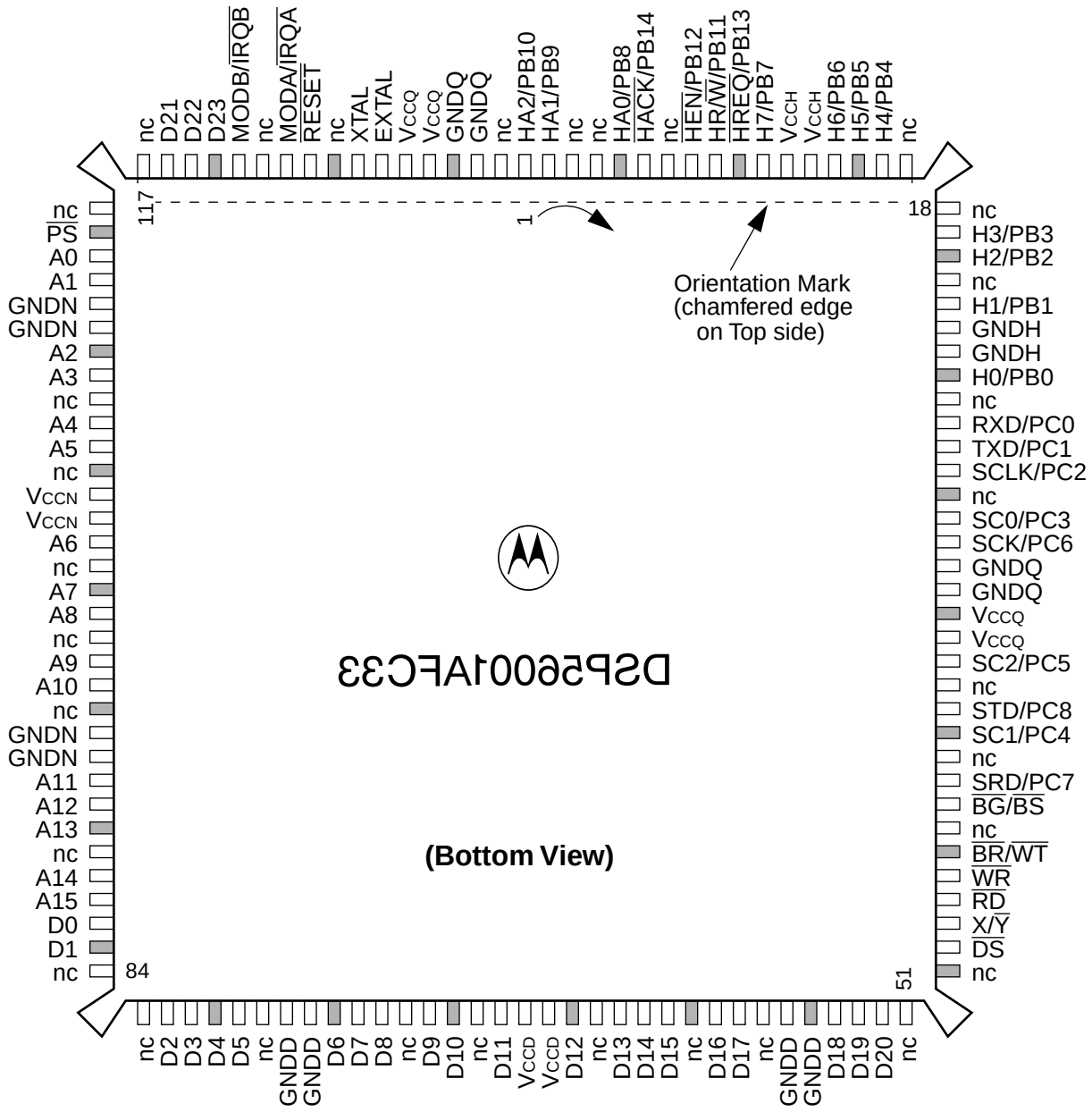


NOTES:

1. "nc" are No Connection pins that are reserved for possible future enhancements. Do not connect these pins to any power, ground, signal traces, or vias.
2. An $\overline{\text{OVERBAR}}$ indicates the signal is asserted when the voltage = ground (active low).
3. To simplify locating the pins, each fifth pin is shaded in the illustration.

Figure 27 Top View of the 132-pin Plastic (FC) Quad Flat Package

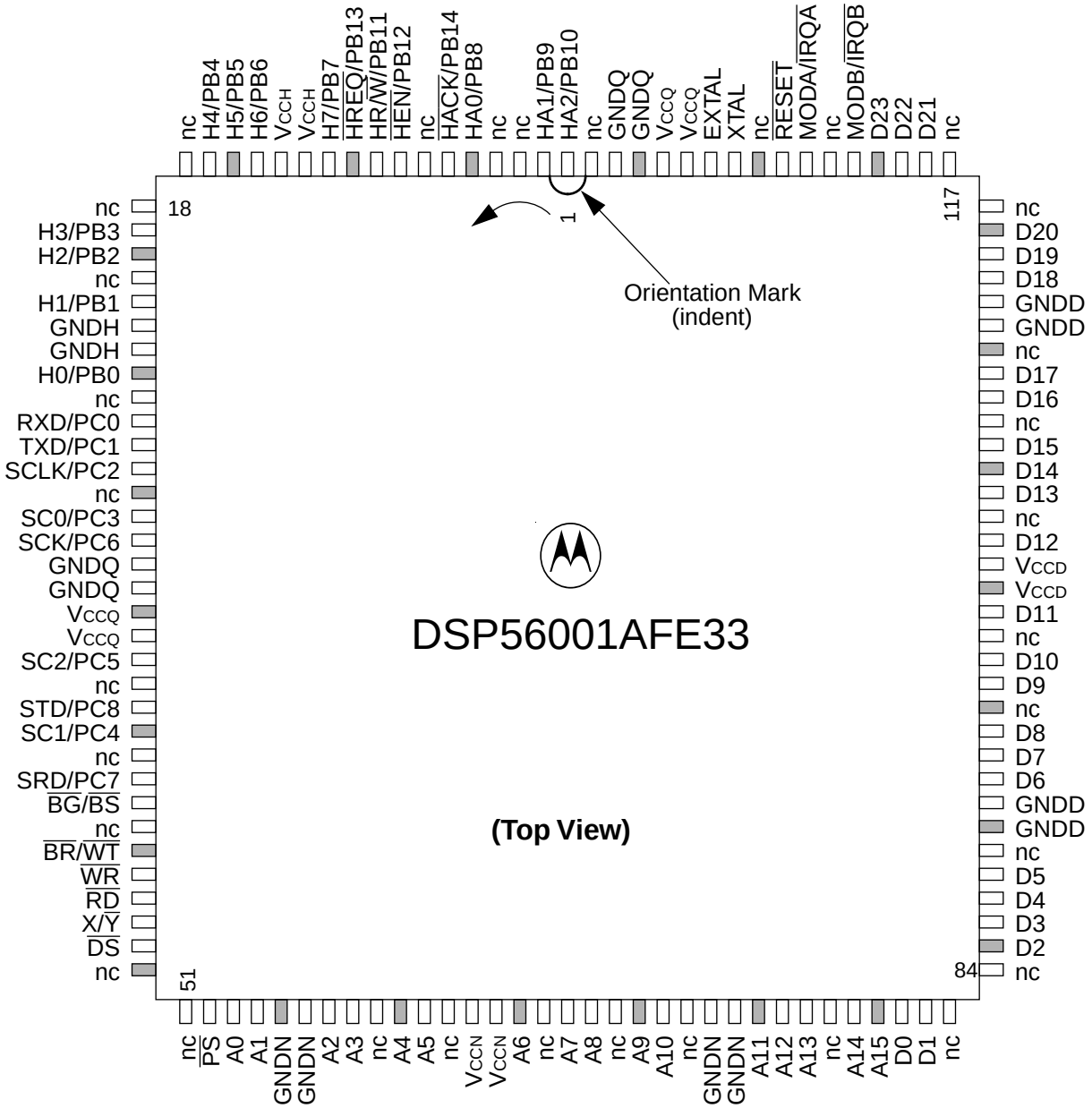
PQFP Bottom View



NOTES:

1. "nc" are No Connection pins that are reserved for possible future enhancements. Do not connect these pins to any power, ground, signal traces, or vias.
2. An OVERBAR indicates the signal is asserted when the voltage = ground (active low).
3. To simplify locating the pins, each fifth pin is shaded in the illustration.

Figure 28 Bottom View of the 132-pin Plastic (FC) Quad Flat Package

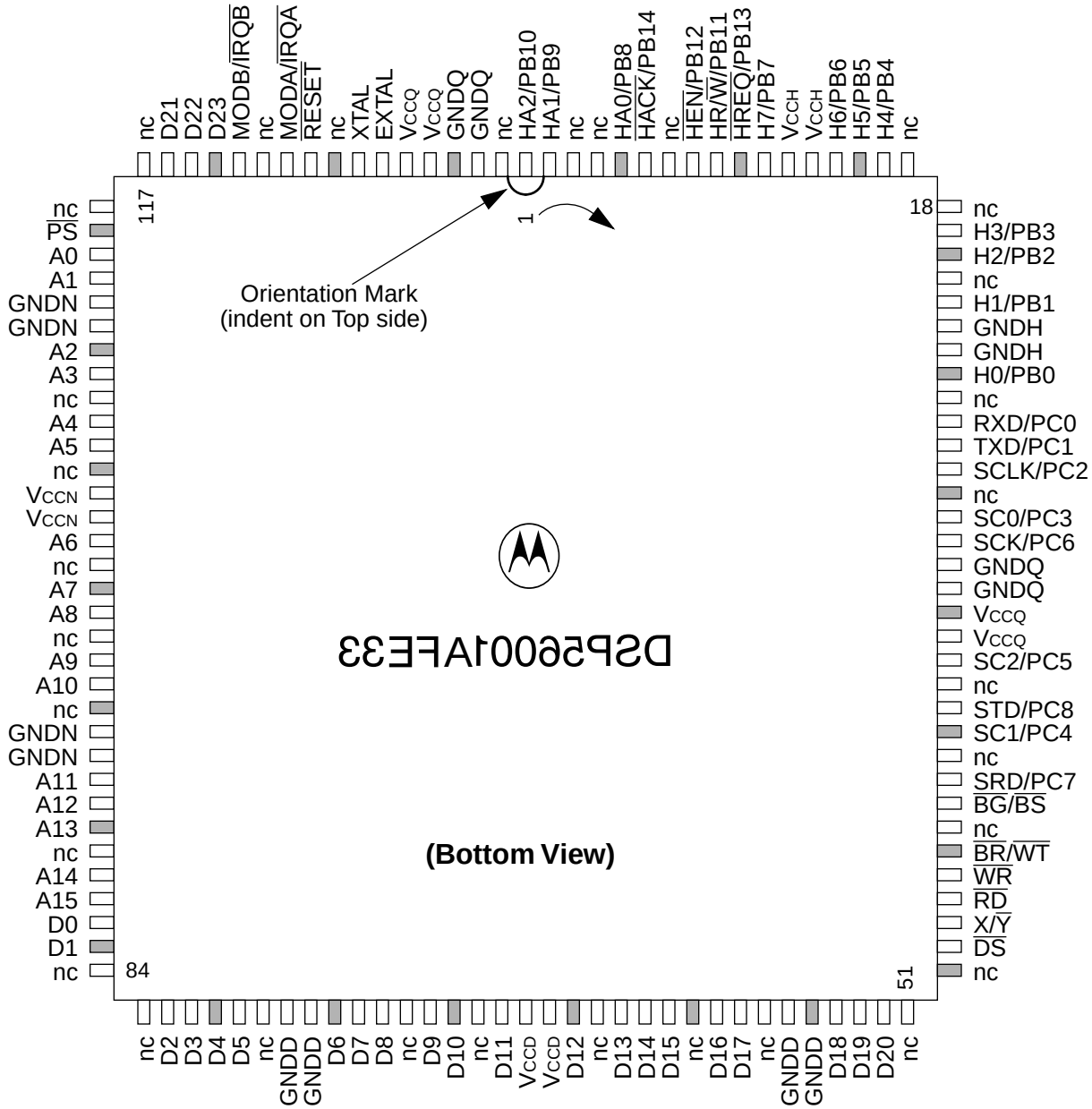


NOTES:

1. "nc" are No Connection pins that are reserved for possible future enhancements. Do not connect these pins to any power, ground, signal traces, or vias.
2. An OVERBAR indicates the signal is asserted when the voltage = ground (active low).
3. To simplify locating the pins, each fifth pin is shaded in the illustration.

Figure 29 Top View of the 132-pin Ceramic (FE) Quad Flat Package

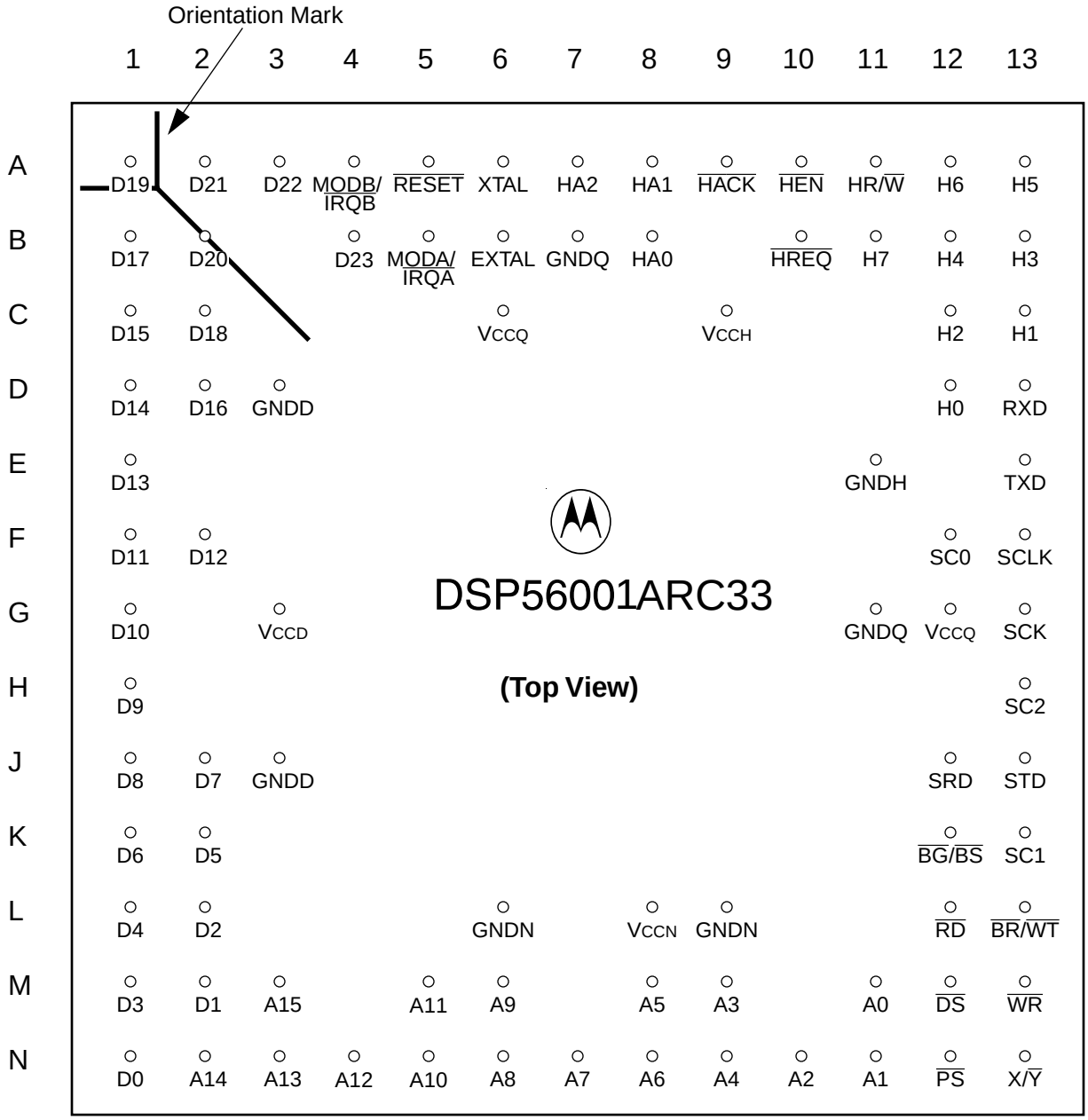
CQFP Bottom View



NOTES:

1. "nc" are No Connection pins that are reserved for possible future enhancements. Do not connect these pins to any power, ground, signal traces, or vias.
2. An $\overline{\text{OVERBAR}}$ indicates the signal is asserted when the voltage = ground (active low).
3. To simplify locating the pins, each fifth pin is shaded in the illustration.

Figure 30 Bottom View of the132-pin Ceramic (FE) Quad Flat Package

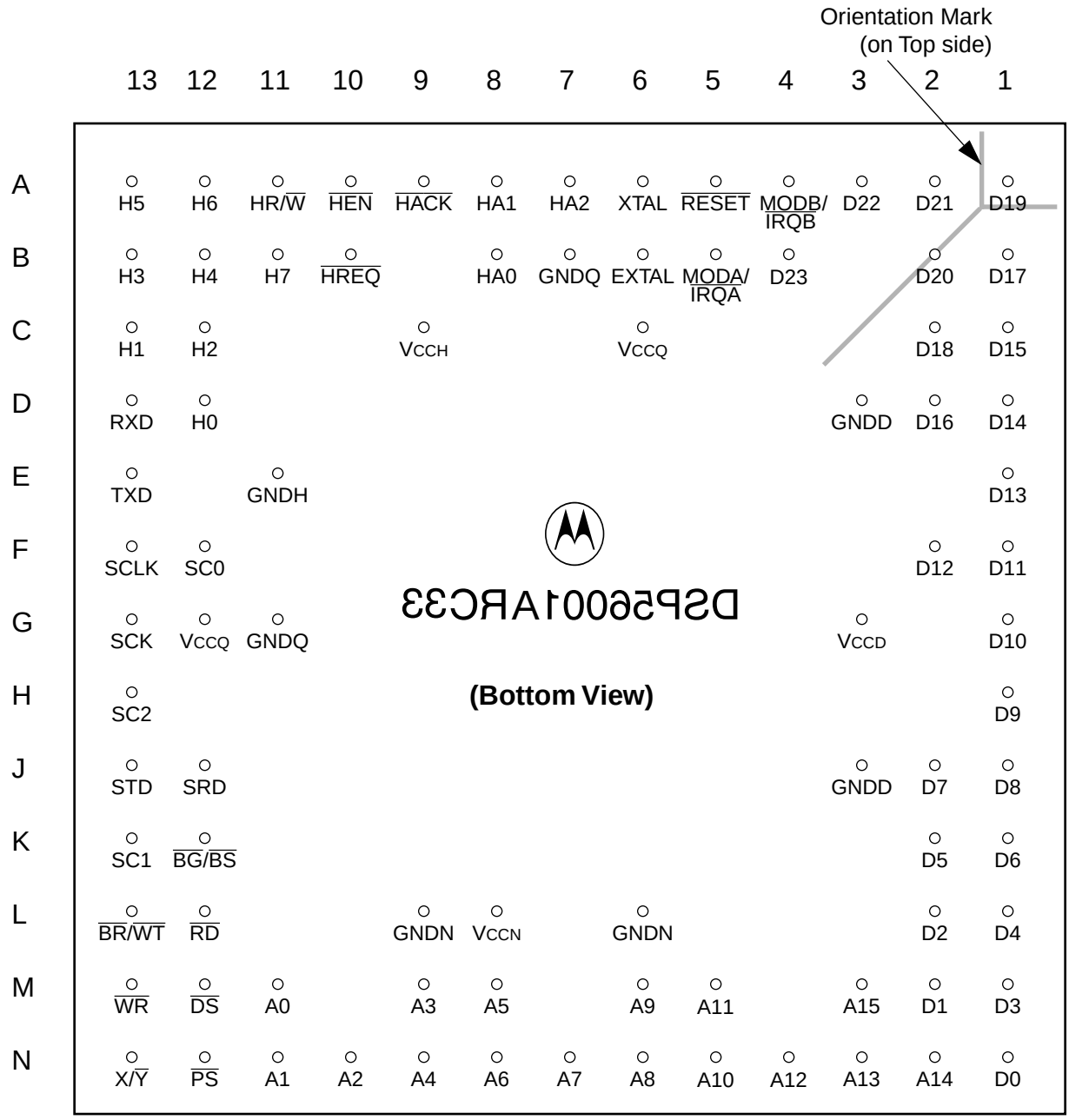


NOTES:

1. “nc” are No Connection pins that are reserved for possible future enhancements. Do not connect these pins to any power, ground, signal traces, or vias.
2. An OVERBAR indicates the signal is asserted when the voltage = ground (active low).

Figure 31 Top View of the 88-pin Ceramic (RC) 13 x13 Pin Grid Array Package

PGA Bottom View



NOTES:

1. “nc” are No Connection pins that are reserved for possible future enhancements. Do not connect these pins to any power, ground, signal traces, or vias.
2. An OVERBAR indicates the signal is asserted when the voltage = ground (active low).

Figure 32 Bottom View of the 88-pin Ceramic (RC) 13 x 13 Pin Grid Array Package

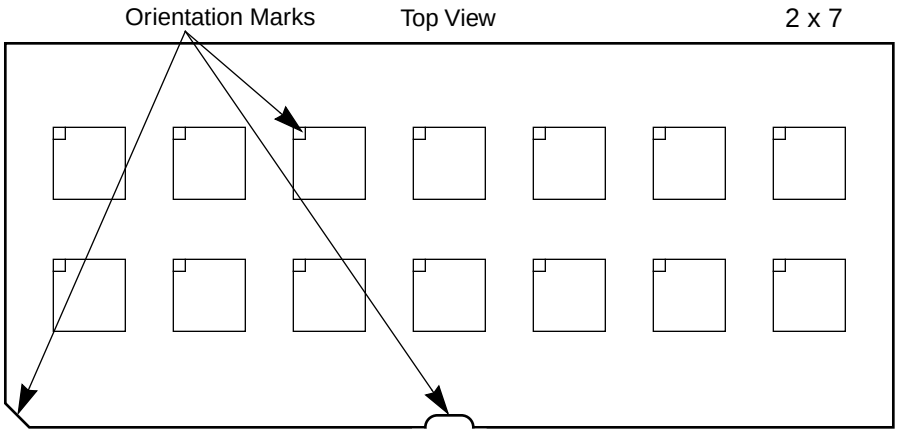


Figure 33 PGA Shipping Tray

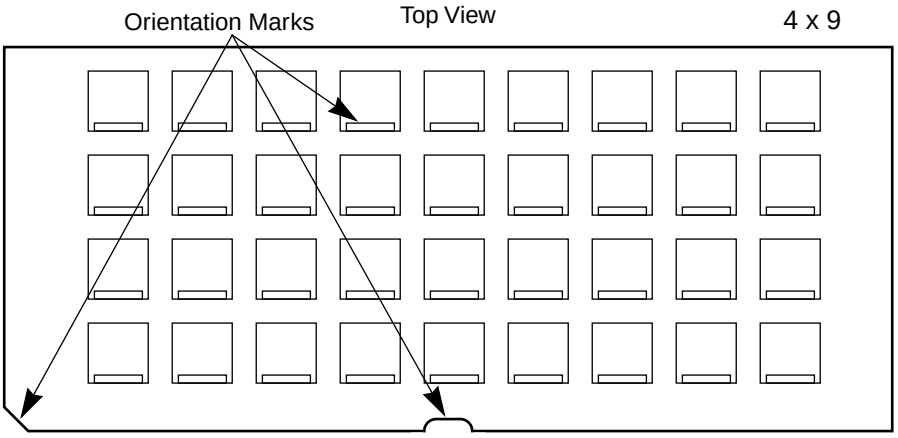


Figure 34 PQFP Shipping Tray

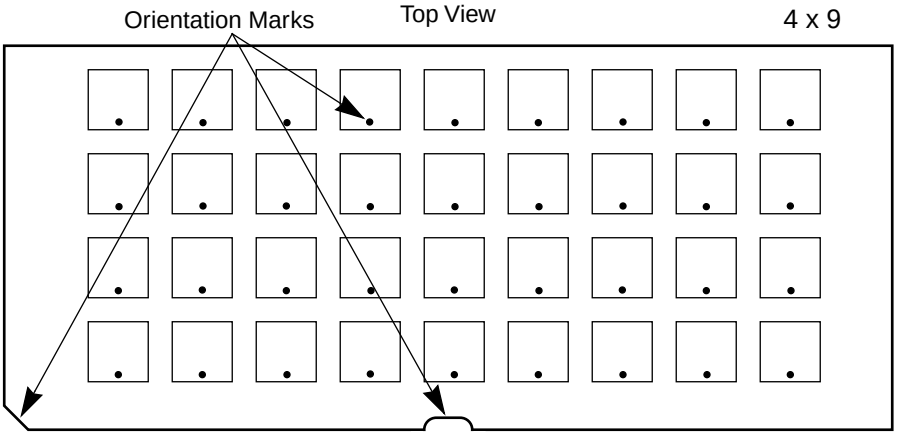


Figure 35 CQFP Shipping Tray

Pin Tables

The DSP56001A signals which may be programmed as general purpose I/O are listed with their primary function in Table 18. Table 19 and Table 20 identify pins on each package in numeric order. Table 21 identifies each signal name in order while giving the pin number for each of the packages. Table 22 groups power and ground leads. Mechanical drawings of the packages are presented in Figure 36 - Figure 38.

Table 18 DSP56001A General Purpose I/O Pin Identification

General Purpose I/O I D	Primary Pin Function	132 pin "FC" PQFP or "FE" CQFP Pin #	88 pin "RC" PGA Pin #
PB0	H0	25	D12
PB1	H1	22	C13
PB2	H2	20	C12
PB3	H3	19	B13
PB4	H4	16	B12
PB5	H5	15	A13
PB6	H6	14	A12
PB7	H7	11	B11
PB8	HA0	5	B8
PB9	HA1	2	A8
PB10	HA2	1	A7
PB11	HR/$\overline{W}$	9	A11
PB12	$\overline{HEN}$	8	A10
PB13	$\overline{HREQ}$	10	B10
PB14	$\overline{HACK}$	6	A9
PC0	RXD	27	D13
PC1	TXD	28	E13
PC2	SCLK	29	F13
PC3	SC0	31	F12
PC4	SC1	40	K13
PC5	SC2	37	H13
PC6	SCK	32	G13
PC7	SRD	42	J12
PC8	STD	39	J13

Table 19 DSP56001A PGA Pin Identification by Pin Number

88 pin "RC" PGA Pin #	Signal Name	88 pin "RC" PGA Pin #	Signal Name	88 pin "RC" PGA Pin #	Signal Name
A1	D19	D1	D14	L6	GNDN
A2	D21	D2	D16	L8	V_{CCN}
A3	D22	D3	GNDD	L9	GNDN
A4	MODB/$\overline{IRQB}$	D12	H0/PB0	L12	$\overline{RD}$
A5	$\overline{RESET}$	D13	RXD/PC0	L13	$\overline{BR}$/$\overline{WT}$
A6	XTAL	E1	D13	M1	D3
A7	HA2/PB10	E11	GNDH	M2	D1
A8	HA1/PB9	E13	TXD/PC1	M3	A15
A9	$\overline{HACK}$/PB14	F1	D11	M5	A11
A10	$\overline{HEN}$/PB12	F2	D12	M6	A9
A11	HR/$\overline{W}$/PB11	F12	SC0/PC3	M8	A5
A12	H6/PB6	F13	SCLK/PC2	M9	A3
A13	H5/PB5	G1	D10	M11	A0
B1	D17	G3	V_{CCD}	M12	$\overline{DS}$
B2	D20	G11	GNDQ	M13	$\overline{WR}$
B4	D23	G12	V_{CCQ}	N1	D0
B5	MODA/$\overline{IRQA}$	G13	SCK/PC6	N2	A14
B6	EXTAL	H1	D9	N3	A13
B7	GNDQ	H13	SC2/PC5	N4	A12
B8	HA0/PB8	J1	D8	N5	A10
B10	$\overline{HREQ}$/PB13	J2	D7	N6	A8
B11	H7/PB7	J3	GNDD	N7	A7
B12	H4/PB4	J12	SRD/PC7	N8	A6
B13	H3/PB3	J13	STD/PC8	N9	A4
C1	D15	K1	D6	N10	A2
C2	D18	K2	D5	N11	A1
C6	V_{CCQ}	K12	$\overline{BG}$/$\overline{BS}$	N12	$\overline{PS}$
C9	V_{CCH}	K13	SC1/PC4	N13	X/$\overline{Y}$
C12	H2/PB2	L1	D4		
C13	H1/PB1	L2	D2		

Table 20 DSP56001A PQFP or CQFP Pin Identification by Pin Number

132 pin "FC" PQFP or "FE" CQFP Pin #	Signal Name	132 pin "FC" PQFP or "FE" CQFP Pin #	Signal Name	132 pin "FC" PQFP or "FE" CQFP Pin #	Signal Name
1	HA2/PB10	28	TXD/PC1	55	GNDN
2	HA1/PB9	29	SCLK/PC2	56	GNDN
3	nc	30	nc	57	A2
4	nc	31	SC0/PC3	58	A3
5	HA0/PB8	32	SCK/PC6	59	nc
6	$\overline{\text{HACK}}$/PB14	33	GNDQ	60	A4
7	nc	34	GNDQ	61	A5
8	$\overline{\text{HEN}}$/PB12	35	V_{CCQ}	62	nc
9	HR/$\overline{\text{W}}$/PB11	36	V_{CCQ}	63	V_{CCN}
10	$\overline{\text{HREQ}}$/PB13	37	SC2/PC5	64	V_{CCN}
11	H7/PB7	38	nc	65	A6
12	V_{CCH}	39	STD/PC8	66	nc
13	V_{CCH}	40	SC1/PC4	67	A7
14	H6/PB6	41	nc	68	A8
15	H5/PB5	42	SRD/PC7	69	nc
16	H4/PB4	43	$\overline{\text{BG}}$/$\overline{\text{BS}}$	70	A9
17	nc	44	nc	71	A10
18	nc	45	$\overline{\text{BR}}$/$\overline{\text{WT}}$	72	nc
19	H3/PB3	46	$\overline{\text{WR}}$	73	GNDN
20	H2/PB2	47	$\overline{\text{RD}}$	74	GNDN
21	nc	48	X/$\overline{\text{Y}}$	75	A11
22	H1/PB1	49	$\overline{\text{DS}}$	76	A12
23	GNDH	50	nc	77	A13
24	GNDH	51	nc	78	nc
25	H0/PB0	52	$\overline{\text{PS}}$	79	A14
26	nc	53	A0	80	A15
27	RXD/PC0	54	A1	81	D0

(table continues on next page)

Table 20 DSP56001A PQFP or CQFP Pin Identification by Pin Number (Continued)

132 pin "FC" PQFP or "FE" CQFP Pin #	Signal Name	132 pin "FC" PQFP or "FE" CQFP Pin #	Signal Name	132 pin "FC" PQFP or "FE" CQFP Pin #	Signal Name
82	D1	99	D11	116	nc
83	nc	100	V_{CCD}	117	nc
84	nc	101	V_{CCD}	118	D21
85	D2	102	D12	119	D22
86	D3	103	nc	120	D23
87	D4	104	D13	121	MODB/$\overline{IRQB}$
88	D5	105	D14	122	nc
89	nc	106	D15	123	MODA/$\overline{IRQA}$
90	GNDD	107	nc	124	$\overline{RESET}$
91	GNDD	108	D16	125	nc
92	D6	109	D17	126	XTAL
93	D7	110	nc	127	EXTAL
94	D8	111	GNDD	128	V_{CCQ}
95	nc	112	GNDD	129	V_{CCQ}
96	D9	113	D18	130	GNDQ
97	D10	114	D19	131	GNDQ
98	nc	115	D20	132	nc

NOTES:

1. "nc" are No Connection pins that are reserved for possible future enhancements. Do not connect these pins to any power, ground, signal traces, or vias.
2. An $\overline{OVERBAR}$ indicates the signal is asserted when the voltage = ground (active low).

Table 21 DSP56001A Pin Identification by Signal Name

Pin Function	132 pin "FC" PQFP or "FE" CQFP Pin #	88 pin "RC" PGA Pin #	Pin Function	132 pin "FC" PQFP or "FE" CQFP Pin #	88 pin "RC" PGA Pin #
A0	53	M11	D7	93	J2
A1	54	N11	D8	94	J1
A2	57	N10	D9	96	H1
A3	58	M9	D10	97	G1
A4	60	N9	D11	99	F1
A5	61	M8	D12	102	F2
A6	65	N8	D13	104	E1
A7	67	N7	D14	105	D1
A8	68	N6	D15	106	C1
A9	70	M6	D16	108	D2
A10	71	N5	D17	109	B1
A11	75	M5	D18	113	C2
A12	76	N4	D19	114	A1
A13	77	N3	D20	115	B2
A14	79	N2	D21	118	A2
A15	80	M3	D22	119	A3
$\overline{BG}$	43	K12	D23	120	B4
$\overline{BR}$	45	L13	$\overline{DS}$	49	M12
$\overline{BS}$	43	K12	EXTAL	127	B6
D0	81	N1	GNDD	90	D3
D1	82	M2	GNDD	91	J3
D2	85	L2	GNDD	111	
D3	86	M1	GNDD	112	
D4	87	L1	GNDH	23	E11
D5	88	K2	GNDH	24	
D6	92	K1	GNDN	55	L6

(table continues on next page)

Table 21 DSP56001A Pin Identification by Signal Name (Continued)

Pin Function	132 pin "FC" PQFP or "FE" CQFP Pin #	88 pin "RC" PGA Pin #	Pin Function	132 pin "FC" PQFP or "FE" CQFP Pin #	88 pin "RC" PGA Pin #
GNDN	56	L9	$\overline{\text{NMI}}$	none	none
GNDN	73		PB0	25	D12
GNDN	74		PB1	22	C13
GNDQ	33	B7	PB2	20	C12
GNDQ	34	G11	PB3	19	B13
GNDQ	130		PB4	16	B12
GNDQ	131		PB5	15	A13
H0	25	D12	PB6	14	A12
H1	22	C13	PB7	11	B11
H2	20	C12	PB8	5	B8
H3	19	B13	PB9	2	A8
H4	16	B12	PB10	1	A7
H5	15	A13	PB11	9	A11
H6	14	A12	PB12	8	A10
H7	11	B11	PB13	10	B10
HA0	5	B8	PB14	6	A9
HA1	2	A8	PC0	27	D13
HA2	1	A7	PC1	28	E13
$\overline{\text{HACK}}$	6	A9	PC2	29	F13
$\overline{\text{HEN}}$	8	A10	PC3	31	F12
HR/$\overline{\text{W}}$	9	A11	PC4	40	K13
$\overline{\text{HREQ}}$	10	B10	PC5	37	H13
$\overline{\text{IRQA}}$	123	B5	PC6	32	G13
$\overline{\text{IRQB}}$	121	A4	PC7	42	J12
MODA	123	B5	PC8	39	J13
MODB	121	A4	$\overline{\text{PS}}$	52	N12

(table continues on next page)

Table 21 DSP56001A Pin Identification by Signal Name (Continued)

Pin Function	132 pin "FC" PQFP or "FE" CQFP Pin #	88 pin "RC" PGA Pin #	Pin Function	132 pin "FC" PQFP or "FE" CQFP Pin #	88 pin "RC" PGA Pin #
$\overline{RD}$	47	L12	nc	4	
$\overline{RESET}$	124	A5	nc	7	
RXD	27	D13	nc	17	
SC0	31	F12	nc	18	
SC1	40	K13	nc	21	
SC2	37	H13	nc	26	
SCK	32	G13	nc	30	
SCLK	29	F13	nc	38	
SRD	42	J12	nc	41	
STD	39	J13	nc	44	
TXD	28	E13	nc	50	
V_{CCD}	100	G3	nc	51	
V_{CCD}	101		nc	59	
V_{CCH}	12	C9	nc	62	
V_{CCH}	13		nc	66	
V_{CCN}	63	L8	nc	69	
V_{CCN}	64		nc	72	
V_{CCQ}	35	C6	nc	78	
V_{CCQ}	36	G12	nc	83	
V_{CCQ}	128		nc	84	
V_{CCQ}	129		nc	89	
$\overline{WR}$	46	M13	nc	95	
$\overline{WT}$	45	L13	nc	98	
X/$\overline{Y}$	48	N13	nc	103	
XTAL	126	A6	nc	107	
nc	3		nc	110	

(table continues on next page)

Table 21 DSP56001A Pin Identification by Signal Name (Continued)

Pin Function	132 pin "FC" PQFP or "FE" CQFP Pin #	88 pin "RC" PGA Pin #	Pin Function	132 pin "FC" PQFP or "FE" CQFP Pin #	88 pin "RC" PGA Pin #
nc	116		nc	125	
nc	117		nc	132	
nc	122				

NOTES:

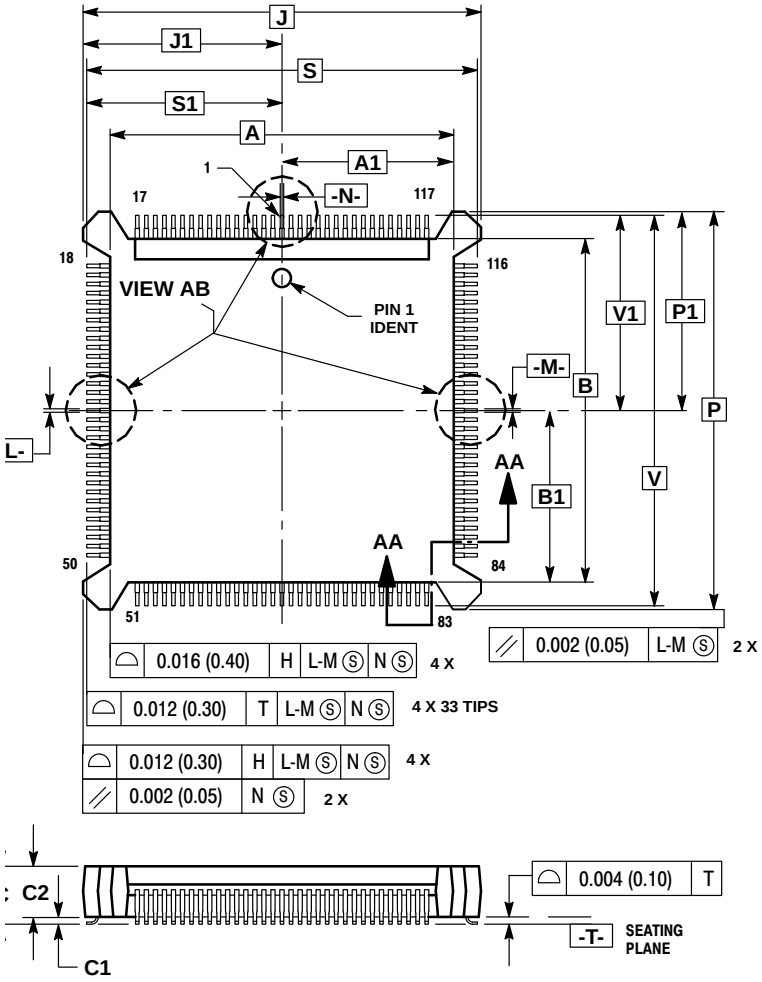
1. "nc" are No Connection pins that are reserved for possible future enhancements. Do not connect these pins to any power, ground, signal traces, or vias.
2. An $\overline{\text{OVERBAR}}$ indicates the signal is asserted when the voltage = ground (active low).

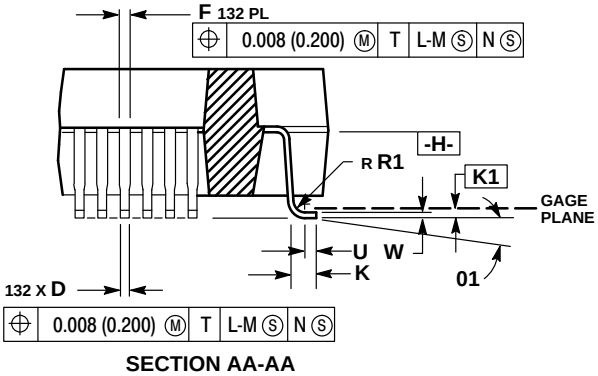
Table 22 DSP56001A Power Supply Pin Identification

Circuit Supplied	Power Supply	132 pin "FC" PQFP or "FE" CQFP Pin #	88 pin "RC" PGA Pin #
Address Bus Buffers	V_{CCN}	63	L8
		64	
	GNDN	55	L6
		56	L9
		73	
		74	
Data Bus Buffers	V_{CCD}	100	G3
		101	
	GNDD	90	D3
		91	J3
		111	
		112	
Internal Logic	V_{CCQ}	35	C6
		36	G12
		128	
		129	
	GNDQ	33	B7
		34	G11
		130	
		131	
Peripherals	V_{CCH}	12	C9
		13	
	GNDH	23	E11
		24	

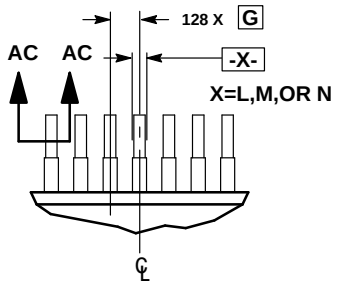
Power and ground pins have special considerations for noise immunity. See the section "Design Considerations".

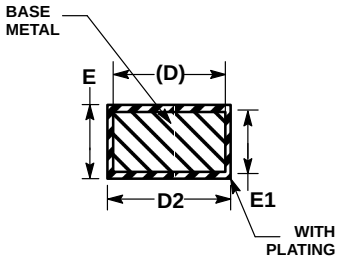
132-pin PQFP





SECTION AA-AA





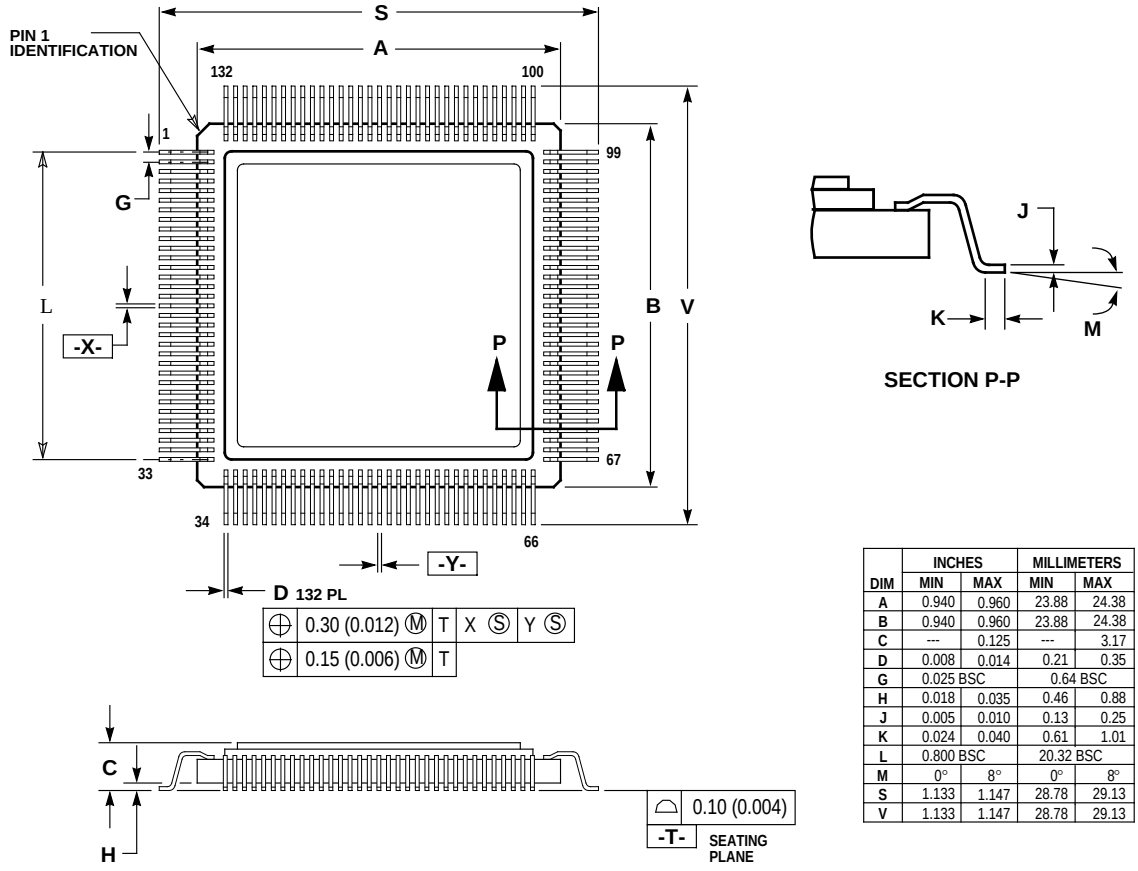
SECTION AC-AC

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS A, B, J, AND P DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION FOR DIMENSIONS A AND B IS 0.010 (0.25), FOR DIMENSIONS J AND P IS 0.007 (0.18).
4. DATUM PLANE -H- IS LOCATED AT THE UNDERSIDE OF LEADS WHERE LEADS EXIT PACKAGE BODY.
5. DATUMS -L-, -M-, AND -N- TO BE DETERMINED WHERE CENTER LEADS EXIT PACKAGE BODY AT DATUM -H-.
6. DIMENSIONS U AND V TO BE DETERMINED AT SEATING PLANE, DATUM -T-.
7. DIMENSIONS A, B, J, AND P TO BE DETERMINED AT DATUM PLANE -H-.
8. DIMENSION F DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.019 (0.48).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.950 BSC		24.13 BSC	
A1	0.475 BSC		12.06 BSC	
B	0.950 BSC		24.13 BSC	
B1	0.475 BSC		12.06 BSC	
C	0.160	0.180	4.06	4.57
C1	0.020	0.040	0.51	1.02
C2	0.135	0.145	3.43	3.68
D	0.008	0.012	0.20	0.30
D1	0.012	0.016	0.30	0.41
D2	0.008	0.011	0.20	0.28
E	0.006	0.008	0.15	0.20
E1	0.005	0.007	0.13	0.18
F	0.012	0.014	0.30	0.36
G	0.025 BSC		0.64 BSC	
J	1.100 BSC		27.94 BSC	
J1	0.550 BSC		13.97 BSC	
K	0.034	0.044	0.86	1.11
K1	0.010 BSC		0.25 BSC	
P	1.100 BSC		27.94 BSC	
P1	0.550 BSC		13.97 BSC	
R1	0.015 REF		0.38 BSC	
S	1.080 BSC		27.43 BSC	
S1	0.540 BSC		13.72 BSC	
U	0.025 REF		0.64 REF	
V	1.080 BSC		27.43 BSC	
V1	0.540 BSC		13.72 BSC	
W	0.006	0.008	0.15	0.20
01	0°	8°	0°	8°

CASE 831A-02
ISSUE B

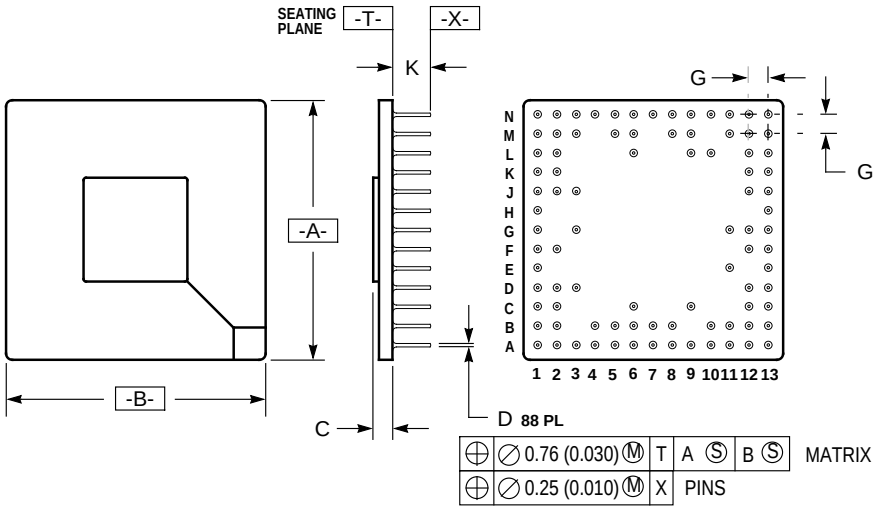
Figure 36 132-pin Plastic Quad Flat Pack (PQFP) Mechanical Information



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.940	0.960	23.88	24.38
B	0.940	0.960	23.88	24.38
C	---	0.125	---	3.17
D	0.008	0.014	0.21	0.35
G	0.025 BSC		0.64 BSC	
H	0.018	0.035	0.46	0.88
J	0.005	0.010	0.13	0.25
K	0.024	0.040	0.61	1.01
L	0.800 BSC		20.32 BSC	
M	0°	8°	0°	8°
S	1.133	1.147	28.78	29.13
V	1.133	1.147	28.78	29.13

CASE 831B-01
ISSUE O

Figure 37 132-pin Ceramic Quad Flat Pack (CQFP) Mechanical Information



DIM	INCHESS		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.340	1.380	34.04	35.05
B	1.340	1.380	34.04	35.05
C	0.085	0.120	2.16	3.04
D	0.017	0.020	0.44	0.50
G	0.100 BSC		2.54 BSC	
K	0.165	0.200	4.20	5.08

CASE 789D-01
ISSUE O

Figure 38 88-pin Ceramic Pin Grid Array (PGA) Package Mechanical Information

Design Considerations

Substituting the DSP56001A for the DSP56001

This section highlights the differences between the DSP56001 and DSP56001A that need to be taken into consideration when substituting the DSP56001A for the DSP56001. New designs should use the DSP56002 due to its enhanced features and speed.

Hardware Considerations

Non-Maskable Interrupt (NMI)

A Non-Maskable Interrupt (NMI) function was previously accessible on the DSP56001 by applying 10 Volts to the MODB / $\overline{\text{IRQB}}$ pin. The DSP56001A does not support a non-maskable interrupt (NMI).

DO NOT APPLY 10 VOLTS TO ANY PIN OF THE DSP56001A (including MODB)! Subjecting any pin of the DSP56001A to voltages in excess of the specified TTL / CMOS levels will permanently damage the device.

AC Electrical Characteristics

The DSP56001A die utilizes a faster technology than the DSP56001. As a result, many DSP56001A signals exhibit faster rise- and fall-times than the same signals on the DSP56001. These faster edges may generate more radiated noise and EMI, and may require more attention to these issues (e.g., the DSP56001A based circuit may require better decoupling).

Software/Application Considerations

Software written for the DSP56001 will generally run unmodified on the DSP56001A. There are, however, certain differences which should be noted. Users should consider the impact these differences may have on each application.

AGU Modify Registers

Numbers between $8000 and $FFFE (inclusive) are not valid values for loading into the modify registers (M0-M7) of the address generation unit on the DSP56001. Certain values within this range, however, enable wrap-around addressing modes on the DSP56001A that are not supported, and inadvertent enabling of these addressing modes may yield unexpected results. Do ***not*** load the modify registers of the DSP56001A with values from $8000 to $FFFE.

Reserved Memory Locations

Certain memory locations are designated as reserved on the DSP56001. Accesses to these memory locations on the DSP56001A will result in unpredictable processor behavior ***including the possibility of halting the processor completely***. In particular, writes to the following X memory locations should be avoided on the DSP56001A:

X:$FFDE, X:$FFDF, X:$FFFC, X:$FFFD

MOVEP to Rn/Nn/Mn Registers

On the DSP56001 there is a pipeline delay when using the MOVEP instruction to change the contents of an address register (Mn, Nn, or Rn). The new contents of the destination address register will not be available for use during the following instruction (i.e, there is a single instruction cycle delay).

On the DSP56001A this pipeline delay has been removed. If an address register (Mn, Nn, or Rn) is directly changed with a MOVEP instruction, the updated contents will be available for use during the following instruction. DSP56001 software which depends on this pipeline delay must be modified when moved onto the DSP56001A.

MOVEP to/from Data ALU Registers

MOVEP Instructions to/from Data ALU Registers take 2 instruction cycles on the DSP56001. On the DSP56001A, these instructions take only 1 instruction cycle. DSP56001 software which is dependent on the timing of this form of the MOVEP instruction must be modified when ported to the DSP56001A.

MOVEP Immediate

MOVEP Immediate instructions take 3 instruction cycles on the DSP56001. On the DSP56001A, these instructions take only 2 instruction cycles. DSP56001 software which is dependent on the timing of this form of the MOVEP instruction must be modified when ported to the DSP56001A.

Illegal Instructions

The instructions listed in Table 23 will ***not*** generate an illegal instruction interrupt on the DSP56001A. None of these instructions are tested on the DSP56001A and should ***not*** be used.

Note: The DEBUG and DEBUGcc instructions are microcoded on the DSP56001A, but the peripherals necessary to make use of this instruction are not available. Any use of the DEBUG or DEBUGcc instructions will completely halt the processor. The processor will exit this state only on reset.

STOP/WAIT Timing

Wake-up from the stop and wait operating modes with $\overline{\text{IRQn}}$ is longer on the DSP56001A by one Tc period.

Table 23 Illegal Instructions

Instruction Symbol	Instruction Name
DEBUG — **DO NOT USE**	Enter debug mode
DEBUGcc — **DO NOT USE**	Enter debug mode conditionally
DEC	Decrement by one
INC	Increment by one
MAC #iiii	Signed multiply-accumulate immediate
MPY #iiii	Signed multiply immediate
MACR #iiii	Signed multiply-accumulate and round immediate
MPYR #iiii	Signed multiply and round immediate

SCI/SSI Initialization Timing

On the DSP56001A, the SCI and SSI clocks are stopped when the peripherals are not enabled in order to save power. As a result, the initialization time of the SCI and SSI is longer on the DSP56001A than on the DSP56001.

Control Registers

The OMR and the Status Register on the DSP56001A have been altered from those on the DSP56001. Refer to Table 24 for details of these alterations.

Host Command Vector Register

The DSP56001A's Host Command Vector Register (CVR) also differs from that of the DSP56001 (see Table 25).

Heat Dissipation

The average chip junction temperature, T_J, in °C, can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JA}) \quad (1)$$

Where:

T_A = ambient temperature, °C

Θ_{JA} = package thermal resistance, junction-to-ambient, °C / W

P_D = $P_{INT} + P_{I/O}$

P_{INT} = $I_{CC} \times V_{CC}$ watts — chip internal power

$P_{I/O}$ = power dissipation on input and output pins — user determined

Table 24 Summary of Control Register Differences

REGISTER	BIT	DSP56001 DEFINITION	DSP56001A DEFINITION	EXPLAINATION OF DIFFERENCE
Status Register	7	Reserved - Read/Written as zero.	Reserved - read as don't care.	On the 001A this bit may be read as 0 or 1. The user should not rely on this bit being a given value.
	14	Reserved - Read/Written as zero.	Reserved - write as zero only, read as don't care.	If this bit is set on the 56001A, the operations performed by the Data ALU change, and 56001 code will yield erroneous results. Write this bit only as zero.
Operating Mode Register	3	Reserved - Read/Written as zero.	Reserved - write as zero only, read as don't care.	If this bit is set, memory reads may be from incorrect locations. Write this bit only as zero.
Port B Control Register	1	Reserved - Written as zero.	Reserved - Written as zero.	Writing this bit as a 1 will result in behavior differences between the 001 and the 001A.

Table 25 Summary of Host Command Vector Register Differences

REGISTER	BIT	DSP56001 DEFINITION	DSP56001A DEFINITION	EXPLAINATION OF DIFFERENCE
Host Command Vector Register (CVR)	5	Reserved - read as zero.	Reserved - read as don't care.	This bit should be written with only a zero on the 56001A.

For most applications $P_{I/O} < P_{INT}$ and $P_{I/O}$ can be neglected. An appropriate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K / (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \times (T_A + 273) + P_D \times \Theta_{JA} \quad (3)$$

Where: K is a constant pertaining to the particular package

K can be determined from equation (2) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A. The total thermal resistance of a package (Θ_{JA}) can be separated into two components, Θ_{JC} and Θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case) surface (Θ_{JC}) and from the case to the outside ambient (Θ_{CA}). These terms are related by the equation:

$$\Theta_{JA} = \Theta_{JC} + \Theta_{CA} \quad (4)$$

Θ_{JC} is device-related and cannot be influenced by the user. However, Θ_{CA} is user-dependent and can be minimized by thermal management techniques such as heat sinks, ambient air cooling, and thermal convection. Thus, good thermal management can significantly reduce Θ_{CA} so that Θ_{JA} approximately equals Θ_{JC}. Values for thermal resistance presented in this document, unless estimated, were derived using the procedure described in Motorola Reliability Report 7843, “Thermal Resistance Measurement Method for MC68XX Microcomponent Devices”, and are provided for design purposes only. Thermal measurements are complex and dependent on procedure and setup. User-derived values for thermal resistance may differ.

Note: Table 6 and Table 7 (page 15) contain the package thermal values for this chip.

Power, Ground, and Noise

Each V_{CC} pin on the DSP should be provided with a low-impedance path to the board's supply. Each GND pin should also be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip as shown in Table 26.

The V_{CC} power supply should be bypassed to GND using at least four 0.1 µF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC} and GND should be less than 0.5" per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes. All output pins on this DSP have fast rise and fall times. Printed Circuit Board (PCB) trace lengths should be minimal. This recommendation particularly applies to the address and data buses as well as the $\overline{RD}$, $\overline{WR}$, $\overline{IRQA}$, $\overline{IRQB}$, $\overline{HEN}$, and $\overline{HACK}$ pins. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PCB traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset.

Power Consumption

Power dissipation is a key issue in portable DSP applications. The following describes some factors which affect current consumption. Current consumption is described by the formula:

$$I = C \times V \times f$$

where: C = node / pin capacitance
V = voltage swing
f = frequency of node / pin toggle

For example, for an address pin loaded with a 50 pF capacitance and operating at 5.5V with a 33 MHz clock, toggling at its maximum possible rate (which is 8.25 MHz), the current consumption is:

$$I = 50 \times 10^{-12} \times 5.5 \times 8.25 \times 10^{6} = 227 \text{ mA}$$

The maximum internal current value (I_{CCI}-max), reflects the maximum possible switching of the internal buses, which is not necessarily a real application case. The typical internal current value (I_{CCI}-typ) reflects the average switching of the internal buses.

The following steps are recommended for applications requiring very low current consumption:

1. minimize external memory accesses; use internal memory accesses instead
2. minimize the number of pins which are switching
3. minimize the capacitive load on the pins
4. connect the unused inputs to pull-up or pull-down resistors

Host Port Considerations

Careful synchronization is required when reading multi-bit registers that are written by another asynchronous system. This is a common problem when two asynchronous systems are connected. The situation exists in the host interface. The following paragraphs present considerations for proper operation.

Host Programming Considerations

1. Unsynchronized Reading of Receive Byte Registers
   When reading receive byte registers, RXH or RXL, the host program should use interrupts or poll the RXDF flag which indicates that data is available. This assures that the data in the receive byte registers will be stable.

2. Overwriting Transmit Byte Registers
   The host program should not write to the transmit byte registers, TXH or TXL, unless the TXDE bit is set, indicating that the transmit byte registers are empty. This guarantees that the transmit byte registers will transfer valid data to the HRX register.

3. Synchronization of Status Bits from DSP to Host
   HC, HREQ, DMA, HF3, HF2, TRDY, TXDE, and RXDF status bits are set or cleared from inside the DSP and read by the host processor (refer to the *User's Manual* for descriptions of these status bits). The host can read these status bits very quickly without regard to the clock rate used by the DSP, but the state of the bit could be changing during the read operation. Generally, this is not a system problem, since the bit will be read correctly in the next pass of any host polling routine. However, if the host asserts $\overline{\text{HEN}}$ for more than timing number (31), with a minimum cycle time of timing number (31) + (32), then these status bits are guaranteed to be stable. Exercise care when reading status bits HF3 and HF2 as an encoded pair. If the DSP changes HF3 and HF2 from 00 to 11, there is a small probability that the host could read the bits during the transition and receive 01 or 10 instead of 11. If the com-

bination of HF3 and HF2 has significance, the host could read the wrong combination. Therefore, read the bits twice and check for consensus.

4. Overwriting the Host Vector
The host program should change the Host Vector register only when the Host Command bit (HC) is clear. This change will guarantee that the DSP interrupt control logic will receive a stable vector.

5. Cancelling a Pending Host Command Exception
The host processor may elect to clear the HC bit to cancel the host command exception request at any time before it is recognized by the DSP. Because the host does not know exactly when the exception will be recognized (due to exception processing synchronization and pipeline delays), the DSP may execute the host command exception after the HC bit is cleared. For these reasons, the HV bits must not be changed at the same time that the HC bit is cleared.

6. Variance in the Host Interface Timing
The Host Interface (HI) may vary. Therefore, a host which attempts to load (bootstrap) the DSP should first make sure that the part has completed its HI port programming (e.g. by setting the INIT bit in ICR then polling it and waiting it to be cleared, then reading the ISR or by writing the TREQ/RREQ together with the INIT and then polling INIT, ISR, and the $\overline{\text{HREQ}}$ pin).

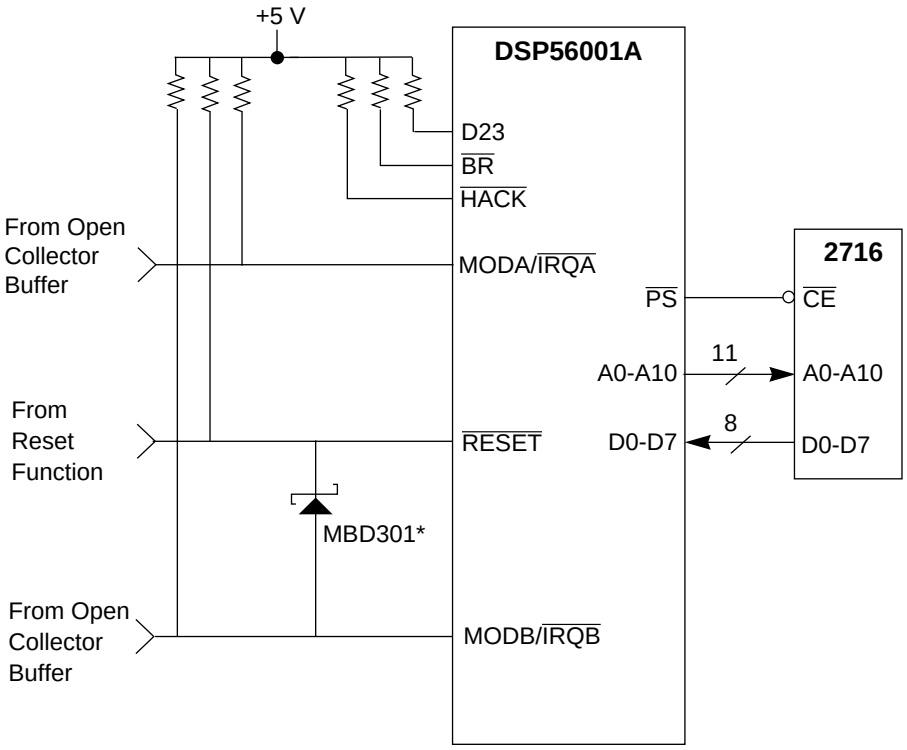
DSP Programming Considerations

1. Synchronization of Status Bits from Host to DSP
DMA, HF1, HF0, and HCP, HTDE, and HRDF status bits are set or cleared by the host processor side of the interface. These bits are individually synchronized to the DSP clock. (Refer to the *User's Manual* for descriptions of these status bits.)

2. Reading HF0 and HF1 as an Encoded Pair
Care must be exercised when reading status bits HF0 and HF1 as an encoded pair, i.e., the four combinations 00, 01, 10, and 11 each have significance. A very small probability exists that the DSP will read the status bits synchronized during transition. Therefore, HF0 and HF1 should be read twice and checked for consensus.

Application Examples

The lowest cost DSP56001A-based system is shown in Figure 39. It uses no run time external memory and requires only two chips, the DSP56001A and a low cost EPROM. The EPROM read access time should be less than 780 nanoseconds when the DSP56001A is operating at a clock rate of 20.5 MHz.

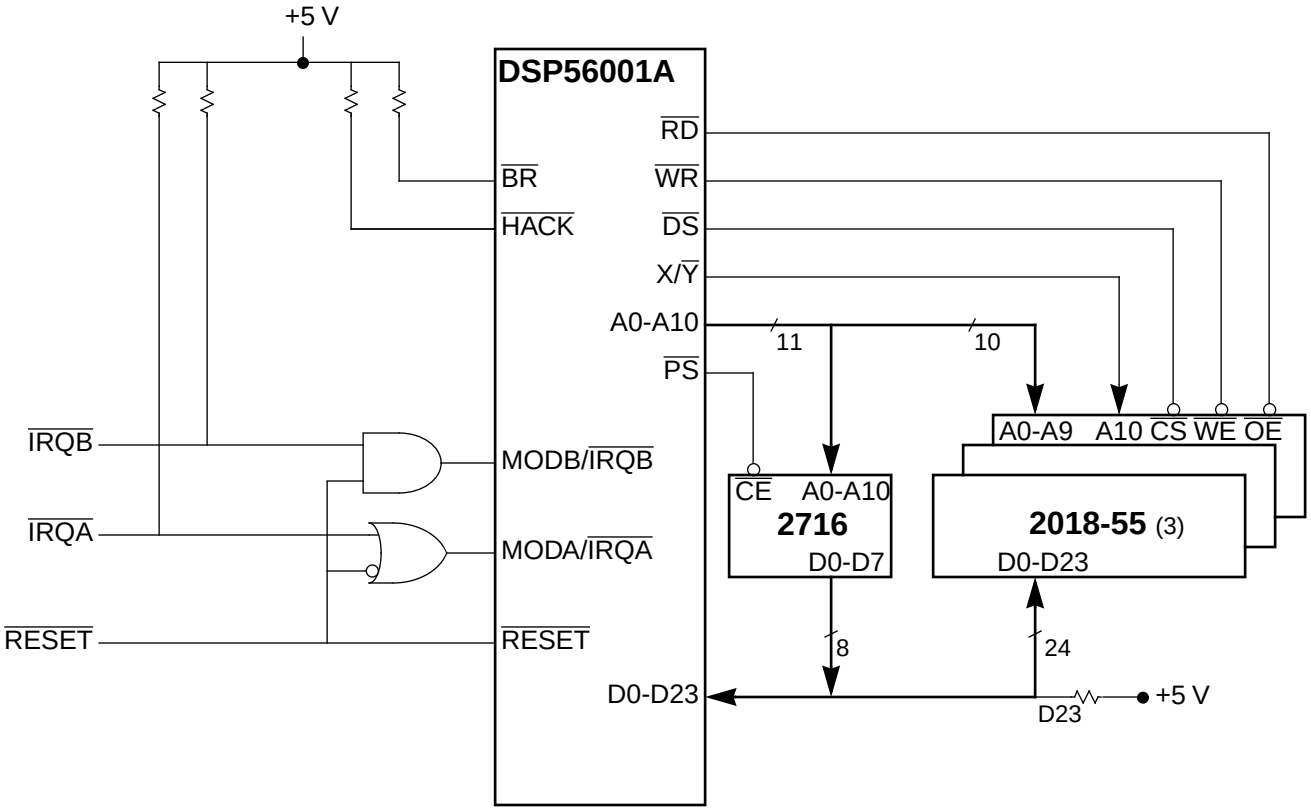


NOTES:

1. ***These diodes **must** be Schottky diodes.
2. All resistors are 15 KΩ unless noted otherwise.
3. When in Reset, $\overline{IRQA}$ and $\overline{IRQB}$ must be deasserted by external peripherals.

Figure 39 No Glue Logic, Low Cost Memory Port Bootstrap — Mode 1

A system with external data RAM memory requires no glue logic to select the external EPROM from bootstrap mode. $\overline{PS}$ is used to enable the EPROM and $\overline{DS}$ is used to enable the high speed data memories as shown in Figure 40.

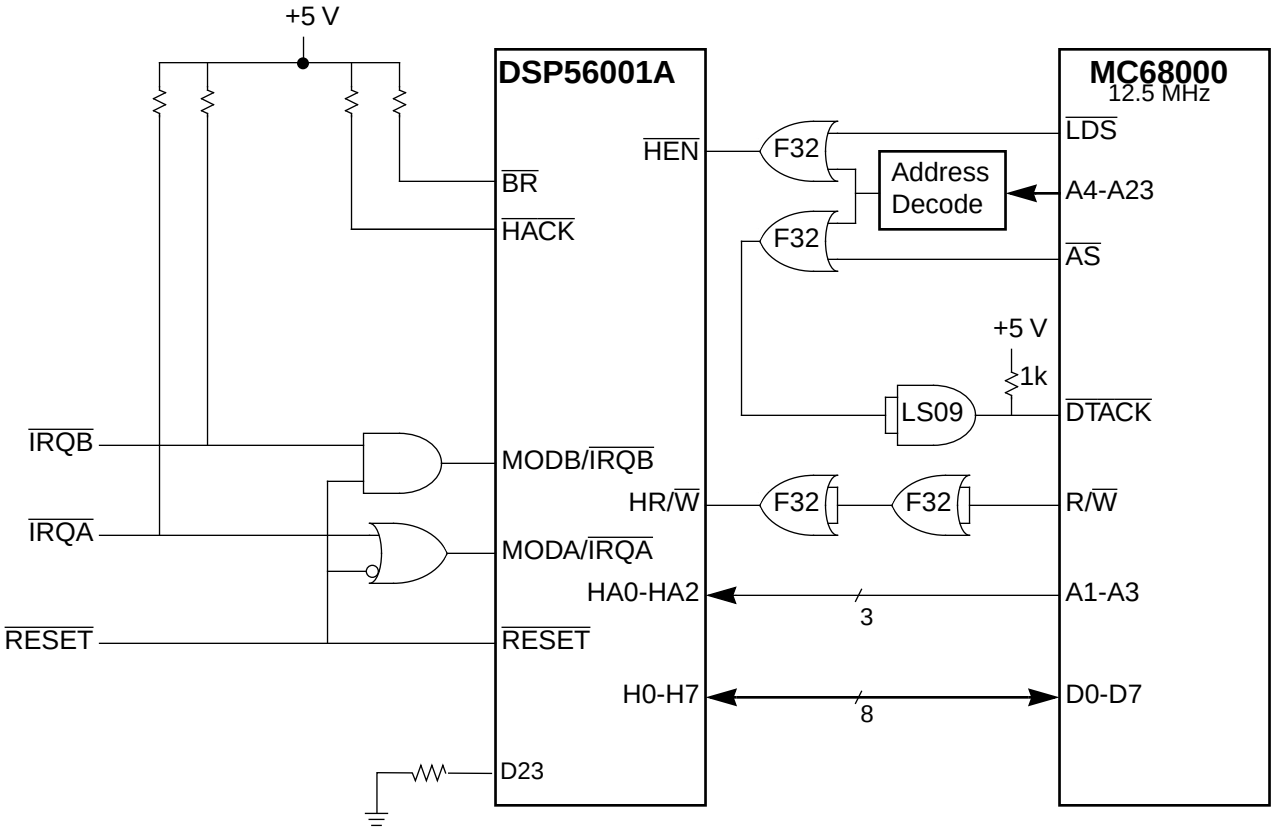


NOTES:

1. All resistors are 15 KΩ unless noted otherwise.
2. When in Reset, $\overline{IRQA}$ and $\overline{IRQB}$ must be deasserted by external peripherals.

Figure 40 Port A Bootstrap with External Data RAM — Mode 1

Figure 41 shows the DSP56001A bootstrapping via the Host Port from an MC68000.



NOTES:

1. All resistors are 15 KΩ unless noted otherwise.
2. When in Reset, $\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$ must be deasserted by external peripherals.

Figure 41 DSP56001A Host Bootstrap Example — Mode 5

In Figure 42, the DSP56001A is operated in mode 3 with external program memory and the reset vector at location $0000. The programmer can overlay the high speed on-chip P:RAM with DSP algorithms by using the MOVEM instruction.

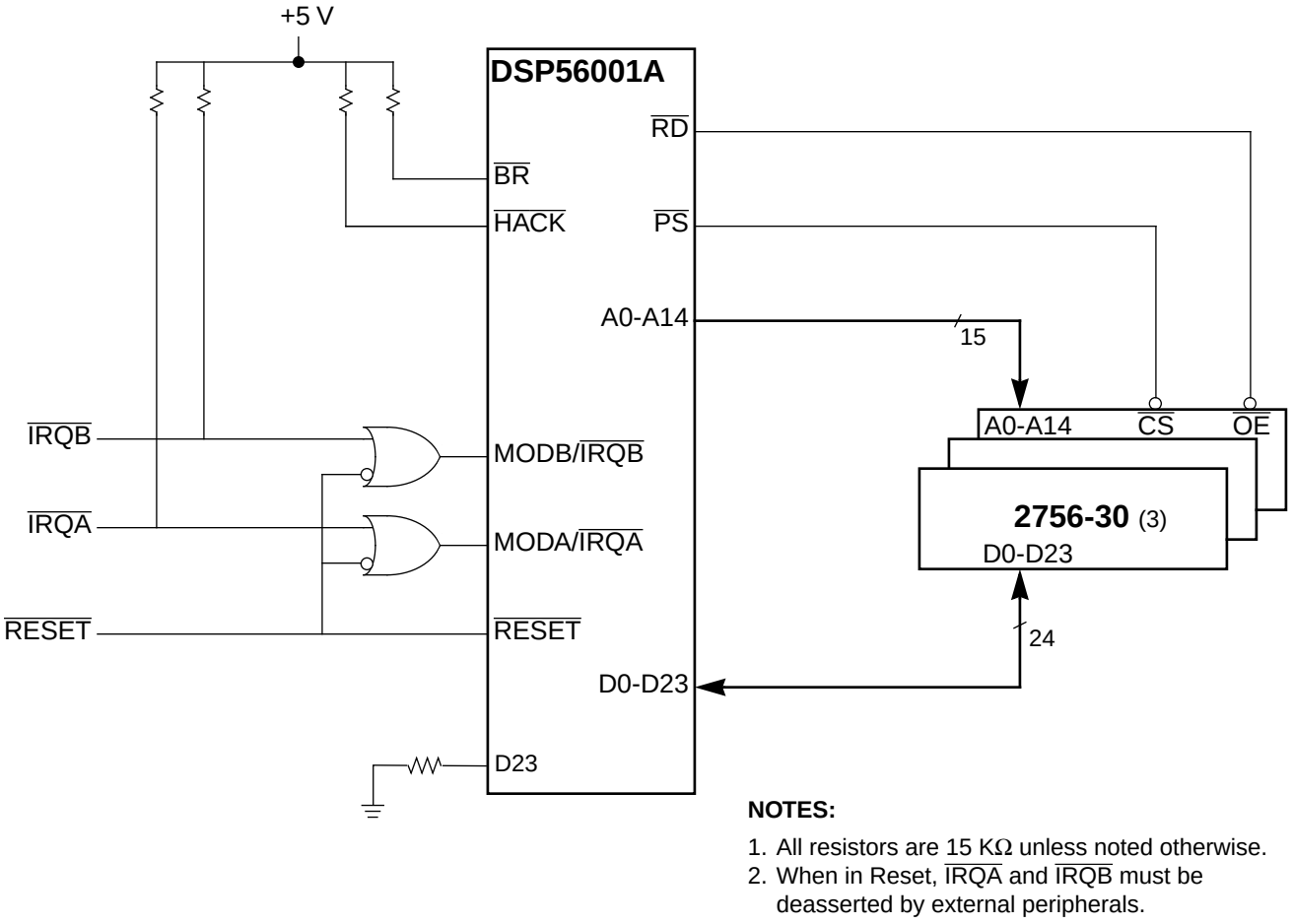


Figure 42 32K Words of External Program ROM — Mode 3

Figure 43 shows a circuit which waits until V_{CC} on the DSP56001A is at least 4.5 V before initiating a $75{,}000 \times T_C$ oscillator stabilization delay required for the on-chip oscillator (only $25 \times T_C$ is required for an external oscillator). This insures that the DSP is operational and stable before releasing the reset signal.

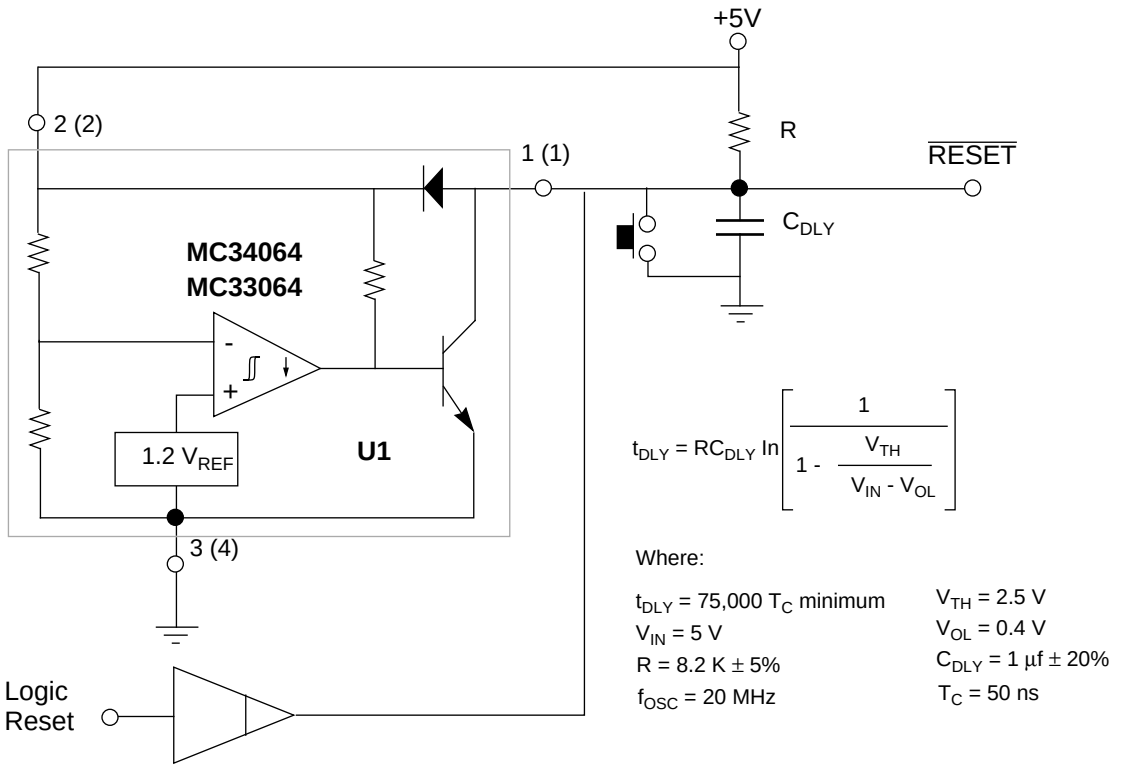


Figure 43 Reset Circuit Using MC34064/MC33064

Figure 44 shows the DSP56001A connected to the bus of an IBM-PC computer. This circuit is complete and does not require external ROM or RAM to load and execute code from the PC. The PAL equations and other details of this circuit are available in the application report entitled “DSP56001 Interface Techniques and Examples” (APR11/D).

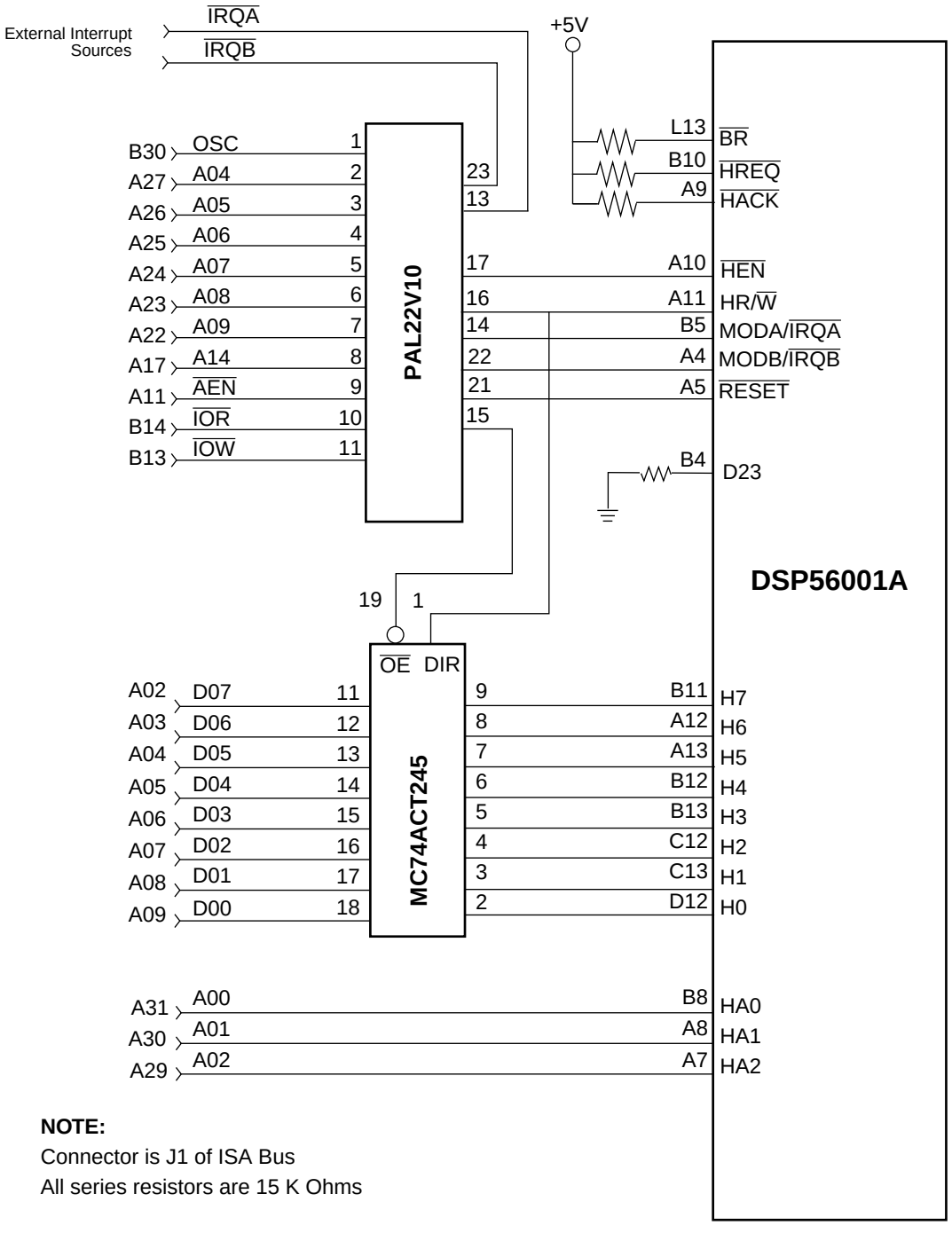


Figure 44 DSP56001A -to- ISA Bus Interface Schematic

ROM Table Listings

μ-Law/A-Law Expansion Tables

The following table contains the mu-law (μ-law) and A-law expansion listings.

Table 23 μ-Law/A-Law Expansion Table Contents

```
        ORG  X:$100
  ;
M_00    DC   $7D7C00  ; 8031
M_01    DC   $797C00  ; 7775
M_02    DC   $757C00  ; 7519
M_03    DC   $717C00  ; 7263
M_04    DC   $6D7C00  ; 7007
M_05    DC   $697C00  ; 6751
M_06    DC   $657C00  ; 6495
M_07    DC   $617C00  ; 6239
M_08    DC   $5D7C00  ; 5983
M_09    DC   $597C00  ; 5727
M_0A    DC   $557C00  ; 5471
M_0B    DC   $517C00  ; 5215
M_0C    DC   $4D7C00  ; 4959
M_0D    DC   $497C00  ; 4703
M_0E    DC   $457C00  ; 4447
M_0F    DC   $417C00  ; 4191
M_10    DC   $3E7C00  ; 3999
M_11    DC   $3C7C00  ; 3871
M_12    DC   $3A7C00  ; 3743
M_13    DC   $387C00  ; 3615
M_14    DC   $367C00  ; 3487
M_15    DC   $347C00  ; 3359
M_16    DC   $327C00  ; 3231
M_17    DC   $307C00  ; 3103
M_18    DC   $2E7C00  ; 2975
M_19    DC   $2C7C00  ; 2847
M_1A    DC   $2A7C00  ; 2719
M_1B    DC   $287C00  ; 2591
M_1C    DC   $267C00  ; 2463
M_1D    DC   $247C00  ; 2335
M_1E    DC   $227C00  ; 2207
M_1F    DC   $207C00  ; 2079
M_20    DC   $1EFC00  ; 1983
M_21    DC   $1DFC00  ; 1919
M_22    DC   $1CFC00  ; 1855
M_23    DC   $1BFC00  ; 1791
M_24    DC   $1AFC00  ; 1727
M_25    DC   $19FC00  ; 1663
M_26    DC   $18FC00  ; 1599
M_27    DC   $17FC00  ; 1535
M_28    DC   $16FC00  ; 1471
M_29    DC   $15FC00  ; 1407
M_2A    DC   $14FC00  ; 1343
M_2B    DC   $13FC00  ; 1279
M_2C    DC   $12FC00  ; 1215
M_2D    DC   $11FC00  ; 1151
M_2E    DC   $10FC00  ; 1087
M_2F    DC   $0FFC00  ; 1023
M_30    DC   $0F3C00  ;  975
M_31    DC   $0EBC00  ;  943
M_32    DC   $0E3C00  ;  911
M_33    DC   $0DBC00  ;  879
M_34    DC   $0D3C00  ;  847
M_35    DC   $0CBC00  ;  815
M_36    DC   $0C3C00  ;  783
M_37    DC   $0BBC00  ;  751
M_38    DC   $0B3C00  ;  719
M_39    DC   $0ABC00  ;  687
M_3A    DC   $0A3C00  ;  655
M_3B    DC   $09BC00  ;  623
M_3C    DC   $093C00  ;  591
M_3D    DC   $08BC00  ;  559
M_3E    DC   $083C00  ;  527
M_3F    DC   $07BC00  ;  495
M_40    DC   $075C00  ;  471
M_41    DC   $071C00  ;  455
M_42    DC   $06DC00  ;  439
M_43    DC   $069C00  ;  423
M_44    DC   $065C00  ;  407
M_45    DC   $061C00  ;  391
M_46    DC   $05DC00  ;  375
M_47    DC   $059C00  ;  359
M_48    DC   $055C00  ;  343
M_49    DC   $051C00  ;  327
M_4A    DC   $04DC00  ;  311
M_4B    DC   $049C00  ;  295
M_4C    DC   $045C00  ;  279
M_4D    DC   $041C00  ;  263
M_4E    DC   $03DC00  ;  247
M_4F    DC   $039C00  ;  231
M_50    DC   $036C00  ;  219
M_51    DC   $034C00  ;  211
M_52    DC   $032C00  ;  203
M_53    DC   $030C00  ;  195
```

Table 23 μ-Law/A-Law Expansion Table Contents (continued)

```
M_54   DC   $02EC00  ;  187        A_84   DC   $118000  ;  560
M_55   DC   $02CC00  ;  179        A_85   DC   $108000  ;  528
M_56   DC   $02AC00  ;  171        A_86   DC   $138000  ;  624
M_57   DC   $028C00  ;  163        A_87   DC   $128000  ;  592
M_58   DC   $026C00  ;  155        A_88   DC   $1D8000  ;  944
M_59   DC   $024C00  ;  147        A_89   DC   $1C8000  ;  912
M_5A   DC   $022C00  ;  139        A_8A   DC   $1F8000  ; 1008
M_5B   DC   $020C00  ;  131        A_8B   DC   $1E8000  ;  976
M_5C   DC   $01EC00  ;  123        A_8C   DC   $198000  ;  816
M_5D   DC   $01CC00  ;  115        A_8D   DC   $188000  ;  784
M_5E   DC   $01AC00  ;  107        A_8E   DC   $1B8000  ;  880
M_5F   DC   $018C00  ;   99        A_8F   DC   $1A8000  ;  848
M_60   DC   $017400  ;   93        A_90   DC   $0AC000  ;  344
M_61   DC   $016400  ;   89        A_91   DC   $0A4000  ;  328
M_62   DC   $015400  ;   85        A_92   DC   $0BC000  ;  376
M_63   DC   $014400  ;   81        A_93   DC   $0B4000  ;  360
M_64   DC   $013400  ;   77        A_94   DC   $08C000  ;  280
M_65   DC   $012400  ;   73        A_95   DC   $084000  ;  264
M_66   DC   $011400  ;   69        A_96   DC   $09C000  ;  312
M_67   DC   $010400  ;   65        A_97   DC   $094000  ;  296
M_68   DC   $00F400  ;   61        A_98   DC   $0EC000  ;  472
M_69   DC   $00E400  ;   57        A_99   DC   $0E4000  ;  456
M_6A   DC   $00D400  ;   53        A_9A   DC   $0FC000  ;  504
M_6B   DC   $00C400  ;   49        A_9B   DC   $0F4000  ;  488
M_6C   DC   $00B400  ;   45        A_9C   DC   $0CC000  ;  408
M_6D   DC   $00A400  ;   41        A_9D   DC   $0C4000  ;  392
M_6E   DC   $009400  ;   37        A_9E   DC   $0DC000  ;  440
M_6F   DC   $008400  ;   33        A_9F   DC   $0D4000  ;  424
M_70   DC   $007800  ;   30        A_A0   DC   $560000  ; 2752
M_71   DC   $007000  ;   28        A_A1   DC   $520000  ; 2624
M_72   DC   $006800  ;   26        A_A2   DC   $5E0000  ; 3008
M_73   DC   $006000  ;   24        A_A3   DC   $5A0000  ; 2880
M_74   DC   $005800  ;   22        A_A4   DC   $460000  ; 2240
M_75   DC   $005000  ;   20        A_A5   DC   $420000  ; 2112
M_76   DC   $004800  ;   18        A_A6   DC   $4E0000  ; 2496
M_77   DC   $004000  ;   16        A_A7   DC   $4A0000  ; 2368
M_78   DC   $003800  ;   14        A_A8   DC   $760000  ; 3776
M_79   DC   $003000  ;   12        A_A9   DC   $720000  ; 3648
M_7A   DC   $002800  ;   10        A_AA   DC   $7E0000  ; 4032
M_7B   DC   $002000  ;    8        A_AB   DC   $7A0000  ; 3904
M_7C   DC   $001800  ;    6        A_AC   DC   $660000  ; 3264
M_7D   DC   $001000  ;    4        A_AD   DC   $620000  ; 3136
M_7E   DC   $000800  ;    2        A_AE   DC   $6E0000  ; 3520
M_7F   DC   $000000  ;    0        A_AF   DC   $6A0000  ; 3392
A_80   DC   $158000  ;  688        A_B0   DC   $2B0000  ; 1376
A_81   DC   $148000  ;  656        A_B1   DC   $290000  ; 1312
A_82   DC   $178000  ;  752        A_B2   DC   $2F0000  ; 1504
A_83   DC   $168000  ;  720        A_B3   DC   $2D0000  ; 1440
```

Table 23 μ-Law/A-Law Expansion Table Contents (continued)

```
A_B4    DC    $230000  ; 1120          A_DA    DC    $00F800  ;   31
A_B5    DC    $210000  ; 1056          A_DB    DC    $00E800  ;   29
A_B6    DC    $270000  ; 1248          A_DC    DC    $009800  ;   19
A_B7    DC    $250000  ; 1184          A_DD    DC    $008800  ;   17
A_B8    DC    $3B0000  ; 1888          A_DE    DC    $00B800  ;   23
A_B9    DC    $390000  ; 1824          A_DF    DC    $00A800  ;   21
A_BA    DC    $3F0000  ; 2016          A_E0    DC    $056000  ;  172
A_BB    DC    $3D0000  ; 1952          A_E1    DC    $052000  ;  164
A_BC    DC    $330000  ; 1632          A_E2    DC    $05E000  ;  188
A_BD    DC    $310000  ; 1568          A_E3    DC    $05A000  ;  180
A_BE    DC    $370000  ; 1760          A_E4    DC    $046000  ;  140
A_BF    DC    $350000  ; 1696          A_E5    DC    $042000  ;  132
A_C0    DC    $015800  ;   43          A_E6    DC    $04E000  ;  156
A_C1    DC    $014800  ;   41          A_E7    DC    $04A000  ;  148
A_C2    DC    $017800  ;   47          A_E8    DC    $076000  ;  236
A_C3    DC    $016800  ;   45          A_E9    DC    $072000  ;  228
A_C4    DC    $011800  ;   35          A_EA    DC    $07E000  ;  252
A_C5    DC    $010800  ;   33          A_EB    DC    $07A000  ;  244
A_C6    DC    $013800  ;   39          A_EC    DC    $066000  ;  204
A_C7    DC    $012800  ;   37          A_ED    DC    $062000  ;  196
A_C8    DC    $01D800  ;   59          A_EE    DC    $06E000  ;  220
A_C9    DC    $01C800  ;   57          A_EF    DC    $06A000  ;  212
A_CA    DC    $01F800  ;   63          A_F0    DC    $02B000  ;   86
A_CB    DC    $01E800  ;   61          A_F1    DC    $029000  ;   82
A_CC    DC    $019800  ;   51          A_F2    DC    $02F000  ;   94
A_CD    DC    $018800  ;   49          A_F3    DC    $02D000  ;   90
A_CE    DC    $01B800  ;   55          A_F4    DC    $023000  ;   70
A_CF    DC    $01A800  ;   53          A_F5    DC    $021000  ;   66
A_D0    DC    $005800  ;   11          A_F6    DC    $027000  ;   78
A_D1    DC    $004800  ;    9          A_F7    DC    $025000  ;   74
A_D2    DC    $007800  ;   15          A_F8    DC    $03B000  ;  118
A_D3    DC    $006800  ;   13          A_F9    DC    $039000  ;  114
A_D4    DC    $001800  ;    3          A_FA    DC    $03F000  ;  126
A_D5    DC    $000800  ;    1          A_FB    DC    $03D000  ;  122
A_D6    DC    $003800  ;    7          A_FC    DC    $033000  ;  102
A_D7    DC    $002800  ;    5          A_FD    DC    $031000  ;   98
A_D8    DC    $00D800  ;   27          A_FE    DC    $037000  ;  110
A_D9    DC    $00C800  ;   25          A_FF    DC    $035000  ;  106
```

Sine Wave Table

This sine wave table (Table 24) is normally used by FFT routines which use bit-reversed address pointers. This table can be used as it is for up to 512 point FFTs; however, for larger FFTs, the table must be copied to a different memory location to allow the reverse-carry addressing mode to be used (see REVERSE-CARRY MODIFIER (Mn = $0000) in the *DSP56001 User's Manual* for additional information)**.**

Table 24 Sine Wave Table Contents

```
     ORG  Y:$100
;
S_00 DC   $000000  ; +0.0000000000     S_24 DC   $62F202  ; +0.7730104923
S_01 DC   $03242B  ; +0.0245412998     S_25 DC   $64E889  ; +0.7883464098
S_02 DC   $0647D9  ; +0.0490676016     S_26 DC   $66CF81  ; +0.8032075167
S_03 DC   $096A90  ; +0.0735644996     S_27 DC   $68A69F  ; +0.8175848722
S_04 DC   $0C8BD3  ; +0.0980170965     S_28 DC   $6A6D99  ; +0.8314697146
S_05 DC   $0FAB27  ; +0.1224106997     S_29 DC   $6C2429  ; +0.8448535204
S_06 DC   $12C810  ; +0.1467303932     S_2A DC   $6DCA0D  ; +0.8577286005
S_07 DC   $15E214  ; +0.1709619015     S_2B DC   $6F5F03  ; +0.8700870275
S_08 DC   $18F8B8  ; +0.1950902939     S_2C DC   $70E2CC  ; +0.8819212914
S_09 DC   $1C0B82  ; +0.2191012055     S_2D DC   $72552D  ; +0.8932244182
S_0A DC   $1F19F9  ; +0.2429800928     S_2E DC   $73B5EC  ; +0.9039893150
S_0B DC   $2223A5  ; +0.2667128146     S_2F DC   $7504D3  ; +0.9142097235
S_0C DC   $25280C  ; +0.2902846038     S_30 DC   $7641AF  ; +0.9238795042
S_0D DC   $2826B9  ; +0.3136816919     S_31 DC   $776C4F  ; +0.9329928160
S_0E DC   $2B1F35  ; +0.3368898928     S_32 DC   $788484  ; +0.9415441155
S_0F DC   $2E110A  ; +0.3598949909     S_33 DC   $798A24  ; +0.9495282173
S_10 DC   $30FBC5  ; +0.3826833963     S_34 DC   $7A7D05  ; +0.9569402933
S_11 DC   $33DEF3  ; +0.4052414000     S_35 DC   $7B5D04  ; +0.9637761116
S_12 DC   $36BA20  ; +0.4275551140     S_36 DC   $7C29FC  ; +0.9700313210
S_13 DC   $398CDD  ; +0.4496113062     S_37 DC   $7CE3CF  ; +0.9757022262
S_14 DC   $3C56BA  ; +0.4713967144     S_38 DC   $7D8A5F  ; +0.9807853103
S_15 DC   $3F174A  ; +0.4928981960     S_39 DC   $7E1D94  ; +0.9852777123
S_16 DC   $41CE1E  ; +0.5141026974     S_3A DC   $7E9D56  ; +0.9891765118
S_17 DC   $447ACD  ; +0.5349975824     S_3B DC   $7F0992  ; +0.9924796224
S_18 DC   $471CED  ; +0.5555701852     S_3C DC   $7F6237  ; +0.9951847792
S_19 DC   $49B415  ; +0.5758082271     S_3D DC   $7FA737  ; +0.9972904921
S_1A DC   $4C3FE0  ; +0.5956993103     S_3E DC   $7FD888  ; +0.9987955093
S_1B DC   $4EBFE9  ; +0.6152315736     S_3F DC   $7FF622  ; +0.9996988773
S_1C DC   $5133CD  ; +0.6343932748     S_40 DC   $7FFFFF  ; +0.9999998808
S_1D DC   $539B2B  ; +0.6531729102     S_41 DC   $7FF622  ; +0.9996988773
S_1E DC   $55F5A5  ; +0.6715589762     S_42 DC   $7FD888  ; +0.9987955093
S_1F DC   $5842DD  ; +0.6895405054     S_43 DC   $7FA737  ; +0.9972904921
S_20 DC   $5A827A  ; +0.7071068287     S_44 DC   $7F6237  ; +0.9951847792
S_21 DC   $5CB421  ; +0.7242470980     S_45 DC   $7F0992  ; +0.9924796224
S_22 DC   $5ED77D  ; +0.7409511805     S_46 DC   $7E9D56  ; +0.9891765118
S_23 DC   $60EC38  ; +0.7572088242     S_47 DC   $7E1D94  ; +0.9852777123
```

Table 24 Sine Wave Table Contents (continued)

```
S_48 DC   $7D8A5F  ; +0.9807853103     S_78 DC   $18F8B8  ; +0.1950902939
S_49 DC   $7CE3CF  ; +0.9757022262     S_79 DC   $15E214  ; +0.1709619015
S_4A DC   $7C29FC  ; +0.9700313210     S_7A DC   $12C810  ; +0.1467303932
S_4B DC   $7B5D04  ; +0.9637761116     S_7B DC   $0FAB27  ; +0.1224106997
S_4C DC   $7A7D05  ; +0.9569402933     S_7C DC   $0C8BD3  ; +0.0980170965
S_4D DC   $798A24  ; +0.9495282173     S_7D DC   $096A90  ; +0.0735644996
S_4E DC   $788484  ; +0.9415441155     S_7E DC   $0647D9  ; +0.0490676016
S_4F DC   $776C4F  ; +0.9329928160     S_7F DC   $03242B  ; +0.0245412998
S_50 DC   $7641AF  ; +0.9238795042     S_80 DC   $000000  ; +0.0000000000
S_51 DC   $7504D3  ; +0.9142097235     S_81 DC   $FCDBD5  ; -0.0245412998
S_52 DC   $73B5EC  ; +0.9039893150     S_82 DC   $F9B827  ; -0.0490676016
S_53 DC   $72552D  ; +0.8932244182     S_83 DC   $F69570  ; -0.0735644996
S_54 DC   $70E2CC  ; +0.8819212914     S_84 DC   $F3742D  ; -0.0980170965
S_55 DC   $6F5F03  ; +0.8700870275     S_85 DC   $F054D9  ; -0.1224106997
S_56 DC   $6DCA0D  ; +0.8577286005     S_86 DC   $ED37F0  ; -0.1467303932
S_57 DC   $6C2429  ; +0.8448535204     S_87 DC   $EA1DEC  ; -0.1709619015
S_58 DC   $6A6D99  ; +0.8314697146     S_88 DC   $E70748  ; -0.1950902939
S_59 DC   $68A69F  ; +0.8175848722     S_89 DC   $E3F47E  ; -0.2191012055
S_5A DC   $66CF81  ; +0.8032075167     S_8A DC   $E0E607  ; -0.2429800928
S_5B DC   $64E889  ; +0.7883464098     S_8B DC   $DDDC5B  ; -0.2667128146
S_5C DC   $62F202  ; +0.7730104923     S_8C DC   $DAD7F4  ; -0.2902846038
S_5D DC   $60EC38  ; +0.7572088242     S_8D DC   $D7D947  ; -0.3136816919
S_5E DC   $5ED77D  ; +0.7409511805     S_8E DC   $D4E0CB  ; -0.3368898928
S_5F DC   $5CB421  ; +0.7242470980     S_8F DC   $D1EEF6  ; -0.3598949909
S_60 DC   $5A827A  ; +0.7071068287     S_90 DC   $CF043B  ; -0.3826833963
S_61 DC   $5842DD  ; +0.6895405054     S_91 DC   $CC210D  ; -0.4052414000
S_62 DC   $55F5A5  ; +0.6715589762     S_92 DC   $C945E0  ; -0.4275551140
S_63 DC   $539B2B  ; +0.6531729102     S_93 DC   $C67323  ; -0.4496113062
S_64 DC   $5133CD  ; +0.6343932748     S_94 DC   $C3A946  ; -0.4713967144
S_65 DC   $4EBFE9  ; +0.6152315736     S_95 DC   $C0E8B6  ; -0.4928981960
S_66 DC   $4C3FE0  ; +0.5956993103     S_96 DC   $BE31E2  ; -0.5141026974
S_67 DC   $49B415  ; +0.5758082271     S_97 DC   $BB8533  ; -0.5349975824
S_68 DC   $471CED  ; +0.5555701852     S_98 DC   $B8E313  ; -0.5555701852
S_69 DC   $447ACD  ; +0.5349975824     S_99 DC   $B64BEB  ; -0.5758082271
S_6A DC   $41CE1E  ; +0.5141026974     S_9A DC   $B3C020  ; -0.5956993103
S_6B DC   $3F174A  ; +0.4928981960     S_9B DC   $B14017  ; -0.6152315736
S_6C DC   $3C56BA  ; +0.4713967144     S_9C DC   $AECC33  ; -0.6343932748
S_6D DC   $398CDD  ; +0.4496113062     S_9D DC   $AC64D5  ; -0.6531729102
S_6E DC   $36BA20  ; +0.4275551140     S_9E DC   $AA0A5B  ; -0.6715589762
S_6F DC   $33DEF3  ; +0.4052414000     S_9F DC   $A7BD23  ; -0.6895405054
S_70 DC   $30FBC5  ; +0.3826833963     S_A0 DC   $A57D86  ; -0.7071068287
S_71 DC   $2E110A  ; +0.3598949909     S_A1 DC   $A34BDF  ; -0.7242470980
S_72 DC   $2B1F35  ; +0.3368898928     S_A2 DC   $A12883  ; -0.7409511805
S_73 DC   $2826B9  ; +0.3136816919     S_A3 DC   $9F13C8  ; -0.7572088242
S_74 DC   $25280C  ; +0.2902846038     S_A4 DC   $9D0DFE  ; -0.7730104923
S_75 DC   $2223A5  ; +0.2667128146     S_A5 DC   $9B1777  ; -0.7883464098
S_76 DC   $1F19F9  ; +0.2429800928     S_A6 DC   $99307F  ; -0.8032075167
S_77 DC   $1C0B82  ; +0.2191012055     S_A7 DC   $975961  ; -0.8175848722
```

Table 24 Sine Wave Table Contents (continued)

```
S_A8 DC   $959267  ; -0.8314697146     S_D4 DC   $8F1D34  ; -0.8819212914
S_A9 DC   $93DBD7  ; -0.8448535204     S_D5 DC   $90A0FD  ; -0.8700870275
S_AA DC   $9235F3  ; -0.8577286005     S_D6 DC   $9235F3  ; -0.8577286005
S_AB DC   $90A0FD  ; -0.8700870275     S_D7 DC   $93DBD7  ; -0.8448535204
S_AC DC   $8F1D34  ; -0.8819212914     S_D8 DC   $959267  ; -0.8314697146
S_AD DC   $8DAAD3  ; -0.8932244182     S_D9 DC   $975961  ; -0.8175848722
S_AE DC   $8C4A14  ; -0.9039893150     S_DA DC   $99307F  ; -0.8032075167
S_AF DC   $8AFB2D  ; -0.9142097235     S_DB DC   $9B1777  ; -0.7883464098
S_B0 DC   $89BE51  ; -0.9238795042     S_DC DC   $9D0DFE  ; -0.7730104923
S_B1 DC   $8893B1  ; -0.9329928160     S_DD DC   $9F13C8  ; -0.7572088242
S_B2 DC   $877B7C  ; -0.9415441155     S_DE DC   $A12883  ; -0.7409511805
S_B3 DC   $8675DC  ; -0.9495282173     S_DF DC   $A34BDF  ; -0.7242470980
S_B4 DC   $8582FB  ; -0.9569402933     S_E0 DC   $A57D86  ; -0.7071068287
S_B5 DC   $84A2FC  ; -0.9637761116     S_E1 DC   $A7BD23  ; -0.6895405054
S_B6 DC   $83D604  ; -0.9700313210     S_E2 DC   $AA0A5B  ; -0.6715589762
S_B7 DC   $831C31  ; -0.9757022262     S_E3 DC   $AC64D5  ; -0.6531729102
S_B8 DC   $8275A1  ; -0.9807853103     S_E4 DC   $AECC33  ; -0.6343932748
S_B9 DC   $81E26C  ; -0.9852777123     S_E5 DC   $B14017  ; -0.6152315736
S_BA DC   $8162AA  ; -0.9891765118     S_E6 DC   $B3C020  ; -0.5956993103
S_BB DC   $80F66E  ; -0.9924796224     S_E7 DC   $B64BEB  ; -0.5758082271
S_BC DC   $809DC9  ; -0.9951847792     S_E8 DC   $B8E313  ; -0.5555701852
S_BD DC   $8058C9  ; -0.9972904921     S_E9 DC   $BB8533  ; -0.5349975824
S_BE DC   $802778  ; -0.9987955093     S_EA DC   $BE31E2  ; -0.5141026974
S_BF DC   $8009DE  ; -0.9996988773     S_EB DC   $C0E8B6  ; -0.4928981960
S_C0 DC   $800000  ; -1.0000000000     S_EC DC   $C3A946  ; -0.4713967144
S_C1 DC   $8009DE  ; -0.9996988773     S_ED DC   $C67323  ; -0.4496113062
S_C2 DC   $802778  ; -0.9987955093     S_EE DC   $C945E0  ; -0.4275551140
S_C3 DC   $8058C9  ; -0.9972904921     S_EF DC   $CC210D  ; -0.4052414000
S_C4 DC   $809DC9  ; -0.9951847792     S_F0 DC   $CF043B  ; -0.3826833963
S_C5 DC   $80F66E  ; -0.9924796224     S_F1 DC   $D1EEF6  ; -0.3598949909
S_C6 DC   $8162AA  ; -0.9891765118     S_F2 DC   $D4E0CB  ; -0.3368898928
S_C7 DC   $81E26C  ; -0.9852777123     S_F3 DC   $D7D947  ; -0.3136816919
S_C8 DC   $8275A1  ; -0.9807853103     S_F4 DC   $DAD7F4  ; -0.2902846038
S_C9 DC   $831C31  ; -0.9757022262     S_F5 DC   $DDDC5B  ; -0.2667128146
S_CA DC   $83D604  ; -0.9700313210     S_F6 DC   $E0E607  ; -0.2429800928
S_CB DC   $84A2FC  ; -0.9637761116     S_F7 DC   $E3F47E  ; -0.2191012055
S_CC DC   $8582FB  ; -0.9569402933     S_F8 DC   $E70748  ; -0.1950902939
S_CD DC   $8675DC  ; -0.9495282173     S_F9 DC   $EA1DEC  ; -0.1709619015
S_CE DC   $877B7C  ; -0.9415441155     S_FA DC   $ED37F0  ; -0.1467303932
S_CF DC   $8893B1  ; -0.9329928160     S_FB DC   $F054D9  ; -0.1224106997
S_D0 DC   $89BE51  ; -0.9238795042     S_FC DC   $F3742D  ; -0.0980170965
S_D1 DC   $8AFB2D  ; -0.9142097235     S_FD DC   $F69570  ; -0.0735644996
S_D2 DC   $8C4A14  ; -0.9039893150     S_FE DC   $F9B827  ; -0.0490676016
S_D3 DC   $8DAAD3  ; -0.8932244182     S_FF DC   $FCDBD5  ; -0.0245412998
```

Ordering Information

Table 25 lists the pertinent information needed to place an order. Consult a Motorola Semiconductor sales office or authorized distributor to determine availability and to order parts.

Table 25 DSP56001A Ordering Information

Part	Package Type	Pin Count	Frequency (MHz)	Order Number
DSP56001A	Ceramic Pin-Grid Array (PGA)	88	20.5	DSP56001ARC20
			27	DSP56001ARC27
			33	DSP56001ARC33
	Plastic Quad Flat Pack (PQFP)	132	20.5	DSP56001AFC20
			27	DSP56001AFC27
			33	DSP56001AFC33
	Ceramic Quad Flat Pack (CQFP)	132	20.5	DSP56001AFE20
			27	DSP56001AFE27
			33	DSP56001AFE33

Literature Distribution Centers:
USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.
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ASIA-PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbor Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.