DSP96002ADM

User's Manual

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Introduction

This document supports the DSP96002 Application Development Module (DSP96002ADM), including a description of its basic structure and operation, the equipment required to use it, the specifications of the key components, schematic diagrams, and a parts list. Section 1 is a Quick Start Guide. Section 2 provides detailed information about key components in the evaluation module. Appendix A has detailed schematics.Appendix B lists the Bill Of Materials (BOM) for the board. Detailed information is provided in the additional documents supplied with this kit.

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SECTION 1

QUICK START GUIDE

1.1 OVERVIEW

The Motorola Application Development System is a tool used to design and test complex software applications and hardware products using a specific Motorola DSP chip. The related Application Development Modules (ADMs) contain the DSP chip and related hardware used for bench development and test. Detailed information about the content and use of the Application Development System is provided in the Application Development System User's Manual (order # DSPADSUM/AD). This manual provides specific information about the DSP96002 Application Development Module (DSP96002ADM). This section provides a summary description of the DSP96002ADM, additional requirements, and quick installation information. Detailed information about the DSP96002ADM design and operation is provided in the remaining sections of this manual.

1.2 EQUIPMENT

The following section gives a brief summary of the equipment required to use the DSP96002 Application Development Module (DSP96002ADM), some of which will be supplied with the module, and some of which must be supplied by the user.

1.2.1 What You Get with the DSP96002ADM

The following materials are provided with the DSP96002ADM:

- DSP96002 Application Development Module board
- DSP96002ADM Product Information
- DSP96002ADM User's Manual (this document)
- Motorola Digital Signal Processor Registration Form

1.2.2 What You Need to Supply

- Motorola Application Development System with appropriate host interface card
- Host Computer system:
  - PC-compatible computer (386 class or higher) running PC-DOS or MS-DOS version 5.0 or later with 8 Mbytes RAM, one open 16-bit ISA expansion slot, free I/O addresses ($100–$102, $200–202, or $300–$303), CD-ROM drive, hard drive with 4 Mbyte of free disk space, and a mouse
  - Sun Microsystems Sun 4 Workstation running Sun Operating System Release 4.1.1 or later (or Solaris Release 2.5 or later), one open SBus expansion slot, CD-ROM drive, and a mouse
  - Hewlett Packard HP7xx Workstation running HPUX Version 9.x (Version 10.x is not supported), one open EISA expansion slot, CD-ROM drive, and a mouse.

1.3 INSTALLATION PROCEDURE

Installation requires the following steps:

1. Using information provided in the Motorola Application Development System User's Manual, install the Motorola Application Development System in the host computer.
2. Prepare the DSP96002ADM board
3. Connect the board to the external Command Converter card

1.3.1 Preparing the DSP96002ADM

CAUTION

Because all electronic components are sensitive to the effects of electrostatic discharge (ESD) damage, correct procedures should be used when handling all components in this kit and inside the supporting personal computer. Use the following procedures to minimize the likelihood of damage due to ESD:

- **Always handle all static-sensitive components only in a protected area, preferably a lab with conductive (anti-static) flooring and bench surfaces.**
- **Always use grounded wrist straps when handling sensitive components.**
- **Never remove components from anti-static packaging until required for installation.**
- **Always transport sensitive components in anti-static packaging.**

Locate the twenty-seven jumper blocks JG1–JG27 on the DSP96002ADM board, as shown in **Figure 1-1** on page 1-6. **Table 1-1** describes the default jumper and switch settings when shipped from the factory.

Read the technical summary in **Section 2** of this manual for additional information about the DSP96002ADM board and its components.

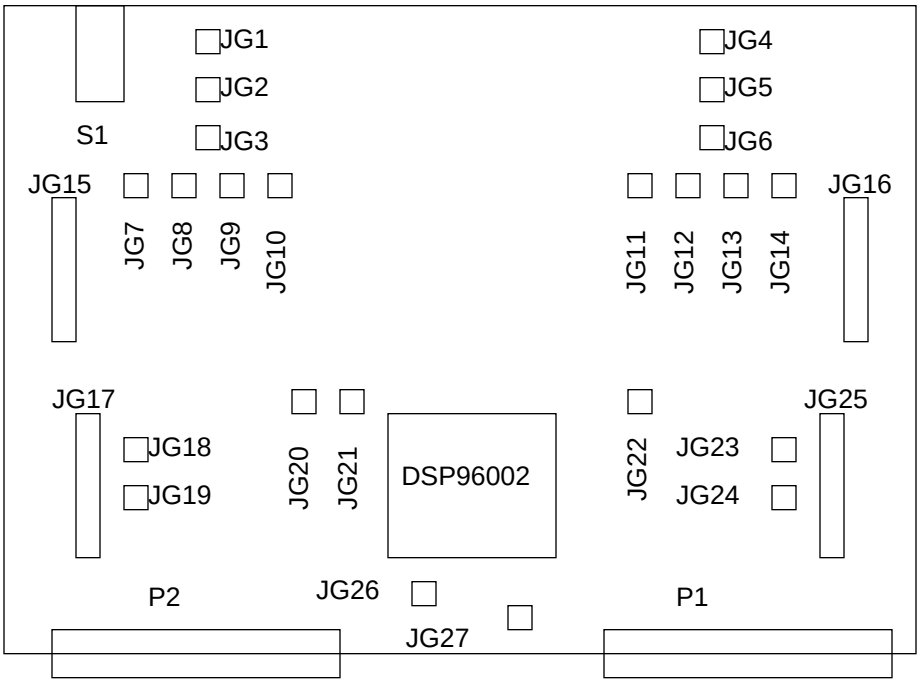


Figure 1-1 DSP96002ADM Key Component Layout

Table 1-1 DSP96002ADM Default Jumper Options

Jumper Block	Place Jumpers between Pins	Comment
JG1	1–2	Exit reset in Mode 0
JG2	1–2	
JG3	1–2	
JG4	1–2	IRQA pass through reset logic
JG5	1–2	IRQB pass through reset logic
JG6	1–2	IRQC pass through reset logic
JG7	1–2	2K words of EPROM
JG8	1–2	
JG9	1–2	
JG10	1–2	
JG11	1–2	
JG12	1–2	
JG13	1–2	
JG14	1–2	
JG15	11–12, 17–18, 19–20	
JG16	11–12, 17–18, 19–20	
JG17	1–3, 7–9, 15–17	Partition SRAM for 64K Program, 32 K X Data, 32 K Y Data
JG18	1–2, 3–4, 5–6	SRAM decoded to appear in $0–$1FFFFFFF address space
JG19	None	EPROM located from $FF000000–$FFFFFFFF
JG20	1–2	Local ADM clock drives DSP
JG21	2–3	$\overline{TA}$ signal always asserted
JG22	2–3	
JG23	1–2, 3–4, 5–6	SRAM decoded to appear in $0–$1FFFFFFF address space
JG24	None	EPROM located from $FF000000–$FFFFFFFF
JG25	1–3, 7–9, 13–15	Partition SRAM for 64K Program, 32 K X Data, 32 K Y Data
JG26	2–3	$\overline{BG}$ signal always asserted
JG27	2–3	
Note: Due to mechanical constraints, some jumper options may require wirewrapping.		

1.3.2 Connecting the DSP96002ADM to the PC and Power

Figure 1-2 shows the interconnection diagram for connecting the PC and the external power supply to the DSP96002ADM board. Using the instructions in the Application Development System User's Manual, connect the Command Converter to the ADM board. Power for the ADM is supplied from the Command Converter module.

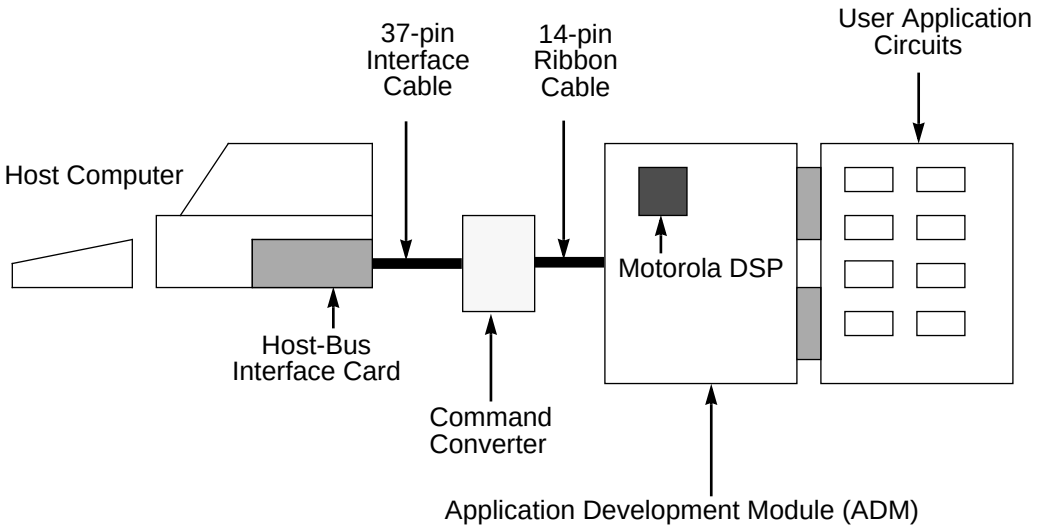


Figure 1-2 Application Development

1.4 USING THE DSP96002ADM

Once the ADM is installed, it becomes a part of the Application Development System. Use information in the Application Development System User's Manual to develop your application design, debug it, and test it.

SECTION 2

DSP96002ADM TECHNICAL SUMMARY

2.1 DSP96002ADM DESCRIPTION AND FEATURES

The DSP96002ADM has various options to facilitate evaluation of the different features of the chip. These options are outlined in this chapter. **Figure 2-1** on page 2-4 shows a block diagram of the DSP96002ADM architecture. To achieve zero wait accesses memory decoding is minimal, therefore memory may overlap into other address blocks within a $20000000 address space. There are a variety of jumper options for partitioning the memory so it appears in all three DSP memory maps. Sockets for SRAMs are available for increasing the memory size to a maximum of 256 K words on each port. EPROM sockets are also available for stand-alone operation. The EPROM is only accessible in Program memory space.

The OnCE port interface connects through a 14-pin ribbon cable to the ADS Command Converter. The command converter controls the DSP96002 in a target system. This interface uses a standard pinout that should be used when designing the target application hardware. It allows the user to evaluate the hardware and software of the application without a special emulator.

An overview description of the DSP96002ADM is also provided in the DSP96002ADM Product Information document (order number DSP96002ADMP/D) included with this kit. The main features of the DSP96002ADM include the following:

- DSP96002 32-bit Digital Signal Processor
- Full speed operation at 40 MHz
- 128 K words of configurable static RAM expandable to 512 K words.
- 2 K Words of EPROM with sockets expandable to 64 K words.
- Stand-alone operation of ADM after initial development.
- Full support of multiple data memory maps.
- Two sets of 96-pin connectors provide access to all DSP96002 pins.
- OnCE port connector that permits easy hookup to the Command Converter.

Note: Call your local Motorola sales office or distributor for additional information about the Motorola Application Development System (ADS) kit. The ADS kit includes two additional boards: a host interface card and an external universal command converter. The host interface card plugs in the host bus (on a PC-compatible or SUN system) inside the computer chassis. The external universal command converter card connects to the host card via a ribbon cable. The command converter card connects to the connector on the DSP96002ADM via another short ribbon cable. The ADS is only compatible with Motorola software tools.

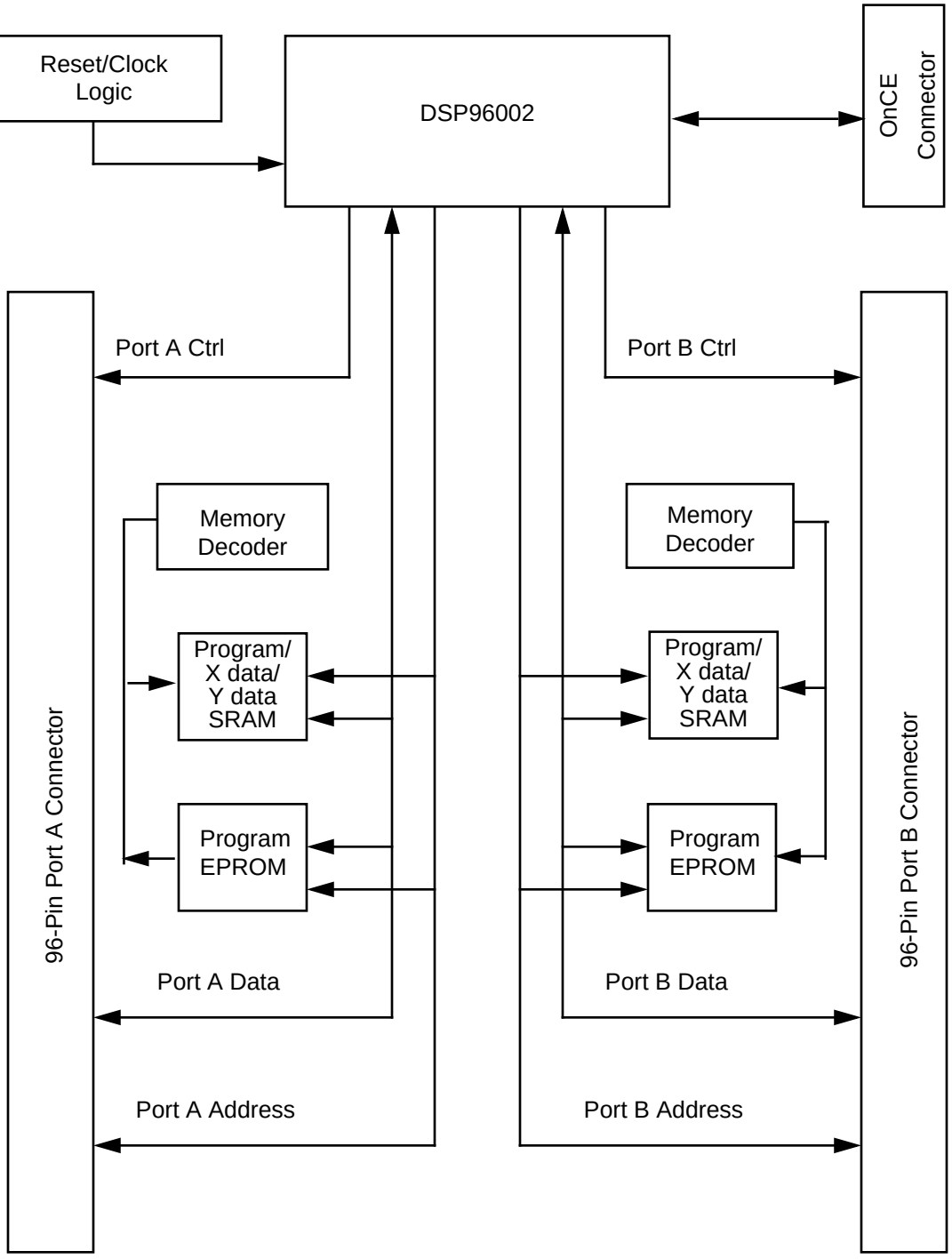


Figure 2-1 DSP96002ADM Functional Block Diagram

2.2 DSP96002 DESCRIPTION

A full description of the DSP96002, including functionality and user information is provided in the following documents included as a part of this kit (either as printed copies or on the documentation CD-ROM):

- **DSP96002 Technical Data—**Provides features list and specifications including signal descriptions, DC power requirements, AC timing requirements, and available packaging
- **DSP96002 User's Manual—**Provides a detailed description of the core processor including internal status and control registers and a detailed description of the family instruction set and detailed information about the on-chip components including the memory and I/O maps, peripheral functionality, and control and status register descriptions for each subsystem

Refer to these documents for detailed information about chip functionality and operation.

2.3 EXTERNAL/INTERNAL RESET INPUT

The DSP96002 may be reset using one of the following:

- Using the ADM reset circuit,
- Invoking an external reset input signal using the open collector circuit tied to P2 connector P2-B30 pin or the J2 connector J2-9,
- Executing a **CFORCE R** command from the ADS96002 user interface program to generate a reset pulse on the J2 connector via the command convertor, or
- When operating in the stand-alone mode without a command convertor, generating a start pulse via S1 on the ADM board. When S1 is toggled, a start pulse is generated on U20 monostable multivibrator and operating mode selection is synchronized to the deassertion of the U20 output.

2.4 CONFIGURING THE DSP96002ADM

There are twenty-seven jumper options on the DSP96002ADM. **Figure 2-2** illustrates the physical locations of jumpers JG1 to JG27. **Table 2-1** on page 2-7 defines the different Jumper Group functions.

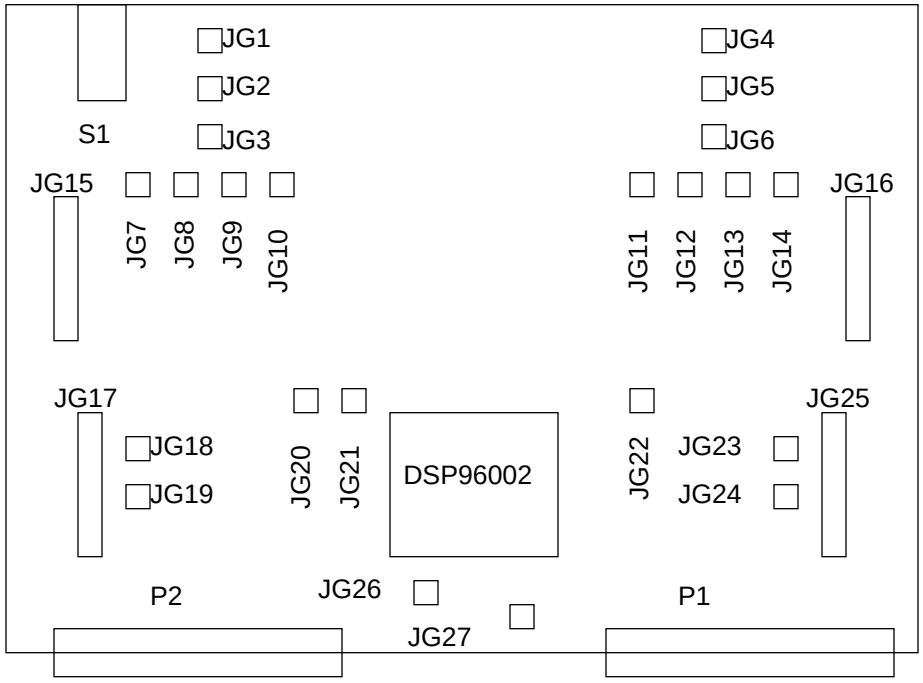


Figure 2-2 DSP96002ADM Key Component Layout

Table 2-1 DSP96002ADM Jumper Functions

Jumper Block	Function
JG1	Selects operating mode out of reset
JG2	
JG3	
JG4	$\overline{\text{IRQ}}$ configuration
JG5	
JG6	
JG7	EPROM size configuration
JG8	
JG9	
JG10	
JG11	
JG12	
JG13	
JG14	
JG15	
JG16	
JG17	SRAM partition configuration (with JG25)
JG18	SRAM address space decoding configuration (with JG23)
JG19	EPROM memory location configuration (with JG24)
JG20	Clock selection
JG21	$\overline{\text{TA}}$ signal configuration
JG22	
JG23	SRAM address space decoding configuration (with JG18)
JG24	EPROM memory location configuration (with JG19)
JG25	SRAM partition configuration (with JG17)
JG26	$\overline{\text{BG}}$ signal cofiguration
JG27	
Note: Due to mechanical constraints, some jumper options may require wirewrapping.	

2.4.1 Operating Mode Selection

Jumpers JG1 to JG3 are used to select one of eight operating modes in which the DSP96002 exits reset. The ADM is factory configured for MODE 0. In MODE 0, the internal program memory occupies the lower portion of the program memory space. Addresses higher than the highest internal program memory location are directed to external program memory. The address of the hardware reset vector is $FFFFFFFE, located in the Port A external program memory space. Refer to the *DSP96002 User's Manual* for a complete description of the chip operating modes. The **Table 2-2** lists the jumper settings required to select each of the eight operating modes.

Table 2-2 Operating Mode Selection

Mode	(MODA) JG3	(MODB) JG2	(MODC) JG1	Comment
0 (default)	1–2	1–2	1–2	PRAM on, reset($FFFFFFFE) Port A
1	2–3	1–2	1–2	PRAM on, reset ($FFFFFFFE) Port B
2	1–2	2–3	1–2	PRAM off, reset ($00000000) Port A
3	2–3	2–3	1–2	PRAM off, reset ($00000000) Port B
4	1–2	1–2	2–3	Bootstrap byte wide Port A
5	2–3	1–2	2–3	Bootstrap byte wide Port B
6	1–2	2–3	2–3	Bootstrap Port A host interface
7	2–3	2–3	2–3	Bootstrap Port B host interface

Note: The ADM is factory configured to exit reset in Mode 0.

2.4.2 External $\overline{\text{IRQA}}$/$\overline{\text{IRQB}}$/$\overline{\text{IRQC}}$ Input Path

The paths for the external input signals MODA / $\overline{\text{IRQA}}$, MODB / $\overline{\text{IRQB}}$, and MODC / $\overline{\text{IRQC}}$ are selected by JG4, JG5, and JG6, respectively. These jumpers allow the designer to use the multiplexed function of these inputs, or to select only the interrupt function of these external signals.

If JG4–JG6 have a jumper connecting pins 1–2, the external signals are ignored during reset. In this case, the DSP96002 uses the jumpers JG1–JG3 to determine the startup mode after reset. Once the mode is set, the external signals are enabled and interrupts received on these lines are accepted and processed. This has the advantage of assuring that the chip uses the appropriate startup mode by eliminating spurious interrupts and noise from these lines.

If JG4–JG6 have a jumper connecting pins 2–3, the external signals are connected directly to the MOD / $\overline{\text{IRQ}}$ pins on the DSP96002 and the multiplexed MOD / $\overline{\text{IRQ}}$ function is used and the setting of JG1–JG3 are ignored during reset.

Table 2-3 gives the jumper options for the $\overline{\text{IRQA}}$ / $\overline{\text{IRQB}}$ / $\overline{\text{IRQC}}$ input paths.

Table 2-3 External $\overline{\text{IRQA}}$ / $\overline{\text{IRQB}}$ / $\overline{\text{IRQC}}$ Input Path

IRQx INPUT PATH	JG4 ($\overline{\text{IRQA}}$)	JG5 ($\overline{\text{IRQB}}$)	JG6 ($\overline{\text{IRQC}}$)
Reset Logic	1–2	1–2	1–2
Directly to pin	2–3	2–3	2–3

Note: The ADM is factory configured for external $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, and $\overline{\text{IRQC}}$ inputs to be gated by the reset logic.

2.4.3 DSP96002 Port A/B User EPROM Decoders

Port A and B both contain sockets that accommodate EPROMs of various densities. Six types of EPROMs, ranging from 2 K × 8 to 64 K × 8, may be installed in the sockets. The lower density EPROMs come in 24-pin packages while the higher density EPROMs are available in 28-pin packages.

CAUTION

Improper installation of EPROM chips may result in chip damage when power is applied. When using 24-pin chips, make sure that the chips are inserted into the center of the EPROM sockets leaving positions 1, 2, 27, and 28 empty.

Sockets must be configured to accommodate the specific package type and memory size. The four jumpers (JG11–JG14) on Port A and the four jumpers (JG7–JG10) on Port B connect V_{CC} to the appropriate power input pin for the package type. The EPROM PAL maps the EPROM to program memory space only, and jumpers JG19 and JG24 select the memory block to which each group of EPROMs is mapped. Jumpers JG15 and JG16 connect the appropriate address pins to the address pins for the installed EPROM device. **Table 2-4** and **Table 2-5** on page 2-11 show how the different device types may be configured.

Table 2-4 Port A/B User EPROM Decoder

OPTION	JG19 / JG24	EPROM MEMORY BLOCK
1	1–2, 3–4, 5–6	$00000000–$1FFFFFFF
2	3–4, 5–6	$20000000–$3FFFFFFF
3	1–2, 5–6	$40000000–$5FFFFFFF
4	5–6	$80000000–$9FFFFFFF
5	1–2, 3–4	$A0000000–$BFFFFFFF
6 (default)	No jumpers	$FF000000–$FFFFFFFF

Note: The ADM is factory-configured to use 2 K words of EPROM at the top of the address map.

Table 2-5 Port A / B User EPROM Selection

EPROM TYPE	JG7–10 / JG11–14	JG15/JG16
2 K × 8	1–2	11–12, 17–18, 19–20
4 K × 8	1–2	11–12, 15–16, 19–20
8 K × 8	1–2	9–10, 13–14, 21–22
16 K × 8	2–3	9–10, 13–14, 21–22
32 K × 8	2–3	9–10, 13–14, 21–22
64 K × 8	2–3	9–10, 13–14, 21–22

2.4.4 DSP96002 Port A/B User SRAM Decoder/Partitions

The DSP96001ADM includes sixteen 64 K × 4-bit high speed CMOS Static RAMs (MCM6209) that provide a working area for user programs and data with zero wait state access.

Note: The SRAM sockets will also accept sixteen 256 K × 4-bit SRAM (MCM6228), which can be used to replace the 64 K × 4-bit SRAM chips if more memory is required.

Port A and Port B both have 64 K × 32 words of SRAM for user program development. The SRAMs may be moved to various blocks of memory and may be partitioned so that P, X and / or Y memory spaces have external memory. Since only the upper 8 bits of the address bus are input into the PAL, either the 64 K × 4 or 256 K × 4 device will work with the DSP96002ADM. The SRAM decoder does not have bus arbitration signals as qualifiers; therefore, any processor that becomes the bus master may directly access the SRAMs. This is useful in shared memory configurations. The SRAM address lines are buffered to decrease the DSP96002 address bus loading.

There are two jumpers (**JG17**, **JG18**) for Port A and two jumpers (**JG23**, **JG25**) for Port B. Jumpers **JG17** (Port A) and **JG25 (Port B)** are for memory block selection while jumpers **JG18** (Port A) and **JG23** (Port B) are for memory map partitioning of the SRAM for the three DSP96002 memory spaces. The following tables show the jumper options that will provide one of five address block selections and a few of the different memory map partitions possible for the SRAM. There are a variety of memory map partitions due to the minimal address decoding done in the PAL and the number of combinations achievable by programming the DSP96002 Port Select Register (PSR).

Table 2-6 Port A/B User SRAM Decoder

OPTION	JG18 / JG23	SRAM MEMORY BLOCK
1	1–2, 3–4, 5–6	$00000000–$1FFFFFFF
2	3–4, 5–6	$20000000–$3FFFFFFF
3	1–2, 5–6	$40000000–$5FFFFFFF
4	5–6	$80000000–$9FFFFFFF
5	No jumpers	$E0000000–$FFFFFFFF

Table 2-7 Port A/B User SRAM Selection

Program Memory	X Data Memory	Y Data Memory	Jumpers for 64 K × 4 SRAMs		PSR		
			JG17	JG25	Bit 0	Bit 8	Bit 16
64 K	32 K	32 K	1–3, 7–9, 15–17	1–3, 7–9, 13–15	0	1	1
32 K	64 K	32 K	1–3, 7–9, 15–17	1–3, 7–9, 13–15	1	1	0
32 K	32 K	64 K	1–3, 7–9, 14–16	1–3, 7–9, 13–15	1	0	1
64 K		64 K	1–3, 7–9, 13–15	1–3, 7–9, 13–15	0	1	0/1
	64 K	64 K	1–3, 7–9, 13–15	1–3, 7–9, 13–15	0/1	0	1
128 K			1–3, 7–9, 13–15	1–3, 7–9, 13–15	0	1	0/1

Note: The SRAMs Jumper Groups are factory configured for 64 K words of Program memory, 32 K words of X data memory, and 32 K words of Y data memory. The PSR is not preset; the user must write the correct values to PSR to enable this memory configuration.

2.4.5 Clock Input Selection

Using jumper JG20, the user can select either the ADM U21 clock output or an external clock input via P1 connector P1-C30 pin as the DSP96002 clock source. The ADM clock is buffered via U6-3 (74AS08 AND Gate), which provides a current source of –2 mA and a current sink of 20 mA. **Table 2-8** shows the clock input/output option selection.

Table 2-8 Clock Input Selection

CLOCK SOURCE	JG20	COMMENT
ADM U6-3 (default)	1–2	Local ADM clock to DSP96002 only
External on P1-C30	3–4	External clock into DSP96002
ADM U6-3	1–2, 3–4	Local ADM clock to DSP96002 and connector
Note: The ADM is factory equipped with a 40.0 MHz local clock oscillator.		

2.4.6 Transfer Acknowledge ($\overline{TA}$) Pullup/Pulldown Option

The transfer acknowledge signal on ports A and B must be asserted true low whenever an external access is made on that port. If no external circuits are provided to assert the transfer acknowledge signal, the DSP96002 bus will remain pending until the transfer acknowledge signal occurs. Jumper groups **JG21 and JG22** provide an option to always assert the $\overline{TA}$ signal so that the DSP96002 does not hang up. When a jumper is placed across pins 2-3 on **JG21 and JG22** , the $\overline{TA}$ input is always pulled down (asserted) through a resistor. If a jumper is placed on pins 1–2 of **JG21 and JG22**, the $\overline{TA}$ signal is pulled up (deasserted). **JG21** controls the Port B side, and **JG22** controls the Port A side.

Note: The ADM is factory configured for the $\overline{TA}$ signal to be pulled down.

2.4.7 Bus Grant ($\overline{BG}$) Pullup/Pulldown Option

The Bus Grant signal ($\overline{BG}$) on ports A and B must be asserted (pulled low) whenever an external access is made on that port. If no external circuits are provided to assert the bus grant signal, the DSP96002 bus will remain pending until $\overline{BG}$ is asserted. Jumper groups **JG26 and JG27** provide an option to keep the $\overline{BG}$ signal asserted, so that the DSP96002 will not hang up. When pins 2–3 of **JG26 and JG27** are jumpered, the $\overline{BG}$ input is always pulled down through a resistor. If pins 1–2 of **JG26 and JG27** are jumpered, the $\overline{BG}$ signal is pulled up. **JG26** controls the Port A side and **JG27** controls the Port B side.

Note: The ADM is factory configured for the $\overline{BG}$ signal to be pulled down.

2.5 DSP96002 ADM CONNECTOR DESCRIPTIONS

Table 2-9 DSP96002 ADM P1/J3 Port A Connector

PIN #	ROW A	ROW B	ROW C
1	aD00	aD25	aA10
2	aD01	aD26	aA09
3	aD02	aD27	aA08
4	aD03	aD28	aA07
5	aD04	aD29	aA06
6	aD05	aD30	aA05
7	aD06	aD31	aA04
8	aD07	aA31	aA03
9	GND	aA30	GND
10	aD08	aA29	aA02
11	GND	aA28	aA01
12	aD09	aA27	aA00
13	aD10	aA26	a$\overline{\text{HA}}$
14	aD11	aA25	a$\overline{\text{HR}}$
15	GND	aA24	a$\overline{\text{HS}}$
16	aD12	aA23	a$\overline{\text{TA}}$
17	GND	aA22	a$\overline{\text{BB}}$
18	aD13	aA21	a$\overline{\text{BG}}$
19	GND	aA20	a$\overline{\text{BR}}$
20	aD14	GND	a$\overline{\text{BA}}$
21	aD15	aA19	a$\overline{\text{BL}}$
22	aD16	aA18	a$\overline{\text{TT}}$
23	aD17	GND	aR/$\overline{\text{W}}$
24	aD18	aA17	aS1
25	aD19	aA16	aS0
26	aD20	aA15	a$\overline{\text{BS}}$
27	aD21	aA14	a$\overline{\text{TS}}$
28	aD22	aA13	a$\overline{\text{AE}}$
29	aD23	aA12	a$\overline{\text{DE}}$
30	aD24	aA11	CLK_I/O
31	(n/c)	(n/c)	(n/c)

Table 2-9 DSP96002 ADM P1/J3 Port A Connector (Continued)

PIN #	ROW A	ROW B	ROW C
32	+5 V	+5 V	+5 V
Note: (n/c) means that the pin is not connected.. Both P1 and J3 are plugs.			

Table 2-10 DSP96002 ADM P2/J4 Port B Connector

PIN #	ROW A	ROW B	ROW C
1	bD00	+5 V	bA00
2	bD01	GND	bA01
3	bD02	b$\overline{DE}$	bA02
4	bD03	b$\overline{HS}$	bA03
5	bD04	b$\overline{HA}$	bA04
6	bD05	$\overline{DR}$	bA05
7	bD06	DSI/OS0	bA06
8	bD07	DSCK/OS1	bA07
9	bD08	DSO	bA08
10	bD09	b$\overline{HR}$	bA09
11	bD10	b$\overline{BG}$	bA10
12	bD11	GND	bA11
13	bD12	+5 V	bA12
14	bD13	b$\overline{BA}$	bA13
15	bD14	b$\overline{BB}$	bA14
16	bD15	b$\overline{BR}$	bA15
17	bD16	b$\overline{BS}$	bA16
18	bD17	bR/$\overline{W}$	bA17
19	bD18	b$\overline{TS}$	bA18
20	bD19	b$\overline{BL}$	bA19
21	bD20	bS0	bA20
22	bD21	GND	bA21
23	bD22	bS1	bA22
24	bD23	b$\overline{AE}$	bA23
25	bD24	b$\overline{TT}$	bA24
26	bD25	b$\overline{TA}$	bA25
27	bD26	MODA/$\overline{IRQA}$	bA26
28	bD27	MODB/$\overline{IRQB}$	bA27

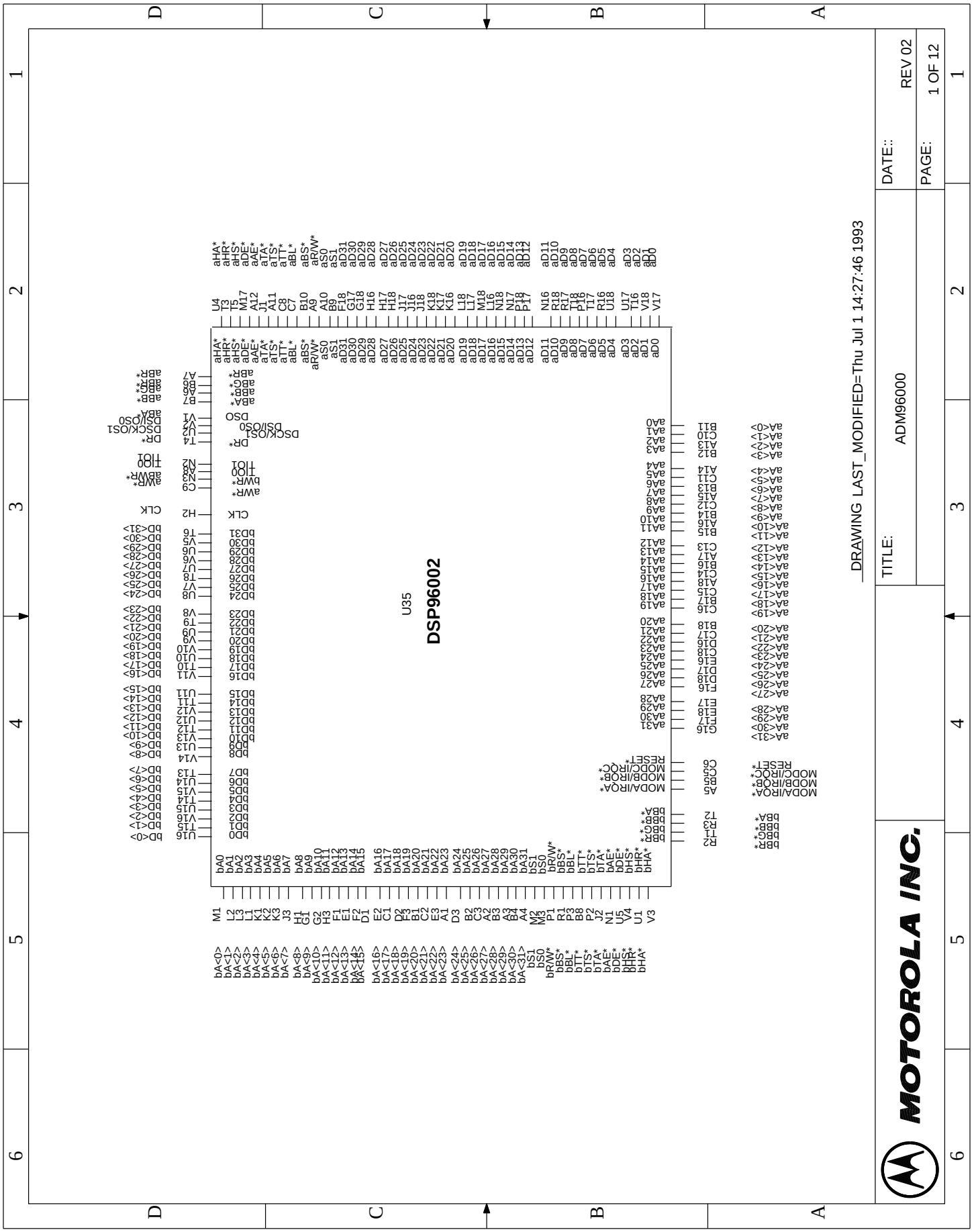
Table 2-10 DSP96002 ADM P2/J4 Port B Connector (Continued)

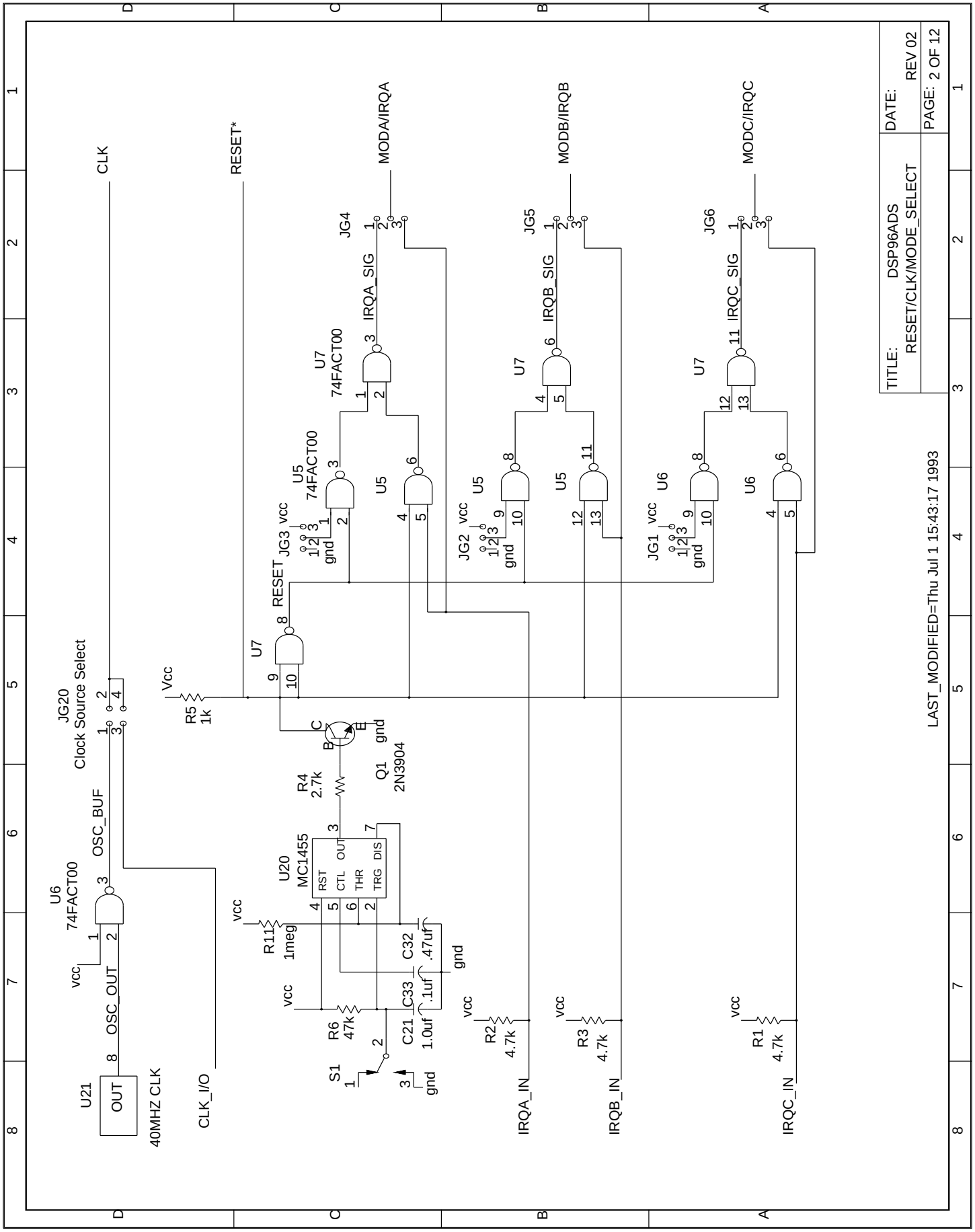
PIN #	ROW A	ROW B	ROW C
29	bD28	MODC/$\overline{\text{IRQC}}$	bA28
30	bD29	$\overline{\text{RESET}}$	bA29
31	bD30	GND	bA30
32	bD31	+5 V	bA31

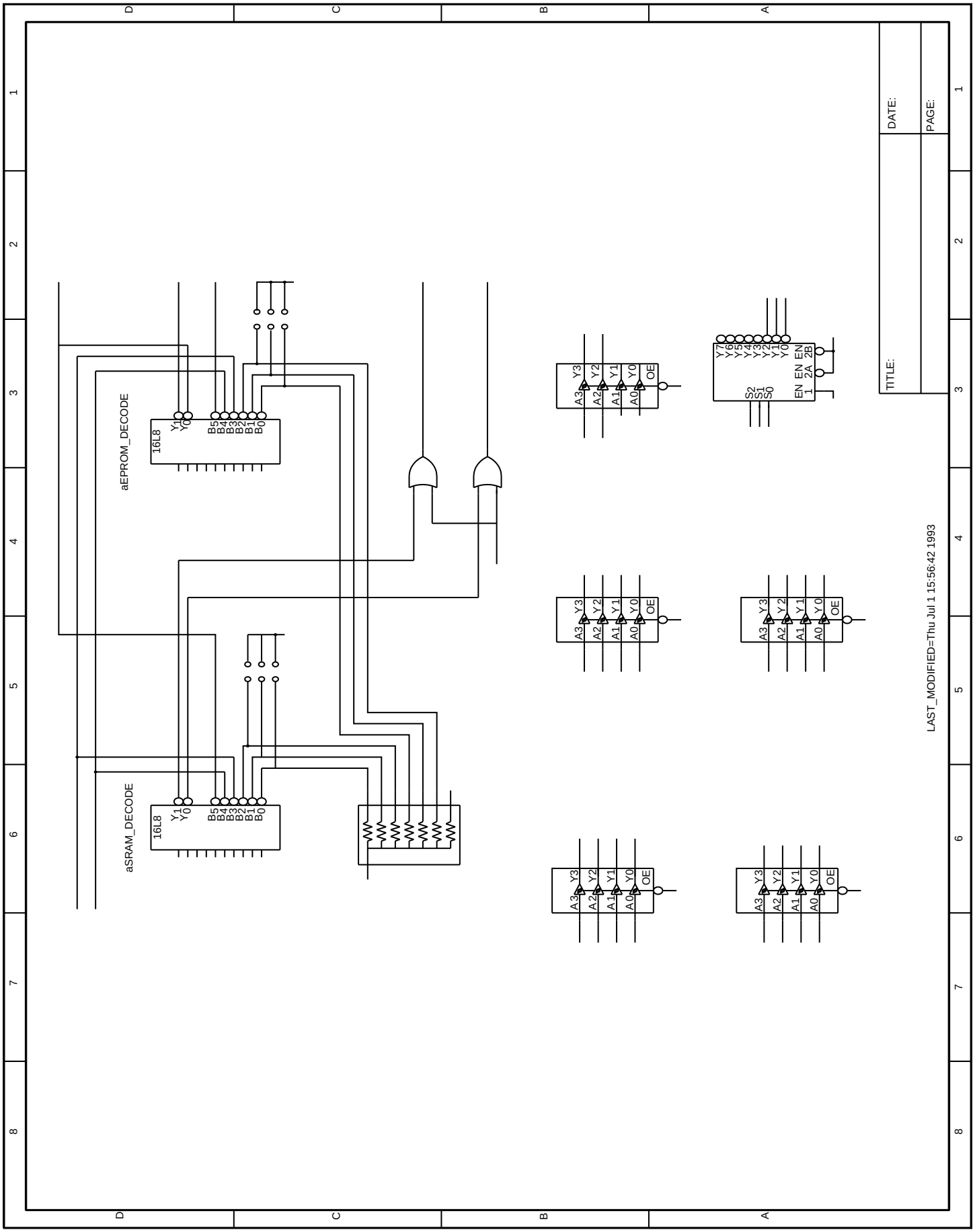
Note: (n/c) means that the pin is not connected. Both P2 and J4 are plugs.

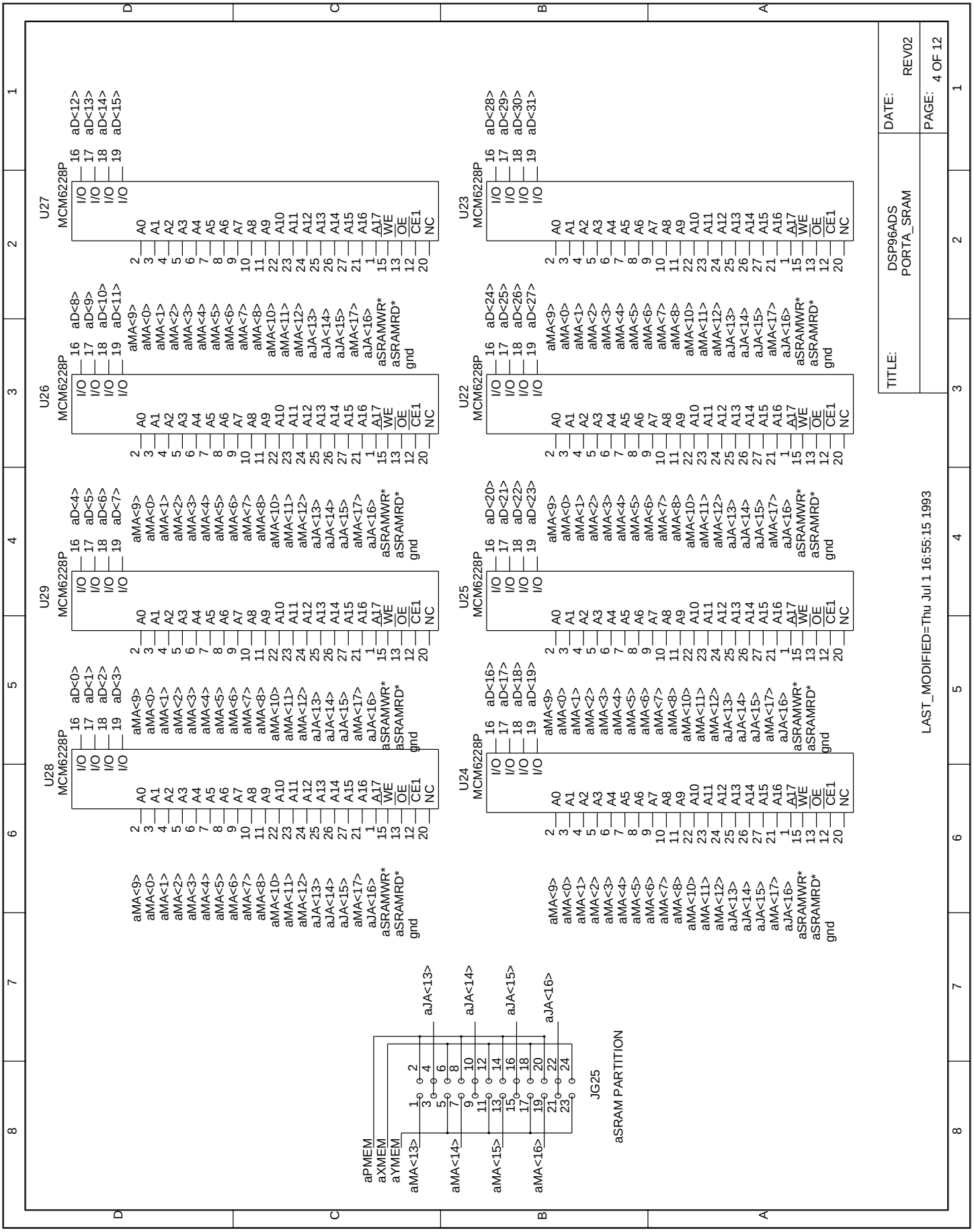
APPENDIX A

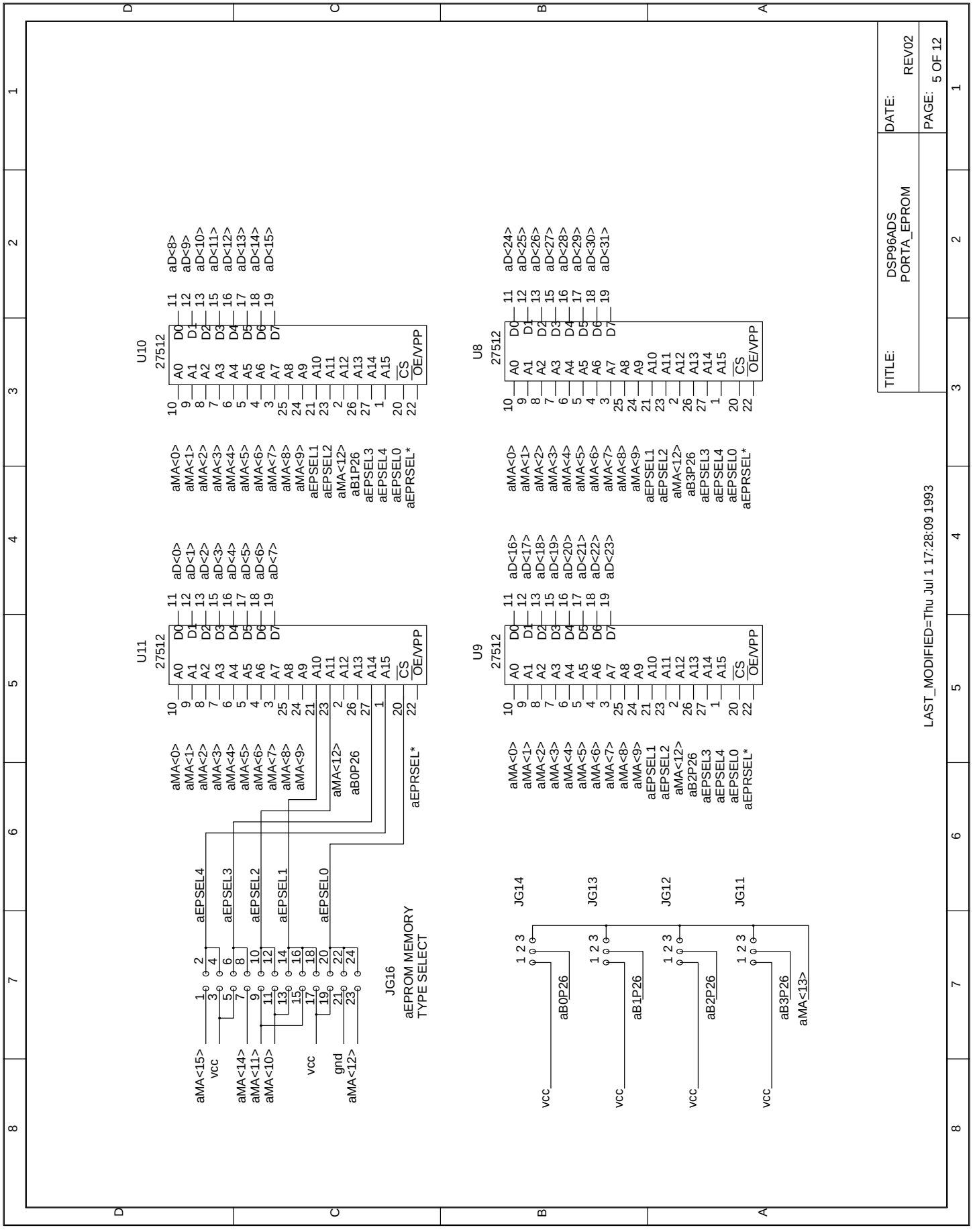
DSP96002ADM SCHEMATICS

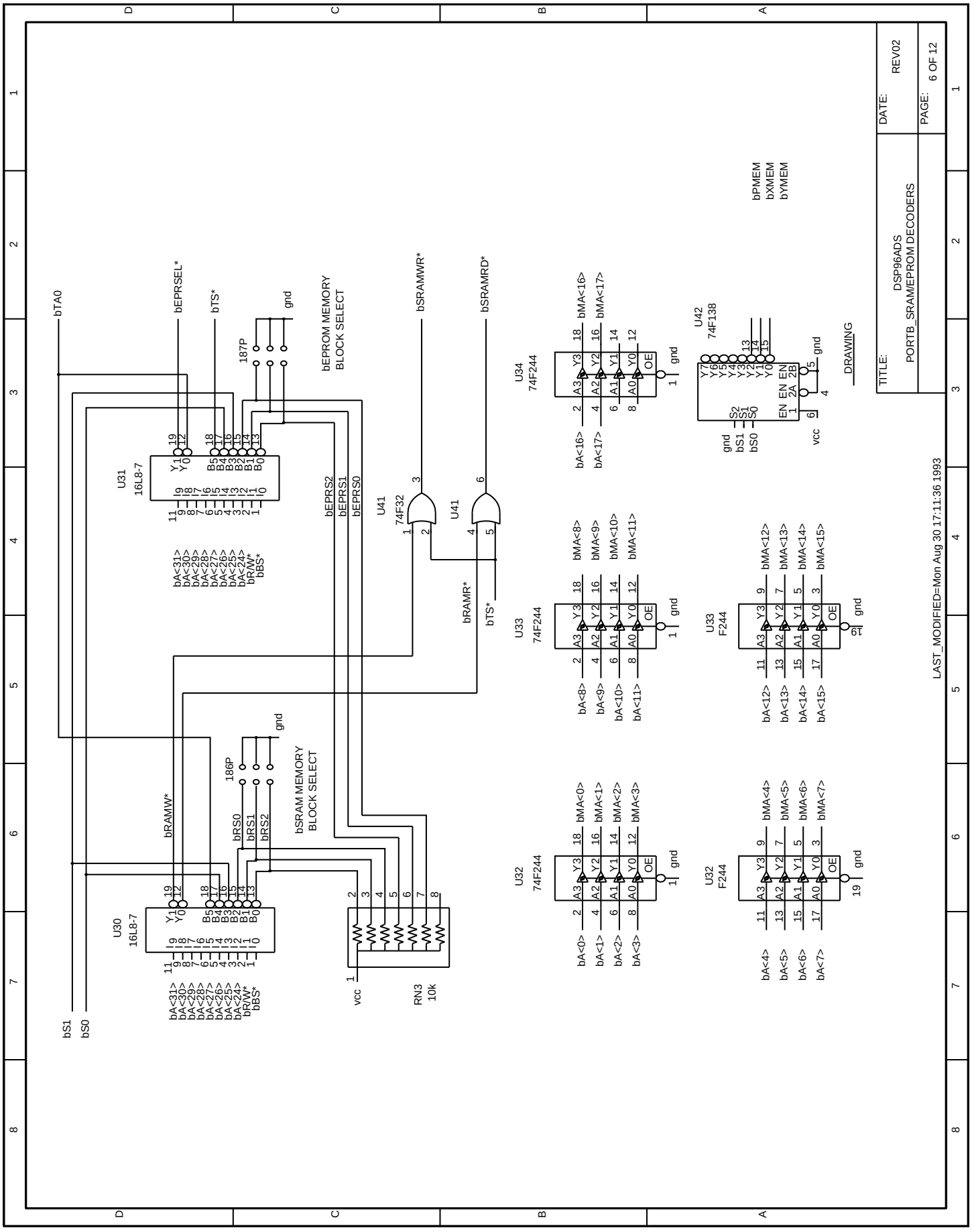

DSP96002
U35
MOTOROLA INC.
TITLE:
ADM96000
DATE::
REV 02
PAGE:
1 OF 12
DRAWING LAST_MODIFIED=Thu Jul 1 14:27:46 1993

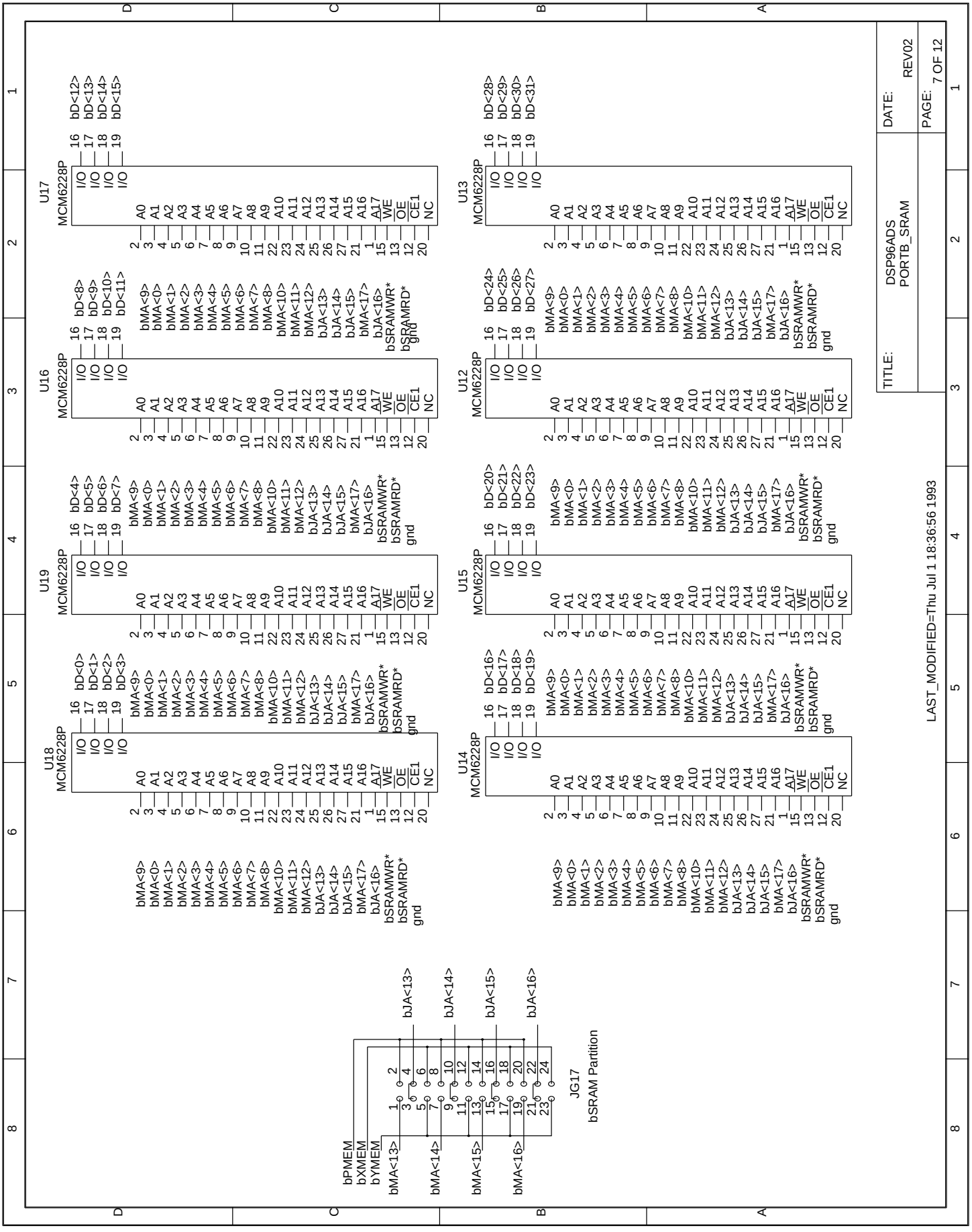

TITLE: DSP96ADS
RESET/CLK/MODE_SELECT
DATE:
REV 02
PAGE: 2 OF 12
LAST_MODIFIED=Thu Jul 1 15:43:17 1993
CLK
RESET*
MODA/IRQA
MODB/IRQB
MODC/IRQC
JG20
Clock Source Select
U6
74FACT00
OSC_BUF
OSC_OUT
U21
OUT
40MHZ CLK
CLK_I/O
Vcc
R5
1k
U7
RESET
JG3
JG4
JG5
JG6
U5
74FACT00
IRQA_SIG
IRQB_SIG
IRQC_SIG
JG2
JG1
gnd
vcc
Q1
2N3904
R4
2.7k
U20
MC1455
RST
CTL
OUT
THR
TRG
DIS
R11
1meg
C32
.47uf
C33
.1uf
C21
1.0uf
R6
47k
S1
R2
4.7k
R3
4.7k
R1
4.7k
IRQA_IN
IRQB_IN
IRQC_IN

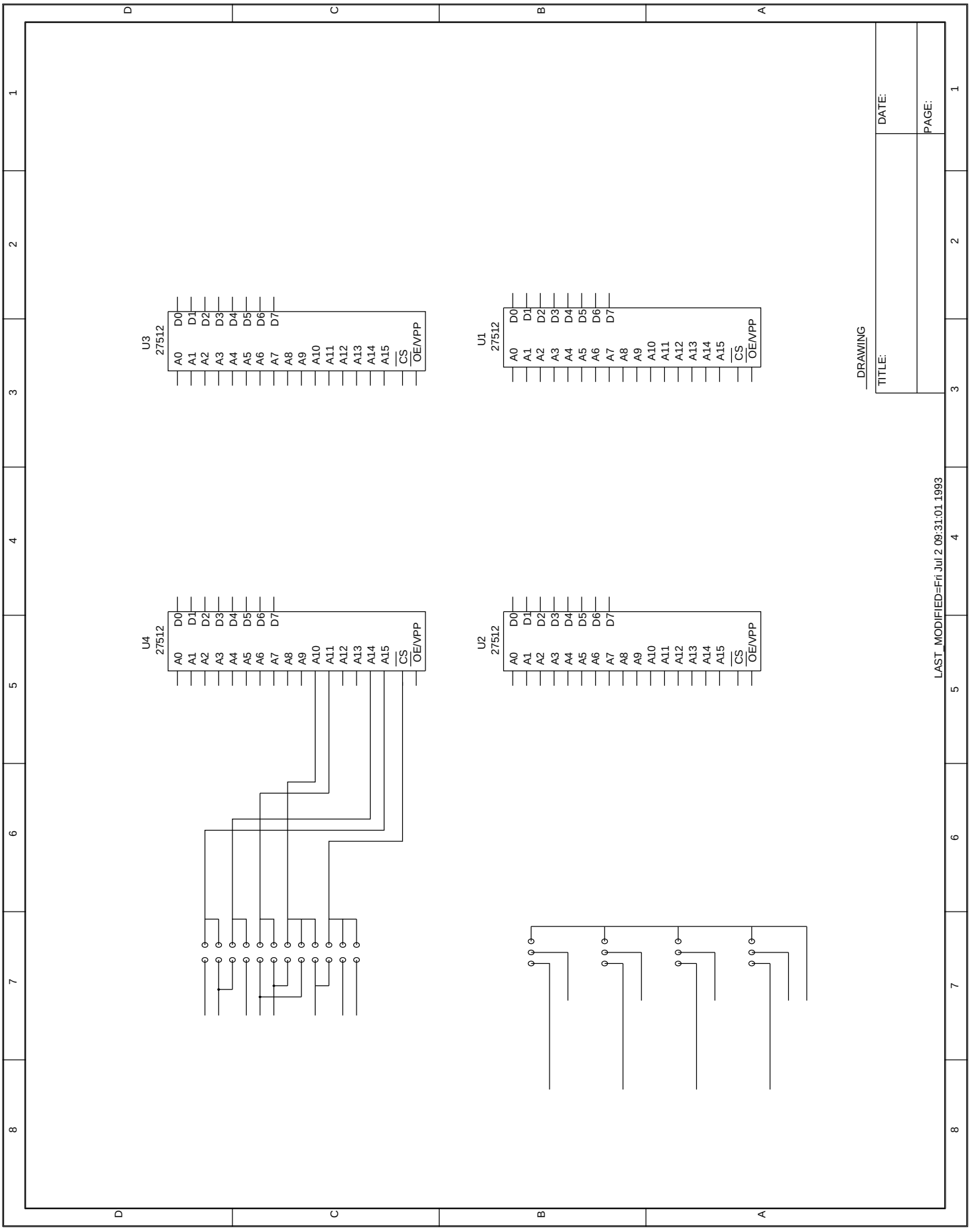

aEPROM_DECODE
16L8
Y1
Y0
B5
B4
B3
B2
B1
B0
aSRAM_DECODE
16L8
Y1
Y0
B5
B4
B3
B2
B1
B0
Y3
Y2
Y1
Y0
A3
A2
A1
A0
OE
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0
S2
S1
S0
EN
1
EN
2A
EN
2B
DATE:
PAGE:
TITLE:
LAST_MODIFIED=Thu Jul 1 15:56:42 1993


U28
MCM6228P
U29
MCM6228P
U24
MCM6228P
U25
MCM6228P
U27
MCM6228P
U26
MCM6228P
U23
MCM6228P
U22
MCM6228P
JG25
aSRAM PARTITION
aPMEM
aXMEM
aYMEM
aMA<13>
aMA<14>
aMA<15>
aMA<16>
aJA<13>
aJA<14>
aJA<15>
aJA<16>
aSRAMWR*
aSRAMRD*
gnd
TITLE:
DSP96ADS
PORTA_SRAM
DATE:
REV02
PAGE:
4 OF 12
LAST_MODIFIED=Thu Jul 1 16:55:15 1993


U11
27512
U10
27512
U9
27512
U8
27512
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 CS OE/VPP
D0 D1 D2 D3 D4 D5 D6 D7
aMA<0> aMA<1> aMA<2> aMA<3> aMA<4> aMA<5> aMA<6> aMA<7> aMA<8> aMA<9>
aEPSEL1 aEPSEL2 aMA<12> aB1P26 aEPSEL3 aEPSEL4 aEPSEL0 aEPRSEL*
aD<0> aD<1> aD<2> aD<3> aD<4> aD<5> aD<6> aD<7>
aD<8> aD<9> aD<10> aD<11> aD<12> aD<13> aD<14> aD<15>
aD<16> aD<17> aD<18> aD<19> aD<20> aD<21> aD<22> aD<23>
aD<24> aD<25> aD<26> aD<27> aD<28> aD<29> aD<30> aD<31>
JG16
aEPROM MEMORY
TYPE SELECT
aEPSEL4 aEPSEL3 aEPSEL2 aEPSEL1 aEPSEL0
aMA<15> vcc aMA<14> aMA<11> aMA<10> vcc gnd aMA<12>
JG14 JG13 JG12 JG11
1 2 3
vcc aB0P26 aB1P26 aB2P26 aB3P26 aMA<13>
TITLE: DSP96ADS PORTA_EPROM
DATE: REV02
PAGE: 5 OF 12
LAST_MODIFIED=Thu Jul 1 17:28:09 1993


bTA0
bEPRSEL*
bTS*
187P
gnd
bEPROM MEMORY
BLOCK SELECT
bSRAMWR*
bSRAMRD*
U31
16L8-7
bEPRS2
bEPRS1
bEPRS0
U41
74F32
bRAMR*
bTS*
bRAMW*
186P
bRS0
bRS1
bRS2
bSRAM MEMORY
BLOCK SELECT
U30
16L8-7
bA<31>
bA<30>
bA<29>
bA<28>
bA<27>
bA<26>
bA<25>
bA<24>
bR/W*
bBS*
vcc
RN3
10k
bS1
bS0
U34
74F244
bA<16>
bA<17>
bMA<16>
bMA<17>
U42
74F138
bPMEM
bXMEM
bYMEM
U33
74F244
bA<8>
bA<9>
bA<10>
bA<11>
bMA<8>
bMA<9>
bMA<10>
bMA<11>
U33
F244
bA<12>
bA<13>
bA<14>
bA<15>
bMA<12>
bMA<13>
bMA<14>
bMA<15>
U32
74F244
bA<0>
bA<1>
bA<2>
bA<3>
bMA<0>
bMA<1>
bMA<2>
bMA<3>
U32
F244
bA<4>
bA<5>
bA<6>
bA<7>
bMA<4>
bMA<5>
bMA<6>
bMA<7>
DRAWING
LAST_MODIFIED=Mon Aug 30 17:11:36 1993
TITLE:
DSP96ADS
PORTB_SRAM/EPROM DECODERS
DATE:
REV02
PAGE:
6 OF 12


U17
MCM6228P
U16
MCM6228P
U19
MCM6228P
U18
MCM6228P
U13
MCM6228P
U12
MCM6228P
U15
MCM6228P
U14
MCM6228P
JG17
bSRAM Partition
bPMEM
bXMEM
bYMEM
TITLE:
DSP96ADS
PORTB_SRAM
DATE:
REV02
PAGE:
7 OF 12
LAST_MODIFIED=Thu Jul 1 18:36:56 1993


U3
27512
U1
27512
U4
27512
U2
27512
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 CS OE/VPP
D0 D1 D2 D3 D4 D5 D6 D7
DRAWING
TITLE:
DATE:
PAGE:
LAST_MODIFIED=Fri Jul 2 09:31:01 1993

P1

aD<0>	P1_A1	aD<25>	P1_B1	aA<10>	P1_C1		
aD<1>	P1_A2	aD<26>	P1_B2	aA<9>	P1_C2		
aD<2>	P1_A3	aD<27>	P1_B3	aA<8>	P1_C3		
aD<3>	P1_A4	aD<28>	P1_B4	aA<7>	P1_C4		
aD<4>	P1_A5	aD<29>	P1_B5	aA<6>	P1_C5		
aD<5>	P1_A6	aD<30>	P1_B6	aA<5>	P1_C6		
aD<6>	P1_A7	aD<31>	P1_B7	aA<4>	P1_C7		
aD<7>	P1_A8	aA<31>	P1_B8	aA<3>	P1_C8		
gnd	P1_A9	aA<30>	P1_B9	gnd	P1_C9		
aD<8>	P1_A10	aA<29>	P1_B10	aA<2>	P1_C10		
gnd	P1_A11	aA<28>	P1_B11	aA<1>	P1_C11		
aD<9>	P1_A12	aA<27>	P1_B12	aA<0>	P1_C12		
aD<10>	P1_A13	aA<26>	P1_B13	aHA*	P1_C13		
aD<11>	P1_A14	aA<25>	P1_B14	aHR*	P1_C14		
gnd	P1_A15	aA<24>	P1_B15	aHS*	P1_C15		
aD<12>	P1_A16	aA<23>	P1_B16	aTA*	P1_C16		
gnd	P1_A17	aA<22>	P1_B17	aBB*	P1_C17		
aD<13>	P1_A18	aA<21>	P1_B18	aBG*	P1_C18		
TIO1	P1_A19	aA<20>	P1_B19	aBR*	P1_C19		
aD<14>	P1_A20	gnd	P1_B20	aBA*	P1_C20		
aD<15>	P1_A21	aA<19>	P1_B21	aBL*	P1_C21		
aD<16>	P1_A22	aA<18>	P1_B22	aTT*	P1_C22		
aD<17>	P1_A23	gnd	P1_B23	aR/W*	P1_C23		
aD<18>	P1_A24	aA<17>	P1_B24	aS1	P1_C24		
aD<19>	P1_A25	aA<16>	P1_B25	aS0	P1_C25		
aD<20>	P1_A26	aA<15>	P1_B26	aBS*	P1_C26		
aD<21>	P1_A27	aA<14>	P1_B27	aTS*	P1_C27		
aD<22>	P1_A28	aA<13>	P1_B28	aAE*	P1_C28		
aD<23>	P1_A29	aA<12>	P1_B29	aDE*	P1_C29		
aD<24>	P1_A30	aA<11>	P1_B30	CLK_I/O	P1_C30		
TIO0	P1_A31	AWR*	P1_B31	BWR*	P1_C31		
vcc	P1_A32	vcc	P1_B32	vcc	P1_C32		

PORTA INTERFACE CONNECTOR

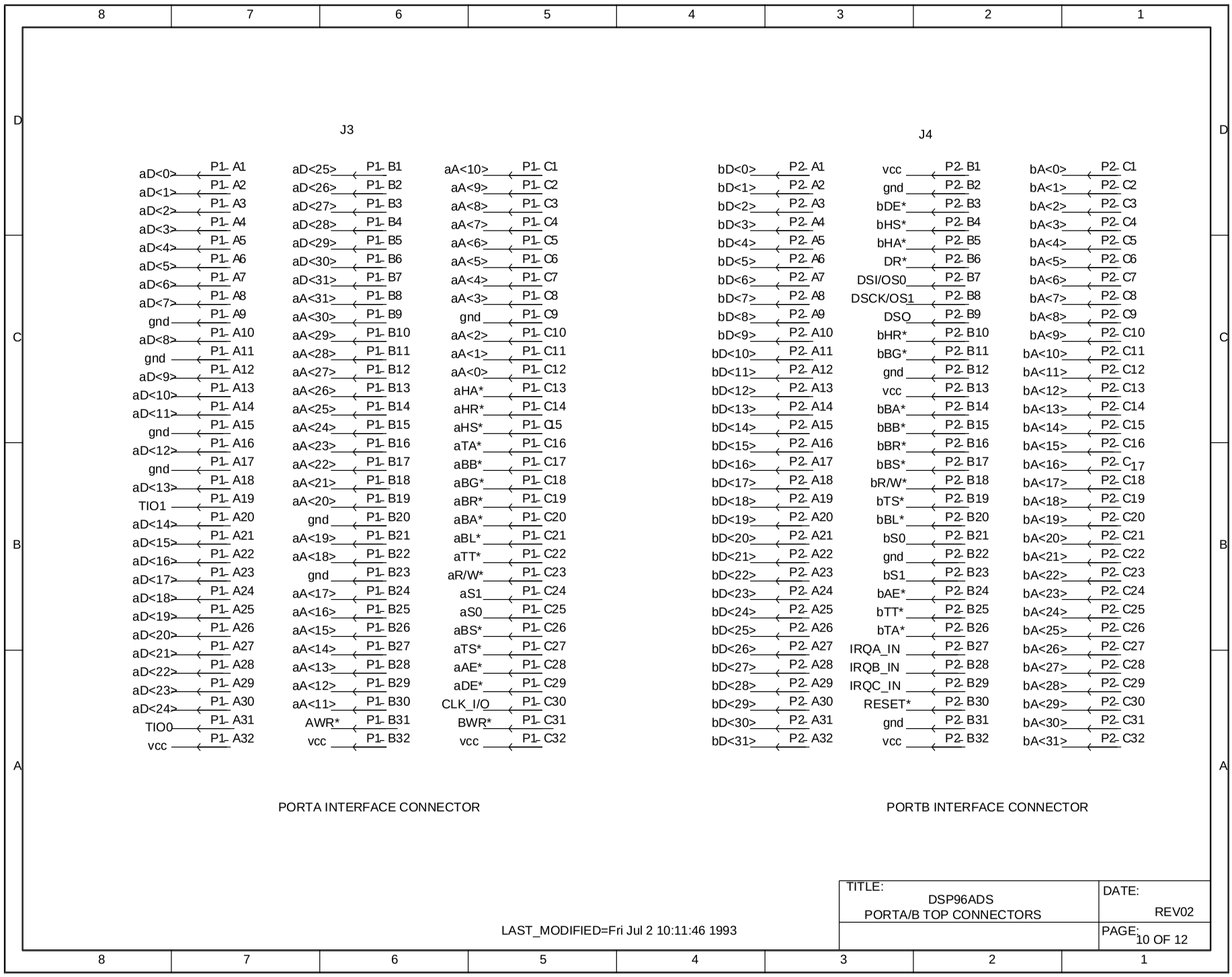
P2

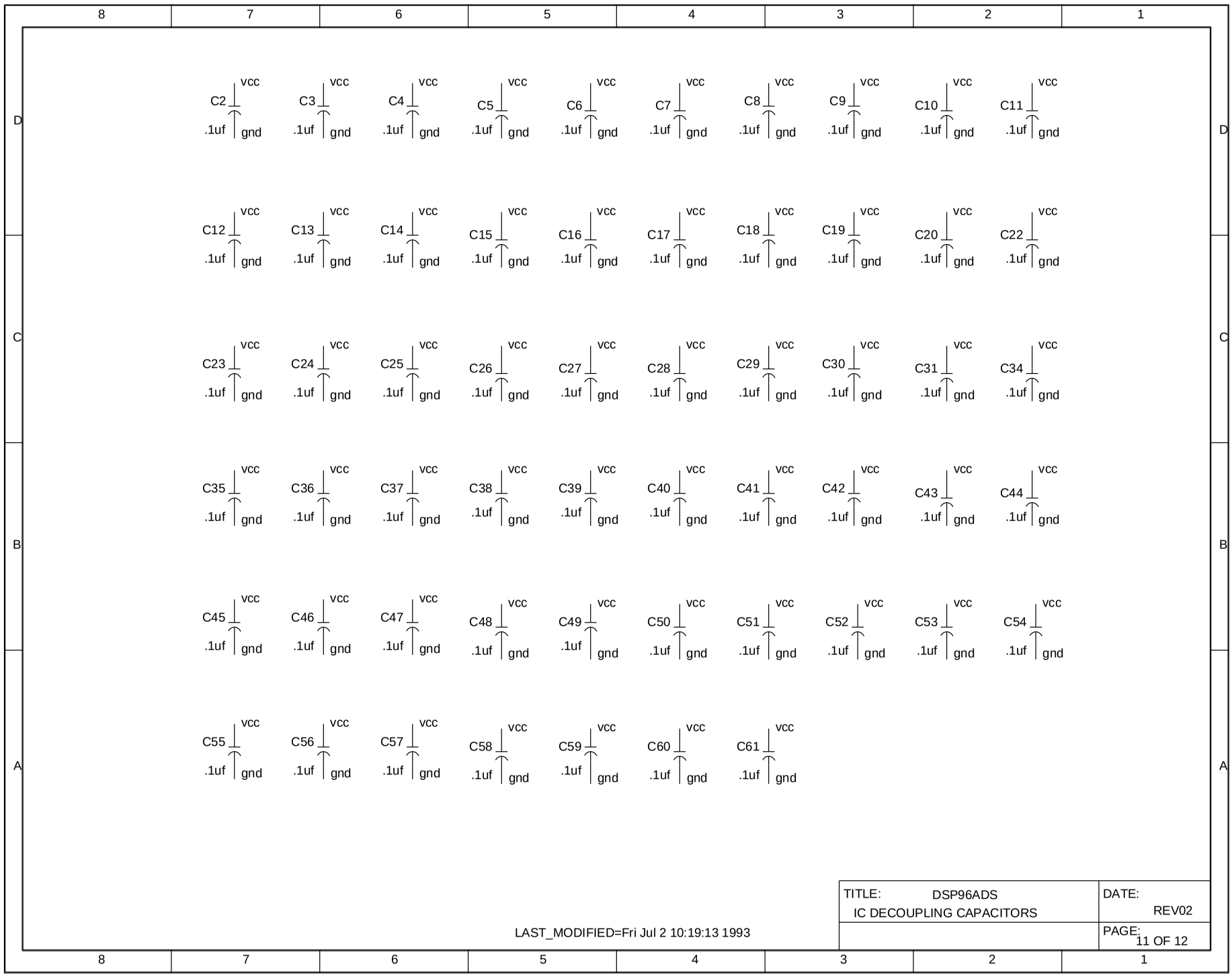
bD<0>	P2_A1	vcc	P2_B1	bA<0>	P2_C1		
bD<1>	P2_A2	gnd	P2_B2	bA<1>	P2_C2		
bD<2>	P2_A3	bDE*	P2_B3	bA<2>	P2_C3		
bD<3>	P2_A4	bHS*	P2_B4	bA<3>	P2_C4		
bD<4>	P2_A5	bHA*	P2_B5	bA<4>	P2_C5		
bD<5>	P2_A6	DR*	P2_B6	bA<5>	P2_C6		
bD<6>	P2_A7	DSI/OS0	P2_B7	bA<6>	P2_C7		
bD<7>	P2_A8	DSCK/OS1	P2_B8	bA<7>	P2_C8		
bD<8>	P2_A9	DSO	P2_B9	bA<8>	P2_C9		
bD<9>	P2_A10	bHR*	P2_B10	bA<9>	P2_C10		
bD<10>	P2_A11	bBG*	P2_B11	bA<10>	P2_C11		
bD<11>	P2_A12	gnd	P2_B12	bA<11>	P2_C12		
bD<12>	P2_A13	vcc	P2_B13	bA<12>	P2_C13		
bD<13>	P2_A14	bBA*	P2_B14	bA<13>	P2_C14		
bD<14>	P2_A15	bBB*	P2_B15	bA<14>	P2_C15		
bD<15>	P2_A16	bBR*	P2_B16	bA<15>	P2_C16		
bD<16>	P2_A17	bBS*	P2_B17	bA<16>	P2_C17		
bD<17>	P2_A18	bR/W*	P2_B18	bA<17>	P2_C18		
bD<18>	P2_A19	bTS*	P2_B19	bA<18>	P2_C19		
bD<19>	P2_A20	bBL*	P2_B20	bA<19>	P2_C20		
bD<20>	P2_A21	bS0	P2_B21	bA<20>	P2_C21		
bD<21>	P2_A22	gnd	P2_B22	bA<21>	P2_C22		
bD<22>	P2_A23	bS1	P2_B23	bA<22>	P2_C23		
bD<23>	P2_A24	bAE*	P2_B24	bA<23>	P2_C24		
bD<24>	P2_A25	bTT*	P2_B25	bA<24>	P2_C25		
bD<25>	P2_A26	bTA*	P2_B26	bA<25>	P2_C26		
bD<26>	P2_A27	IRQA_IN	P2_B27	bA<26>	P2_C27		
bD<27>	P2_A28	IRQB_IN	P2_B28	bA<27>	P2_C28		
bD<28>	P2_A29	IRQC_IN	P2_B29	bA<28>	P2_C29		
bD<29>	P2_A30	RESET*	P2_B30	bA<29>	P2_C30		
bD<30>	P2_A31	gnd	P2_B31	bA<30>	P2_C31		
bD<31>	P2_A32	vcc	P2_B32	bA<31>	P2_C32		

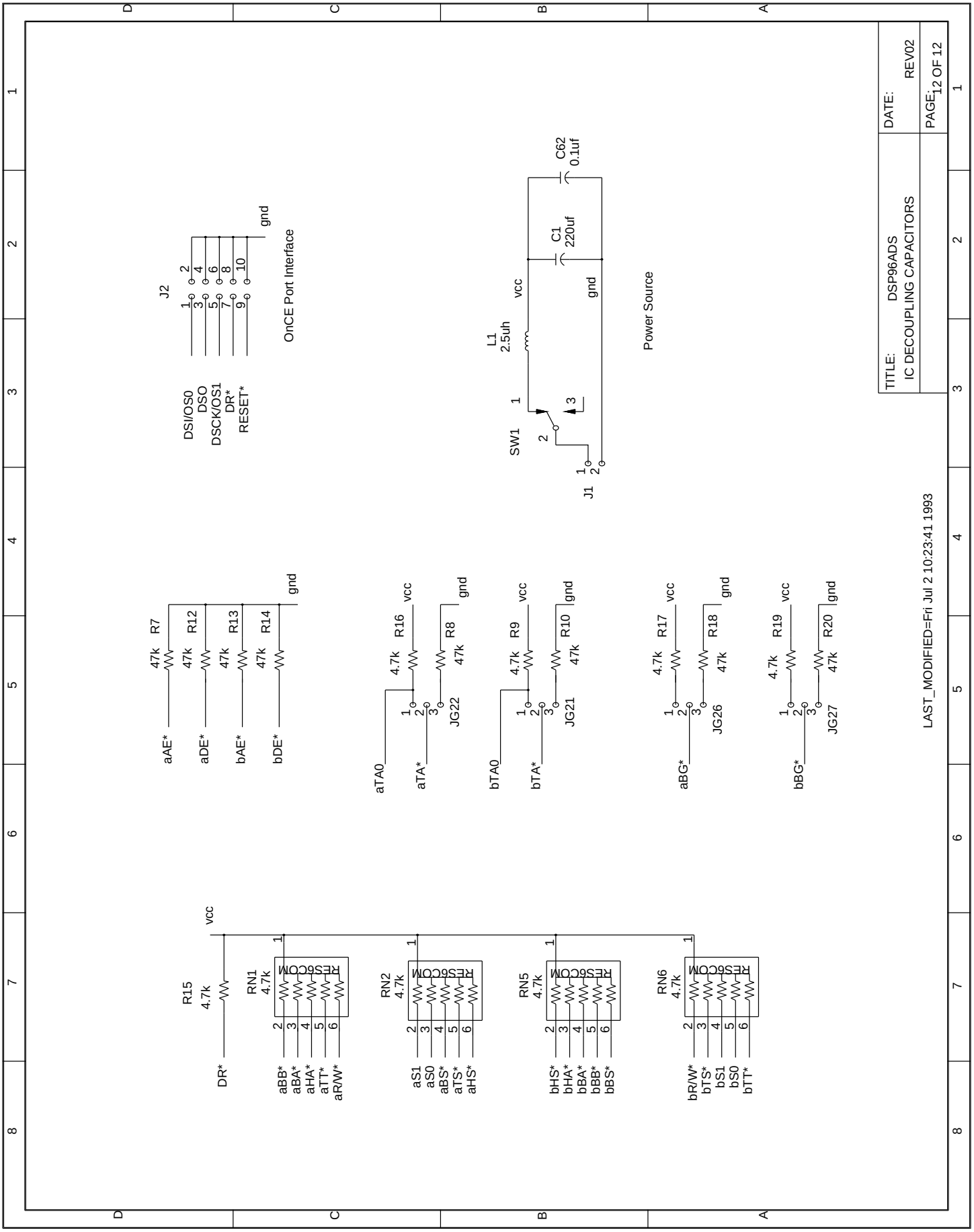
PORTB INTERFACE CONNECTOR

LAST_MODIFIED=Fri Jul 2 09:58:58 1993

TITLE: DSP96ADS PORTA/B Edge CONNECTORS	DATE: REV02
	PAGE: 9 OF 12


J3
aD<0> P1-A1
aD<1> P1-A2
aD<2> P1-A3
aD<3> P1-A4
aD<4> P1-A5
aD<5> P1-A6
aD<6> P1-A7
aD<7> P1-A8
gnd P1-A9
aD<8> P1-A10
gnd P1-A11
aD<9> P1-A12
aD<10> P1-A13
aD<11> P1-A14
gnd P1-A15
aD<12> P1-A16
gnd P1-A17
aD<13> P1-A18
TIO1 P1-A19
aD<14> P1-A20
aD<15> P1-A21
aD<16> P1-A22
aD<17> P1-A23
aD<18> P1-A24
aD<19> P1-A25
aD<20> P1-A26
aD<21> P1-A27
aD<22> P1-A28
aD<23> P1-A29
aD<24> P1-A30
TIO0 P1-A31
vcc P1-A32
aD<25> P1-B1
aD<26> P1-B2
aD<27> P1-B3
aD<28> P1-B4
aD<29> P1-B5
aD<30> P1-B6
aD<31> P1-B7
aA<31> P1-B8
aA<30> P1-B9
aA<29> P1-B10
aA<28> P1-B11
aA<27> P1-B12
aA<26> P1-B13
aA<25> P1-B14
aA<24> P1-B15
aA<23> P1-B16
aA<22> P1-B17
aA<21> P1-B18
aA<20> P1-B19
gnd P1-B20
aA<19> P1-B21
aA<18> P1-B22
gnd P1-B23
aA<17> P1-B24
aA<16> P1-B25
aA<15> P1-B26
aA<14> P1-B27
aA<13> P1-B28
aA<12> P1-B29
aA<11> P1-B30
AWR* P1-B31
vcc P1-B32
aA<10> P1-C1
aA<9> P1-C2
aA<8> P1-C3
aA<7> P1-C4
aA<6> P1-C5
aA<5> P1-C6
aA<4> P1-C7
aA<3> P1-C8
gnd P1-C9
aA<2> P1-C10
aA<1> P1-C11
aA<0> P1-C12
aHA* P1-C13
aHR* P1-C14
aHS* P1-C15
aTA* P1-C16
aBB* P1-C17
aBG* P1-C18
aBR* P1-C19
aBA* P1-C20
aBL* P1-C21
aTT* P1-C22
aR/W* P1-C23
aS1 P1-C24
aS0 P1-C25
aBS* P1-C26
aTS* P1-C27
aAE* P1-C28
aDE* P1-C29
CLK_I/O P1-C30
BWR* P1-C31
vcc P1-C32
PORTA INTERFACE CONNECTOR
J4
bD<0> P2-A1
bD<1> P2-A2
bD<2> P2-A3
bD<3> P2-A4
bD<4> P2-A5
bD<5> P2-A6
bD<6> P2-A7
bD<7> P2-A8
bD<8> P2-A9
bD<9> P2-A10
bD<10> P2-A11
bD<11> P2-A12
bD<12> P2-A13
bD<13> P2-A14
bD<14> P2-A15
bD<15> P2-A16
bD<16> P2-A17
bD<17> P2-A18
bD<18> P2-A19
bD<19> P2-A20
bD<20> P2-A21
bD<21> P2-A22
bD<22> P2-A23
bD<23> P2-A24
bD<24> P2-A25
bD<25> P2-A26
bD<26> P2-A27
bD<27> P2-A28
bD<28> P2-A29
bD<29> P2-A30
bD<30> P2-A31
bD<31> P2-A32
vcc P2-B1
gnd P2-B2
bDE* P2-B3
bHS* P2-B4
bHA* P2-B5
DR* P2-B6
DSI/OS0 P2-B7
DSCK/OS1 P2-B8
DSO P2-B9
bHR* P2-B10
bBG* P2-B11
gnd P2-B12
vcc P2-B13
bBA* P2-B14
bBB* P2-B15
bBR* P2-B16
bBS* P2-B17
bR/W* P2-B18
bTS* P2-B19
bBL* P2-B20
bS0 P2-B21
gnd P2-B22
bS1 P2-B23
bAE* P2-B24
bTT* P2-B25
bTA* P2-B26
IRQA_IN P2-B27
IRQB_IN P2-B28
IRQC_IN P2-B29
RESET* P2-B30
gnd P2-B31
vcc P2-B32
bA<0> P2-C1
bA<1> P2-C2
bA<2> P2-C3
bA<3> P2-C4
bA<4> P2-C5
bA<5> P2-C6
bA<6> P2-C7
bA<7> P2-C8
bA<8> P2-C9
bA<9> P2-C10
bA<10> P2-C11
bA<11> P2-C12
bA<12> P2-C13
bA<13> P2-C14
bA<14> P2-C15
bA<15> P2-C16
bA<16> P2-C17
bA<17> P2-C18
bA<18> P2-C19
bA<19> P2-C20
bA<20> P2-C21
bA<21> P2-C22
bA<22> P2-C23
bA<23> P2-C24
bA<24> P2-C25
bA<25> P2-C26
bA<26> P2-C27
bA<27> P2-C28
bA<28> P2-C29
bA<29> P2-C30
bA<30> P2-C31
bA<31> P2-C32
PORTB INTERFACE CONNECTOR
LAST_MODIFIED=Fri Jul 2 10:11:46 1993
TITLE:
DSP96ADS
PORTA/B TOP CONNECTORS
DATE:
REV02
PAGE:
10 OF 12


8 7 6 5 4 3 2 1
D C B A
C2 C3 C4 C5 C6 C7 C8 C9 C10 C11
C12 C13 C14 C15 C16 C17 C18 C19 C20 C22
C23 C24 C25 C26 C27 C28 C29 C30 C31 C34
C35 C36 C37 C38 C39 C40 C41 C42 C43 C44
C45 C46 C47 C48 C49 C50 C51 C52 C53 C54
C55 C56 C57 C58 C59 C60 C61
vcc
.1uf
gnd
LAST_MODIFIED=Fri Jul 2 10:19:13 1993
TITLE: DSP96ADS
IC DECOUPLING CAPACITORS
DATE: REV02
PAGE: 11 OF 12


TITLE: DSP96ADS
IC DECOUPLING CAPACITORS
DATE: REV02
PAGE: 12 OF 12
LAST_MODIFIED=Fri Jul 2 10:23:41 1993
OnCE Port Interface
J2
DSI/OS0
DSO
DSCK/OS1
DR*
RESET*
gnd
Power Source
L1
2.5uh
vcc
C1
220uf
C62
0.1uf
SW1
J1
gnd
R7
R12
R13
R14
47k
aAE*
aDE*
bAE*
bDE*
R16
R8
R9
R10
R17
R18
R19
R20
4.7k
aTA0
aTA*
bTA0
bTA*
aBG*
bBG*
JG22
JG21
JG26
JG27
R15
RN1
RN2
RN5
RN6
RES6COM
DR*
aBB*
aBA*
aHA*
aTT*
aR/W*
aS1
aS0
aBS*
aTS*
aHS*
bHS*
bHA*
bBA*
bBB*
bBS*
bR/W*
bTS*
bS1
bS0
bTT*

APPENDIX B

DSP96002ADM BILL OF MATERIALS

B.1 DSP96002ADM—ELECTRICAL PARTS LIST REV. 1.8 --10/20/93

Qty	Description	Ref. Designators	Vendor Part #
Integrated Circuits			
1	DSP96002	U35	Motorola
4	WS57C191B35D	U1–U4, U8–U11	WaferScale Integration
1	MC1455P1	U20	Motorola
3	74FACT00	U5, U6, U7	Motorola
2	74F138	U42, U43	Motorola
2	74F32	U41, U44	Motorola
3	PAL16L8-7	U30, U31, U39, U40	TI, AMD
6	74F244	U32–U34, U36–U38	Motorola
16	MCM6209P15	U12–U19, U22–U29	Motorola
1	40 MHz osc.	U21	NDK-TD1100C-40
Resistors			
1	1 MΩ	R11	
9	47 kΩ	R6, R7, R8, R10, R12–R14, R18, R20	
8	4.7 kΩ	R1–R3, R9, R15–R17, R19	
1	2.7 KΩ	R4	
1	1 kΩ	R5	
Resistor Networks			
4	4.7 kΩ (6 pin)	RN1, RN2, RN5, RN6	Bourne 4606X-101-472
2	10 kΩ (8 pins)	RN3, RN4	Bourne 4610X-101-103
Transistors			
1	2N3904	Q1	Motorola
Capacitors			
1	.47 µf	C32	AVX SA305E474ZAA
1	220 µf	C1	Sprague 501D227M016MM
58	.1 µf	C2–C20, C22–C31, C33–C61	AVX SA105E104ZAA
1	1 µf	C21	AVX SA405E105ZAA

B.2 DSP96002ADM—HARDWARE PARTS LIST REV. 1.8 --10/20/93

Qty	Description	Ref. Designator	Vendor Part #
		Jumpers	
4	2 row × 12 Bergstiks	JG15–JG17, JG25	R.N. NSH-12DB-S2-TG30
1	2 row × 2 Bergstiks	JG20	R.N. NSH-04DB-S2-TG30
2	(18) 1 row × 3 Bergstiks	JG1–JG14, JG21, JG22, JG26, JG27	R.N. NSH-36SB-S2-TG30
4	2 row × 3 Bergstiks	JG18, JG19, JG23, JG24	R.N. NSH-06DB-S2-TG30
1	2 row × 5 Bergstiks	J2	R.N. NSH-10DB-S2-TG30
6	1 row × 32 Bergstiks	J3, J4	R.N. NSH-32SB-S2-TG30
		Sockets	
1	18 × 18 PGA socket	U35	R.N. PGA-244AH3-S-TG
4	20 pin (300 mil) sockets	U30, U31, U39, U40	ICT-203-S-TG
16	28 pin (300 mil) sockets	U12–U19, U22–U29	R.N. ICE-283-S-TG
8	28 pin (600 mil) sockets	U1–U4, U8–U11	R.N. ICT-286-S-TG
1	14 pin (300 mil) socket	U21	RN - ICA-143-SCO-TG30
		Connectors	
2	96 pos. connector	P1, P2	R.N. DIN96CPCSR1TR
1	2 pos.power terminal block	J1	Augat-MC6-P102-02
		Switches	
1	SPST momentary switch	S1	C&K - 8125-S-D9-R2-BE
1	SPST power switch		C&K 7101-S-D9-A2-BE
		Miscellaneous	
4	Rubber Feet		Amatom #5186
1	Ferrite Bead		Miller FB73-226