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DSP56002P/D

MOTOROLA
SEMICONDUCTOR
PRODUCT INFORMATION

DSP56002
DSP56L002

Product Brief
24-bit Digital Signal Processor

The DSP56002 and the DSP56L002 are MPU-style general purpose Digital Signal Processors (DSPs), composed of an efficient 24-bit digital signal processor core, program and data memories, various peripherals, and support circuitry. The 56000-Family-compatible DSP core is fed by on-chip program RAM, two independent data RAMs, and two data ROMs with sine and A-law and μ-law tables. The DSP56002/L002 contains a Serial Communication Interface (SCI), Synchronous Serial Interface (SSI), parallel Host Interface (HI), Timer/Event Counter, Phase-Locked Loop (PLL), and On-chip Emulation (OnCE™) port. This combination of features, illustrated in Figure 1, makes the DSP56002/L002 a cost-effective, high-performance solution for high-precision general-purpose digital signal processing.

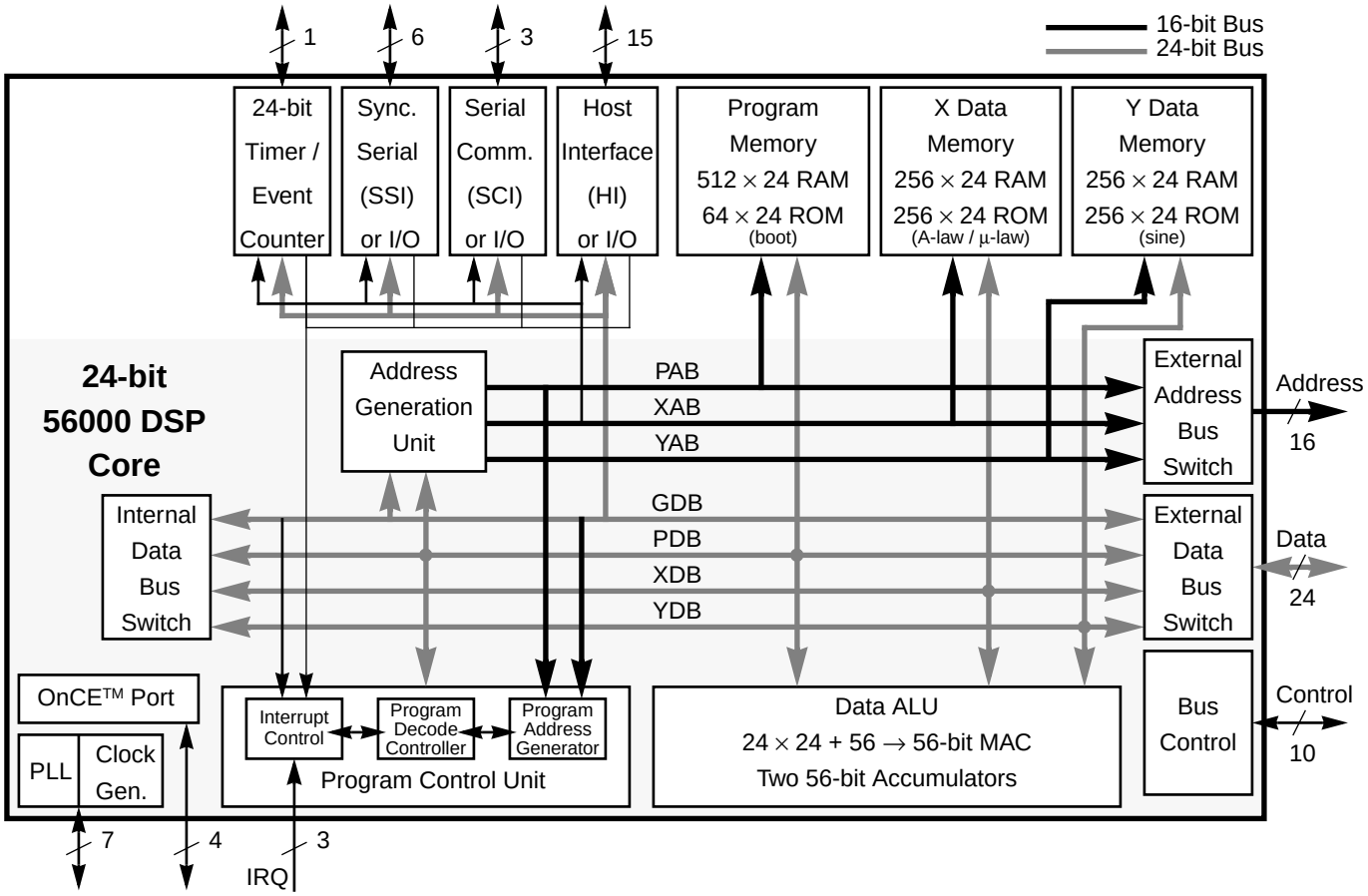

Figure 1 DSP56002/L002 Block Diagram

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DSP56002/L002 Features

Digital Signal Processing Core

- Efficient, object code compatible, 24-bit 56000-Family DSP engine
  - — Up to 33 Million Instructions Per Second (MIPS) – 30.3 ns instruction cycle at 66 MHz
  - — Up to 198 Million Operations Per Second (MOPS) at 66 MHz
  - — Performs a 1024-point complex Fast Fourier Transform (FFT) in 59,898 clocks
  - — Highly parallel instruction set with unique DSP addressing modes
  - — Two 56-bit accumulators including extension byte
  - — Parallel 24 × 24-bit multiply-accumulate in 1 instruction cycle (2 clock cycles)
  - — Double precision 48 × 48-bit multiply with 96-bit result in 6 instruction cycles
  - — 56-bit Addition/Subtraction in 1 instruction cycle
  - — Fractional and integer arithmetic with support for multiprecision arithmetic
  - — Hardware support for block-floating point FFT
  - — Hardware nested DO loops
  - — Zero-overhead fast interrupts (2 instruction cycles)
  - — Four 24-bit internal data buses and three 16-bit internal address buses for maximum information transfer on-chip

Memory

- On-chip Harvard architecture permitting simultaneous accesses to program and two data memories
- 512 × 24-bit on-chip program RAM and 64 × 24-bit bootstrap ROM
- Two 256 × 24-bit on-chip data RAMs
- Two 256 × 24-bit on-chip data ROMs containing sine, A-law and μ-law tables
- External memory expansion with 16-bit address and 24-bit data buses
- Bootstrap loading from external data bus, Host Interface, or Serial Communications Interface

Peripheral and Support Circuits

- Byte-wide Host Interface (HI) with direct memory access support
- Synchronous Serial Interface (SSI) to communicate with codecs and synchronous serial devices
  - — Up to 32 software-selectable time slots in network mode
- Serial Communication Interface (SCI) for full-duplex asynchronous communications
- 24-bit Timer/Event Counter also generates and measures digital waveforms
- On-chip peripheral registers memory mapped in data memory space
- Double buffered peripherals

- Up to 25 general purpose I/O (GPIO) pins
- Three external interrupt request pins; one non-maskable
- On-Chip Emulation (OnCE) port for unobtrusive, processor speed-independent debugging
- Software-programmable, Phase-Locked Loop-based (PLL) frequency synthesizer for the core clock
- Power-saving Wait and Stop modes
- Fully static, HCMOS design for operating frequencies from 66 MHz or 40 MHz down to DC
- 132-pin Ceramic Pin Grid Array (PGA) package; 13 × 13 array
- 132-pin Plastic Quad Flat Pack (PQFP) surface-mount package; 24 × 24 × 4 mm
- 144-pin Thin Quad Flat Pack (TQFP) surface-mount package; 20 × 20 × 1.4 mm
- 3.3 V (DSP56L002) and 5 V (DSP56002) Power supply options

The DSP56002 and DSP56L002 are identical except that the DSP56002 operates at 5 volts, while the DSP56L002 operates at 3.3 volts with a resultant reduction in power consumption and the need for fewer batteries in a portable application.

Documentation

The three documents listed in Table 1 are required for a complete description of the DSP56002/L002 and are necessary to properly design with the part. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, or a Motorola Literature Distribution Center listed on the back page.

Table 1 DSP56002/L002 Documentation

Topic	Description	Order Number
DSP56000 Family Manual	Detailed description of the 56000-family architecture and the 16-bit core processor and instruction set	DSP56KFAMUM/AD
DSP56002 User's Manual	Detailed description of memory, peripherals, and interfaces	DSP56002UM/AD
DSP56002/L002 Data Sheet	Electrical and timing specifications, and pin and package descriptions	DSP56002/D