DSP56002ADM

User's Manual

Motorola, Incorporated
Semiconductor Products Sector
6501 William Cannon Drive West
Austin, TX 78735-8598

Introduction

This document supports the DSP56002 Application Development Module (DSP56002ADM), including a description of its basic structure and operation, the equipment required to use it, the specifications of the key components, schematic diagrams, and a parts list. **Section 1** is a Quick Start Guide. **Section 2** provides detailed information about key components in the evaluation module. **Appendix A** has detailed schematics. **Appendix B** lists the Bill Of Materials (BOM) for the board. Detailed information is provided in the additional documents supplied with this kit.

Order this document by: DSP56002ADMUM/AD

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SECTION 1

QUICK START GUIDE

1.1 OVERVIEW

The Motorola Application Development System (ADS) is a tool used to design and test complex software applications and hardware products using a specific Motorola Digital Signal Processor (DSP) chip. The related Application Development Modules (ADMs) contain the DSP chip and related hardware used for bench development and testing. Detailed information about the content and use of the ADS is provided in the ADS User's Manual (order number DSPADSUM/AD).

This manual provides specific information about the DSP56002 Application Development Module (DSP56002ADM). This section provides a summary description of the DSP56002ADM, additional requirements, and quick installation information. Detailed information about the DSP56002ADM design and operation is provided in the remaining sections of this manual.

1.2 EQUIPMENT

The following section gives a brief summary of the equipment required to use the DSP56002ADM, some of which will be supplied with the module and some of which must be supplied by the user.

1.2.1 What You Get with the DSP56002ADM

The following materials are provided with the DSP56002ADM:

- DSP56002ADM Board
- DSP56002ADM Product Information
- DSP56002ADM User's Manual (this document)
- Motorola DSP Registration Form

1.2.2 What You Need to Supply

The DSP56002ADM requires the following supplemental components for operation:

- Motorola ADS with appropriate host interface card
- Host Computer system:
  - PC-compatible computer (486 class or higher) with:
    - MS-DOS version 6.0 or later, or Windows 3.1 or later, or Windows 95
    - 8 Megabytes RAM
    - one open 16-bit ISA or a PCI expansion slot
    - free I/O addresses ($100–$102, $200–$202, or $300–$303)
    - CD-ROM drive
    - hard drive with 4 Megabytes of free disk space
    - mouse
  - Sun Microsystems Sun 4 Workstation running Sun Operating System Release 4.1.1 or later (or Solaris Release 2.5 or later), one open SBus expansion slot, CD-ROM drive, and a mouse, or
  - Hewlett Packard HP7xx Workstation running HPUX Version 9.x (Version 10.x is not supported), one open EISA expansion slot, CD-ROM drive, and a mouse

1.3 INSTALLATION PROCEDURE

Installation requires the following steps:

1. Using information provided in the Motorola ADS User's Manual, install the Motorola ADS in the host computer.
2. Prepare the DSP56002ADM board.
3. Connect the board to the external Command Converter card.

1.3.1 Preparing the DSP56002ADM

CAUTION

Because all electronic components are sensitive to the effects of electrostatic discharge (ESD) damage, correct procedures should be used when handling all components in this kit and inside the supporting personal computer. Use the following procedures to minimize the likelihood of damage due to ESD:

- **Always handle all static-sensitive components in a protected area, preferably a lab with conductive (antistatic) flooring and bench surfaces.**
- **Always use grounded wrist straps when handling sensitive components.**
- **Never remove components from antistatic packaging until required for installation.**
- **Always transport sensitive components in antistatic packaging.**

Locate the twenty-two jumper blocks JP1–JP22 on the DSP56002ADM board, as shown in **Figure 1-1**. Table 1-1 on page 1-7 describes the default jumper and switch settings when shipped from the factory.

Read **Section 2** of this manual, DSP56002ADM Technical Summary, for additional information about the DSP56002ADM board and its components.

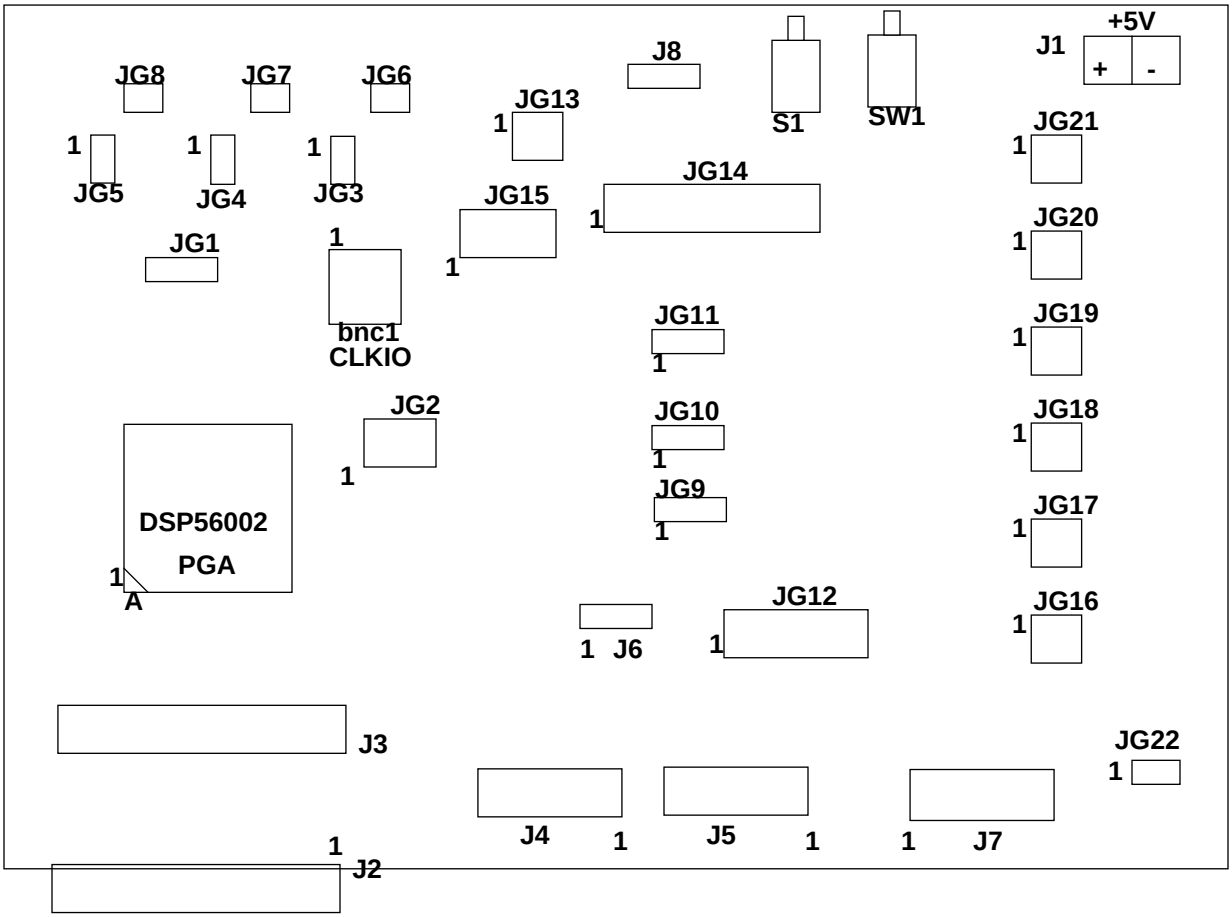


Figure 1-1 ADM Connector and Jumper Group Locations

Table 1-1 DSP56002 ADM Default Jumper Options

Jumper Group	Jumpers	Comment
JG1	3–4	ADM buffered clock
JG2	3–4	ADM reset circuit
JG3,JG4,JG5	1–2, 2–3, 1–2	Mode 2 on reset
JG6,JG7,JG8	1–2,1–2,1–2	External IRQ input path
JG9,JG10,JG11	1–2,1–2,1–2	24-pin EPROM device
JG12	1–2, 8–10, 12–14,16–18	2K words of EPROM (WS57C291B)
JG13	1–3, 2–4	EPROM in Upper Memory
JG14	3–4, 9–10	8K P, 4K X, 4K Y Partition
JG15	3–4	SRAM in Lower Memory
JG16–JG21	1–2, 1–2, 1–2, 1–2, 1–2, 1–2	24-pin SRAM devices (MCM6290)
JG22	11–2	DSP56002 PLL disabled on reset

Note: Some jumper options may require being wirewrapped due to mechanical constraints.

1.3.2 Connecting the DSP56002ADM to the PC and Power

Figure 1-2 shows the interconnection diagram for connecting the PC and the external power supply to the DSP56002ADM board. Using the instructions in the *ADS User's Manual*, connect the Command Converter to the ADM board. Power for the ADM is supplied from the Command Converter module.

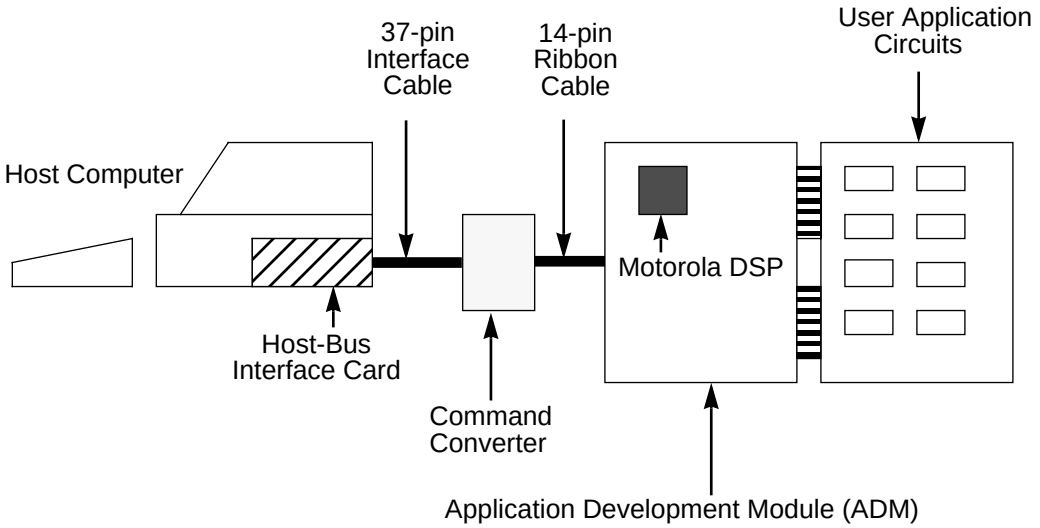


Figure 1-2 Application Development

1.4 USING THE DSP56002ADM

Once the ADM is installed, it becomes a part of the ADS. Use information in the *ADS User's Manual* to develop your application design, debug it, and test it.

SECTION 2

DSP56002ADM TECHNICAL SUMMARY

2.1 DSP56002ADM DESCRIPTION AND FEATURES

The DSP56002ADM has various options to facilitate evaluation of the different features of the chip. These options are outlined in this chapter with a statement on the default factory jumpers with which the Application Developement Module (ADM) will be shipped.

Figure 2-1 on page 2-5 illustrates the ADM architecture. Memory decoding is minimal to achieve zero wait accesses. Therefore, memory may overlap into other address blocks within a 32 K address space. There are a variety of jumper options for partitioning the memory to make it appear in all three Digital Signal Processor (DSP) memory maps.

Sockets for 256 K Static Random Access Memories (SRAMs) are available for increasing memory size to the maximum 64 K words for each of the three external memory spaces. Electronically Programmable Read Only Memory (EPROM) sockets are also available for stand alone operation. The EPROM is only accessable in program memory space.

Connectors exist for each on-chip peripheral port as well as two 96 pin access points to hook boards and/or logic analyzers. An Audio Engineering Society/European Broadcasters Union (AES/EBU) connector is also provided so that a user may hook the DSP56401 AES/EBU evaluation board for developing digital stereo application software.

The OnCE™ port interface connector normally hooks to the ADS Command Converter, providing the user a way of controlling the DSP56002 in a target system. This connector has a standard pinout that should be used to design the target application hardware. It will allow the user to evaluate the hardware and software of the application without using a special emulator.

An overview description of the DSP56002ADM is also provided in the DSP56002ADM Product Information document (order number DSP56002ADMP/D) included with this kit. The main features of the DSP56002ADM include the following:

- Full speed operation at 40–66 MHz
- 16 K words of configurable SRAM expandable to 64 K words
- Additional SOJ sockets for 256 K words of Fast SRAM
- 2 K words of EPROM with sockets expandable to 32 K words
- Stand-alone operation of ADM after initial development
- Full support of multiple data memory maps
- 96-Pin connector which provides access to all DSP56002 pins

- RS232 voltage converter for Asynchronous Serial Interface
- OnCE port Connector for easy hookup to DSP56002 Command Converter
- Separate connectors for easy access to on-chip peripherals
- AES/EBU connector for interface to DSP56401 EVB

Call your local Motorola sales office or distributor for additional information about the Motorola Application Development System (ADS) kit. The ADS kit includes two additional boards: a host interface card and an external universal Command Converter. The host interface card plugs in the host bus (on a IBM-compatible PC, HP7xx workstation, or Sun/Sun-compatible system) inside the computer chassis. The external universal Command Converter card connects to the host card via a 37-pin ribbon cable. The Command Converter card connects to the JTAG connector on the DSP56002ADM via another short 14-pin ribbon cable. The ADS is only compatible with Motorola software tools.

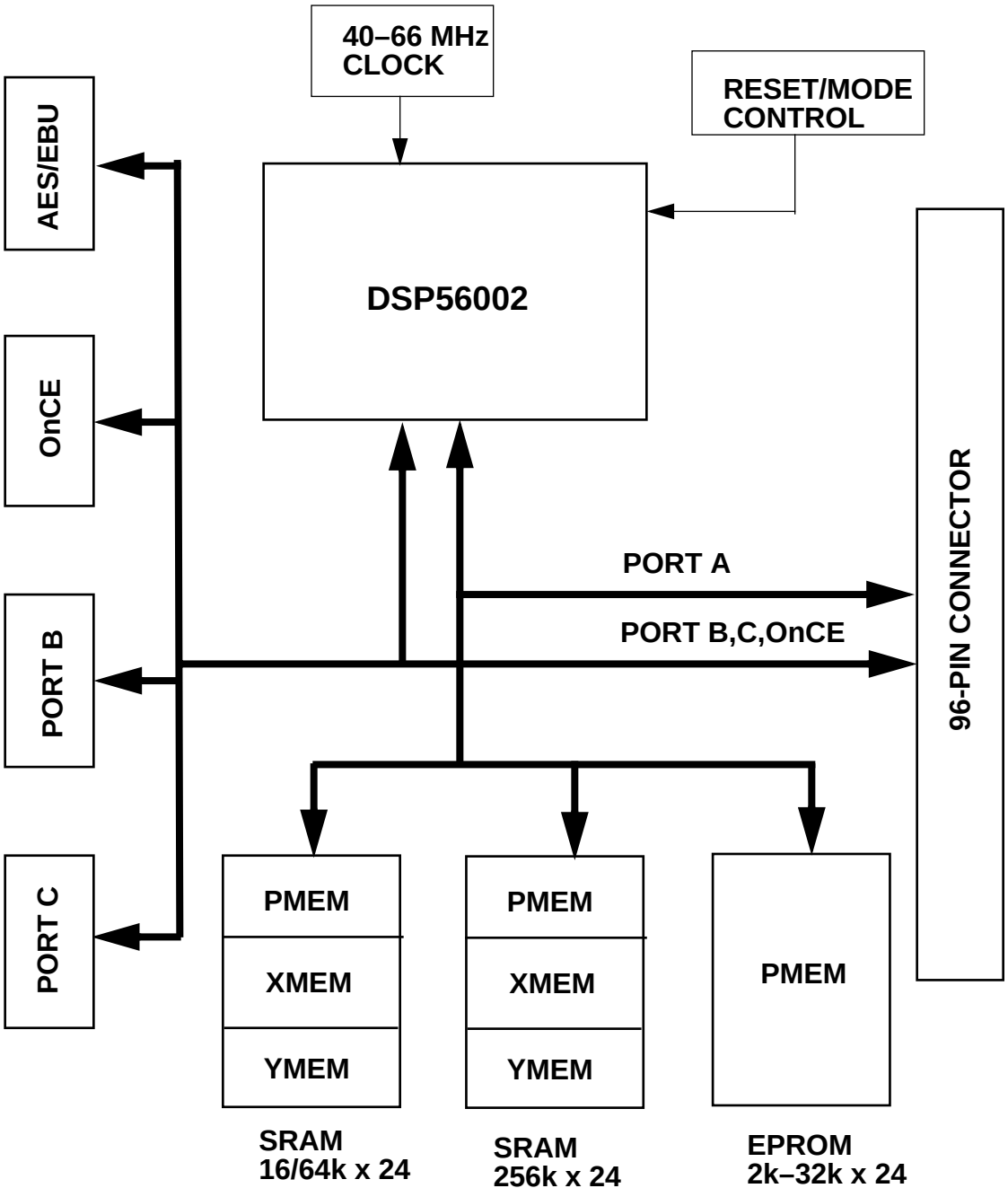


Figure 2-1 DSP56002ADM Block Diagram

2.2 DSP56002 DESCRIPTION

A full description of the DSP56002, including functionality and user information, is provided in the following documents included as a part of this kit (either as printed copies or on the documentation CD-ROM):

- **DSP56002 Technical Data—**Provides features list and specifications including signal descriptions, DC power requirements, AC timing requirements, and available packaging
- **DSP56002 User's Manual—**Provides an overview description of the DSP and detailed information about the on-chip components including the memory and I/O maps, peripheral functionality, and control and status register descriptions for each subsystem
- **DSP56000 Family Manual—**Provides a detailed description of the core processor including internal status and control registers and a detailed description of the family instruction set

Refer to these documents for detailed information about chip functionality and operation.

2.2.1 DSP56002 USER EPROM DECODERS

The ADM contains sockets which will accommodate 2k × 8, 4k × 8, 8k × 8, 16k × 8, and 32k × 8 EPROMs. The EPROM sockets use the pinout and dimensions for Waferscale Integration Inc. devices. The 2k × 8, 4k × 8, and 8k × 8 EPROMS come in a 24-pin package and the 16k × 8 and 32k × 8 EPROMs come in a 28-pin package. The 2k × 8, 4k × 8, and 8k × 8 devices must be inserted in the lower twenty-four pins of the 28-pin sockets leaving pins 1, 2, 27, 28 of the socket blank. When using 24-pin devices JG9, JG10, and JG11 must be configured to bring the +5 V supply to the EPROMS.

For the proper address signals to arrive at the particular EPROM density chosen, JG12 and JG13 must be configured correctly. JG12 provides the options for EPROM density while JG13 provides the options for mapping the EPROM to the upper 32k of program memory or to program memory and Port C Bit 2 equal to a logic 1. These mapping options are useful when inserting SRAMs into the 256k × 4 sockets to provide EPROM and SRAM in program memory without causing a bus conflict. The following tables illustrate how to configure the sockets correctly for the five different EPROM densities.

Table 2-1 EPROM Density Jumper Selection

EPROM Type	JG9–JG11	JG12
2K x 8(WS57C291B)	1–2	1–2, 8–10, 12–14, 16–18
4K x 8(WS57C43B)	1–2	1–2, 5–6, 8–10, 12–14, 16–18
8K x 8(WS57C49B)	1–2	1–4, 5–6, 8–10, 12–14, 16–18
16K x 8(WS57C51B)	2–3	1–3, 11–13, 15–17
32K x 8(WS57C71C)	2–3	1–3, 7–9, 11–13, 15–17

Table 2-2 EPROM Memory Space Selection

Memory Map	JG13
Pmem ($8000–$FFFF)	1–3, 2–4
Pmem & Port C Bit 2 = 1	2–4, 3–5

Note: The ADM is factory configured for the 2k×8 EPROMS in upper 32K address of program memory space (JG9–JG11 1–2, JG13 1–3 and 2–4).

2.2.2 DSP56002 User SRAM Decoder/Partitions

There are six 16k × 4 bit high speed Complementary Metal Oxide Semiconductor (CMOS) SRAMs (MCM6290) which provide a working area for user programs and data. Provision has been made to accomodate six 64k × 4 bit devices (MCM6209) into the same sockets. Also available are six SOJ sockets which will accommodate 256k × 4 SRAMS (MCM6229A) for gathering large data samples.

The 16 K and 64 K SRAMs may be moved to the lower or upper 32 K of memory and may be partitioned so that program or data memory spaces have external memory. If the upper address memory space is used, there is a 1 wait state penalty due to the inversion of the A15 address line.

16k × 4 devices must be inserted in the lower 24 pins of the 28-pin dual-in-line sockets leaving pins 1, 2, 27, and 28 of the socket blank clear. To provide power to the 16k × 4 devices JG16–JG21 are configured so that pins 1–2 are common. If 64k × 4 devices are used, then Pin 26 of the SRAM becomes an address input. JG16–JG21 pins 2–3 must be common.

SRAM decoding does not have bus arbitration signals as qualifiers. Any processor which becomes bus master from the 96-pin expansion connector may therefore directly access the SRAMs. This is useful in shared memory configurations.

Jumper group JG14 is for memory block selection as well as SRAM program memory and data memory map partitioning. There are a variety of possible options for SRAM partitioning and memory address start. It should be noted that the SRAM decoder is a minimal decoder in order to achieve maximum performance.

Jumper group JG15 is used to select the memory enable signals to the 16 K / 64 K SRAMs and the 256 K SRAMs. This jumper group provides the options for enabling both banks of SRAMs so they will not conflict with each other.

Using both banks of SRAMs will provide the user with a maximum of 64 K words for program memory and 256 K words for data memory. This is very useful for gathering large samples of data. The EPROMs may also be used with 64 K program memory when using the Port C Bit 2 (PC2) as a disable line to the EPROMs and an enable bit to both banks of SRAMs. A logic 1 on the PC2 line will select the EPROM; a logic 0 will select the SRAM. Note that because the PC2 line has a pullup resistor, the default value at reset will be logic 1.

Port C Bit 3 (PC3) is used to select between two 64 K X and Y data memory banks, allowing up to 256 K total data memory. The following tables show the jumper options that will provide memory partitions with different memory types and densities.

Table 2-3 User SRAM with EPROM inUpper 32 K Address

Memory Partition	JG13	JG14	JG15	JG16–21
(MCM6290) 8K P, 4K X, 4K Y	1–3, 2–4	3–4, 9–10	3–4	3–4
(MCM6290) 0 P, 8K X, 8K Y	1–3, 2–4	1–2, 7–8	1–2	3–4
(MCM6290) 16K in P,X or Y	1–3, 2–4	1–2, 5–6	3–4	3–4

Table 2-3 User SRAM with EPROM inUpper 32 K Address

Memory Partition	JG13	JG14	JG15	JG16–21
(MCM6290) 8 K P, 8 K X or Y	1–3, 2–4	1–2, 9–10	3–4	3–4
(MCM6209) 32 K P, 16 K X, 16 K Y	1–3, 2–4	1–2, 5–6, 11–12, 17–18	3–4	1–2
(MCM6209) 0 P, 32 K X, 32 K Y	1–3, 2–4	1–2, 5–6, 11–12, 19–20	1–2	1–2
(MCM6209) 0 P, 64 K in X, or Y	1–3, 2–4	1–2, 5–6, 13–14, 15–16	1–2	1–2
(MCM6209) 32 K P,32K D	1–3, 2–4	1–2, 5–6, 13–14, 17–18	3–4	1–2

Note: SRAMs will reside in lower 32 K of address space.

Table 2-4 User SRAM with EPROM Selected with PORT C Bit 2

Memory Partition	JG13	JG14	JG15	JG16–21
(MCM6209) 64 K in P, X, or Y	2–4, 3–5	1–2, 5–6, 13–14, 15–16	7–8	1–2
(MCM6229A) 64 K P RAM, 64 K X RAM, 64 K Y RAM	2–4, 3–5	21–22, 27–28	17–18	N.A.

Table 2-5 User SRAM with No EPROM

Memory Partition	JG13	JG14	JG15	JG16–21
(MCM6290) (MCM6229A) 16 K P , 128 K X, 128 K Y Port C Bit 3 selects 64k banks	4–6	1–2, 5–6, 23–24, 25–26	5–6, 15–16	3–4
(MCM6209) Upper 32K 32K P, 16K X, 16K Y	4–6	1–2, 5–6, 11–12, 17–18	9–10	1–2
(MCM6209) 64K in P	4–6	1–2, 5–6, 13–14, 15–16	5–6	1–2
(MCM6209) 64K in P, X, or Y	4–6	1–2, 5–6, 13–14,15–16	11–12	1–2

Table 2-5 User SRAM with No EPROM

Memory Partition	JG13	JG14	JG15	JG16–21
(MCM6229A) 64 K in P, 64 K X, 64 K Y	4–6	21–22, 27–28	13–14	N.A.
(MCM6209) (MCM6229A) 64 K in P, 128 K X, 128 K Y Port C Bit 3 selects 64 K banks	4–6	1–2, 5–6, 13–14, 15–16, 23–24, 25–26	5–6, 15–16	1–2

Notes: **1.** The SRAMs are factory configured for 16k × 4 devices, with 8 K words in program and 8 K words in data memory in the lower 32 K address space (JG14 3–4 and 9–10, JG15–JG21 3–4).

2. Caution should be taken when selecting SRAM options so that memory mapped external circuits on the 96-pin expansion connector do not conflict with the SRAM area.

2.2.3 DSP56002 Operating Mode Selection

Jumper groups JG3, JG4, and JG5 are used to select one of the eight operating modes in which the DSP56002 will exit reset. The ADM is factory configured for MODE 2. In MODE 2, the internal program memory occupies the lower portion of the program memory space. Addresses higher than the highest internal program memory location are directed to external program memory. Refer to the *DSP56002 Technical Summary* for a complete description of the chip operating modes.

The following table shows the JG3, JG4, and JG5 selection necessary to achieve any of the eight operating modes available on the DSP56002.

Table 2-6 Operating Mode Selection

Mode	JG3	JG4	JG5	COMMENT
0	1–2	1–2	1–2	PRAM enabled, reset at $0000
1	2–3	1–2	1–2	Bootstrap from EPROM
2	1–2	2–3	1–2	PRAM enabled, reset at $E000
3	2–3	2–3	1–2	PRAM disabled, reset at $0000
4	1–2	1–2	2–3	Bootstrap from Host port

Table 2-6 Operating Mode Selection

Mode	JG3	JG4	JG5	COMMENT
5	2–3	1–2	2–3	Reserved for bootstrap
6	1–2	2–3	2–3	Bootstrap from SCI (external clock)
7	2–3	2–3	2–3	Reserved for bootstrap

Note: The ADM is factory configured to exit reset in Mode 2 (JG3 1–2, JG4 2–3, JG5 1–2).

2.2.4 Clock Input Selection

There are three options for clock input selection. The DSP56002 clock source may be either the ADM crystal oscillator chip output, an external clock input, or a third or fifth overtone oscillator. Jumper JG1 provides the selection path for the clock.

Table 2-7 CLOCK SOURCE SELECTION

Clock Source	JG1	Comment
ADM Buffered Clock	3–4	External clock source
External in P1–B5/BNC1	1–2	BNC Clock source
ADM buffered Clock Out	1–2, 3–4	Local clock chip source
Overtone Oscillator circuit	5–6, 7–8	Local oscillator source

Note: The ADM is factory configured for a 40 MHz clock oscillator chip (JG1 3–4).

2.2.5 External/Internal Reset Input

The DSP56002 may be reset using the ADM reset circuit or from an external reset input signal provided by the J2 and J3 connectors. Executing a *cforce r* command from the ADS56002 user interface program will generate a reset pulse on the J6 connector via the Command Converter.

A user may also generate a reset pulse via S1 on the ADM board when operating in the stand-alone mode without a Command Converter. When S1 is toggled a reset pulse is generated on a monostable multivibrator and operating mode selection will be synchronized to the deassertion of its output. JG2 pins 1–2 provide external reset input, and pins 3–4 provide ADM reset circuit output to J2 and J3 connectors.

Note: The ADM is configured to use the ADM reset circuit as reset source (JG2 3–4).

2.2.6 External IRQA/B/C Input Path

The external input path for IRQA, IRQB and IRQC may be directed through the reset logic or directly into the DSP56002 IRQ input pins via JG6, JG7, JG8. The reset logic path insures that the appropriate operating mode is selected during reset without any spurious external interrupts. The direct path to the processor pins allows users to design their own interrupt circuits.

Table 2-8 External IRQ Input Path

Comment	JG6	JG7	JG8
IRQA,B,C Reset Logic	1–2	1–2	1–2
IRQA,B,C Directly to pin	2–3	2–3	2–3

Note: The ADM is factory configured for external IRQA and IRQB , and IRQC inputs to pass through the reset logic (JG6 1–2, JG7 1–2, JG8 1–2).

2.3 DSP56002 ADM CONNECTOR DESCRIPTION

The ADM has various connectors which bring out signals from the DSP for easy access by the user. This section describes these connectors.

Table 2-9 DSP56002 ADM J2 / J3 BusConnector

Pin #	Row A	Row B	Row C
1	D23	VCC	A15
2	D22	GND	A14
3	D21	$\overline{\text{RESETIN}}$	A13
4	D20	R5	A12
5	D19	CLK_IO	A11
6	D18	IRQC_IN	A10
7	D17	IRQB_IN	A09
8	D16	R4	A08
9	D15	IRQA_IN	A07
10	D14	R3	A06
11	D13	GND	A05
12	D12	CKOUT	A04
13	D11	PLOCK	A03
14	D10	PINIT	A02
15	D09	OS1/DSCK	A01
16	D08	OS0/DSI	A00
17	D07	DSO	PC8/STD
18	D06	$\overline{\text{DR}}$	PC7/SRD
19	D05	$\overline{\text{WT}}$	PC6/SCK
20	D04	VCC	PC5/SC2
21	D3	GND	PC4/SC1

Table 2-9 DSP56002 ADM J2 / J3 BusConnector

Pin #	Row A	Row B	Row C
22	D2	$\overline{BN}$	PC3/SC0
23	D1	$\overline{BS}$	PC2/SCLK
24	D0	$\overline{WR}$	PC1/TXD
25	PB0/H0	$\overline{RD}$	PC0/RXD
26	PB1/H1	$\overline{X/Y}$	PB2/H2
27	PB3/H3	$\overline{PS}$	PB4/H4
28	PB5/H5	$\overline{DS}$	PB6/H6
29	PB7/H7	$\overline{BR}$	PB8/H8
30	PB9/H9	$\overline{BG}$	PB10/HA0
31	PB11/H11	GND	PB12/HEN
32	PB13/H13	+VCC	PB14/HACK

Table 2-10 DSP56002 ADM J4 Host Port Connector

Pin #	Description	Pin #	Description
1	PB0/H0	2	PB1/H1
3	PB2/H2	4	PB3/H3
5	PB4/H4	6	PB5/H5
7	PB6/H6	8	PB7/H7
9	PB8/HA0	10	PB9/HA1
11	PB10/HA2	12	PB11/HRW
13	PB12/HEN	14	PB13/HREQ
15	PB14/HACK	16	GND
17	GND	18	VCC

Table 2-11 DSP56002 ADM J5 PORT C Connector

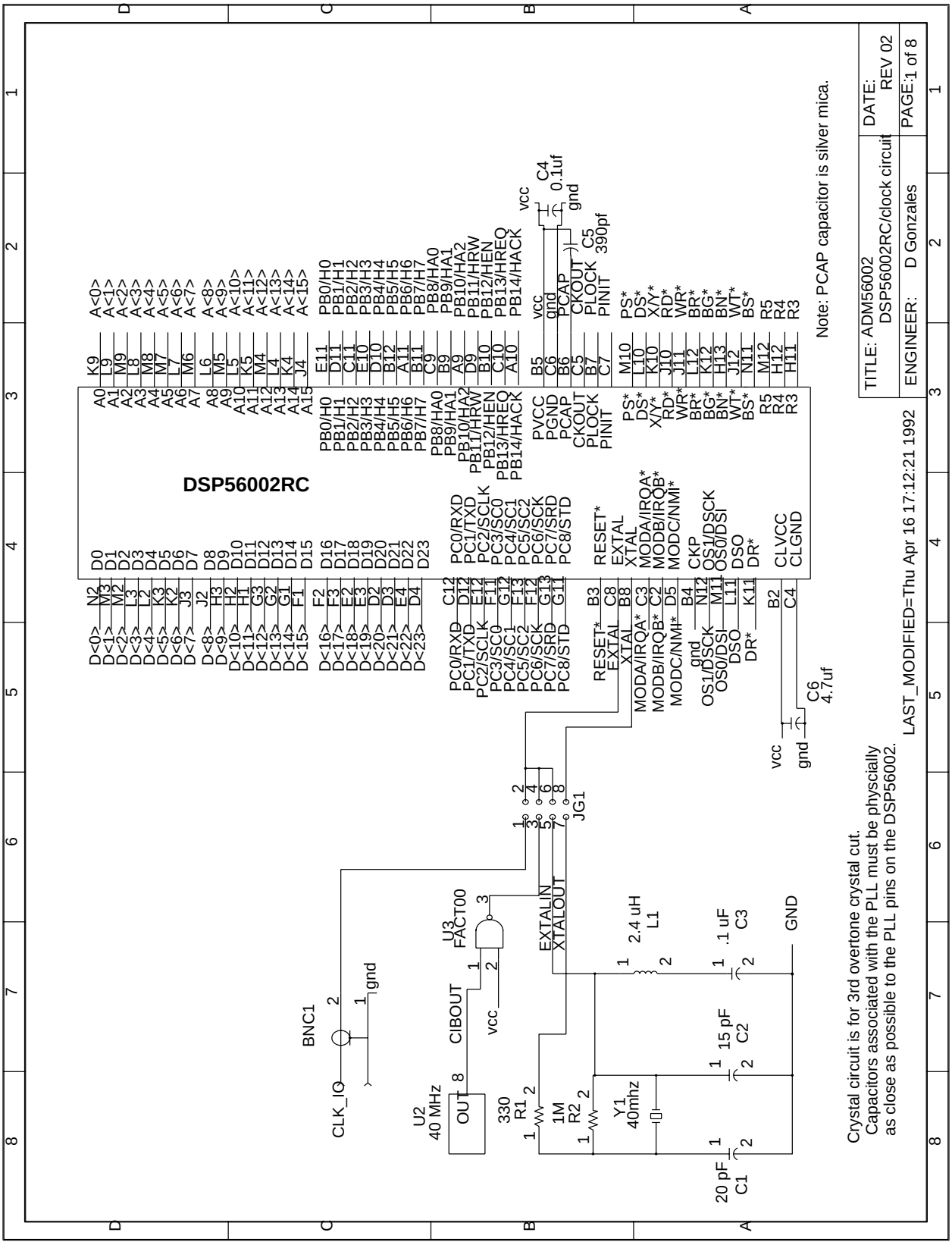
Pin #	Description	Pin #	Description
1	PC0/RXD	2	PC1/TXD
3	PC2/SCLK	4	GND
5	PC3/SC0	6	PC4/SC1
7	PC5/SC2	8	PC6/SCK
9	GND	10	PC7/SRD
11	PC8/STD	12	VCC

Table 2-12 DSP56002 ADM J6 OnCE Connector

Pin #	Signal	Signal Description
1	DSI/OS0	Debug Serial Input/Output Status 0
2	GND	GND
3	DSO	Debug Serial Output/Acknowledge Output
4	GND	GND
5	DSCK/OS1	Debug Serial Clock/Output Status 1
6	GND	GND
7	$\overline{DR}$	Debug Request Input
8	No Connect	Used as Key
9	$\overline{RESET}$	Reset Input
10	GND	GND
11	Vdd	Target Vdd - Supplies OnCE Buffer (HC367)
12	GND	GND
13	No Connect	—
14	GND	GND

APPENDIX A

DSP56002ADM SCHEMATICS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U3
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vcc
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R2
Y1
40mhz
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C1
15 pF
C2
2.4 uH
L1
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C3
EXTALIN
XTALOUT
GND
JG1
C4
0.1uf
C5
390pf
C6
4.7uf
PCAP
CKOUT
PLOCK
PINIT
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Crystal circuit is for 3rd overtone crystal cut.
Capacitors associated with the PLL must be physcially
as close as possible to the PLL pins on the DSP56002.
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DSP56002RC/clock circuit
DATE:
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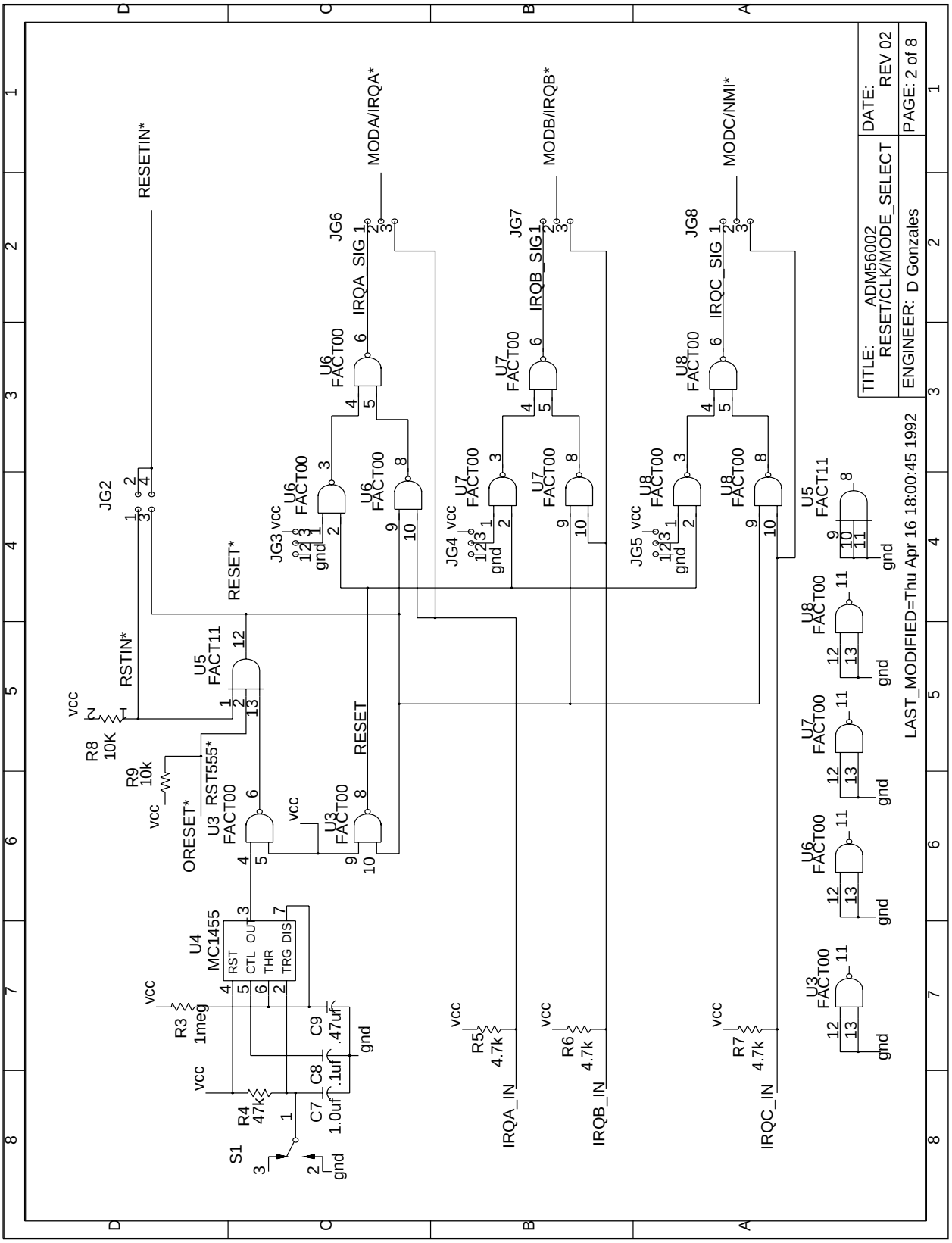
ENGINEER: D Gonzales
PAGE:1 of 8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ENGINEER: D Gonzales
PAGE: 2 of 8
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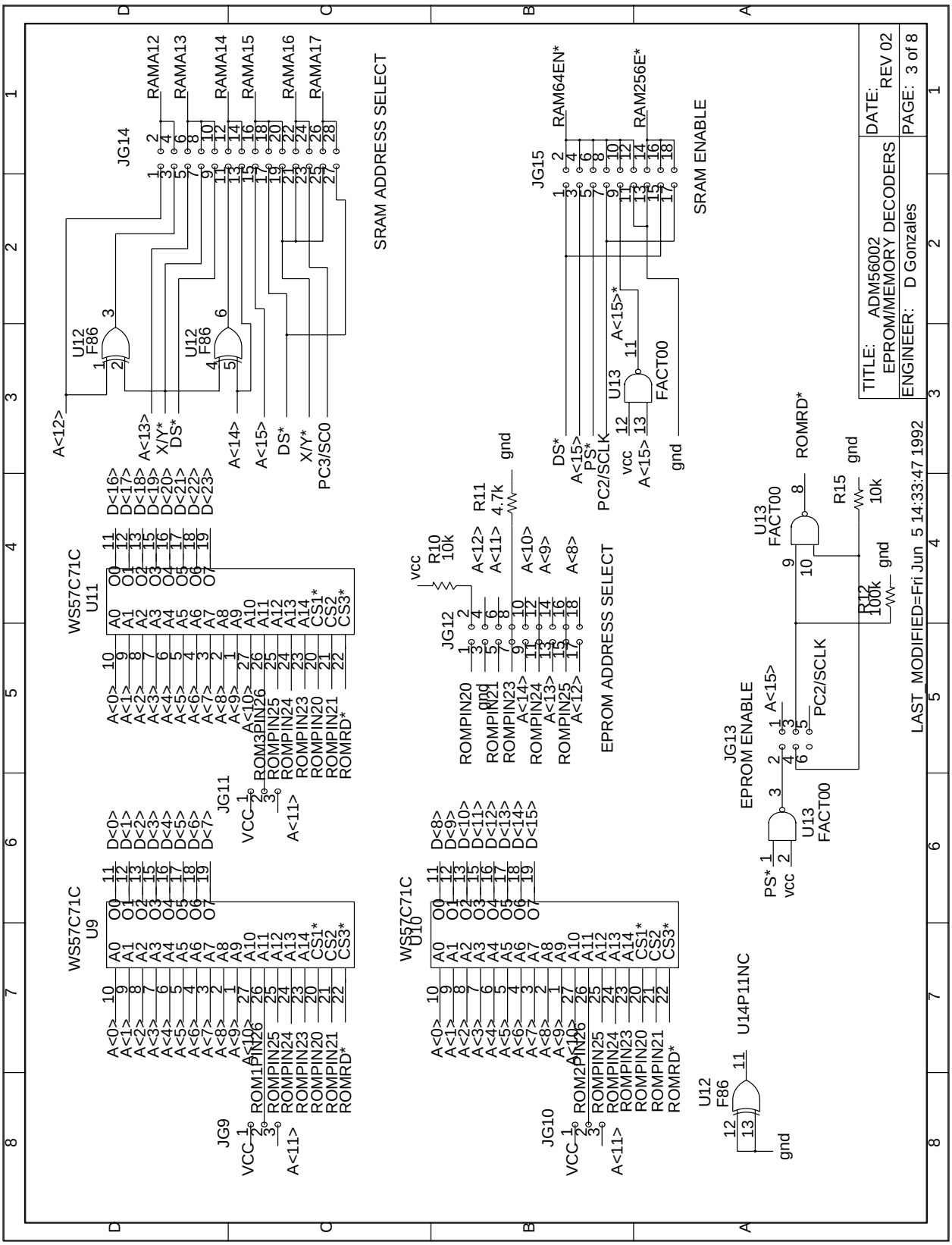
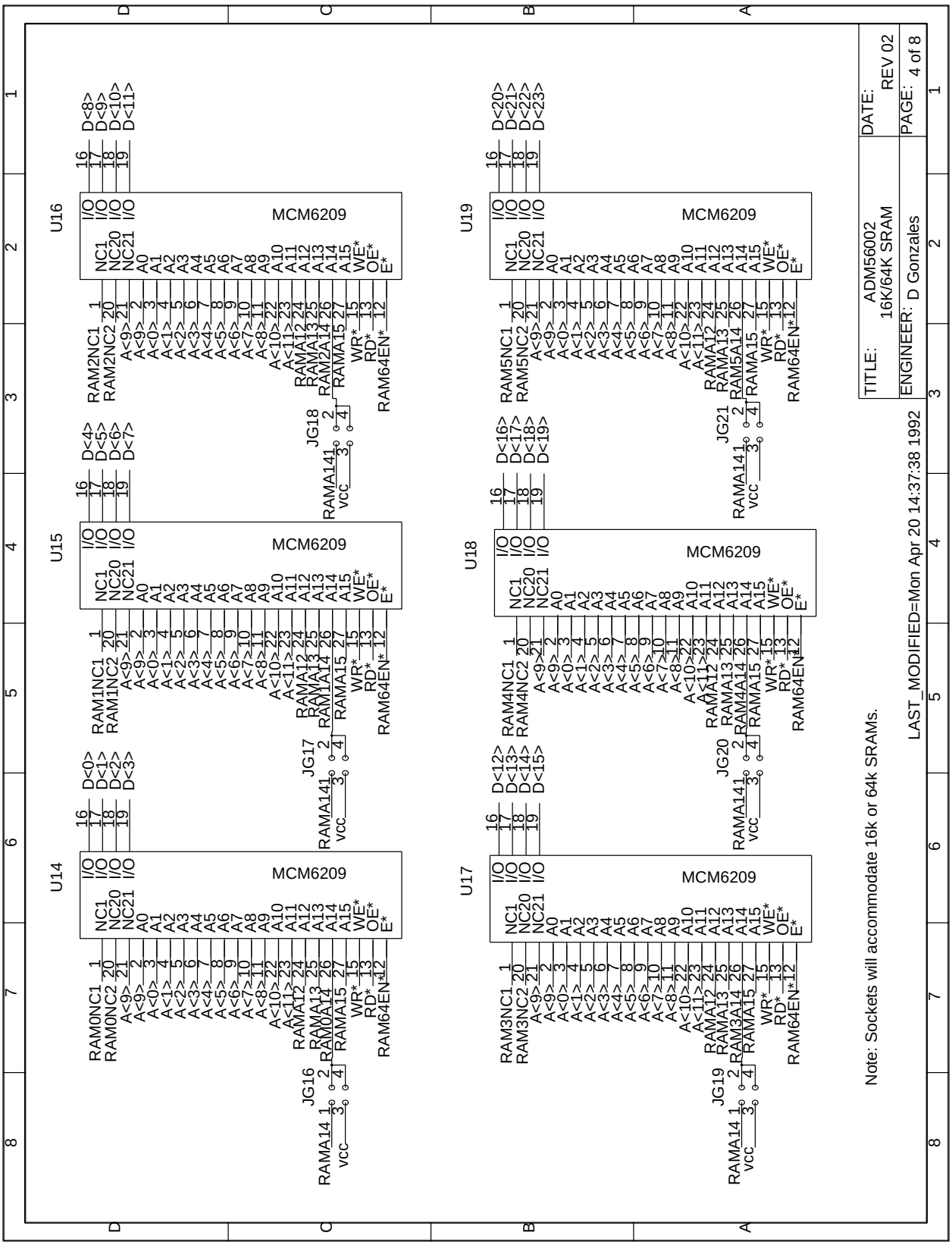
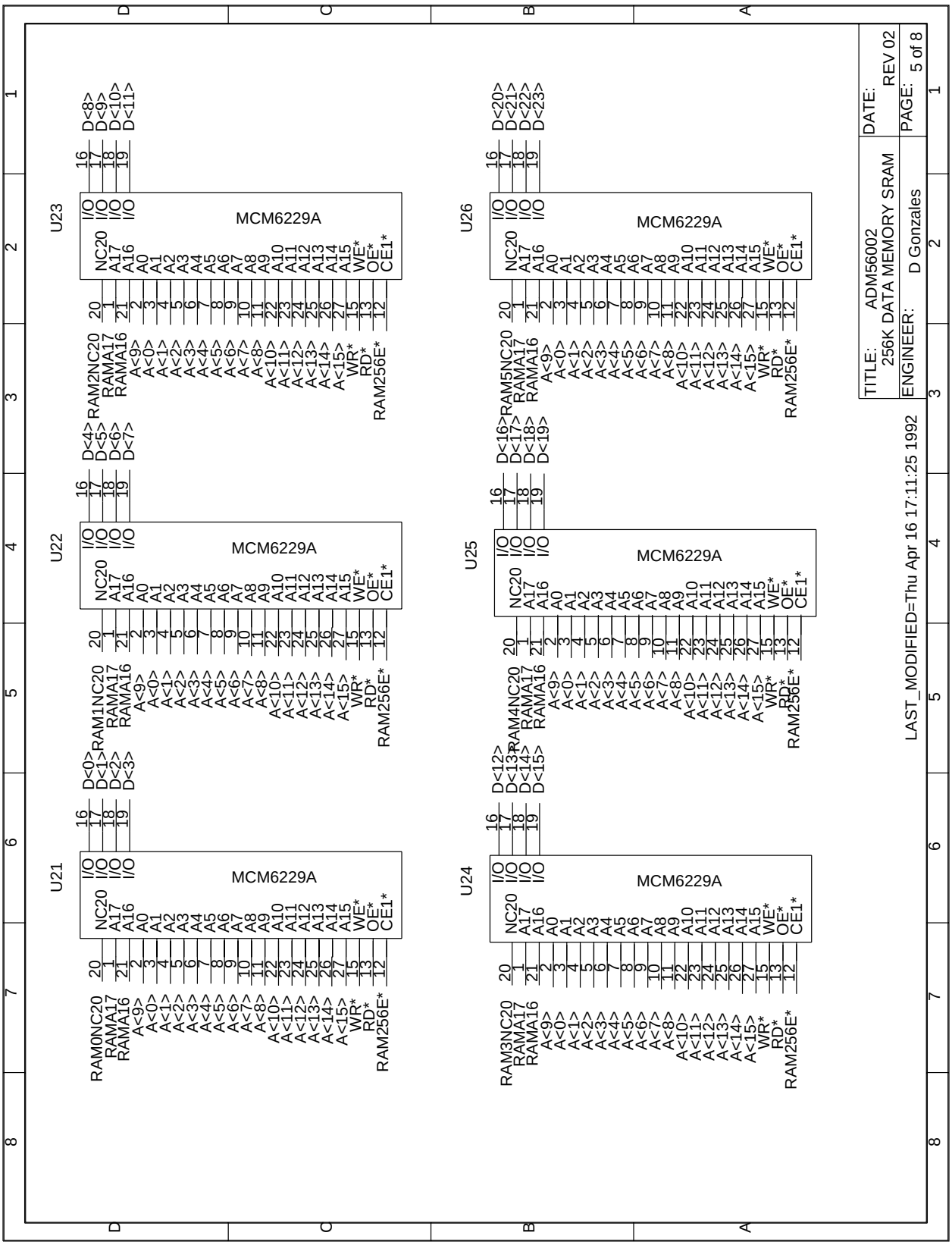
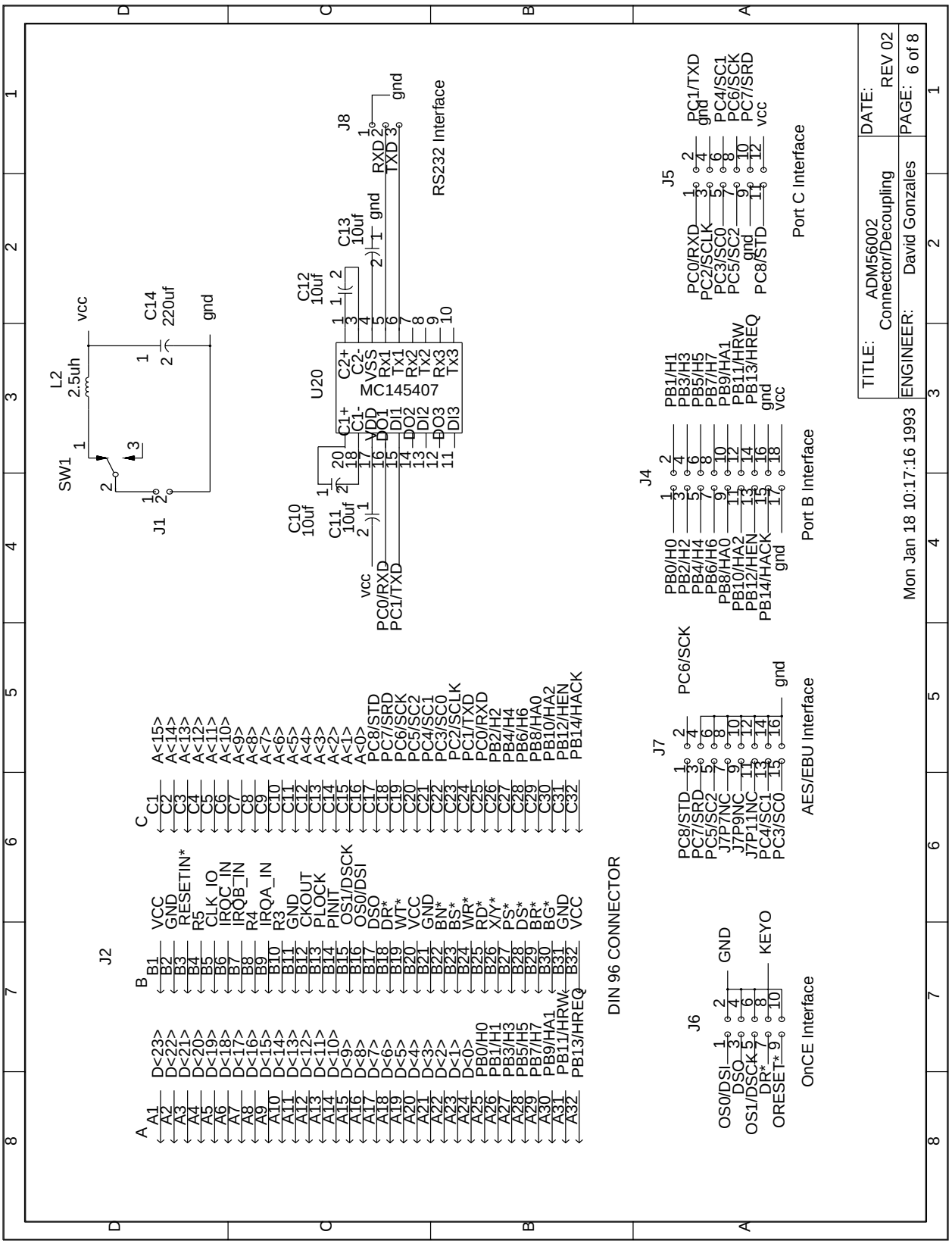
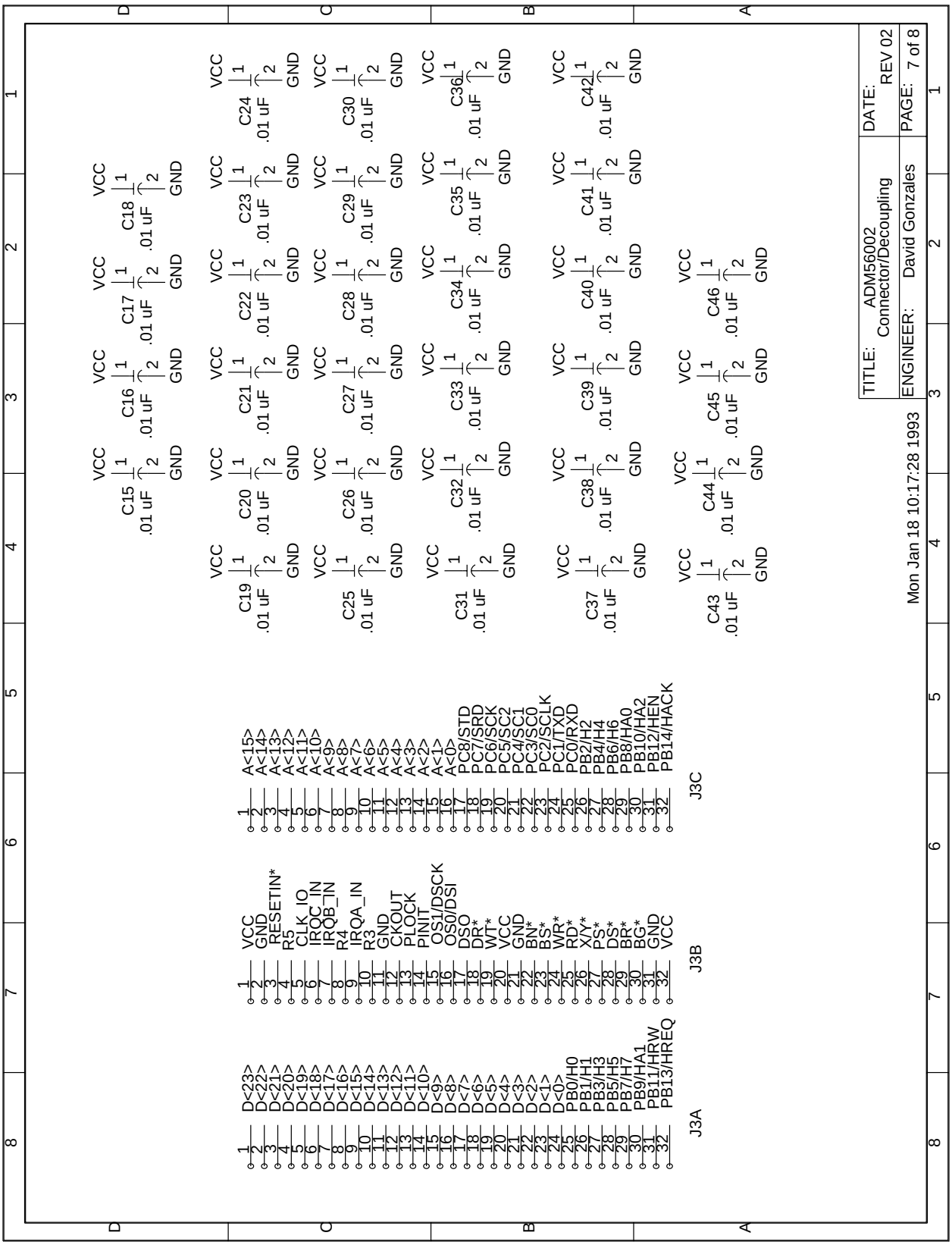
ORESET*
RST555*
RESET
MODA/IRQA*
MODB/IRQB*
MODC/NMI*
IRQA_IN
IRQB_IN
IRQC_IN
IRQA_SIG
IRQB_SIG
IRQC_SIG
JG2
JG3
JG4
JG5
JG6
JG7
JG8
U3
U4
U5
U6
U7
U8
MC1455
RST
CTL
OUT
THR
TRG
DIS
FACT00
FACT11
R3 1meg
R4 47k
R5 4.7k
R6 4.7k
R7 4.7k
R8 10K
R9 10k
C7 1.0uf
C8 .1uf
C9 .47uf
S1
vcc
gnd


SRAM ADDRESS SELECT
SRAM ENABLE
EPROM ADDRESS SELECT
EPROM ENABLE
WS57C71C
U9
U10
U11
JG9
JG10
JG11
JG12
JG13
JG14
JG15
U12
F86
U13
FACT00
U14P11NC
R10
10k
R11
4.7k
R12
100k
R15
10k
RAMA12
RAMA13
RAMA14
RAMA15
RAMA16
RAMA17
RAM64EN*
RAM256E*
ROMRD*
ROMPIN20
ROMPIN21
ROMPIN23
ROMPIN24
ROMPIN25
PC2/SCLK
PC3/SC0
TITLE: ADM56002
EPROM/MEMORY DECODERS
DATE: REV 02
ENGINEER: D Gonzales
PAGE: 3 of 8
LAST MODIFIED=Fri Jun 5 14:33:47 1992


U14
U15
U16
U17
U18
U19
MCM6209
RAM0NC1
RAM0NC2
RAM1NC1
RAM1NC2
RAM2NC1
RAM2NC2
RAM3NC1
RAM3NC2
RAM4NC1
RAM4NC2
RAM5NC1
RAM5NC2
JG16
JG17
JG18
JG19
JG20
JG21
RAMA14
RAMA13
RAMA12
RAMA15
RAMA141
RAM64EN*
TITLE: ADM56002 16K/64K SRAM
DATE: REV 02
ENGINEER: D Gonzales
PAGE: 4 of 8
LAST_MODIFIED=Mon Apr 20 14:37:38 1992
Note: Sockets will accommodate 16k or 64k SRAMs.


U21
MCM6229A
RAM0NC20
RAMA17
RAMA16
RAM256E*
U22
MCM6229A
RAM1NC20
RAMA17
RAMA16
RAM256E*
U23
MCM6229A
RAM2NC20
RAMA17
RAMA16
RAM256E*
U24
MCM6229A
RAM3NC20
RAMA17
RAMA16
RAM256E*
U25
MCM6229A
RAM4NC20
RAMA17
RAMA16
RAM256E*
U26
MCM6229A
RAM5NC20
RAMA17
RAMA16
RAM256E*
TITLE: ADM56002
256K DATA MEMORY SRAM
DATE: REV 02
ENGINEER: D Gonzales
PAGE: 5 of 8
LAST_MODIFIED=Thu Apr 16 17:11:25 1992


TITLE: ADM56002 Connector/Decoupling
DATE: REV 02
ENGINEER: David Gonzales
PAGE: 6 of 8
Mon Jan 18 10:17:16 1993
DIN 96 CONNECTOR
RS232 Interface
Port B Interface
Port C Interface
AES/EBU Interface
OnCE Interface
MC145407


J3A
D<23>
D<22>
D<21>
D<20>
D<19>
D<18>
D<17>
D<16>
D<15>
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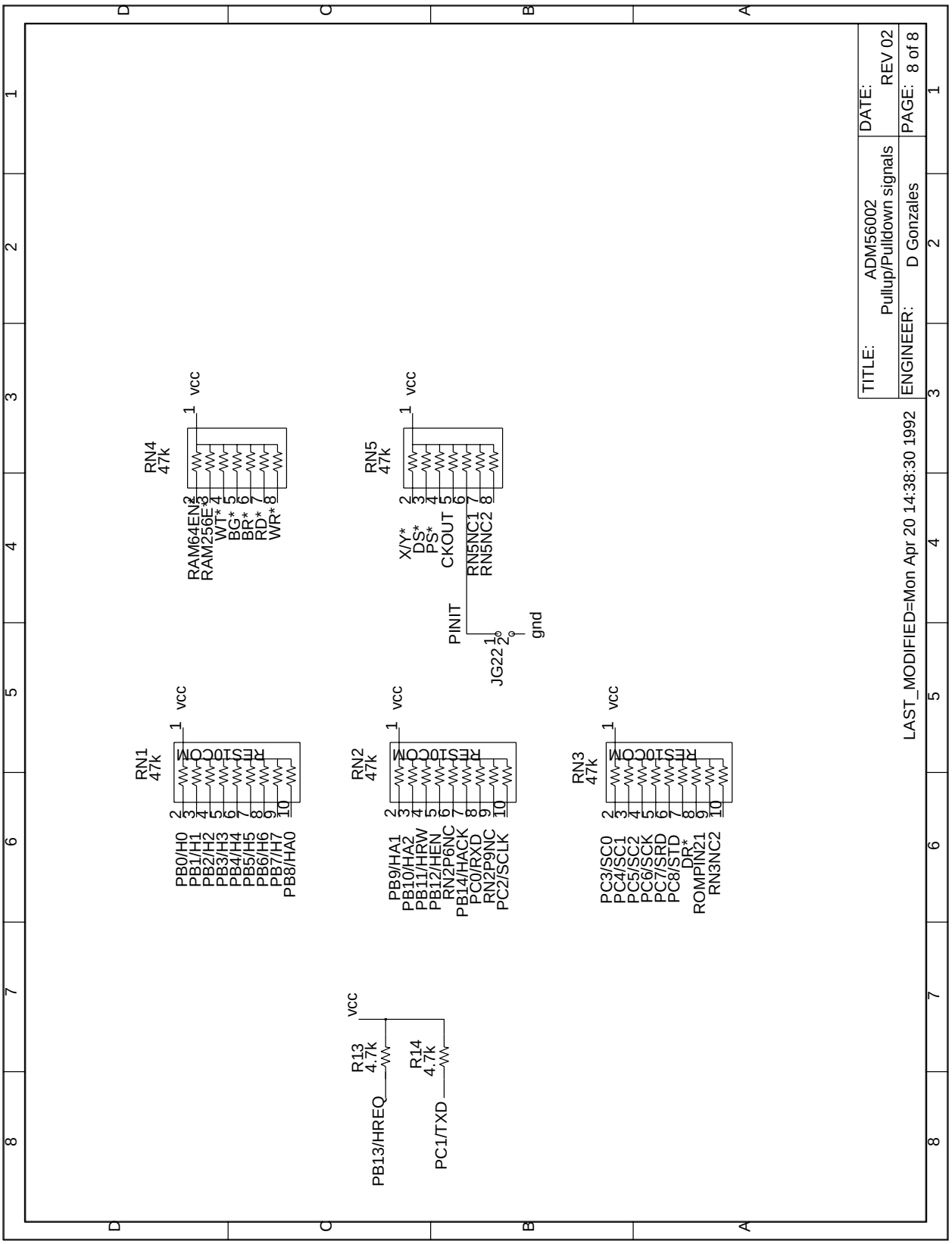
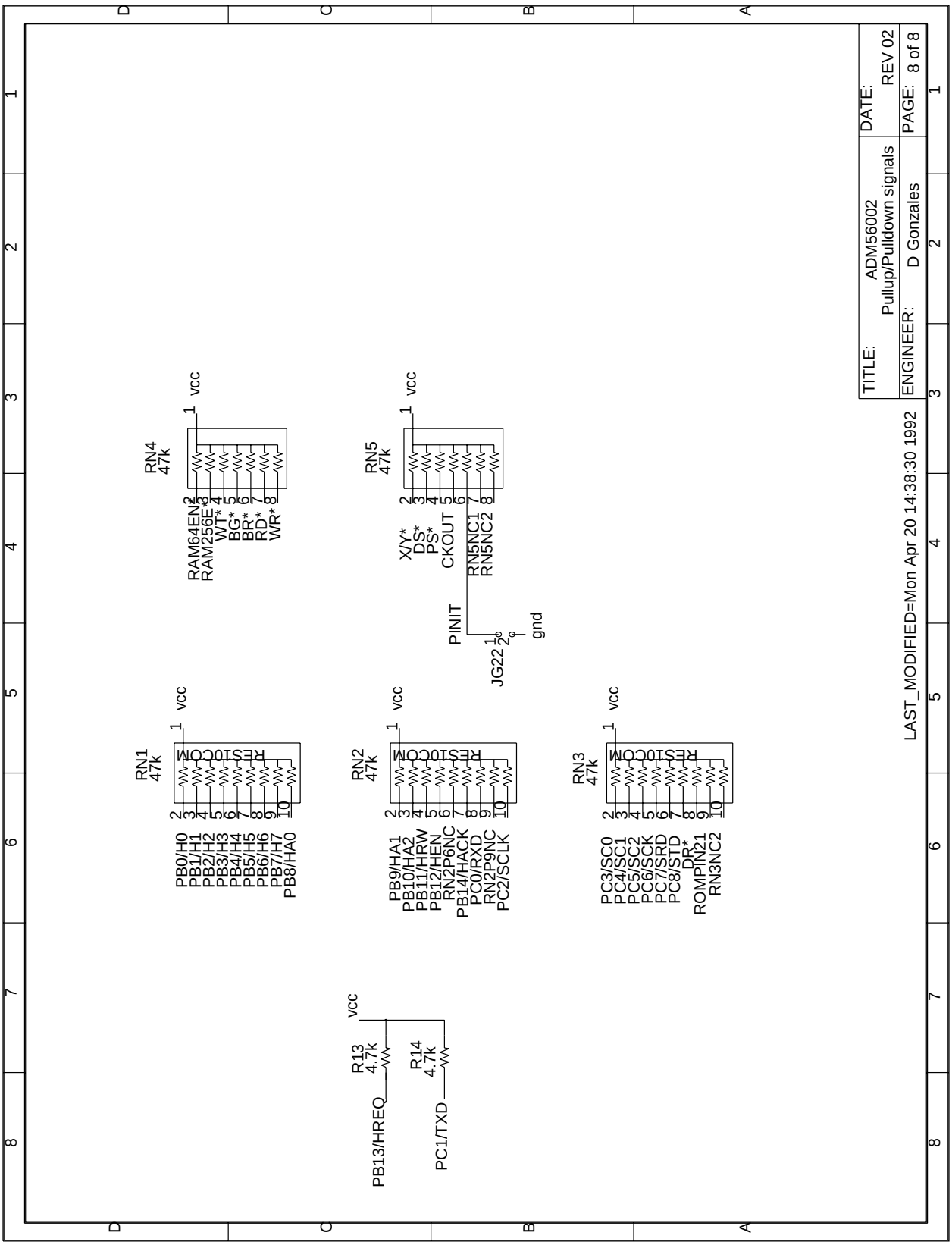
D<3>
D<2>
D<1>
D<0>
PB0/H0
PB1/H1
PB3/H3
PB5/H5
PB7/H7
PB9/HA1
PB11/HRW
PB13/HREQ
J3B
VCC
GND
RESETIN*
R5
CLK_IO
IRQC_IN
IRQB_IN
R4
IRQA_IN
R3
GND
CKOUT
PLOCK
PINIT
OS1/DSCK
OS0/DSI
DSO
DR*
WT*
VCC
GND
BN*
BS*
WR*
RD*
X/Y*
PS*
DS*
BR*
BG*
GND
VCC
J3C
A<15>
A<14>
A<13>
A<12>
A<11>
A<10>
A<9>
A<8>
A<7>
A<6>
A<5>
A<4>
A<3>
A<2>
A<1>
A<0>
PC8/STD
PC7/SRD
PC6/SCK
PC5/SC2
PC4/SC1
PC3/SC0
PC2/SCLK
PC1/TXD
PC0/RXD
PB2/H2
PB4/H4
PB6/H6
PB8/HA0
PB10/HA2
PB12/HEN
PB14/HACK
C15 .01 uF
C16 .01 uF
C17 .01 uF
C18 .01 uF
C19 .01 uF
C20 .01 uF
C21 .01 uF
C22 .01 uF
C23 .01 uF
C24 .01 uF
C25 .01 uF
C26 .01 uF
C27 .01 uF
C28 .01 uF
C29 .01 uF
C30 .01 uF
C31 .01 uF
C32 .01 uF
C33 .01 uF
C34 .01 uF
C35 .01 uF
C36 .01 uF
C37 .01 uF
C38 .01 uF
C39 .01 uF
C40 .01 uF
C41 .01 uF
C42 .01 uF
C43 .01 uF
C44 .01 uF
C45 .01 uF
C46 .01 uF
TITLE: ADM56002 Connector/Decoupling
DATE: REV 02
ENGINEER: David Gonzales
PAGE: 7 of 8
Mon Jan 18 10:17:28 1993


RN1
47k
vcc
PB0/H0
PB1/H1
PB2/H2
PB3/H3
PB4/H4
PB5/H5
PB6/H6
PB7/H7
PB8/HA0
RN2
47k
vcc
PB9/HA1
PB10/HA2
PB11/HRW
PB12/HEN
RN2P6NC
PB14/HACK
PC0/RXD
RN2P9NC
PC2/SCLK
RN3
47k
vcc
PC3/SC0
PC4/SC1
PC5/SC2
PC6/SCK
PC7/SRD
PC8/STD
DR*
ROMPIN21
RN3NC2
RN4
47k
vcc
RAM64EN*
RAM256E*
WT*
BG*
BR*
RD*
WR*
RN5
47k
vcc
X/Y*
DS*
PS*
CKOUT
RN5NC1
RN5NC2
PINIT
JG22
gnd
R13
4.7k
vcc
PB13/HREQ
R14
4.7k
PC1/TXD
TITLE: ADM56002 Pullup/Pulldown signals
DATE: REV 02
ENGINEER: D Gonzales
PAGE: 8 of 8
LAST_MODIFIED=Mon Apr 20 14:38:30 1992


TITLE: ADM56002 Pullup/Pulldown signals
DATE: REV 02
ENGINEER: D Gonzales
PAGE: 8 of 8
LAST_MODIFIED=Mon Apr 20 14:38:30 1992
RN1 47k
RN2 47k
RN3 47k
RN4 47k
RN5 47k
vcc
gnd
PB0/H0
PB1/H1
PB2/H2
PB3/H3
PB4/H4
PB5/H5
PB6/H6
PB7/H7
PB8/HA0
PB9/HA1
PB10/HA2
PB11/HRW
PB12/HEN
RN2P6NC
PB14/HACK
PC0/RXD
RN2P9NC
PC2/SCLK
PC3/SC0
PC4/SC1
PC5/SC2
PC6/SCK
PC7/SRD
PC8/STD
DR*
ROMPIN21
RN3NC2
RAM64EN*
RAM256E*
WT*
BG*
BR*
RD*
WR*
X/Y*
DS*
PS*
CKOUT
RN5NC1
RN5NC2
PINIT
JG22
R13 4.7k
R14 4.7k
PB13/HREQ
PC1/TXD

APPENDIX B

DSP56002ADM BILL OF MATERIALS

B.1 DSP56002ADM BILL OF MATERIAL

B.1.1 DSP56002 ADM—Electrical Parts List

The following DSP56002ADM electrical parts list is for Rev. 1.03 - 05-27-1992.

Table 2-13 DSP56002 ADM—Electrical Parts List

Qty	Description	Ref. Designators	Vendor Part #
1	DSP56002RC	U1	Motorola
1	MPA53-40mhz	U2	Conner Winfield
5	74FACT00	U3,6-8,13	Motorola
1	MC1455P1	U4	Motorola
1	74FACT11	U5	Motorola
3	WS57C291B-45T	U9-11	Waferscale Integration
1	74F86	U12	Motorola
6	MCM6290P15	U14-19	Motorola
1	MC14507P	U20	Motorola
1	330	R1	—
2	1 meg	R2,3	—
1	47 K	R4	—
5	4.7 K	R5-7,13,14	—
1	100k	R12	—
4	10k	R8-10	—
3	47 K	RN1-3	Bourne 4610X-101-RC
2	47 K	RN4-5	Bourne 4608X-101-RC
1	2.2uH	L1	Miller 9230-28
1	Ferrite Bead	L2	Miller FB73-226, two turns of 30ga.
1	20pf	C1	CDE EC200(JD)03

Table 2-13 DSP56002 ADM—Electrical Parts List

Qty	Description	Ref. Designators	Vendor Part #
1	15pf	C2	CDE CC150(JD)03
3	0.1uf	C3,4,8	Kemet C322C104M5R5CA
1	390pf	C5	CDE CDS-FY391(JGF)03
1	4.7pf	C6	Mallory VTH4R7M35
1	1.0uf	C7	Kemet C340C105M5R5CA
1	0.47uf	C9	Kemet C330C474M5R5CA
4	10uf	C10-13	Mallory VTH10M35
1	220uf	C14	Sprague 501D227M016MM
32	0.01uf	C15-46	Kemet C322C103M5R5CA
1	40 MHz crystal	Y1	International Crystal 471163

B.1.2 DSP56002 ADM—Hardware Parts List

The following DSP56002ADM hardware parts list is for Rev. 1.03 - 05-27-1992.

Table 2-14 DSP56002 ADM—Hardware Parts List

Qty	Description	Ref. Designators	Vendor Part #
1	2 row x 4 berg	JG1	R.N. NSH-08DB-S2-TG30
7	2 row x 2 berg	JG2,16-21	R.N. NSH-04DB-S2-TG30
9	1 row x 3 berg	JG3-11	R.N. NSH-03SB-S2-TG30
1	2 row x 9 berg	JG12	R.N. NSH-09DB-S2-TG30
1	2 row x 3 berg	JG13	R.N. NSH-06DB-S2-TG30
1	1 row x10 berg	JG14	R.N. NSH-10SB-S2-TG30
1	2 row x 6 berg	JG15	R.N. NSH-12DB-S2-TG30
1	1 row x 2 berg	JG22	R.N. NSH-02DB-S2-TG30
1	2 pos terminal blk	J1	Augat/RDI-MC6-P102-02
1	96 pos. VME (male)	J2	R.N. DIN96CPCSR1TR
3	1 row x 32 berg	J3A,B,C	R.N. NSH-32SB-S2-TG30
1	1 row x18 berg	J4	R.N. NSH-18SB-S2-TG30
1	1 row x12 berg	J5	R.N. NSH-12SB-S2-TG30
1	2 row x 5 berg	J6	R.N. NSH-10DB-S2-TG30
1	2 row x 8 berg	J7	R.N. NSH-08DB-S2-TG30
1	1 row x 3 berg	J8	R.N. NSH-03SB-S2-TG30
1	BNC vertical conn	BNC1	AMP 227699-3
1	13 x 13 PGA 144 pin	U1	R.N. PGA-144BH3-S-TG
1	14 pin(300mil) CLK	U4	R.N. ICT-143-SCO-TG30
9	28 pin(300mil) DIP	U9-11,14-19	R.N. ICT-283-S-TG
1	20 pin(300mil) DIP	U20	R.N. ICT-083-S-TG
1	SPST Moment Switch	S1	C&K 8125-S-D9-R2-BE

Table 2-14 DSP56002 ADM—Hardware Parts List

Qty	Description	Ref. Designators	Vendor Part #
1	SPST Toggle Switch	SW1	C&K 7101--S-D9-A2-BE
4	Rubber Feet		Amatom #5186