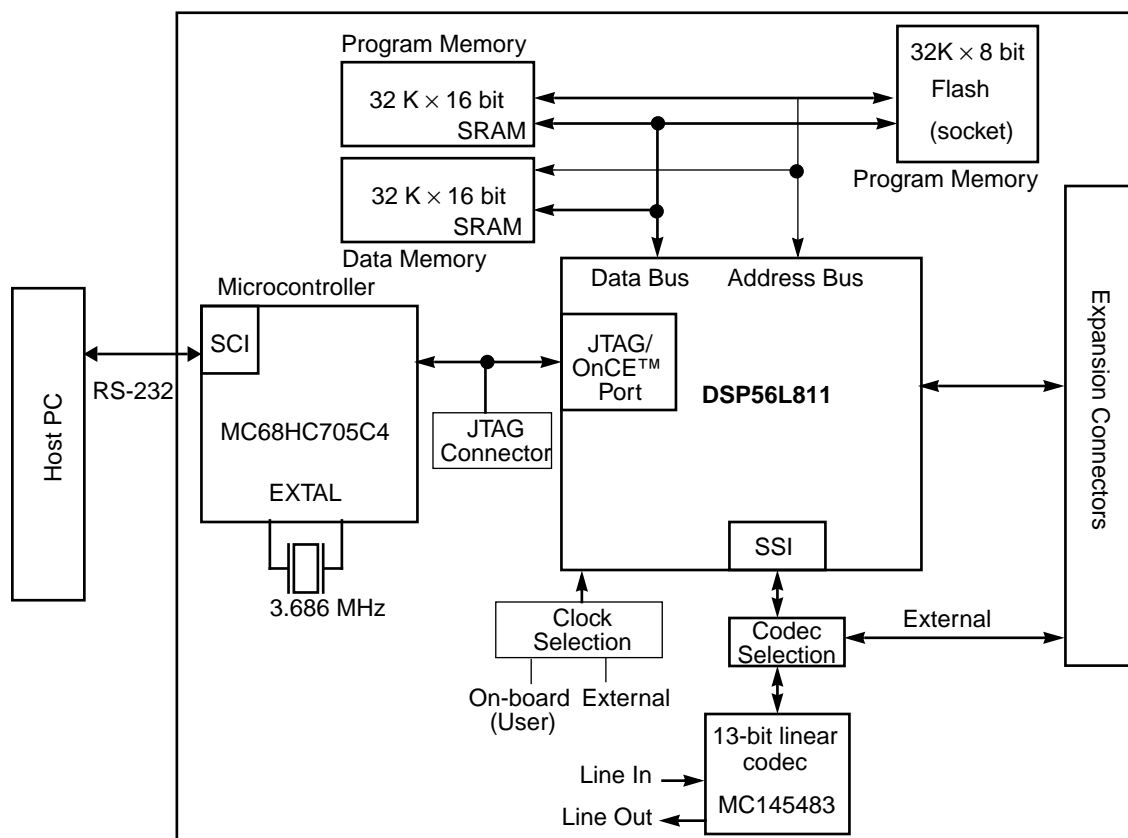


# DSP56L811EVM

## Advance Information DSP56L811 Evaluation Module

The DSP56L811 Evaluation Module (DSP56L811EVM) is designed as a low-cost platform for developing real-time software and hardware products to support a new generation of applications in digital messaging, two-way radio, speech processing, and consumer electronics. The user can download software to on-chip or on-board RAM, then run and debug it. The 16-bit precision of the DSP56L811 Digital Signal Processor (DSP) combined with the on-board 64 K × 16-bit external SRAM and Motorola's MC145483 13-bit linear voice audio codec makes the DSP56L811EVM ideal for developing and implementing many messaging and audio processing algorithms, as well as for learning the architecture and instruction set of the DSP56L811 processor. The user can connect hardware, such as external memories and other devices, such as A/D or D/A converters, keypads, displays, and so forth via the expansion connectors. **Figure 1** shows the functional block diagram for the DSP56L811EVM.



**Figure 1** DSP56L811EVM Functional Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Preliminary Information

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## Features

### Hardware

- 16-bit DSP56L811 Digital Signal Processor
  - DSP56800 core
    - Efficient 16-bit fixed point DSP56800 family DSP engine
    - Up to 20 Million Instructions Per Second (MIPS) at 40 MHz
    - Single-cycle 16 x 16-bit parallel Multiplier-Accumulator
    - Two 36-bit accumulators including extension bits
    - 16-bit bidirectional barrel shifter
    - Parallel instruction set with unique DSP addressing modes
    - Hardware DO and REP loops
    - DO loops nestable in software
    - Address buses:
      - One 16-bit internal memory address bus (XAB1)
      - One 16-bit internal memory address bus (XAB2)
      - One 19-bit internal program address bus
      - One 16-bit external address bus
    - Data buses:
      - One 16-bit bidirectional internal memory data bus (CGDB)
      - One 16-bit unidirectional internal memory data bus (XDB2)
      - One 16-bit bidirectional dedicated Peripheral Data Bus (PGDB)
      - One 16-bit bidirectional internal Program Data Bus (PDB)
      - One 16-bit bidirectional external data bus (EDB)
    - Instruction set supports both DSP and controller functions
    - Controller style addressing modes and instructions for compact code
    - Efficient C Compiler and local variable support
    - Software subroutine and interrupt stack with unlimited depth

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- On-Chip Memories
    - On-chip Harvard architecture permits up to three simultaneous accesses to program and data memory
    - 1 K × 16 Program RAM
    - 64 × 16 bootstrap ROM
    - 2 K × 16 X-data RAM
    - Programs can run out of X-data RAM
  - Peripheral and Support Circuits
    - External Memory Interface (EMI)
    - Sixteen dedicated General Purpose Input/Output (GPIO) pins (eight pins programmable as interrupts)
    - Serial Peripheral Interface (SPI) support: Two configurable 4-pin ports (SPI0 and SPI1) (or eight additional GPIO lines)
      - Supports LCD drivers, A/D subsystems, and MCU systems
      - Supports inter-processor communications in a multiple master system
      - Demand-driven master or slave devices with high data rates
    - Synchronous Serial Interface (SSI) support: One 6-pin port (or six additional GPIO lines)
      - Supports serial devices with one or more industry-standard codecs, other DSPs, microprocessors, and Motorola SPI-compliant peripherals
      - Asynchronous or synchronous transmit and receive sections with separate or shared internal/external clocks and frame syncs
      - Network mode using frame sync and up to 32 time slots
      - 8-bit, 10-bit, 12-bit, and 16-bit data word lengths
    - Three programmable 16-bit timers (accessed using two I/O pins that can also be programmed as two additional GPIO lines)
    - Computer-Operating Properly (COP) and Real-Time Interrupt (RTI) timers
    - Two external interrupt/mode control pins
    - One external reset pin for hardware reset
    - JTAG/On-Chip Emulation (OnCE) 5-pin port for unobtrusive, processor speed-independent debugging
    - Software-programmable, Phase Lock Loop-based (PLL) frequency synthesizer for the DSP core clock

### Preliminary Information

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- Energy Efficient Design
    - Power-saving wait and multiple Stop modes available
    - Fully static, HCMOS design for 40 MHz to DC operating frequencies
    - 100-pin plastic Thin Quad Flat Pack (TQFP) surface-mount package
    - 2.7 V–3.6 V power supply
  - 32 K × 16-bit Fast Static RAM for expansion program memory
  - 32 K × 16-bit Fast Static RAM for expansion data memory
  - 13-bit linear audio codec
  - Command Converter
    - Motorola MC68HC705C4 for high-speed JTAG/OnCE command conversion
    - JTAG connector for use with the Application Development System (ADS) command converter card
  - Connectors
    - RS-232 serial interface with local microcontroller support for JTAG/OnCE port
    - Two 70-pin connectors that allow access to all DSP56L811 pins

## Software

- Motorola's DSP56xxx cross assembler
  - Produces DSP56L811 binary code from source code using labels, sections, and macro definitions incorporating the DSP's complete instruction set, all addressing modes, and all memory spaces
  - Offers macros, expression evaluation, and functions for strings, data conversion, and transcendentals
  - Creates reports for cross-references, instruction cycle count, and memory usage
  - Provides extensive error checking and reporting
- Domain Technologies debug software with Windows-based user interface
  - Symbolic debugging
  - Windows for data, code, DSP registers, commands, peripherals, etc.
  - Data and registers displayed in fractional, decimal, or hexadecimal format
  - Graphical display of memory segments
  - Up to eight simultaneous software breakpoints
  - Built-in-line assembler and disassembler

### Preliminary Information

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## User Requirements

The user must provide the following:

- Power supply (9–12 V DC, 500 mA with 2.5 mm coaxial connector)
- RS-232 cable (DB9 plug to DB9 receptacle)
- Audio source and a cable with 1/8-inch stereo plugs
- IBM PC compatible computer (386 class or higher) running Windows 3.1 (or higher) with an RS-232 serial port capable of 9,600–56,600 bit-per-second operation, 4 Mbytes RAM, 3-1/2 inch diskette drive, CD-ROM drive, hard drive with 4 Mbyte of free disk space, and a mouse

## Supporting Documentation

The first three documents listed in **Table 1** are required for a complete description of the DSP56L811 and are necessary to design properly with the part. The fourth and fifth documents provide a description of the DSP56L811EVM, including installation and use. These documents are provided with the DSP56L811EVM. Additional copies are available from one of the following locations (see back cover for detailed information):

- A local Motorola distributor
- A Motorola semiconductor sales office
- A Motorola Literature Distribution Center
- The World Wide Web (WWW)

The DSP56L811EVM can be ordered by the number listed below from your Motorola distributor or semiconductor sales office.

**Table 1** Documentation List

| Document Name            | Description  | Order Number   |
|--------------------------|--|----------------|
| DSP56800 Family Manual   | Detailed description of the DSP56800 family processor core and instruction set                             | DSP56800FM/AD  |
| DSP56L811 User's Manual  | Detailed functional description of the DSP56L811 memory configuration, operation, and register programming | DSP56L811UM/AD |
| DSP56L811 Technical Data | DSP56L811 features list and physical, electrical, timing, and package specifications                       | DSP56L811/D    |


## Preliminary Information

**Table 1** Documentation List

| Document Name                    | Description   | Order Number     |
|----------------------------------|---|------------------|
| DSP56L811EVM Product Information | Overview description of the DSP56L811EVM, including block diagram and list of features                                      | DSP56L811EVMP/D  |
| DSP56L811EVM User's Manual       | Detailed functional description of the DSP56L811EVM, including requirements, installation, and general operating guidelines | DSP56L811EMUM/AD |
| DSP56L811EVM                     | DSP56L811 Evaluation Module kit with hardware, software, and documentation  | DSP56L811EVM     |

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