# DSP56824

*Advance Information*

## 16-BIT DIGITAL SIGNAL PROCESSOR

The DSP56824 is a member of the DSP56800 core-based family of Digital Signal Processors (DSPs). This general purpose DSP combines processing power with configuration flexibility, making it an excellent cost-effective solution for signal processing and control functions. Because of its low cost, configuration flexibility, and compact program code, the DSP56824 is well-suited for cost-sensitive applications, such as digital wireless messaging, servo and motor control, digital answering machines / feature phones, modems, and digital cameras. The DSP56800 core consists of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The MPU-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C Compilers. The DSP56824 supports program execution from either internal or external memories. Two data operands can be accessed from the on-chip data RAM per instruction cycle. The rich set of programmable peripherals and ports provides support for interfacing multiple external devices, such as codecs, microprocessors, or other DSPs. The DSP56824 also provides two external dedicated interrupt lines and sixteen to thirty-two General Purpose Input / Output (GPIO) lines, depending on peripheral configuration (see **Figure 1**).

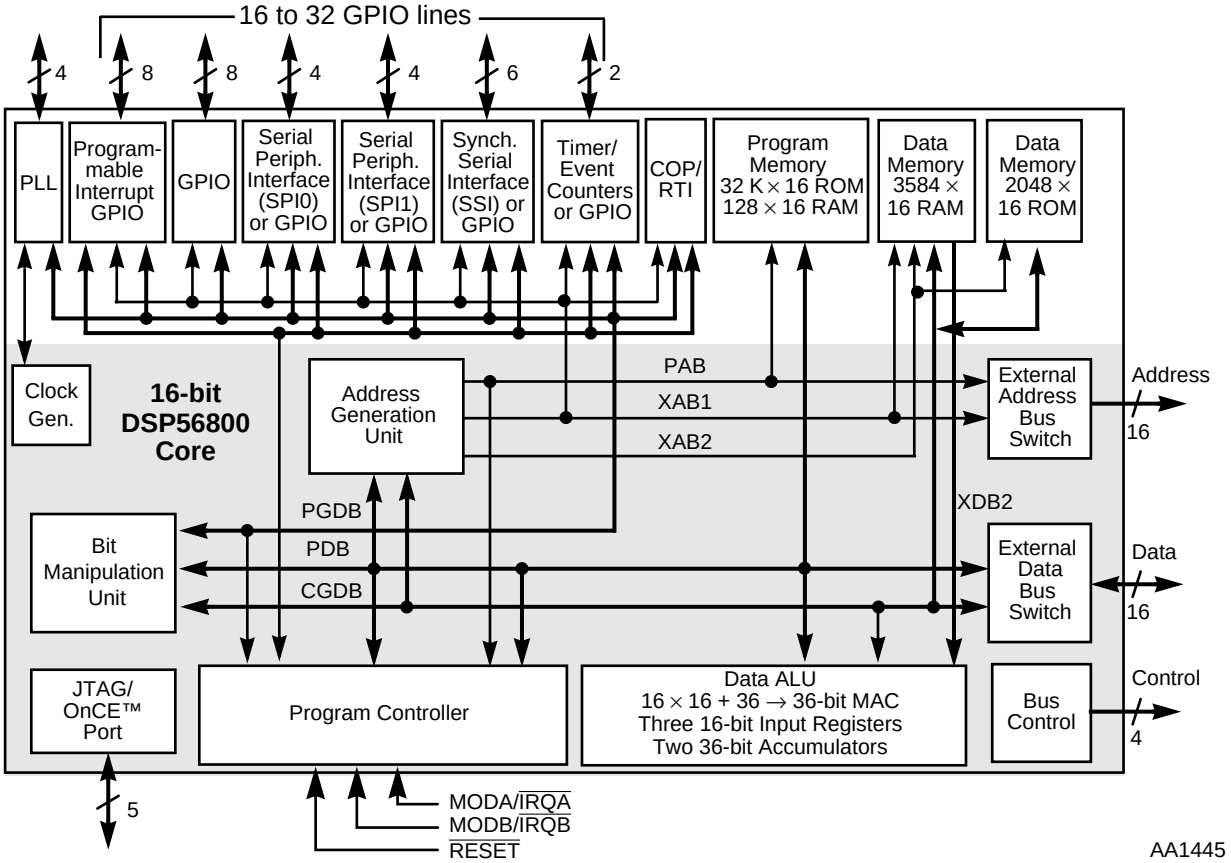


**Figure 1** DSP56824 Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

# DSP56824 FEATURES

## Digital Signal Processing Core

- Efficient 16-bit DSP56800 family DSP engine
- As many as 35 Million Instructions Per Second (MIPS) at 70 MHz
- Single-cycle 16 × 16-bit parallel Multiplier-Accumulator (MAC)
- Two 36-bit accumulators including extension bits
- 16-bit bidirectional barrel shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three internal address buses and one external address bus
- Four internal data buses and one external data bus
- Instruction set supports both DSP and controller functions
- Controller style addressing modes and instructions for compact code
- Efficient C Compiler and local variable support
- Software subroutine and interrupt stack with unlimited depth

## Memory

- On-chip Harvard architecture permits as many as three simultaneous accesses to program and data memory
- On-chip memory
  - 32 K × 16 Program ROM
  - 128 × 16 Program RAM
  - 3.5 K × 16 X RAM usable for both data and programs
  - 2 K × 16 X data ROM
- Off-chip memory expansion capabilities
  - As much as 64 K × 16 X data memory
  - As much as 64 K × 16 program memory
  - External memory expansion port programmable for 1 to 15 wait states
- Programs can run out of X data RAM

## Peripheral Circuits

- External Memory Interface (Port A)
- Sixteen dedicated GPIO pins (eight pins programmable as interrupts)
- Serial Peripheral Interface (SPI) support: Two configurable four-pin ports (SPI0 and SPI1) (or eight additional GPIO lines)
  - Supports LCD drivers, A / D subsystems, and MCU systems
  - Supports inter-processor communications in a multiple master system
  - Supports demand-driven master or slave devices with high data rates
- Synchronous Serial Interface (SSI) support: One 6-pin port (or six additional GPIO lines)
  - Supports serial devices with one or more industry-standard codecs, other DSPs, microprocessors, and Motorola SPI-compliant peripherals
  - Allows implementing synchronous or synchronous transmit and receive sections with separate or shared internal / external clocks and frame syncs
  - Supports Network mode using frame sync and as many as 32 time slots
  - Can be configured for 8-bit, 10-bit, 12-bit, and 16-bit data word lengths
- Three programmable 16-bit timers (accessed using two I / O pins that can also be programmed as two additional GPIO lines)
- Computer-Operating Properly (COP) and Real-Time Interrupt (RTI) timers
- Two external interrupt / mode control pins
- One external reset pin for hardware reset
- JTAG / On-Chip Emulation (OnCE™) 5-pin port for unobtrusive, processor speed-independent debugging
- Extended debug capability with second breakpoint and 8-level OnCE FIFO history buffer
- Software-programmable, Phase Lock Loop-based (PLL-based) frequency synthesizer for the DSP core clock

## Energy Efficient Design

- A single 2.7–3.6 V power supply
- Power-saving Wait and multiple Stop modes available
- Fully static, HCMOS design for 70 MHz to dc operating frequencies
- Available in plastic 100-pin Thin Quad Flat Pack (TQFP) surface-mount package

## PRODUCT DOCUMENTATION

The three documents listed in **Table 1** are required for a complete description of the DSP56824 and are necessary to design properly with the part. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or through the Motorola DSP home page on the Internet (the source for the latest information).

**Table 1** DSP56824 Chip Documentation

| Topic | Description | Order Number |
|---|---|---|
| DSP56800 Family Manual | Detailed description of the DSP56800 family architecture, and 16-bit DSP core processor and the instruction set | DSP56800FM/AD |
| DSP56824 User's Manual | Detailed description of memory, peripherals, and interfaces of the DSP56824 | DSP56824UM/AD |
| DSP56824 Technical Data Sheet | Electrical and timing specifications, pin descriptions, and package descriptions | DSP56824/D |



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