MOTOROLA

TECHNICAL BULLETIN

DSP56800 Family Digital Signal Processors

Comparison of Features

March 16, 1998

This short Technical Bulletin summarizes the differences in features for the current members of the DSP56800 family of Digital Signal Processors (DSPs) as of the date of publication. Complete information on these DSPs is available in the following documents:

- DSP56800 Family
  - DSP56800 Family Manual (DSP56800FM/AD)
- DSP56L811
  - DSP56L811 User's Manual (DSP56L811UM/AD)
  - DSP56L811 Technical Data (DSP56L811/D)
  - DSP56L811 Technical Bulletin
- DSP56LF812
  - DSP56LF812 User's Manual (DSP56LF812UM/AD)
  - DSP56LF812 Technical Data (DSP56LF812/D)
  - DSP56LF812 Chip Errata
- DSP56824
  - DSP56824 User's Manual (DSP56824UM/AD)
  - DSP56824 Technical Data (DSP56824/D)
  - DSP56824 Chip Errata

The difference tables reference these documents in the following fashion: "Technical Bulletin" always refers to the DSP56L811 Technical Bulletin. References to all other documents refer to the applicable User's Manual or Data Sheet for the chip listed in the column in the difference table. Applicable Technical Bulletins and Chip Errata are available on the World Wide Web (WWW) at:

http://www.motorola-dsp.com

Table 1 lists the functional differences provided in this document:

Table 1: Functional Differences

Difference Summary	Table
Feature Differences	Table 2
Electrical Changes	Table 3
Core Instructions Differences	Table 4
Peripheral Differences	Table 5
Debug Instruction Differences	Table 6

FEATURE DIFFERENCES

The feature differences listed in **Table 2** exist for the current members of the DSP56800 family.

Table 2: Feature Differences

Feature	DSP56L811	DSP56LF812	DSP56824
Program RAM	1K	—	128
Program ROM	—	—	32K
Program Flash	—	24K	—
X Data RAM	2K	2K	3.5K
X Data ROM	—	—	2K
X Data Flash	—	2K[1]	—
SSI[2]	—	Enhanced	Enhanced
FIFO	—	Added	Added
PLL VCO select	—	N/A	Added[3]
Second debug breakpoint	—	Enhanced	Enhanced
Positive edge-triggered IRQs	—	—	Added
Size (S) bit	—	Added	Added
Maximum core frequency	40 MHz (20 MIPS)	40 MHz (20 MIPS)	70 MHz (35 MIPS)
Typical power	1.1 ma/MIPS	1.1 ma/MIPS	0.55 ma/MIPS

Notes:

1. On the DP56LF812, the X Flash memory occupies the X memory map in the locations from X:$0800 to X:$0FFF. Writes to these locations in X memory should be avoided, since these writes will wrap to the locations X:$0000 to X:$07FF. For example, the following instructions produce identical results.

```
move #0,x:$0000
move #0,x:$0800
```

2. The SSI on the DSP56LF812 and DSP56824 has been enhanced to completely decouple the frame synchronization and clocking protocols of the receive and transmit sections of the peripheral. This was accomplished by adding five new control bits to the SSI Status Register (SSR) of the DSP56L811. This register is renamed the SSI Status/Control Register (SCSR) for the DSP56LF812 and DSP56824. The address of the SSI Time Slot Register (STSR) is changed for the DSP56LF812 and DSP56824 to accomodate this enhancement. Note that the SSI setup for ths DSP56LF812 and DSP56824 must be slightly modified from what was used on a DSP56L811. See the SSI section of the appropriate user's manual for more details on this enhancement.
3. The PLL on the DSP56824 has been enhanced to support frequencies as high as 70 MHz, requiring a new control bit, the VCO Curve Select 0 (VCS0) bit (Bit 3), in the PLL Control Register 1 (PCR1) to set a high (45–70 MHz) or low (10–45 MHz) frequency range in the PLL. Note that for designs transitioning from the DSP56L811 or DSP56LF812, this bit needs to be set for PLL output frequencies less than 45 MHz, where it was previously a reserved bit that was cleared on reset. See the PLL section of the DSP56824 User's Manual (DSP56824UM/AD) for more details on this enhancement.

ELECTRICAL DIFFERENCES

The electrical differences provided in **Table 3** exist for the current members of the DSP56800 family.

Table 3: Electrical Changes

Electrical Change	DSP56L811	DSP56LF812	DSP56824
Clock oscillator amplifier enhanced	See Data Sheet	See Data Sheet	See Data Sheet
Asserting $\overline{\text{TRST}}$ with RESET	See Technical Bulletin	See User's Manual	See User's Manual
External oscillator start-up time	See Technical Bulletin	No longer specified	No longer specified
PLL circuitry values	See Technical Bulletin	See Data Sheet	See Data Sheet

CORE INSTRUCTION DIFFERENCES

The core instruction differences listed in **Table 4** exist for the current members of the DSP56800 family.

Table 4: Core Instructions Differences

Core Instructions	DSP56L811	DSP56LF812	DSP56824
Instruction fetch from X memory	See Technical Bulletin	Fixed	Fixed
Data ALU instructions with accumulator as destination	See Technical Bulletin	Fixed	Fixed
MOVEs from an accumulator	See Technical Bulletin	See Technical Bulletin	See Technical Bulletin
Pipeline stalls in DO loops	See Technical Bulletin	See Technical Bulletin	See Technical Bulletin
Saturation mode	See Technical Bulletin	See Technical Bulletin	See Technical Bulletin
LEA instruction enhancements	See Technical Bulletin	See Technical Bulletin	See Technical Bulletin
REP instruction restrictions	See Technical Bulletin	See Technical Bulletin	See Technical Bulletin
Pipeline dependency on Stack Pointer (SP)	See Technical Bulletin	See Technical Bulletin	See Technical Bulletin
Hardware stack overflow enhancement	See Technical Bulletin	See Technical Bulletin	See Technical Bulletin
Carry (C) bit update	See Technical Bulletin	See Technical Bulletin	See Technical Bulletin

Table 4: Core Instructions Differences (Continued)

Core Instructions	DSP56L811	DSP56LF812	DSP56824
P-Fetch breakpoint limitation	See Technical Bulletin	See Technical Bulletin	See Technical Bulletin
LSLL instruction	See Technical Bulletin	See Technical Bulletin	See Technical Bulletin
COP reset restriction	See Technical Bulletin	N/A	Fixed
CMP instruction	See Technical Bulletin	See Technical Bulletin	Fixed
IRQA and Port B interrupts and Wait mode	See Technical Bulletin	See Technical Bulletin	Fixed
Premature exit from nested DO loops	See Technical Bulletin	See Technical Bulletin	Fixed
Prescalar clock at CLKO	See Technical Bulletin	See Technical Bulletin	See Technical Bulletin

PERIPHERAL DIFFERENCES

The on-chip peripheral differences listed in **Table 5** exist for the current members of the DSP56800 family.

Table 5: Peripheral Differences

Peripheral Difference	DSP56L811	DSP56LF812	DSP56824
SSI write/read requires instruction delay	Problem	Fixed	Fixed
TDBE and TDE flags do not change state	Problem	Fixed	Fixed
TDE flag cleared incorrectly	Problem	Fixed	Fixed
TDBE flag cleared incorrectly	Problem	Fixed	Fixed
New reset value for PCR1 register	See Technical Bulletin	See Technical Bulletin	See Technical Bulletin
General-purpose timers do not work if using external memory with wait states	Problem	Problem	Fixed

DEBUG INSTRUCTION DIFFERENCES

The debug instruction differences listed in **Table 6** exist for the current members of the DSP56800 family.

Table 6: Debug Instruction Differences

Debug Instruction Differences	DSP56L811	DSP56LF812	DSP56824
Interrupt processing in Debug Mode	Problem	Fixed	Fixed
Single stepping of ADD a,x:<aa> and ADD a,x:(sp-xx) instructions	Problem	Fixed	Fixed
Shift-type instruction operation	Problem	Fixed	Fixed
Boundary Scan Access	Problem	Fixed	Fixed

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