DSP56011

Advance Information
24-BIT DVD DIGITAL SIGNAL PROCESSOR

Motorola developed the DSP56011 as a high-performance programmable Digital Signal Processor (DSP) for Digital Versatile Disc (DVD), High-Definition Television (HDTV), and Advanced Set-top audio decoding. The DSP56011 is optimized with audio-specific peripherals and customized memory configuration, and may be programmed with Motorola's certified software for Dolby AC-3 5.1 Channel Surround, Dolby Pro Logic, and MPEG1 Layer 2. These applications use Motorola's 24-bit DSP56000 architecture and are the highest quality solutions available. Flexible peripheral modules and interface software allow simple connection to a wide variety of video / system decoders. In addition, the DSP56011 offers switchable memory space configuration, a large user-definable Program ROM and two independent data RAMs and ROMs, a Serial Audio Interface (SAI), Serial Host Interface (SHI), Parallel Host Interface (HI) with Direct Memory Access (DMA) for communicating with other processors, dedicated I / O lines, on-chip Phase Lock Loop (PLL), On-Chip Emulation (OnCE™) port, and on-chip Digital Audio Transmitter (DAX). **Figure 1** shows the functional blocks of the DSP56011.

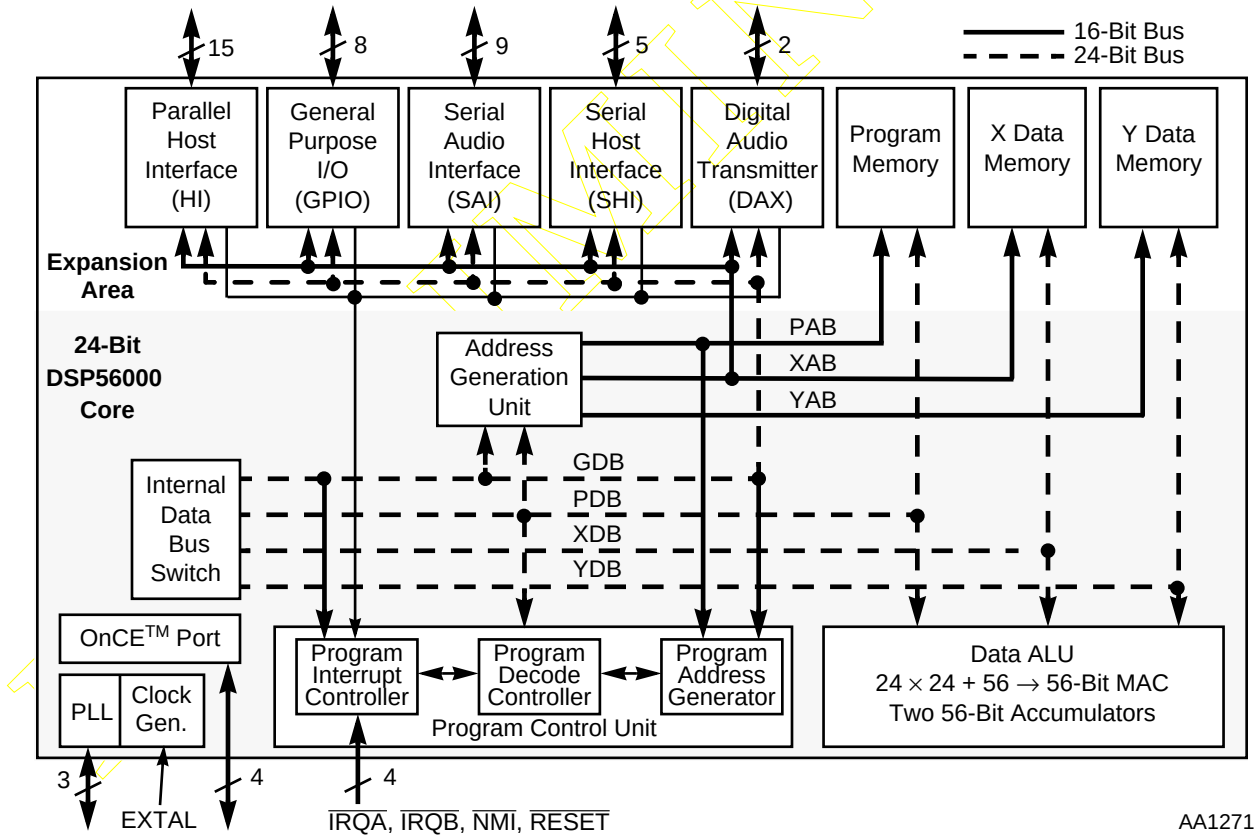

Figure 1 DSP56011 Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Preliminary Information

MOTOROLA

FEATURES

Digital Signal Processing Core

- Efficient, object-code compatible, 24-bit DSP56000 family DSP engine
- 47.5 Million Instructions Per Second (MIPS) with 21.05 ns instruction cycle at 95 MHz
- Highly parallel instruction set with unique DSP addressing modes
- Two 56-bit accumulators including extension byte
- Parallel 24 × 24-bit multiply-accumulate in 1 instruction cycle (2 clock cycles)
- Double precision 48 × 48-bit multiply with 96-bit result in 6 instruction cycles
- 56-bit addition / subtraction in 1 instruction cycle
- Fractional and integer arithmetic with support for multi-precision arithmetic
- Hardware support for block-floating point Fast Fourier Transforms (FFT)
- Hardware nested DO loops
- Zero-overhead fast interrupts (2 instruction cycles)
- PLL-based clocking with a wide range of frequency multiplications (1 to 4096) and power saving clock divider (2^i : i = 0 to 15), which reduces clock noise
- Four 24-bit internal data buses and three 16-bit internal address buses for simultaneous accesses to one program and two data memories

Memory

- Modified Harvard architecture allows simultaneous access to program and data memories
- 12800 × 24-bit on-chip Program ROM*
- 4096 × 24-bit on-chip X data RAM and 3584 × 24-bit on-chip X data ROM[1]
- 4352 × 24-bit on-chip Y data RAM and 2048 × 24-bit on-chip Y data ROM[1]
- 512 × 24-bit on-chip Program RAM and 64 × 24-bit bootstrap ROM
- As much as 2304 × 24 bits of X and Y data RAM can be switched to Program RAM, giving a total of 2816 × 24 bits of Program RAM

1.These ROMs may be factory programmed with data/program provided by the applicaton developer.

Table 1 lists the memory configurations of the DSP56011.

Table 1 DSP56011 Internal Memory Configurations

Memory Type	No Switch (PEA = 0, PEB = 0)	Switch A (PEA = 1, PEB = 0)	Switch B (PEA = 0, PEB = 1)	Switch A+B (PEA = 1, PEB = 1)
Program RAM	0.5 K	1.25 K	2.0 K	2.75 K
X data RAM	4.0 K	3.25 K	3.25 K	2.5 K
Y data RAM	4.25 K	4.25 K	3.5 K	3.5 K
Program ROM	12.5 K	12.5 K	12.5 K	12.5 K
X data ROM	3.5 K	3.5 K	3.5 K	3.5 K
Y data ROM	2.0 K	2.0 K	2.0 K	2.0 K

Peripheral and Support Circuits

- SAI includes:
  - Two receivers and three transmitters
  - Master or slave capability
  - I^2S, Sony, and Matsushita audio protocol implementations
  - Two sets of SAI interrupt vectors
- SHI features:
  - Single master capability
  - SPI and I^2C protocols
  - 10-word receive FIFO
  - Support for 8-, 16- and 24-bit words.
- Byte-wide Parallel Host Interface with DMA support capable of reconfiguration as fifteen General Purpose Input/Output (GPIO) lines
- DAX features one serial transmitter capable of supporting S/PDIF, IEC958, CP-340, and AES/EBU formats.
- Eight dedicated, independent, programmable GPIO lines
- On-chip peripheral registers memory mapped in data memory space
- OnCE port for unobtrusive, processor speed-independent debugging
- Software programmable PLL-based frequency synthesizer for the core clock
- Power saving Wait and Stop modes
- Fully static, HCMOS design from specified operating frequency down to dc
- 100-pin plastic Thin Quad Flat Pack (TQFP) surface-mount package
- 5 V power supply

DOCUMENTATION

Table 2 lists the documents that provide a complete description of the DSP56011 and are required to design properly with the part. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or through the Motorola DSP home page on the Internet (the source for the latest information).

Table 2 Additional DSP56011 Documentation

Document Name	Description	Order Number
DSP56000 Family Manual	Detailed description of the 56000-family architecture and the 24-bit core processor and instruction set	DSP56KFAMUM/AD
DSP56011 User's Manual	Detailed description of memory, peripherals, and interfaces	DSP56011UM/AD
DSP56011 Technical Data	Electrical and timing specifications and pin and package descriptions	DSP56011/D

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