DSP56302A

Advance Information

24-BIT DIGITAL SIGNAL PROCESSOR

The DSP56302A is a member of the DSP56300 core family of programmable CMOS Digital Signal Processors (DSPs). This family uses a high performance, single-clock-cycle-per-instruction engine providing a two-fold performance increase over Motorola's popular DSP56000 core, while retaining code compatibility. Significant architectural enhancements in the DSP56300 family include a barrel shifter, 24-bit addressing, instruction cache, and Direct Memory Access (DMA). The DSP56302A offers 66/80/100 MIPS at 3.0–3.6 V using an internal 66/80/100 MHz clock. The large on-chip memories can support wireless infrastructure and local loop applications and allow the chip to be used for RAM-based emulation of low-cost ROM-based solutions. The DSP56300 core family offers a new level of performance in speed and power provided by its rich instruction set and low power dissipation, enabling a new generation of wireless, telecommunications, and multimedia products.

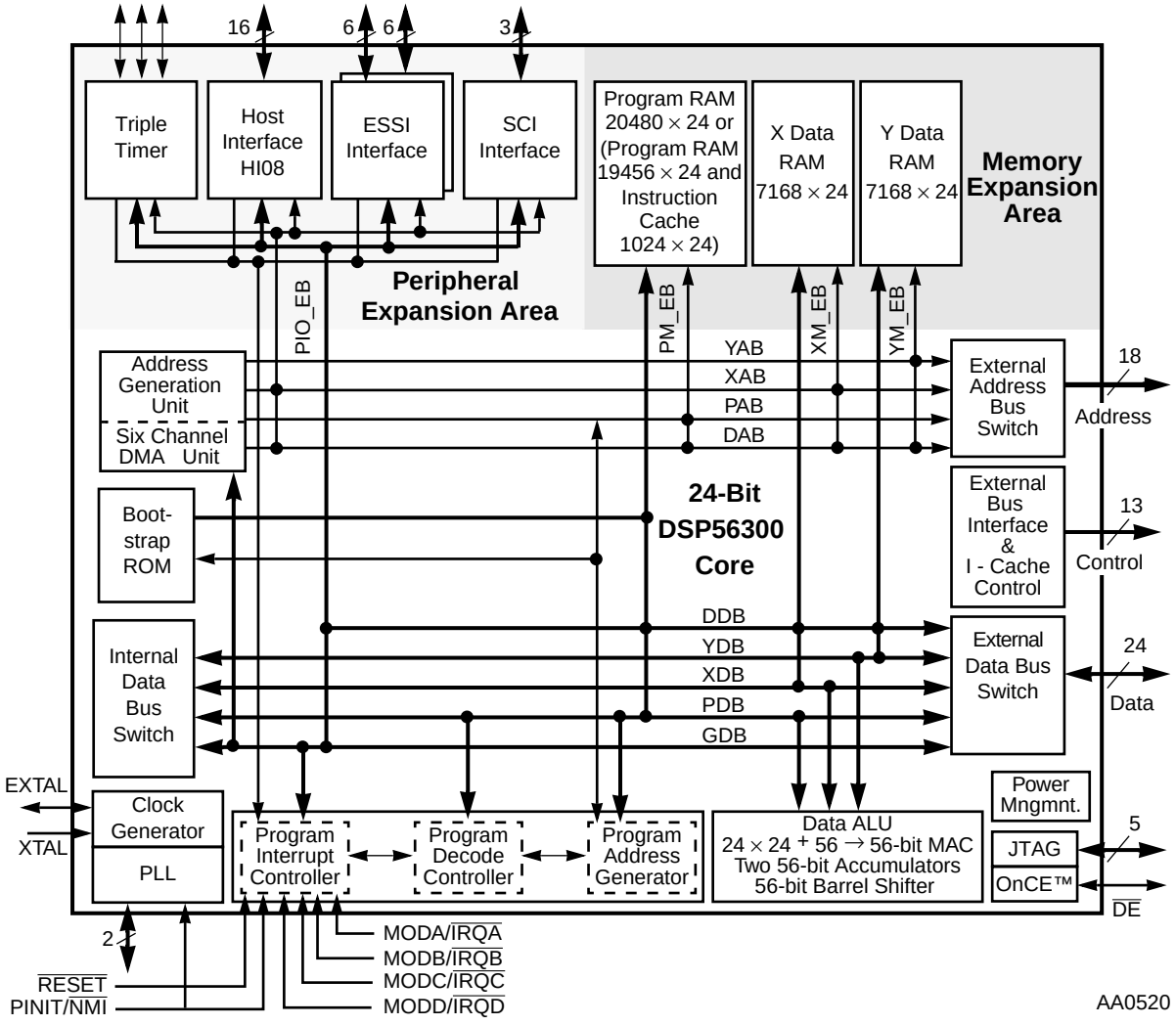

Figure 1 DSP56302A Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Preliminary Data

FEATURES

- High Performance DSP56300 Core
  - 66 / 80 / 100 Million Instructions Per Second (MIPS) with a 66 / 80 / 100 MHz clock at 3.0–3.6 V
  - Object code compatible with the DSP56000 core with highly parallel instruction set
  - Data Arithmetic Logic Unit (Data ALU) with fully pipelined 24 x 24-bit parallel Multiplier-Accumulator (MAC), 56-bit parallel barrel shifter (fast shift and normalization; bit stream generation and parsing), conditional ALU instructions, and 24-bit or 16-bit arithmetic support under software control
  - Program Control Unit (PCU) with Position Independent Code (PIC) support, addressing modes optimized for DSP applications (including immediate offsets), on-chip instruction cache controller, on-chip memory-expandable hardware stack, nested hardware DO loops, and fast auto-return interrupts
  - Direct Memory Access (DMA) with six DMA channels supporting internal and external accesses; one-, two-, and three-dimensional transfers (including circular buffering); end-of-block-transfer interrupts; and triggering from interrupt lines and all peripherals
  - Phase Lock Loop (PLL) allows change of low power Divide Factor (DF) without loss of lock and has output clock with skew elimination
  - Hardware debugging support including On-Chip Emulation (OnCE™) module, Joint Action Test Group (JTAG) Test Access Port (TAP), and Address Trace mode reflects internal Program RAM accesses at the external port
- On-Chip Memories and Off-Chip Memory Expansion
  - Program RAM, Instruction Cache, X data RAM, and Y data RAM sizes are programmable.

Instruction Cache	Switch Mode	Program RAM Size	Instruction Cache Size	X Data RAM Size	Y Data RAM Size
disabled	disabled	20480 × 24-bit	0	7168 × 24-bit	7168 × 24-bit
enabled	disabled	19456 × 24-bit	1024 × 24-bit	7168 × 24-bit	7168 × 24-bit
disabled	enabled	24576 × 24-bit	0	5120 × 24-bit	5120 × 24-bit
enabled	enabled	23552 × 24-bit	1024 × 24-bit	5120 × 24-bit	5120 × 24-bit

  - 192 x 24-bit bootstrap ROM
- Off-chip memory expansion
  - Data memory expansion to two 256 K × 24-bit word memory spaces (or up to two 4 M × 24-bit word memory spaces by using the Address Attribute AA0–AA3 signals)
  - Program memory expansion to one 256 K × 24-bit words memory space (or up to one 4 M × 24-bit word memory space by using the Address Attribute AA0–AA3 signals)

  - External memory expansion port
  - Chip Select Logic for glueless interface to SRAMs
  - On-chip DRAM Controller for glueless interface to DRAMs
- On-Chip Peripherals
  - 3.0–3.6 V I/O interface
  - Enhanced DSP56000-like 8-bit parallel Host Interface (HI08) supports a variety of buses (e.g., ISA) and provides glueless connection to a number of industry standard microcomputers, microprocessors, and DSPs
  - Two Enhanced Synchronous Serial Interfaces (ESSI0 and ESSI1), each with one receiver and three transmitters (allows six-channel home theater)
  - Serial Communications Interface (SCI) with baud rate generator
  - Triple timer module
  - Up to thirty-four programmable General Purpose Input/Output (GPIO) pins, depending on which peripherals are enabled
- Reduced Power Dissipation
  - Very low power CMOS design
  - Wait and Stop low power standby modes
  - Fully-static logic, operation frequency down to 0 Hz (dc)
  - Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent)
- Packaging
  - 144-pin TQFP
  - 196-pin PBGA

TARGET APPLICATIONS

The DSP56302A is intended for applications requiring a large amount of on-chip memory, such as wireless infrastructure applications. It is also intended as a RAM-based emulation part for low-cost ROM-based solutions

PRODUCT DOCUMENTATION

The three manuals listed in **Table 1** are required for a complete description of the DSP56302A and are necessary to design properly with the part. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or the Motorola DSP home page on the Internet, which will have the latest information (see the address below).

Table 1 DSP56302A Documentation

Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the DSP56300 family processor core and instruction set	DSP56300FM / AD
DSP56302 User's Manual	Detailed functional description of the DSP56302 memory configuration, operation, and register programming	DSP56302UM / AD
DSP56302A Technical Data	DSP56302A features list and physical, electrical, timing, and package specifications	DSP56302A / D

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