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DSP56156
DSP56156ROM

Advance Information

16-bit Digital Signal Processor

The DSP56156 is a general-purpose MPU-style Digital Signal Processor (DSP). On a single semiconductor chip, the DSP56156 comprises a very efficient 16-bit digital signal processing core, program and data memories, a number of peripherals, and system support circuitry. Unique features of the DSP56156 include a built-in sigma-delta (∑Δ) codec and phase-locked loop (PLL). This combination of features makes the DSP56156 a cost-effective, high-performance solution for many DSP applications, especially speech coding, digital communications, and cellular base stations.

The central processing unit of the DSP56156 is the DSP56100 core processor. Like all DSP56100-based DSPs, the DSP56156 consists of three execution units operating in parallel, allowing up to six operations to be performed during each instruction cycle. This parallelism greatly increases the effective processing speed of the DSP56156. The MPU-style programming model and instruction set allow straightforward generation of efficient, compact code. The basic architectures and development tools of Motorola's 16-bit, 24-bit, and 32-bit DSPs are so similar that understanding how to design and program one greatly reduces the time needed to learn the others.

On-Chip Emulation (OnCE™ port) circuitry provides convenient and inexpensive debug facilities normally available only through expensive external hardware. Development costs are reduced and in-field testing is greatly simplified using the OnCE™ port. Figure 1 illustrates the DSP56156 in detail.

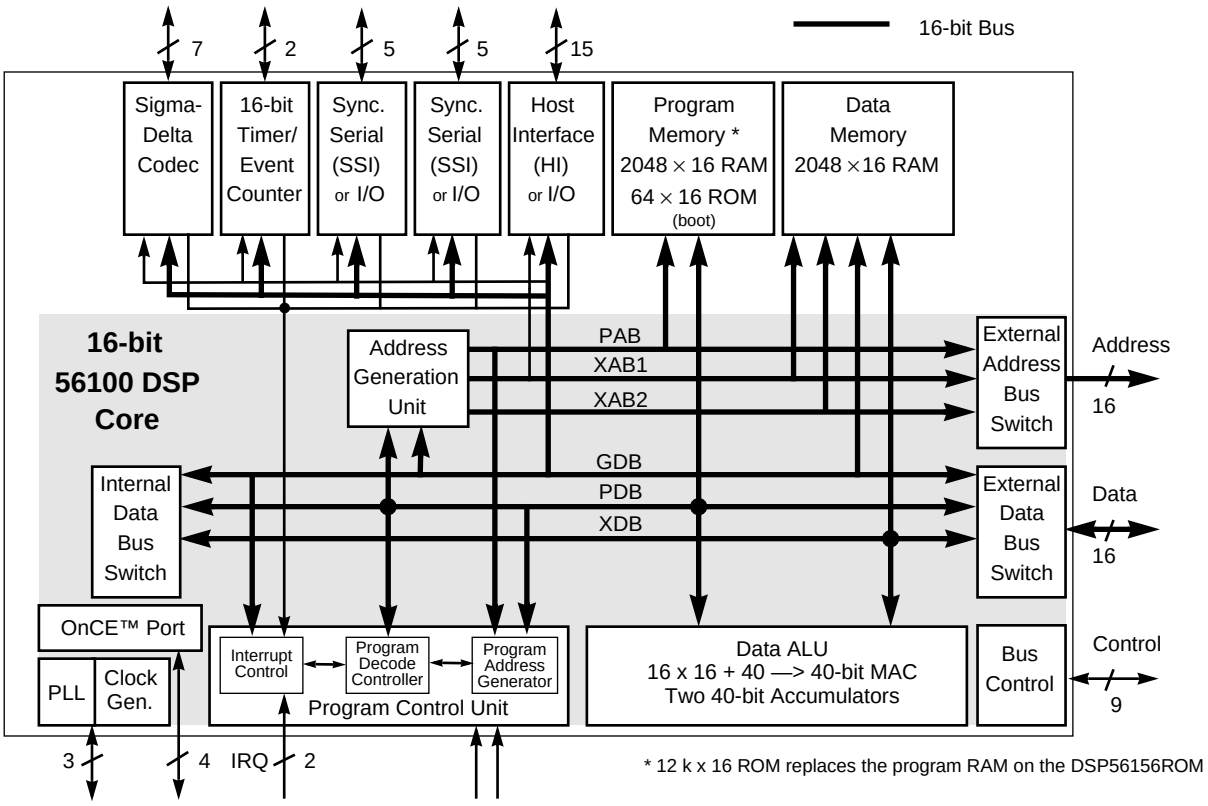

Figure 1 DSP56156 Block Diagram

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DSP56156 Features

Digital Signal Processing Core

- Efficient, object code compatible, 16-bit 56100-Family DSP engine
  - Up to 30 Million Instructions Per Second (MIPS) – 33 ns instruction cycle at 60 MHz
  - Up to 180 Million Operations Per Second (MOPS) at 60 MHz
  - Highly parallel instruction set with unique DSP addressing modes
  - Two 40-bit accumulators including extension byte
  - Parallel 16 × 16-bit multiply-accumulate in 1 instruction cycle (2 clock cycles)
  - Double precision 32 × 32-bit multiply with 72-bit result in 6 instruction cycles
  - Least Mean Square (LMS) adaptive loop filter in 2 instructions
  - 40-bit Addition/Subtraction in 1 instruction cycle
  - Fractional and integer arithmetic with support for multiprecision arithmetic
  - Hardware support for block-floating point FFT
  - Hardware-nested DO loops including infinite loops
  - Zero-overhead fast interrupts (2 instruction cycles)
  - Three 16-bit internal data buses and three 16-bit internal address buses for maximum information transfer on-chip

Memory

- On-chip Harvard architecture permitting simultaneous accesses to program and memories
- 2048 × 16-bit on-chip program RAM and 64 ×16-bit bootstrap ROM (or 12 k × 16-bit on-chip program ROM on the DSP56156ROM)
- 2048 × 16-bit on-chip data RAM
- External memory expansion with 16-bit address and data buses
- Bootstrap loading from external data bus, Host Interface, or Synchronous Serial Interface

Peripheral and Support Circuits

- Byte-wide Host Interface (HI) with Direct Memory Access support
- Two Synchronous Serial Interfaces (SSI) to communicate with codecs and synchronous serial devices
  - Built in μ-law and A-law compression/expansion
  - Up to 32 software-selectable time slots in network mode
- 16-bit Timer/Event Counter also generates and measures digital waveforms
- On-chip sigma-delta voice band Codec:
  - Sampling clock rates between 100 kHz and 3 MHz
  - Four software-programmable decimation/interpolation ratios
  - Internal voltage reference ($^2/_5$ of positive power supply)
  - No external components required

- On-chip peripheral registers memory mapped in data memory space
- Double buffered peripherals
- Up to 27 general purpose I/O pins
- Two external interrupt request pins
- On-Chip Emulation (OnCE™) port for unobtrusive, processor speed-independent debugging
- Software-programmable, Phase-Locked Loop-based (PLL) frequency synthesizer for the core clock

Miscellaneous Features

- Power-saving Wait and Stop modes
- Fully static, HCMOS design for operating frequencies from 40 or 60 MHz down to DC
- 112-pin Ceramic Quad Flat Pack (CQFP) surface-mount package; 20 × 20 × 3 mm
- 112-pin Plastic Thin Quad Flat Pack (TQFP) surface-mount package; 20 × 20 × 1.5 mm
- 5 V power supply

Product Documentation

This data sheet plus the two manuals listed in Table 1 are required for a complete DSP56156 description and are necessary to properly design with the part. Documentation is available from a local Motorola distributor, a semiconductor sales office, or through a Motorola Literature Distribution Center.

Table 1 DSP56156 Documentation

Topic	Description	Order Number
DSP56100 Family Manual	Detailed description of the 56000-family architecture and the 16-bit core processor and instruction set	DSP56100FAMUM/AD
DSP56156 User's Manual	Detailed description of memory, peripherals, and interfaces	DSP56156UM/AD
DSP56156 Data Sheet	Pin and package descriptions, and electrical and timing specifications	DSP56156/D

Related Documentation

Table 2 lists additional documentation relevant to the DSP56156.

Table 2 Related Motorola Documentation

Topic	Description	Order Number
DSP Family Brochure	Overview of all DSP product families	BR1105/D
Development Tools	Product Brief. Includes ordering information	DSPTOOLSP/D
Fractional and Integer Arithmetic	Application Report. Includes code	APR3/D
Fast Fourier Transforms (FFTs)	Application Report. Comprehensive FFT algorithms and code for DSP56001, DSP56156, and DSP96002	APR4/D
G.722 Audio Processing	Application Report. Theory and code using SB-ADPCM	APR404/D
Dr. BuB Bulletin Board	Flyer. Motorola's electronic bulletin board where free DSP software is available	BR297/D
Third Party Compendium	Brochures from companies selling hardware and software that supports Motorola DSPs	DSP3RDPTYPAK/D
University Support Program	Flyer. Motorola's program that supports universities in DSP research and education	BR382/D

Data Sheet Contents

This data sheet contains:

- signal definitions and pin locations
- electrical specifications and timings
- package descriptions
- design considerations
- ordering information

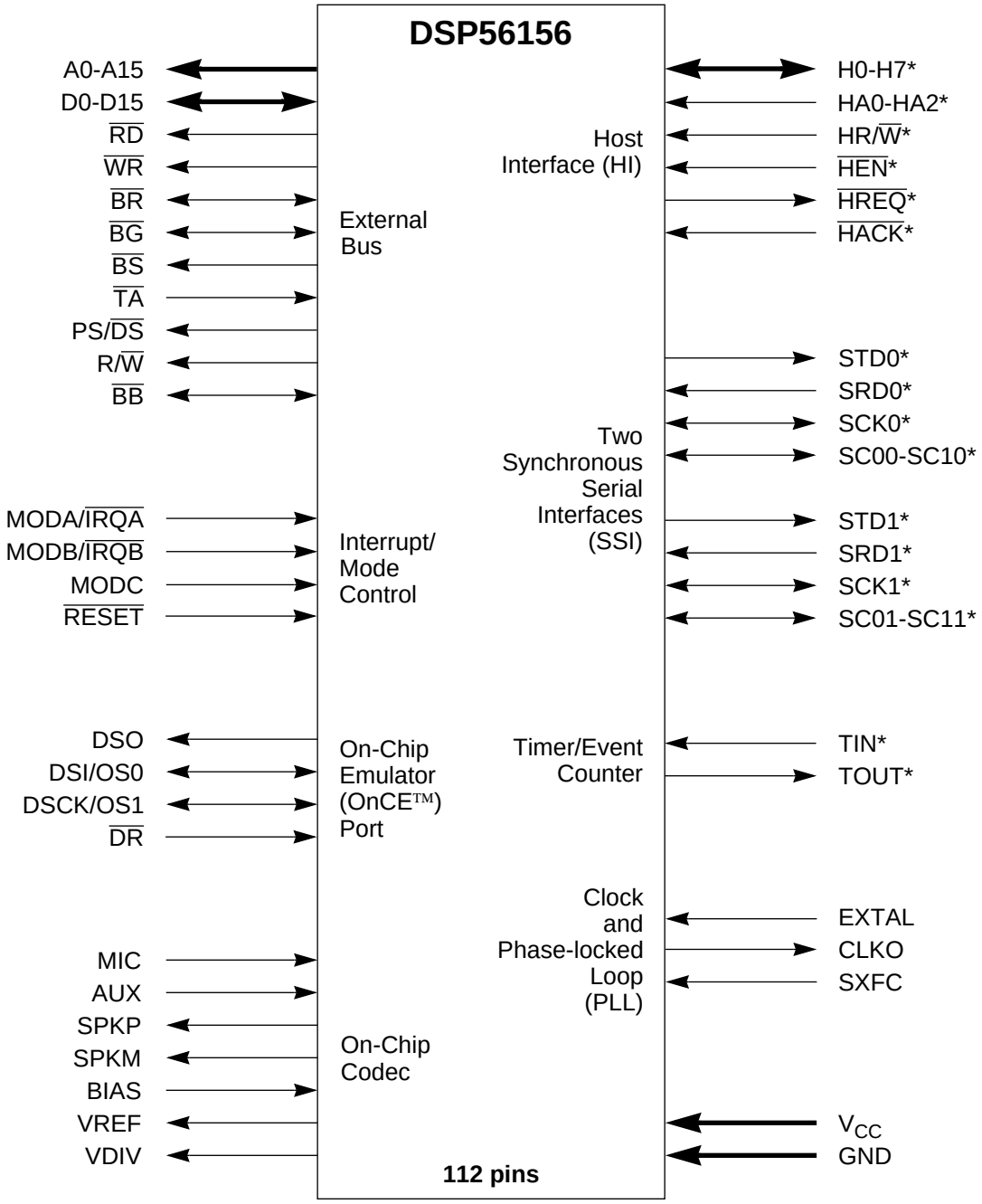
Pin Groupings

The DSP56156 is available in a 112-pin Ceramic Quad Flat Pack (CQFP) and a 112-pin Plastic Thin Quad Flat Pack (TQFP). The input and output signals are organized into the functional groups indicated in Table 3. Figure 2 illustrates the chip's pin functions.

Table 3 Functional Pin Groupings

Functional Group	Number of Pins
Address	16
Data Bus	16
Bus Control	9
Host Interface (HI)	15
Synchronous Serial Interfaces (SSI)	10
Timer Interface	2
Interrupt and Mode Control	4
Phase-Locked Loop (PLL) and Clock	3
On-Chip Emulation (OnCE™ Port)	4
On-Chip Codec	7
Power (V_{CC})	10
Ground (GND)	16
Total	112

NOTE: $\overline{\text{OVERBARS}}$ are used throughout this document to indicate a signal which is at Ground voltage (typically a TTL logic low — V_{IL} or V_{OL}) when the function is logically true. These signals are, likewise, at V_{CC} voltage (typically a TTL logic high — V_{IH} or V_{OH}) when the function is logically false.



* These pins have an alternate function of general purpose input/output.

Figure 2 DSP56156 Pin Functions

Pin Descriptions

Address and Data Bus

A0-A15 (Address Bus) — three-state, active high outputs. A0-A15 change in t0 and specify the address for external program and data memory accesses. If there is no external bus activity, A0-A15 remain at their previous values. A0-A15 are three-stated during hardware reset.

D0-D15 (Data Bus) — three-state, active high, bidirectional input/outputs. Read data is sampled on the trailing edge of t2, while write data output is enabled by the leading edge of t2 and three-stated at the leading edge of t0. If there is no external bus activity, D0-D15 are three-stated. D0-D15 are also three-stated during hardware reset.

Bus Control

PS/$\overline{\text{DS}}$ (Program/Data Memory Select) — three-state, active low output. This output is asserted only when external data memory is referenced. PS/$\overline{\text{DS}}$ timing is the same for the A0-A15 address lines. PS/$\overline{\text{DS}}$ is high for program memory access and is low for data memory access. If the external bus is not used during an instruction cycle (t0, t1, t2, t3), PS/$\overline{\text{DS}}$ goes high in t0. PS/$\overline{\text{DS}}$ is in the high impedance state during hardware reset.

R/$\overline{\text{W}}$ (Read/Write) — three-state, active low output. Timing is the same as the address lines, providing an "early write" signal. R/$\overline{\text{W}}$ (which changes in t0) is high for a read access and is low for a write access. If the external bus is not used during an instruction cycle (t0, t1, t2, t3), R/$\overline{\text{W}}$ goes high in t0. R/$\overline{\text{W}}$ is three-stated during hardware reset.

$\overline{\text{WR}}$ (Write Enable) — three-state, active low output. This output is asserted during external memory write cycles. When $\overline{\text{WR}}$ is asserted in t1, the data bus pins D0-D15 become outputs and the DSP puts data on the bus during the leading edge of t2. When $\overline{\text{WR}}$ is deasserted in t3, the external data has been latched inside the external device. When $\overline{\text{WR}}$ is asserted, it qualifies the A0-A15 and PS/$\overline{\text{DS}}$ pins. $\overline{\text{WR}}$ can be connected directly to the $\overline{\text{WE}}$ pin of a static RAM. $\overline{\text{WR}}$ is three-stated during hardware reset or when the DSP is not bus master.

$\overline{\text{RD}}$ (Read Enable) — three-state, active low output. This output is asserted during external memory read cycles. When $\overline{\text{RD}}$ is asserted in late t0/early t1, the data bus pins D0-D15 become inputs and an external device is enabled onto the data bus. When $\overline{\text{RD}}$ is deasserted in t3, the external data is latched inside the DSP. When $\overline{\text{RD}}$ is asserted, it qualifies the A0-A15 and PS/$\overline{\text{DS}}$ pins. $\overline{\text{RD}}$ can be connected directly to the $\overline{\text{OE}}$ pin of a static RAM or ROM. $\overline{\text{RD}}$ is three-stated during hardware reset or when the DSP is not bus master.

$\overline{\text{BS}}$ (Bus Strobe) — three-state, active low output. Asserted at the start of a bus cycle (during t0) and deasserted at the end of the bus cycle (during t2). This pin provides an "early bus start" signal which can be used as address latch and as an "early bus end" signal which can be used by an external bus controller. $\overline{\text{BS}}$ is three-stated during hardware reset.

$\overline{TA}$ (Transfer Acknowledge) — active low input. If there is no external bus activity, the $\overline{TA}$ input is ignored by the DSP. When there is external bus cycle activity, $\overline{TA}$ can be used to insert wait states in the external bus cycle. $\overline{TA}$ is sampled on the leading edge of the clock. Any number of wait states from 1 to infinity may be inserted by using $\overline{TA}$. If $\overline{TA}$ is sampled high on the leading edge of the clock beginning the bus cycle, the bus cycle will end 2T after the $\overline{TA}$ has been sampled low on a leading edge of the clock; if the Bus Control Register (BCR) value does not program more wait states. The number of wait states is determined by the $\overline{TA}$ input or by the Bus Control Register (BCR), whichever is longer. $\overline{TA}$ is still sampled during the leading edge of the clock when wait states are controlled by the BCR value. In that case, $\overline{TA}$ will have to be sampled low during the leading edge of the last period of the bus cycle programmed by the BCR (2T before the end of the bus cycle programmed by the BCR) in order not to add any wait states. $\overline{TA}$ should always be deasserted during t3 to be sampled high by the leading edge of T0. If $\overline{TA}$ is sampled low (asserted) at the leading edge of the t0 beginning the bus cycle, and if no wait states are specified in the BCR register, zero wait states will be inserted in the external bus cycle, regardless the status of $\overline{TA}$ during the leading edge of T2.

$\overline{BR}$ (Bus Request) — active low output when in master mode, active low input when in slave mode. After power-on reset, this pin is an input (slave mode). In this mode, the bus request $\overline{BR}$ allows another device such as a processor or DMA controller to become the master of the DSP external data bus D0-D15 and external address bus A0-A15. The DSP asserts $\overline{BG}$ a few T states after the $\overline{BR}$ input is asserted. The DSP bus controller releases control of the external data bus D0-D15, address bus A0-A15 and bus control pins PS/$\overline{DS}$, $\overline{RD}$, $\overline{WR}$, and R/$\overline{W}$ at the earliest time possible consistent with proper synchronization. These pins are then placed in the high impedance state and

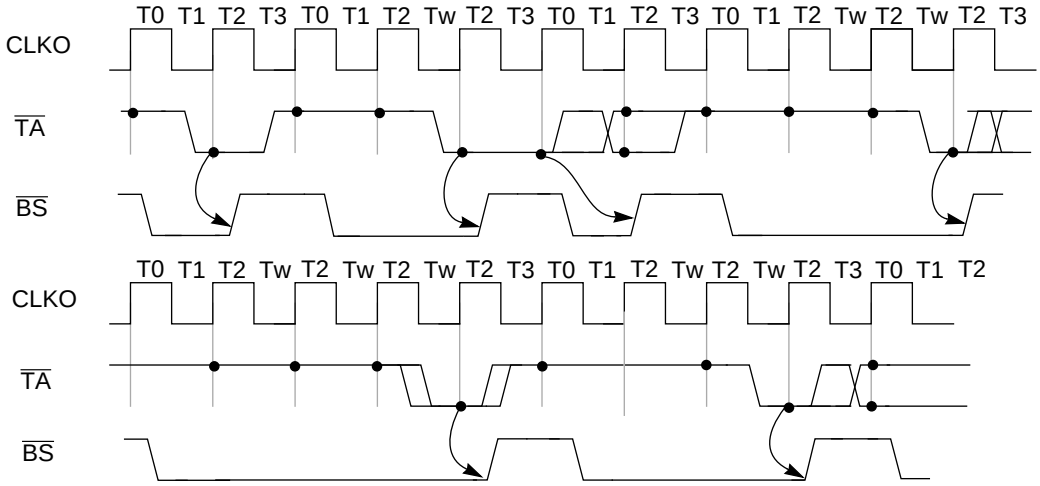


Figure 3 $\overline{TA}$ Controlled Accesses

the $\overline{BB}$ pin is deasserted. The DSP continues executing instructions only if internal program and data memory resources are accessed. If the DSP requests the external bus while $\overline{BR}$ input pin is asserted, the DSP bus controller inserts wait states until the external bus becomes available ($\overline{BR}$ and $\overline{BB}$ deasserted). Note that interrupts are not serviced when a DSP instruction is waiting for the bus controller. Note also that $\overline{BR}$ is prevented from interrupting the execution of a read/ modify/write instruction.

If the master bit in the OMR register is set, this pin becomes an output (Master Mode). In this mode, the DSP is not the external bus master and has to assert $\overline{BR}$ to request the bus mastership. The DSP bus controller will insert wait states until $\overline{BG}$ input is asserted and will then begin normal bus accesses after the rising of the clock which sampled $\overline{BB}$ high. The $\overline{BR}$ output signal will remain asserted until the DSP no longer needs the bus. In this mode, the Request Hold bit (RH) of the Bus Control Register (BCR) allows $\overline{BR}$ to be asserted under software control.

During external accesses caused by an instruction executed out of external program memory, $\overline{BR}$ remains asserted low for consecutive external X memory accesses and continues toggling for consecutive external P memory accesses unless the Request Hold bit (RH) is set inside the Bus Control Register (BCR).

In the master mode, $\overline{BR}$ can also be used for non arbitration purpose: if $\overline{BG}$ is always asserted, $\overline{BR}$ is asserted in t0 of every external bus access. It can then be used as a chip select to turn a external memory device off and on between internal and external bus accesses. $\overline{BR}$ timing is in that case similar to A0-A15, R/$\overline{W}$ and PS/$\overline{DS}$; it is asserted and deasserted during t0.

$\overline{BG}$ (Bus Grant) — active low input when in master mode, active low output when in slave mode. Output after power on reset if the slave is selected, this pin is asserted to acknowledge an external bus request. It indicates that the DSP will release control of the external address bus A0-A15, data bus D0-D15 and bus control pins when $\overline{BB}$ is deasserted. The $\overline{BG}$ output is asserted in response to a $\overline{BR}$ input. When the $\overline{BG}$ output is asserted and $\overline{BB}$ is deasserted, the external address bus A0-A15, data bus D0-D15 and bus control pins are in the high impedance state. $\overline{BG}$ assertion may occur in the middle of an instruction which requires more than one external bus cycle for execution. Note that $\overline{BG}$ assertion will not occur during indivisible read-modify-write instructions (BFSET, BFCLR, BFCHG). When $\overline{BR}$ is deasserted, the $\overline{BG}$ output is deasserted and the DSP regains control of the external address bus, data bus, and bus control pins when the $\overline{BB}$ pin is sampled high.

This pin becomes an input if the master bit in the OMR register is set (Master Mode). It is asserted by an external processor when the DSP may become the bus master. The DSP can start normal external memory access after the $\overline{BB}$ pin has been deasserted by the previous bus master. When $\overline{BG}$ is deasserted, the DSP will release the bus as soon as the current transfer is completed. The state of $\overline{BG}$ may be tested by testing the BS bit in the Bus Control Register. $\overline{BG}$ is ignored during hardware reset.

$\overline{BB}$ (Bus Busy) — active low input when not bus master, active low output when bus master. This pin is asserted by the DSP when it becomes the bus master and it performs an external access. It is deasserted when the DSP releases bus mastership. $\overline{BB}$ becomes an input when the DSP is no longer the bus master.

Interrupt and Mode Control

MODA/$\overline{IRQA}$ (Mode Select A/External Interrupt Request A) — input. This input has two functions:

- to select the initial chip operating mode and,
- to allow an external device to request a DSP interrupt after internal synchronization.

MODA is read and internally latched in the DSP when the processor exits the reset state. MODA and MODB select the initial chip operating mode. Several clock cycles after leaving the reset state, the MODA pin changes to the external interrupt request $\overline{IRQA}$. The chip operating mode can be changed by software after reset.

The $\overline{IRQA}$ input is a synchronized external interrupt request which indicates that an external device is requesting service. It may be programmed to be level sensitive or negative edge triggered. If level sensitive triggering is selected, an external pull up resistor is required for wired-OR operation. If the processor is in the stop standby state and $\overline{IRQA}$ is asserted, the processor will exit the stop state.

MODB/$\overline{IRQB}$ (Mode Select B/External Interrupt Request B) — input. This input has two functions:

- to select the initial chip operating mode and,
- to allow an external device to request a DSP interrupt after internal synchronization.

MODB is read and internally latched in the DSP when the processor exits the reset state. MODA and MODB select the initial chip operating mode. Several clock cycles after leaving the reset state, the MODB pin changes to the external interrupt request $\overline{IRQB}$. After reset, the chip operating mode can be changed by software.

The $\overline{IRQB}$ input is an external interrupt request which indicates that an external device is requesting service. It may be programmed to be level sensitive or negative edge triggered. If level sensitive triggering is selected, an external pull up resistor is required for wired-OR operation.

MODC (Mode Select C) — input. This input selects the initial bus operating mode. When tied high, the external bus is programmed in the master mode ($\overline{BR}$ output and $\overline{BG}$ input) and when tied low the bus is programmed in the slave mode ($\overline{BR}$ input and $\overline{BG}$ output). MODC is read and internally latched in the DSP when the processor exits the reset state. After $\overline{RESET}$, the bus operating mode can be changed by software by writing the MC bit of the OMR register.

$\overline{RESET}$ (Reset) — input. This input is a direct hardware reset of the processor. When $\overline{RESET}$ is asserted, the DSP is initialized and placed in the reset state. A Schmitt

trigger input is used for noise immunity. When the reset pin is deasserted, the initial chip operating mode is latched from the MODA and MODB pins, and the initial bus operating mode is latched from the MODC pin. The internal reset signal should be deasserted synchronized with the internal clocks.

Host Interface

H0-H7 (Host Data Bus) — bidirectional. This bidirectional data bus is used to transfer data between the host processor and the DSP. This bus is an input unless enabled by a host processor read. H0-H7 may be programmed as Port B general purpose parallel I/O pins called PB0-PB7 when the Host Interface (HI) is not being used.

HA0-HA2 (Host Address 0-2) — input*. These inputs provide the address selection for each HI register and are stable when $\overline{\text{HEN}}$ is asserted. HA0-HA2 may be programmed as Port B general purpose parallel I/O pins called PB8-PB10 when the HI is not being used.

HR/$\overline{\text{W}}$ (Host Read/Write) — input*. This input selects the direction of data transfer for each host processor access. If HR/$\overline{\text{W}}$ is high and $\overline{\text{HEN}}$ is asserted, H0-H7 are outputs and DSP data is transferred to the host processor. If HR/$\overline{\text{W}}$ is low and $\overline{\text{HEN}}$ is asserted, H0-H7 are inputs and host data is transferred to the DSP. When $\overline{\text{HEN}}$ is asserted, HR/$\overline{\text{W}}$ is stable. HR/$\overline{\text{W}}$ may be programmed as a general purpose I/O pin called PB11 when the HI is not being used.

$\overline{\text{HEN}}$ (Host Enable) — input*. This input enables a data transfer on the host data bus. When $\overline{\text{HEN}}$ is asserted and HR/$\overline{\text{W}}$ is high, H0-H7 becomes an output and DSP data may be latched by the host processor. When $\overline{\text{HEN}}$ is asserted and HR/$\overline{\text{W}}$ is low, H0-H7 is an input and host data is latched inside the DSP when $\overline{\text{HEN}}$ is deasserted. Normally a chip select signal derived from host address decoding and an enable clock is connected to the Host Enable. $\overline{\text{HEN}}$ may be programmed as a general purpose I/O pin called PB12 when the HI is not being used.

$\overline{\text{HREQ}}$ (Host Request) — output*. This open-drain output signal is used by the HI to request service from the host processor. $\overline{\text{HREQ}}$ may be connected to an interrupt request pin of a host processor, a transfer request of a DMA controller, or a control input of external circuitry. $\overline{\text{HREQ}}$ is asserted when an enabled request occurs in the HI. $\overline{\text{HREQ}}$ is deasserted when the enabled request is cleared or masked, DMA HACK is asserted, or the DSP is reset. $\overline{\text{HREQ}}$ may be programmed as a general purpose I/O pin (not open-drain) called PB13 when the HI is not being used.

$\overline{\text{HACK}}$ (Host Acknowledge) — input*. This input has two functions:

- to provide a host acknowledge signal for DMA transfers and,
- to control handshaking and to provide a host interrupt acknowledge compatible with MC68000 family processors.

If programmed as a host acknowledge signal, $\overline{\text{HACK}}$ may be used as a data strobe for HI DMA data transfers. If programmed as an MC68000 host interrupt

* These pins can be bidirectional when programmed as general purpose I/O.

acknowledge, $\overline{\text{HACK}}$ enables the HI Interrupt Vector Register (IVR) onto the host data bus H0-H7 if the Host Request $\overline{\text{HREQ}}$ output is asserted. In this case, all other HI control pins are ignored and the HI state is not affected. $\overline{\text{HACK}}$ may be programmed as a general purpose I/O pin called PB14 when the HI is not being used.

16-bit Timer

TIN (Timer Input) — input*. This input receives external pulses to be counted by the on-chip 16-bit timer when external clocking is selected. The pulses are internally synchronized to the DSP core internal clock. TIN may be programmed as a general purpose I/O pin called PC10 when the external event function is not being used.

TOUT (Timer Output) — output*. This output generates pulses or toggles on a timer overflow event or a compare event. TOUT may be programmed as a general purpose I/O pin called PC11 when disabled by the timer out enable bits (TO2-TO0).

Synchronous Serial Interfaces (SSI)

STD0-1 (SSI0-1 Transmit Data) — output*. These output pins transmit serial data from the SSI0-1 Transmit Shift Register. STD0 and STD1 may be programmed as a general purpose I/O pin called PC0 and PC5, respectively, when the STD function is not being used.

SRD0-1 (SSI0-1 Receive Data) — input*. These input pins receive serial data and transfer the data to the SSI0-1 Receive Shift Register. SRD0 and SRD1 may be programmed as a general purpose I/O pin called PC1 and PC6, respectively, when the SRD function is not being used.

SCK0-1 (SSI0-1 Serial Clock) — bidirectional. These bidirectional pins provide the serial bit rate clock for the SSI0-1 interface. SCK0 and SCK1 may be programmed as a general purpose I/O pin called PC2 and PC7, respectively, when the SSI0-1 interfaces are not being used.

SC10-11 (SSI0-1 Serial Control 1) — bidirectional. These bidirectional pins are used by the SSI0-1 serial interface as frame sync I/O or flag I/O. SC10 and SC11 may be programmed as a general purpose I/O pin called PC3 and PC8, respectively, when the SSI0-1 are not using these pins.

SC00-01 (SSI0-1 Serial Control 0) — bidirectional. These bidirectional pins are used by the SSI0-1 serial interface as frame sync I/O or flag I/O. SC00 and SC01 may be programmed as a general purpose I/O pin called PC4 and PC9, respectively, when the SSI0-1 are not using these pins.

***** These pins can be bidirectional when programmed as general purpose I/O.

On-Chip Emulation (OnCE™ Port)

DSI/OS0 (Debug Serial Input/Chip Status 0) — bidirectional. The DSI/OS0 pin, when an input, is the pin through which serial data or commands are provided to the OnCE port controller. The data received on the DSI pin will be recognized only when the DSP has entered the debug mode of operation. Data must have valid TTL logic levels before the serial clock falling edge. Data is always shifted into the OnCE serial port most significant bit (MSB) first. When the DSP is not in the debug mode, the DSI/OS0 pin provides information about the chip status if it is an output and used in conjunction with the OS1 pin.

DSCK/OS1 (Debug Serial Clock/Chip Status 1) — bidirectional. The DSCK/OS1 pin, when an input, is the pin through which the serial clock is supplied to the OnCE port. The serial clock provides pulses required to shift data into and out of the OnCE serial port. Data is clocked into the OnCE port on the falling edge and is clocked out of the OnCE serial port on the rising edge. If the DSCK/OS1 pin is an output and used in conjunction with the OS0 pin, it provides information about the chip status when the DSP is not in the debug mode.

DSO (Debug Serial) — output. The debug serial output provides the data contained in one of the OnCE port controller registers as specified by the last command received from the command controller. When idle, this pin is high. When the requested data is available, the DSO line will be asserted (negative true logic) for four T cycles (one instruction cycle) to indicate that the serial shift register is ready to receive clocks in order to deliver the data. When the chip enters the debug mode due to an external debug request ($\overline{DR}$), an internal software debug request (DEBUG), a hardware breakpoint occurrence or a trace/step occurrence, this line will be asserted for three T cycles to indicate that the chip has entered the debug mode and is waiting for commands. Data is always shifted out the OnCE serial port with the most significant bit first.

$\overline{DR}$ (Debug Request) — input. The debug request input provides a means of entering the debug mode of operation. This pin, when asserted, will cause the DSP to finish the current instruction being executed, enter the debug mode, and wait for commands to be entered from the debug serial input line.

On-Chip Codec

AUX (Auxiliary) — input. This pin is selected as the analog input to the A/D converter when the INS bit is set in the codec control register COCR. This pin should be left floating when the codec is not used.

BIAS (Bias current) — input. This input is used to determine the bias current for the analog circuitry. Connecting a resistor between BIAS and GNDA will program the current bias generator. This pin should be left floating when the codec is not used.

MIC (Microphone) — input. This pin is selected as the analog input to the A/D converter when the INS bit is cleared in

the codec control register COCR. This pin should be left floating when the codec is not used.

SPKP **(Speaker Plus)** — **output**. This pin is the positive analog output from the on-chip D/A converter. This pin should be left floating when the codec is not used.

SPKM **(Speaker Minus)** — **output**. This pin is the negative analog output from the on-chip D/A converter. This pin should be left floating when the codec is not used.

VREF **(Voltage Reference)** — **output**. This pin is the op-amp buffer output in the reference voltage generator. It has a value of $(^2/_5)V_{CCA}$. This pin should always be connected to the GNDA through two capacitors, even when the codec is not used.

VDIV **(Voltage Division)** — **output**. This output pin is also the output to the on-chip op-amp buffer in the reference voltage generator. It is connected to a resistor divider network located within the codec block which provides a voltage equal to $(^2/_5)V_{CCA}$. This pin should be connected to the GND via a capacitor when the codec is used and should be left floating when the codec is not used.

Power, Ground, and Clock

V_{CC} **(Power)** — Power pins

GND **(Ground)** — Ground pins

V_{CCS} **(Synthesizer Power)** — This pin supplies a quiet power source to the Phase-Locked Loop (PLL) to provide greater frequency stability.

GNDS **(Synthesizer Ground)** — This pin supplies a quiet ground source to the PLL to provide greater frequency stability.

V_{CCA} **(Analog Power)** — This pin is the positive analog supply input. It should be connected to V_{CC} when the codec is not used.

GNDA **(Analog Ground)** — This pin is the analog ground return. It should be connected to digital GND when the codec is not used.

EXTAL **(External Clock)** — **input.** This input should be driven by an external clock or by an external oscillator. After being squared, the input frequency can be used as the DSP core internal clock. In that case, it is divided by two to produce a four phase instruction cycle clock, the minimum instruction time being two input clock periods. This input frequency is also used, after division, as input clock for the on-chip codec and the on-chip PLL.

CLKO **(Clock Output)** — **output.** This pin outputs a buffered clock signal. By programming two bits (CS1-CS0) inside the PLL Control Register (PLCR), the user can select between outputting a squared version of the signal applied to EXTAL, a squared version of the signal applied to EXTAL divided by 2, and a delayed version of the DSP core master clock. The clock frequency on this pin can be disabled by setting the Clockout Disable bit (CD; bit 7) of the Operating Mode Register (OMR). When disabled, the pin can be left floating.

SXFC **(External Filter Capacitor)** — This pin adds an external capacitor to the PLL filter circuit. A low leakage capacitor should be connected between and located very close to SXFC and V_{CCS}.

Electrical Characteristics and Timing

CAUTION: Exceeding maximum electrical ratings will permanently damage or disable the chip, or impair the chip's long term reliability.

The DSP56156 is fabricated in high density HCMOS with TTL compatible inputs and CMOS compatible outputs.

Table 4 Maximum Electrical Ratings (GND = 0 Vdc)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	V
All Input Voltages	V_{IN}	GND - 0.5 to V_{CC} + 0.5	V
Current Drain per Pin excluding V_{CC} and GND	I	10	mA
Storage Temperature	T_{stg}	-55 to +150	°C

Table 5 Operating Conditions

Supply Voltage V_{CC}		Junction Temperature T_J (°C)	
Min	**Max**	**Min**	**Max**
4.5	5.5	-40	115

Table 6 Thermal Characteristics of CQFP and TQFP Packages

Thermal Resistance Characteristics	Symbol	Value		Rating
		CQFP	TQFP	
Junction to Ambient	Θ_{JA}	40	49	°C/W
Junction to Case (estimated)	Θ_{JC}	7	8	°C/W

NOTE: This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

Preliminary

Analog I/O Characteristics

(V_{CCA} = 5.0 V dc ± 10%, T_J = -40° to +125°C)

The analog I/O characteristics of this device are listed in Table 7.
For additional information regarding the use of analog signals, see "Design Considerations" at the end of this document.

Table 7 Analog I/O Characteristics

Characteristic	Min	Typ	Max	Unit
Input Impedance on MIC and AUX (See Note 1)	46	78	1400	kΩ
Input Capacitance on MIC and AUX	—	—	10	pF
Peak Input Voltage on the MIC/AUX Input for Full Scale Linearity (0.14 dBm0): (See Note 2) 6 dB - MGS1 - 0 = 00 0 dB - MGS1 - 0 = 01 6 dB - MGS1 - 0 = 10 17 dB - MGS1 - 0 = 11	 — — — —	 — — — —	 1.414 0.707 354 100	 Vp Vp mVp mVp
Internal Input Gain Variation; G = -6 dB, 0 dB, 6 dB or 17 dB (±0.83 dB variation due to 10% variation on V_{CC}):	G - 0.83	G	G + 0.83	dB
VREF Output Voltage	1.8	2	2.2	V
VREF Output Current	—	—	±1	mA
DC Offset Between SPKP and SPKM	—	—	100	mV
Allowable Differential Load Capacitance on SPKP and SPKM (with 1 kΩ in series)	0	—	0.05	µF
Allowable Single-ended Load Capacitance on SPKP or SPKM (with 0.5 kΩ in series)	0 (See Note 3)	—	100 0.1	µF
Maximum Single-ended Signal Output Level	—	—	1	Vp
Maximum Differential Signal Output Level	—	—	2	Vp
Single-ended Load Resistance	500	—	—	Ω
Differential Load Resistance	1	—	—	kΩ
Resistance BIAS	—	10 (See Note 4)	—	kΩ
Internal Output Volume Control Variation VC = -20, -15, -10, -5, 0, 6, 12, 18, 24, 30, 35 dB (± 0.83 dB variation due to 10% variation on V_{CC})	VC - 0.83	VC	VC + 0.83	dB

NOTES:
1. Minimum value reached for a Codec clock of 3 MHz, typical for 2 MHz and maximum for 100 kHz
2. 0 dBm0 corresponds to 3.14 dB below the input saturation level
3. AC coupling is necessary in single-ended mode when the load resistor is not tied to VREF
4. ± 10%

Preliminary

A/D and D/A Performance

(V_{CCA} = 5.0 V dc ± 10%, T_J = -40° to +125°C)

The A/D and D/A performance of the codec section are given in Table 8 with an example presented in Figure 4.

Table 8 A/D and D/A Performance of Codec

Characteristic	Level	Min	Typ (See Note 1)	Max	Unit
Analog to Digital Section Signal to Noise plus Distortion Ratio (S/N+T)	0 dBm0 (See Note 2)	55	65	—	dB
	-50 dBm0	15	20	—	dB
Digital to Analog Section Signal to Noise plus Distortion Ratio (S/N+T)	0 dB	55	65	—	dB
	-50 dB	15	20	—	dB

NOTES: 1. 0 dB gain on the A/D and D/A; Codec clock at 1.538 MHz with 128 decimation/interpolation ratio and tested at 1502 Hz
2. 0 dBm0 corresponds to -3.14 dB below the input saturation level

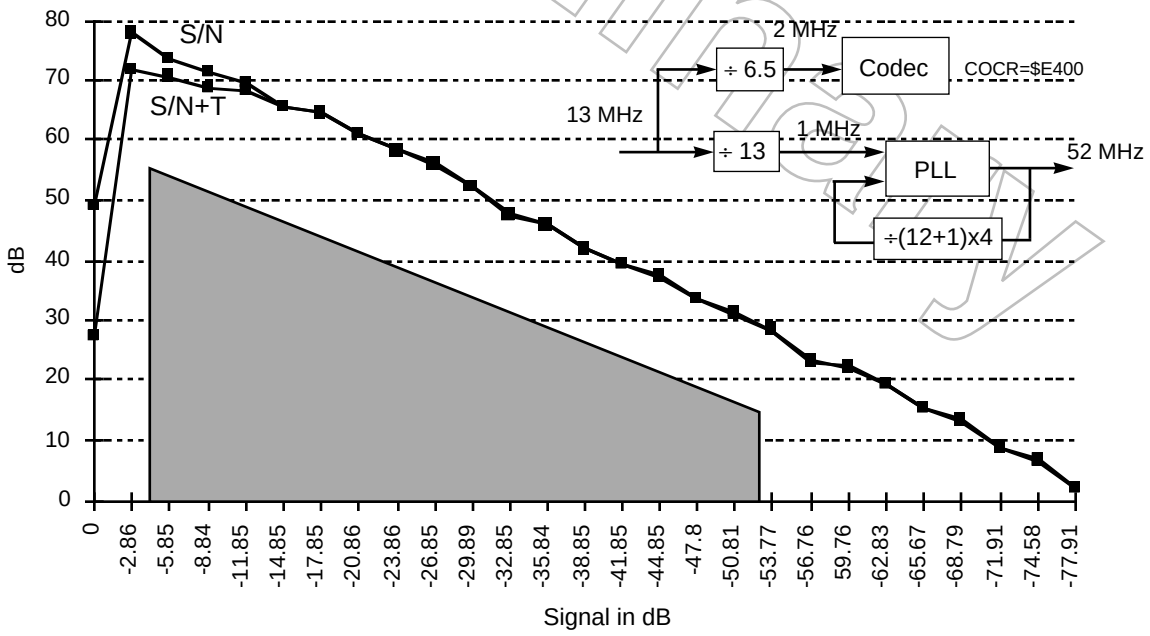


Figure 4 Example: S/N and S/N+T Performance for the A/D Section

Preliminary

Other On-Chip Codec Characteristics

(V_{CCA} = 5.0 V dc ± 10%, T_J = -40° to +125°C, C_L = 50 pF + 1 TTL Load)

The analog I/O characteristics of this device are shown in Table 9.

Table 9 Analog I/O Characteristics of On-Chip Codec

Characteristic	Min	Typ	Max	Unit
Codec Master Clock	0.1	2.048	3	MHz
Codec Sampling Rate	78	16000	37000	Hz
A/D Section Group Delay	—	—	0.2	msec
D/A Section Group Delay	—	—	0.2	msec

Preliminary

DC Electrical Characteristics

(GND = 0 V dc)

(V_{CC} = 5.0 V dc ± 10%, T_J = -40° to +125°C, C_L = 50 pF + 1 TTL Load)

The DC electrical characteristics of this device are shown in Table 10.

Table 10 DC Electrical Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage except EXTAL, $\overline{\text{RESET}}$, MODA, MODB, MODC	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage except EXTAL, MODA, MODB, MODC	V_{IL}	-0.5	—	0.8	V
Input High Voltage EXTAL DC coupled EXTAL AC coupled (See Note 1)	V_{IHC}	 70% of V_{CC} 1	 — —	 V_{CC} V_{CC}	V
Input Low Voltage EXTAL DC coupled EXTAL AC coupled (See Note 1)	V_{ILC}	 -0.5 -0.5	 — —	 20% of V_{CC} V_{CC}-1	V
Input High Voltage $\overline{\text{RESET}}$	V_{IHR}	2.5	—	V_{CC}	V
Input High Voltage MODA, MODB, MODC	V_{IHM}	3.5	—	V_{CC}	V
Input Low Voltage MODA, MODB, MODC	V_{ILM}	-0.5	—	2.0	V
Input Leakage Current EXTAL $\overline{\text{RESET}}$, MODA, MODB, MODC, $\overline{\text{TA}}$, $\overline{\text{DR}}$, $\overline{\text{BR}}$	I_{IN}	 -100 -1	—	 100 1	 µA µA
Three-State (Off-State) Input Current (@2.4 V/0.5 V)	TSI	-10	—	10	µA
Output High Voltage (I_{OH} = -10 µA)	V_{OHC}	V_{CC} -0.1	—	—	V
Output High Voltage (I_{OH} = -0.4 mA)	V_{OH}	2.4	—	—	V
Output Low Voltage (I_{OL} = 10 µA)	V_{OLC}	—	—	0.1	V
Output Low Voltage (I_{OL} = 3.2 mA R/$\overline{\text{W}}$ I_{OL} = 1.6 mA; Open Drain $\overline{\text{HREQ}}$ I_{OL} = 6.7 mA, TXD I_{OL} = 6.7 mA)	V_{OL}	—	—	0.4	V
Input Capacitance (See Note 2)	C_{IN}	—	10	—	pF

NOTES: 1. When EXTAL is AC coupled, V_{IHC} - V_{ILC} ≥ 1 V must be true.
2. Input capacitance is periodically sampled and not 100% tested in production.

Preliminary

AC Electrical Characteristics

(GND = 0 V dc)

The timing waveforms in the **AC Electrical Characteristics** are tested with a V_{IL} maximum of 0.5 V and a V_{IH} minimum of 2.4 V for all pins, except EXTAL, $\overline{RESET}$, MODA, MODB and MODC. These five pins are tested using the input levels set forth in the **DC Electrical Characteristics**. AC timing specifications which are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition. The DSP56156 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.8 V and 2.0 V respectively.

Clock Operation Timing

The system clock to the DSP56156 must be externally supplied to EXTAL as illustrated in Figure 6.

Table 11 Clock Operation Timing

Num	Characteristics	Sym	40 MHz		50 MHz		60 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	Frequency of Operation (EXTAL)	f	0	40	0	50	0	60	MHz
2	Instruction Cycle Time = $2T_C$	I_{CYC}	50	∞	40	∞	33	∞	ns
3	Wait State Time = T_C = 2T	—	25	∞	20	∞	16.6	∞	ns
4	EXTAL Cycle Period	T_C	25	∞	20	∞	16.6	∞	ns
5	EXTAL Rise Time (See Note 1)		—	4	—	3	—	3	ns
6	EXTAL Fall Time (See Note 1)		—	4	—	3	—	3	ns
7	EXTAL Width High 48-52% duty cycle (See Notes 2, 3, 4)	T_H	12	∞	9.6	∞	8	∞	ns
8	EXTAL Width Low 48%-52% duty cycle (See Notes 2, 3, 4)	T_L	12	∞	9.6	∞	8	∞	ns

NOTES: 1. Rise and fall time may be relaxed to 12 ns maximum if the EXTAL input frequency is less than or equal to 20 MHz. If the EXTAL input frequency is between 20 MHz and 40 MHz, rise and fall time should meet the specified values in the 40 MHz column (4 ns maximum).

2. The duty cycle may be relaxed to 43-57% if the EXTAL input frequency is less than or equal to 20 MHz. If the EXTAL input frequency is between 20 MHz and 40 MHz, the duty cycle should be such that T_H and T_L meet the specified values in the 40 MHz column (12 ns minimum).

3. $T = I_{CYC} / 4$ is used in the electrical characteristics. The exact length of each T is affected by the duty cycle of the external clock input.

4. Duty cycles and EXTAL widths are measured at the EXTAL input signal midpoint when AC coupled and at $V_{CC}/2$ when not AC coupled.

Preliminary

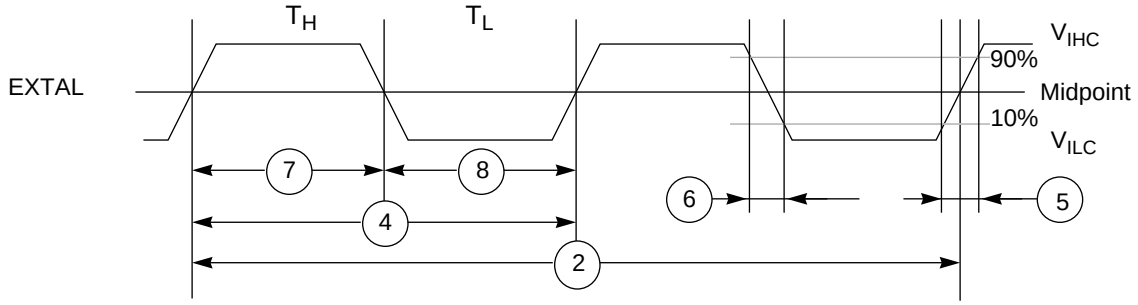


Figure 5 External Clock Timing

Other Clock and PLL Operation Timing

Clock and PLL timings are listed in Table 12 and the clocking configurations are illustrated in Figure 6.

Table 12 Clock and PLL Timing

Characteristics	Min	Max	Unit
PLL Output frequency	10	Max Fosc (See Note 1)	MHz
EXTAL Input Clock Amplitude (See Note 2)	1	V_{CC}	Vpp

NOTES: 1. Maximum DSP operating frequency. See Table 11.
2. An AC coupling capacitor is required on EXTAL if the levels are out of the normal CMOS level range (V_{ILC}>20% of V_{CC} or V_{IHC}<70% of V_{CC}).

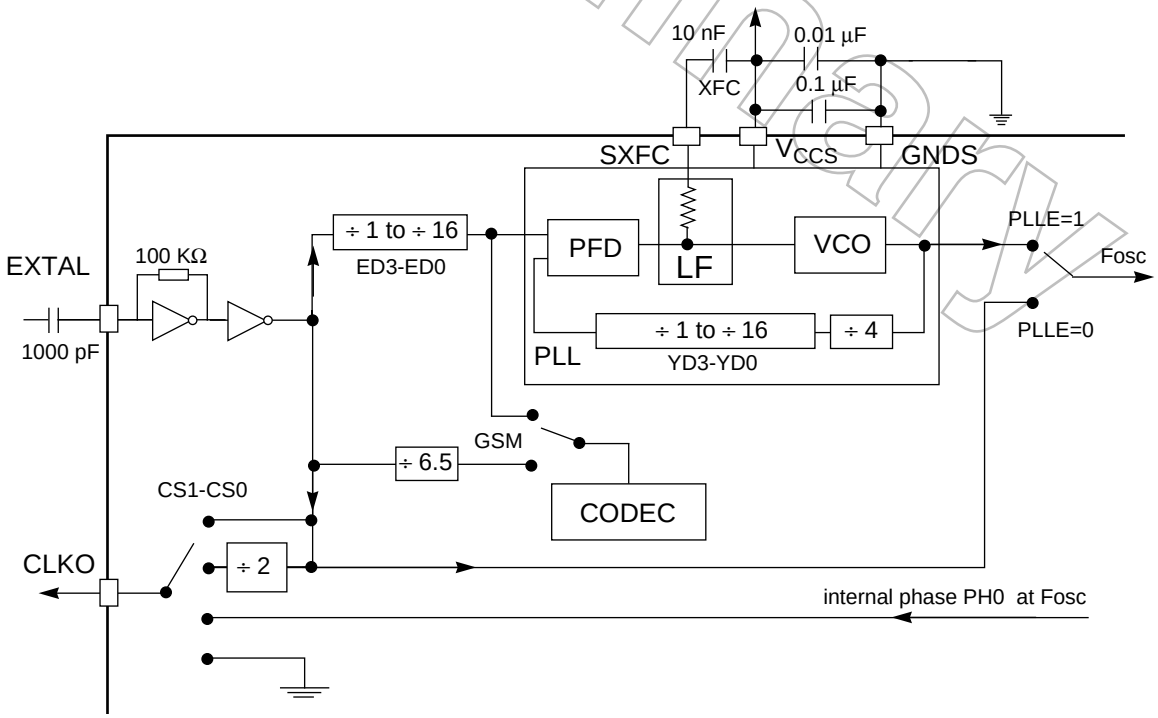


Figure 6 Clocking Configurations

Preliminary

Reset, Stop, Wait, Mode Select, and Interrupt Timing

(V_{CC} = 5.0 V dc ± 10%, T_J = -40° to +125°C, C_L = 50 pF + 1 TTL Load)
cyc = Clock cycle = $^1/_2$ instruction cycle = 2 T cycles
ws = Number of wait states programmed into external bus access using BCR (WS = 0 - 31)

Table 13 Reset, Stop, Wait, Mode Select, and Interrupt Timing

Num	Characteristics	40 MHz		50 MHz		60 MHz		Unit
		Min	Max	Min	Max	Min	Max	
10	$\overline{\text{RESET}}$ Assertion to Address, Data and Control Signals High Impedance	—	25	—	23	—	21	ns
11	Minimum Stabilization Duration (See Note 1) OMR bit 6=0 OMR bit 6=1	600KT 60T	— —	600KT 60T	— —	600KT 60T	— —	ns ns
12	Asynchronous $\overline{\text{RESET}}$ Deassertion to First External Address Output (See Note 7)	16T	18T+20	16T	18T+17	16T	18T+15	ns
13	Synchronous Reset Setup Time from $\overline{\text{RESET}}$ Deassertion to Rising Edge of CLKO	7	cyc-4	6	cyc-3	5	cyc-2	ns
14	Synchronous Reset Delay Time from CLKO High to the First External Access (See Note 7)	16T+3	16T+20	16T+ 3	16T+18	16T+3	16T+16	ns
15	Mode Select Setup Time	22	—	20	—	18	—	ns
16	Mode Select Hold Time	0	—	0	—	0	—	ns
17	Edge-triggered Interrupt Request Width	13	—	11	—	9	—	ns
18	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to External Data Memory Access Out Valid - Caused by First Interrupt Instruction Fetch - Caused by First Interrupt Instruction Execution	11T+4 19T+4	— —	11T+4 19T+4	— —	11T+3 19T+3	— —	ns ns
19	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to General Purpose Output Valid Caused by the Execution of the First Interrupt Instruction	22T+5	—	22T+4	—	22T+3	—	ns
20	Delay from External Data Memory Address Output Valid Caused by First Interrupt Instruction Execution to Interrupt Request Deassertion for Level Sensitive Fast Interrupts (See Note 2)	—	5T-26 + cyc × ws	—	5T-24 + cyc × ws	—	5T-22 + cyc × ws	ns

Preliminary

(V_{CC} = 5.0 V dc ± 10%, T_J = -40° to +125°C, C_L = 50 pF + 1 TTL Load)

Table 13 Reset, Stop, Wait, Mode Select, and Interrupt Timing (continued)

Num	Characteristics	40 MHz		50 MHz		60 MHz		Unit
		Min	Max	Min	Max	Min	Max	
21	Delay from General-Purpose Output Valid Caused by the Execution of the First Interrupt Instruction to $\overline{IRQA}$, $\overline{IRQB}$ Deassertion for Level Sensitive Fast Interrupts — If 2nd Interrupt Instruction is:							
	Single Cycle (See Note 2)	—	cyc - 29	—	cyc - 27	—	cyc - 26	ns
	Two Cycles	—	3 cyc - 29	—	3 cyc - 27	—	3 cyc - 26	ns
22	Synchronous setup time from $\overline{IRQA}$, $\overline{IRQB}$ assertion to Synchronous falling edge of CLKO (See Notes 5 and 6)	14	cyc-3	13	cyc-2	12	cyc-1	ns
23	Falling Edge of CLKO to First Interrupt Vector Address Out Valid after Synchronous recovery from Wait State (See Notes 3 and 5)	27T+3	27T+20	27T+3	27T+18	27T+3	27T+16	ns
24	$\overline{IRQA}$ Width Assertion to Recover from Stop State (See Note 4)	15	—	13	—	12	—	ns
25	Delay from $\overline{IRQA}$ Assertion to Fetch of first instruction (exiting Stop) (See Notes 1 and 3)							
	OMR bit 6=0	524303T+4	—	524303T+3	—	524303T+3	—	ns
	OMR bit 6=1	47T+4	—	47T+3	—	47T+3	—	ns
28	Duration for Level Sensitive $\overline{IRQA}$ Assertion to Cause the Fetch of First $\overline{IRQA}$ Interrupt Instruction (exiting Stop) (See Notes 1 and 3)							
	OMR bit 6=0	524303T	—	524303T	—	524303T	—	ns
	OMR bit 6=1	47T	—	47T	—	47T	—	ns
29	Delay from Level Sensitive $\overline{IRQA}$ Assertion to First Interrupt Vector Address Out Valid (exiting Stop) (See Notes 1 and 3)							
	OMR bit 6=0	524303T+4	—	524303T+3	—	524303T+3	—	ns
	OMR bit 6=1	47T+4	—	47T+3	—	47T+3	—	ns

Preliminary

NOTES:

1. Circuit stabilization delay is required during reset when using an external clock in two cases:
   - after power-on reset
   - when recovering from Stop mode
2. When using fast interrupts, $\overline{IRQA}$ or $\overline{IRQB}$ is defined as level-sensitive, then timings 20 and 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the negative edge-triggered mode is recommended when using fast interrupts.
3. The interrupt instruction fetch is visible on the pins only in Mode 3.
4. The minimum is specified for the duration of an edge triggered $\overline{IRQA}$ interrupt required to recover from the Stop state. This is not the minimum required so that the $\overline{IRQA}$ interrupt is accepted.
5. Timing #22 is for all IRQx interrupts while timing #23 is only when exiting the Wait state.
6. Timing #22 triggers off T1 in the normal state and off phi1 when exiting the Wait state.
7. The instruction fetch is visible on the pins only in Mode 2 and Mode 3.

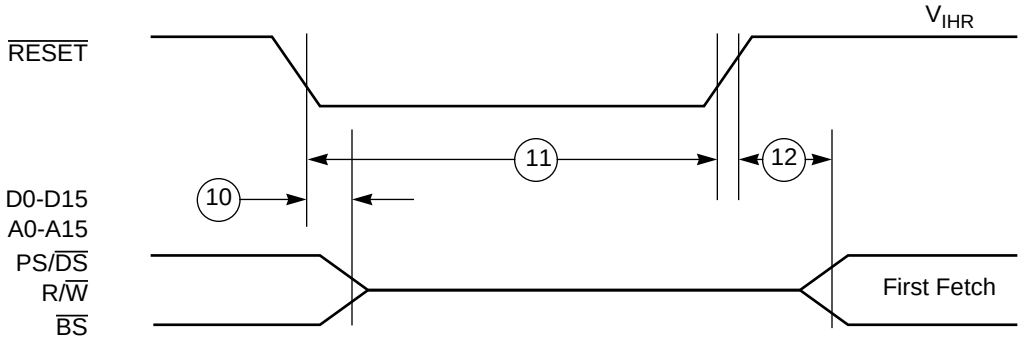


Figure 7 Asynchronous Reset Timing

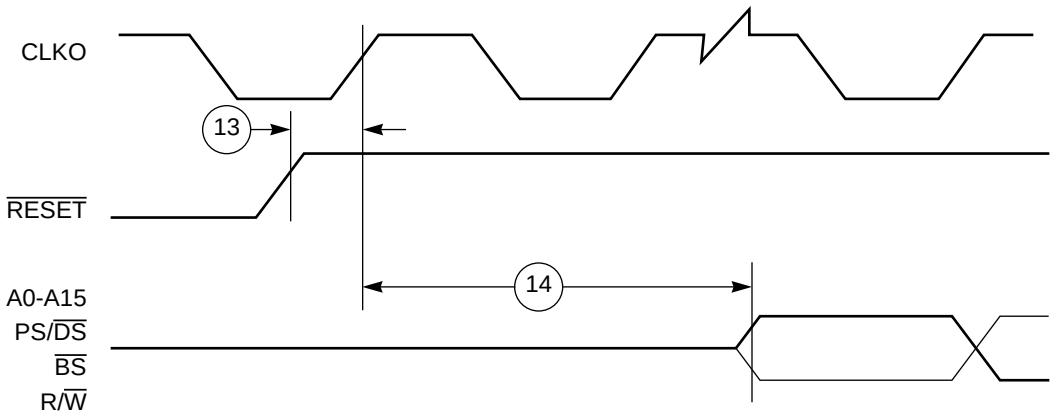


Figure 8 Synchronous Reset Timing

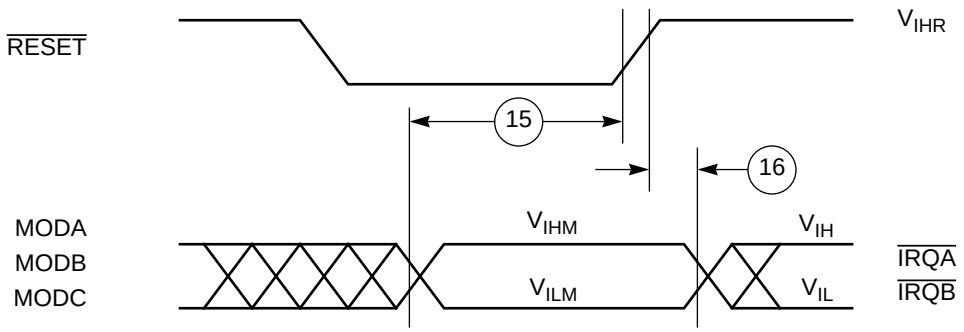


Figure 9 Operating Mode Select Timing

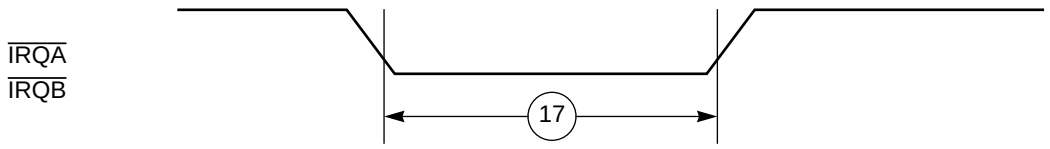


Figure 10 External Interrupt Timing (Negative Edge-Triggered)

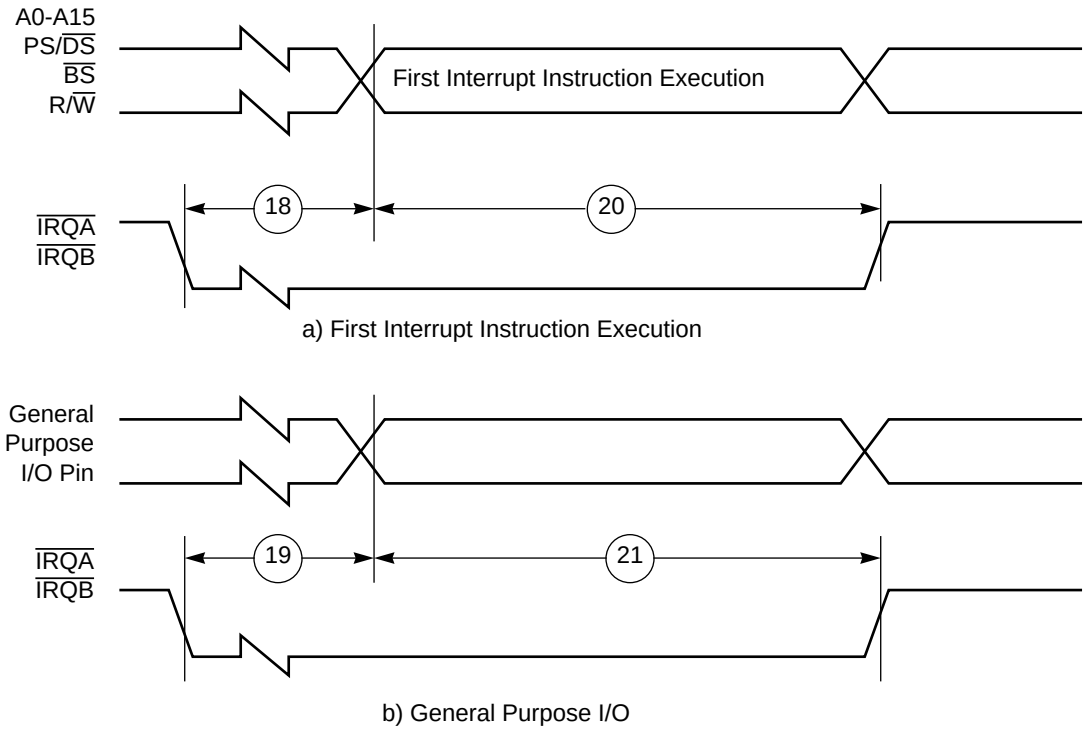


Figure 11 External Level-Sensitive Fast Interrupt Timing

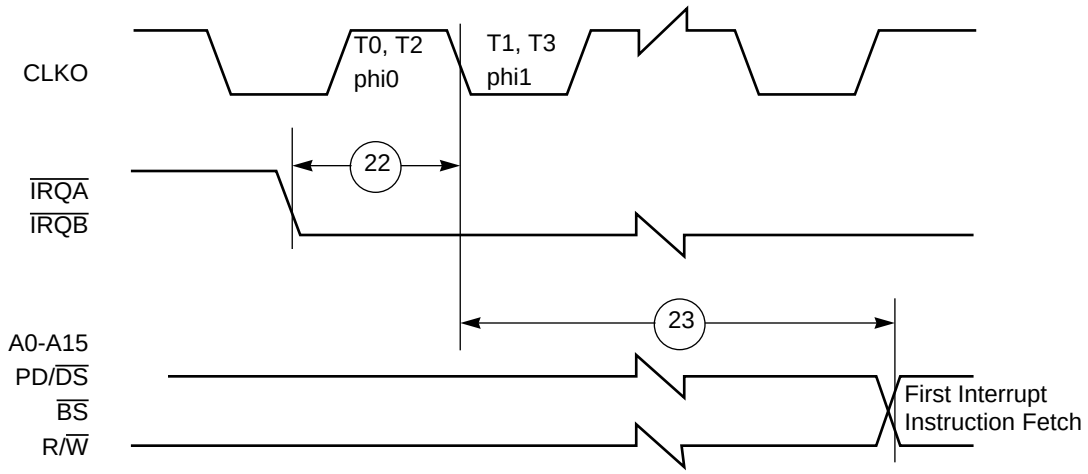


Figure 12 Synchronous Interrupt from Wait State Timing

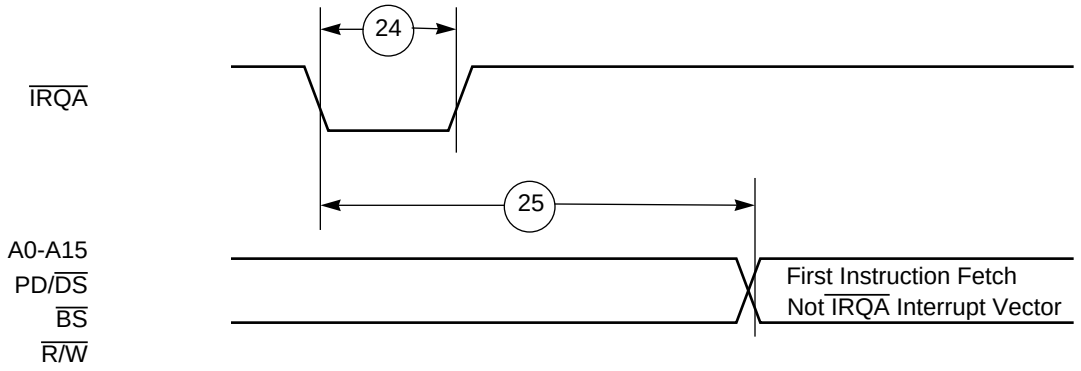


Figure 13 Recovery from Stop State Using Asynchronous Interrupt Timing

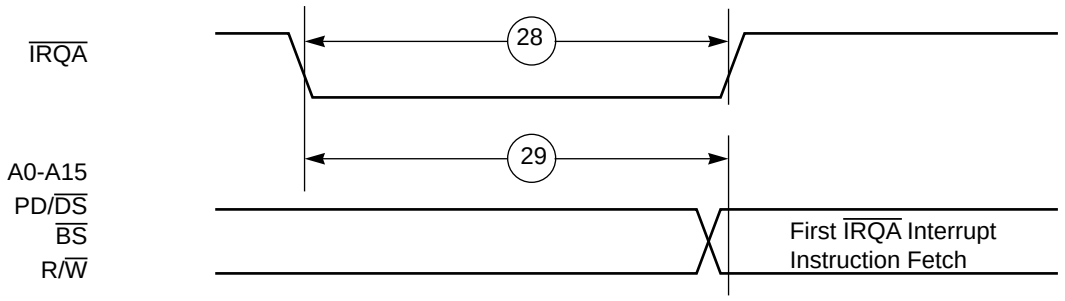


Figure 14 Recovery from Stop State Using $\overline{\text{IRQA}}$ Interrupt Service

Table 14 Wait and Stop Timings

Num	Characteristics	40 MHz		50 MHz		60 MHz		Unit
		Min	Max	Min	Max	Min	Max	
30	$\overline{DR}$ Asserted to CLK high (Setup Time for Synchronous Recovery from Wait State)	10	cyc - 4	9	cyc - 3	8	cyc - 2	ns
31	CLK high to DSO ($\overline{ACK}$) Valid (Enter Debug Mode) after Synchronous Recovery from Wait State	18 cyc	—	18 cyc	—	18 cyc	—	ns
32	$\overline{DR}$ to DSO ($\overline{ACK}$) Valid (Enter Debug Mode)							
	- After Asynchronous Recovery from Stop State	29 cyc	—	29 cyc	—	29 cyc	—	ns
	- After Asynchronous Recovery from Wait State	18 cyc	—	18 cyc	—	18 cyc	—	ns
33	$\overline{DR}$ Assertion Width							
	- to Recover from Wait/Stop without entering debug mode	12	10 cyc	11	10 cyc	10	10 cyc	ns
	- to Recover from Wait/Stop short wake-up and enter debug mode	29 cyc	—	29 cyc	—	29 cyc	—	ns
	- to Recover from Stop long wake-up and enter debug mode	262157 cyc	—	262157 cyc	—	262157 cyc	—	ns

Preliminary

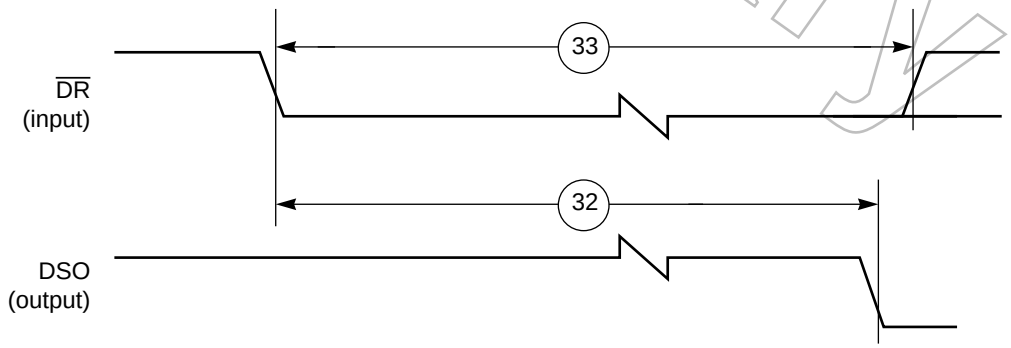


Figure 15 Recovery from Wait State Using $\overline{DR}$ Pin — Synchronous Timing

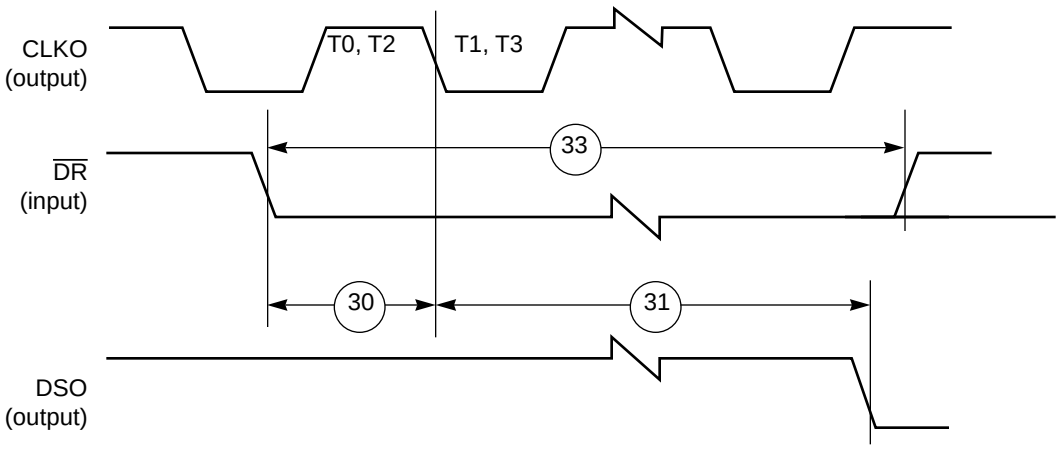


Figure 16 Recovery from Wait/Stop State Using $\overline{DR}$ Pin — Asynchronous Timing

Capacitance Derating

The DSP56156 External Bus Timing Specifications are designed and tested at the maximum capacitive load of 50 pF, including stray capacitance. Typically, the drive capability of the External Bus pins (A0-A15, D0-D15, PS/$\overline{DS}$, $\overline{RD}$, $\overline{BS}$, $\overline{WR}$, R/$\overline{W}$) derates linearly at 1 ns per 12 pF of additional capacitance from 50 pF to 250 pF of loading. Port B and C pins derate linearly at 1 ns per 5 pF of additional capacitance from 50 pF to 250 pF of loading.

When an internal memory access follows an external memory access, the PS/$\overline{DS}$, R/$\overline{W}$, $\overline{RD}$ and $\overline{WR}$ strobes remain deasserted and A0-A15 do not change from their previous state.

External Bus Synchronous Timing

(V_{CC} = 5.0 V dc ± 10%, T_J = -40° to +125°C, C_L = 50 pF + 1 TTL Load)

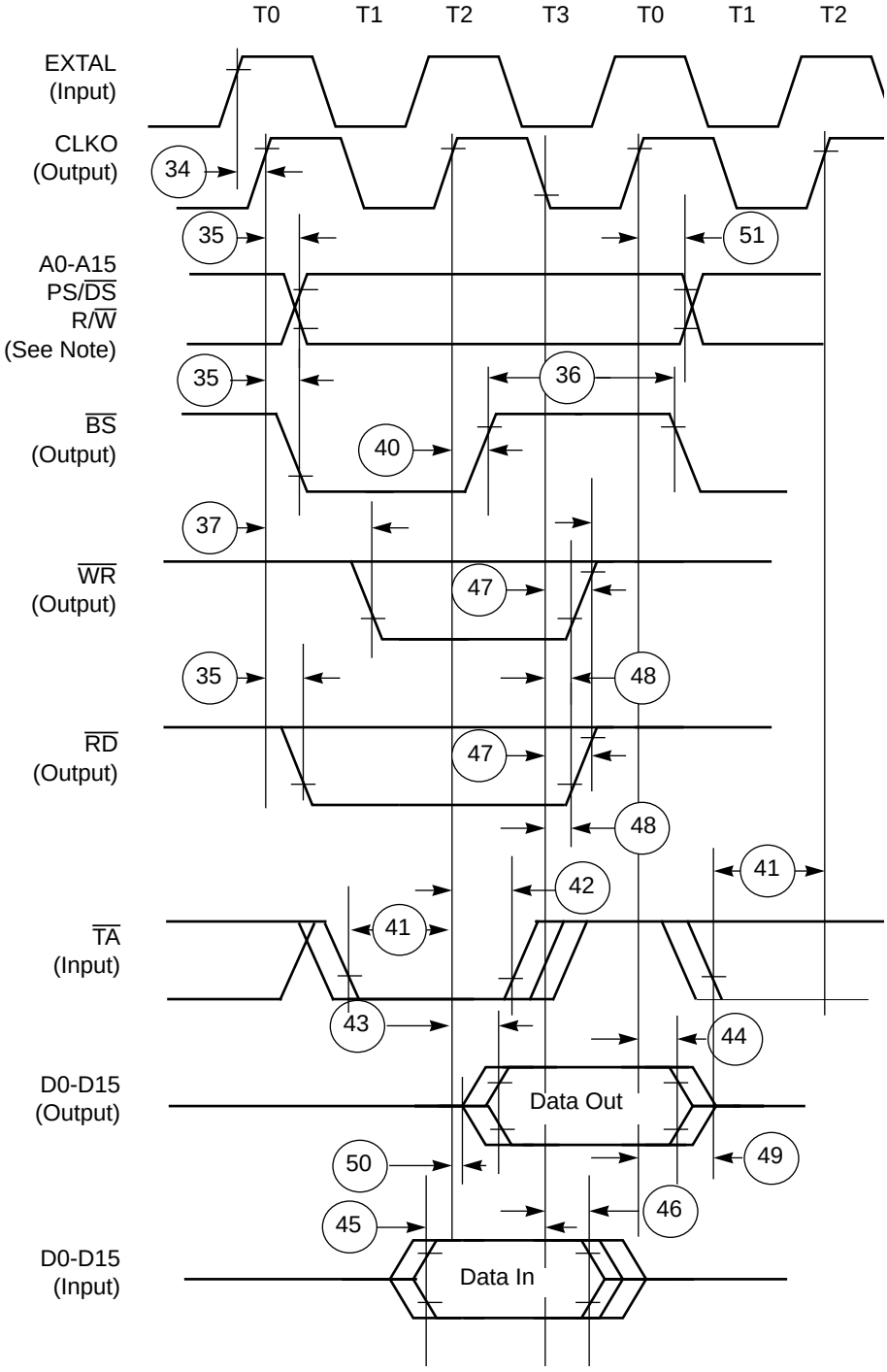
Table 15 lists external bus synchronous timing. Figure 17 and Figure 18 illustrate the bus timings with no wait states and two wait states, respectively.

Table 15 External Bus Synchronous Timing

Num	Characteristic	40 MHz		50 MHz		60 MHz		Unit
		Min	Max	Min	Max	Min	Max	
34	EXTAL CLK In High to CLKO High	2.4	9	2.4	9	2.4	9	ns
35	CLKO High to a. A0-A15 Valid	4.7	12	4.7	12	4.7	12 (See Note)	ns
	b. PS/$\overline{DS}$, R/$\overline{W}$ Valid, $\overline{BS}$, $\overline{RD}$ Asserted	4.7	14	4.7	14	4.7	4	ns
36	$\overline{BS}$ Width Deasserted	18.3	—	13.4	—	9.8	—	ns
37	CLKO High to $\overline{WR}$ Asserted Low	T+3.1	T+12.4	T+3.1	T+12.4	T+3.1	T+12.4	ns
38	$\overline{WR}$ and $\overline{RD}$ Deasserted High to $\overline{BS}$ Asserted Low (2 Successive Bus Cycles)	14.3	15.8	11.8	13.3	10.2	11.8	ns
39	<intentionally blank>							
40	CLKO High to $\overline{BS}$ Deasserted	2.6	10.3	2.6	10.3	2.6	10.3	ns
41	$\overline{TA}$ Valid to CLKO High (Setup)	4.5	—	4.5	—	4.5	—	ns
42	CLKO High to $\overline{TA}$ Invalid (Hold)	0	—	0	—	0	—	ns
43	CLKO High to D0-D15 Out Valid	1.7	7.1	1.7	7.1	1.7	7.1	ns
44	CLKO High to D0-D15 Out Invalid	2.0	—	2.0	—	2.0	—	ns
45	D0-D15 In Valid to CLKO Low (Setup)	6	—	6	—	6	—	ns
46	CLKO Low to D0-D15 In Invalid (Hold)	0	—	0	—	0	—	ns
47	CLKO Low to $\overline{WR}$, $\overline{RD}$ Deasserted	—	10	—	10	—	10	ns
48	$\overline{WR}$, $\overline{RD}$ Hold Time from CLKO Low	2.2	—	2.2	—	2.2	—	ns
49	CLKO High to D0-D15 Three-state	0	6	0	6	0	6	ns
50	CLKO High to D0-D15 Out Active	1.2	4.2	1.2	4.2	1.2	4.2	ns
51	CLKO High to A0-A15, PS/$\overline{DS}$, R/$\overline{W}$ Invalid	2.8	—	2.8	—	2.8	—	ns

NOTE: 10 ns C_L = 25 pF

Preliminary



NOTE: During Read-Modify-Write instructions and internal instructions, the address lines do not change state.

Figure 17 External Bus Synchronous Timing — No Wait States

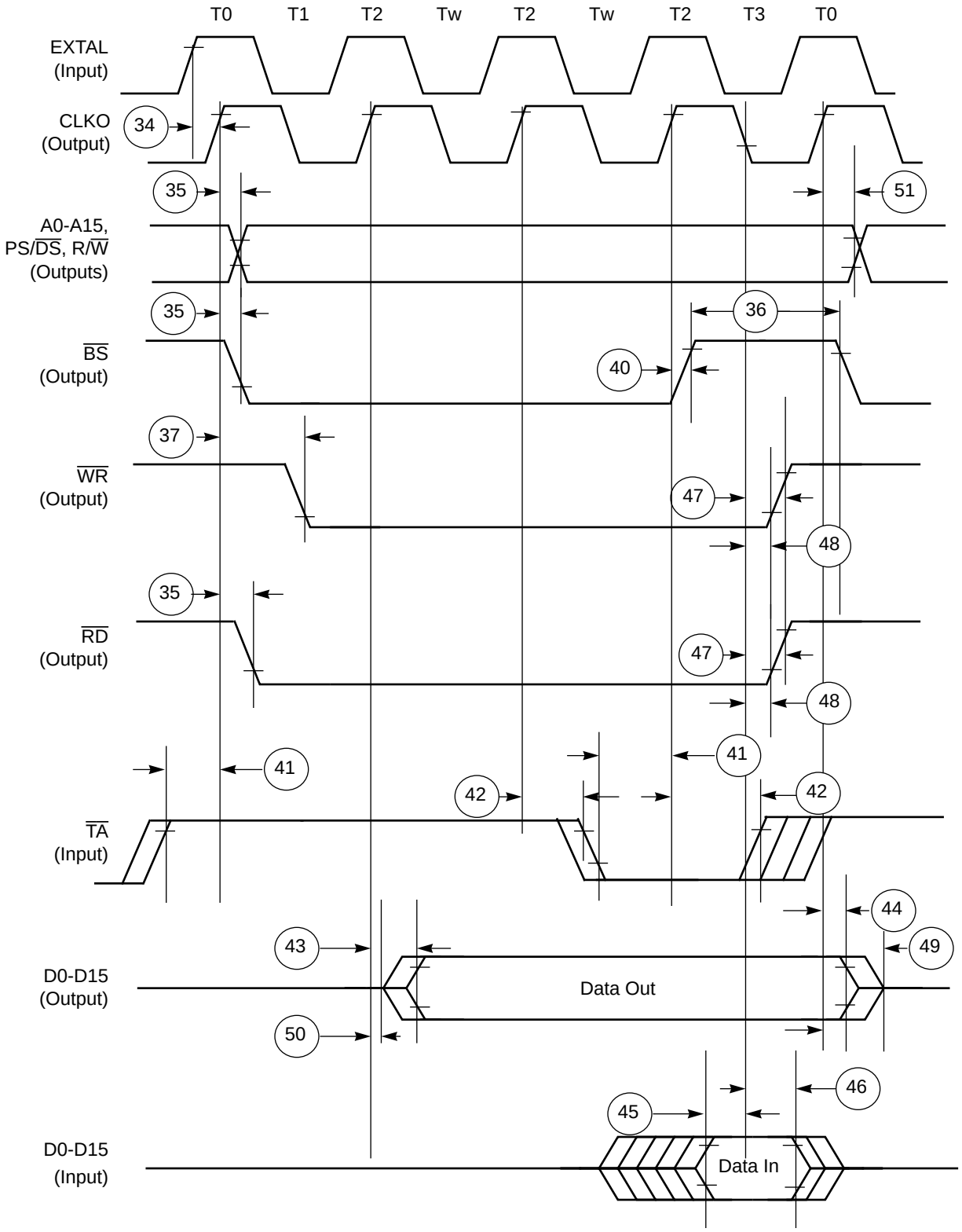


Figure 18 External Bus Synchronous Timing – Two Wait States

External Bus Asynchronous Timing

(V_{CC} = 5.0 V dc ± 10%, T_J = -40° to +125°C, C_L = 50 pF + 1 TTL Load)

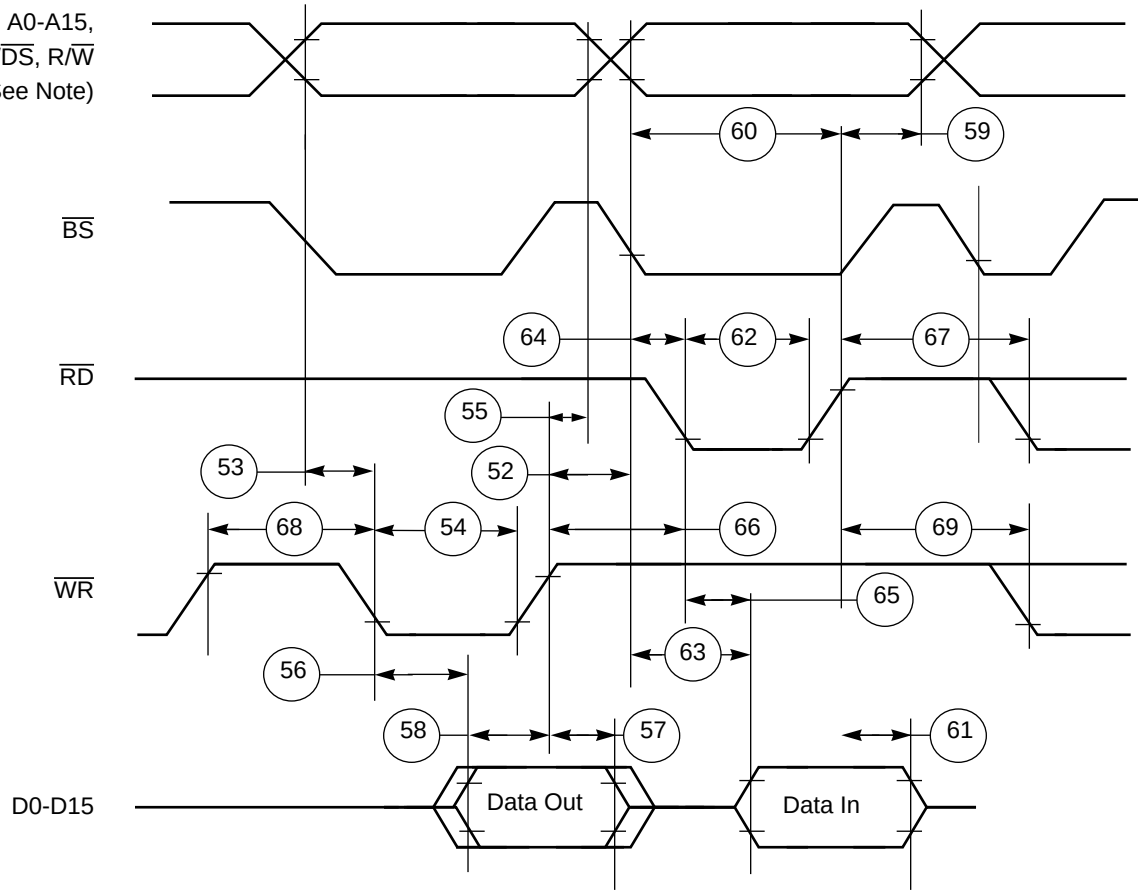
cyc = Clock cycle = $^1/_2$ instruction cycle = 2 T cycles
WS = Number of Wait States, Determined by BCR Register (WS = 0 to 31)
WT = WS × cyc = 2T × WS

Table 16 External Bus Asynchronous Timing

Num	Characteristic	40 MHz		50 MHz		60 MHz		Unit
		Min	Max	Min	Max	Min	Max	
52	$\overline{WR}$ and $\overline{RD}$ deasserted High to $\overline{BS}$ Asserted Low (2 Successive Bus Cycles)	14.3	15.8	11.8	13.3	10.2	11.8	ns
53	Address Valid to $\overline{WR}$ Asserted	13.2	16.7	10.8	14.2	9	12.6	ns
54	$\overline{WR}$ Width Asserted WS=0 WS>0	 20.2 WT+20.2	 — —	 15.1 WT+15.1	 — —	 11.8 WT+11.8	 — —	ns
55	$\overline{WR}$ Deasserted to R/$\overline{W}$ Address Invalid	9.7	—	7.3	—	5.7	—	ns
56	$\overline{WR}$ Asserted to D0-D15 Out Valid	7.1	11.0	4.5	8.4	2.8	6.9	ns
57	Data Out Hold Time from $\overline{WR}$ Deasserted	6.3	11.5	3.7	9	2.2	7.7	ns
58	Data Out Set Up Time to $\overline{WR}$ Deasserted WS=0 WS>0	 13.7 WT+13.7	 — —	 11.3 WT+11.3	 — —	 9.5 WT+9.5	 — —	ns
59	$\overline{RD}$ Deasserted to Address Not Valid	7.2	—	4.8	—	3.1	—	ns
60	Address Valid to $\overline{RD}$ Deasserted	37.9	—	30.5	—	25.3	—	ns
61	Input Data Hold to $\overline{RD}$ Deasserted	0.0	—	0.0	—	0.0	—	ns
62	$\overline{RD}$ Assertion Width WS=0 WS>0	 31.2 WT+31.2	 — —	 23.8 WT+23.8	 — —	 18.6 W+18.6	 — —	ns
63	Address Valid to Input Data Valid WS=0 WS>0	 — —	 20 WT+20	 — —	 12 WT+12	 — —	(See Note 1) 8 WT+8	ns
64	Address Valid to $\overline{RD}$ Asserted (See Note 2)	2.2	5.7	2.2	5.7	2.2	5.7	ns
65	$\overline{RD}$ Asserted to Input Data Valid WS=0 WS>0	 — —	 20 WT+20	 — —	 12 WT+12	 — —	(See Note 1) 8 WT+8	ns
66	$\overline{WR}$ Deasserted to $\overline{RD}$ Asserted	14.3	—	11.8	—	10.2	—	ns
67	$\overline{RD}$ Deasserted to $\overline{RD}$ Asserted	14.3	—	11.8	—	10.2	—	ns
68	$\overline{WR}$ Deasserted to $\overline{WR}$ Asserted	25.3	—	20.3	—	17.0	—	ns
69	$\overline{RD}$ Deasserted to $\overline{WR}$ Asserted	25.3	—	20.3	—	17.0	—	ns

NOTES: 1. 10 ns for C_L = 25 pF
2. The PS/$\overline{DS}$ transition can be delayed with respect to the Address transition and occur after $\overline{RD}$ assertion.

Preliminary



NOTE: During Read-Modify-Write instructions and internal instructions, the address lines do not change state.

Figure 19 External Bus Asynchronous Timing

Bus Arbitration Timing — Slave Mode

(V_{CC} = 5.0 V dc ± 10%, T_J = -40° to +125°C, C_L = 50 pF + 1 TTL Load)

cyc = Clock cycle = $^1/_2$ instruction cycle = 2 T cycles
WS = Number of Wait States for external X or P memory, Determined by BCR Register (WS = 0 to 31)
WT = WS × cyc=2T × WS
WX = Number of Wait States for external X memory, Determined by BCR Register (WS = 0 to 31)
WP = Number of Wait States for external P memory, Determined by BCR Register (WS = 0 to 31)

Table 17 Slave Mode

Num	Characteristics		40/50/60 MHz Min	40/50/60 MHz Max	Unit
70	$\overline{BR}$ Input to CLKO low setup time		0	1	ns
71	Delay from $\overline{BR}$ Input Assertion to $\overline{BG}$ Output Assertion	(See Note 1) (See Note 2) (See Note 3) (See Note 4) (See Note 5)	5T+1.9 3T+1.9 5T+1.9 NA T+1.9	9T+4.2 6T+WT+4.2 26T+4T x WX +2T x WP+4.2 NA 3T+4.2	ns
72	CLKO high to $\overline{BG}$ Output Assertion		1.9	5.2	ns
73	$\overline{BG}$ Output Deassertion Duration	(See Note 1) (See Note 5) (See Note 6)	5T-0.5 2T-0.5 3T-0.5	— — —	ns
74	CLKO High to Control Bus High Impedance		2.7	6.5	ns
75	CLKO High to $\overline{BB}$ Output Deassertion		3.2	7.8	ns
76	CLKO High to $\overline{BB}$ Input		3.3	8.1	ns
77	$\overline{BR}$ Input Deassertion to $\overline{BG}$ Output Deassertion	(See Note 1) (See Note 5) (See Note 7)	4T+2.5 3T+3.2 3T+3.2	9T+6.4 8T+7.8 8T+8.0	ns
78	CLKO Low to $\overline{BG}$ Deassertion CLKO High to $\overline{BG}$ Deassertion CLKO High to $\overline{BG}$ Deassertion	(See Note 1) (See Note 5) (See Note 7)	2.5 3.2 3.2	6.4 7.8 8.0	ns
79	CLKO High to $\overline{BB}$ Output Active		1.3	3.6	ns
80	CLKO High to $\overline{BB}$ Output Assertion		2.3	5	ns
81	CLKO High to Address and Control Bus Active		1	3	ns
82	CLKO High to Address and Control Bus Valid		2	4.4	ns

NOTES:
1. With no external access from the DSP56156
2. During external read or write access
3. During external read-modify-write access
4. During Stop mode — external bus is released and $\overline{BG}$ is always low
5. During Wait mode
6. With external accesses pending by the DSP56156
7. Slave mode, when bus is still busy after bus request has been deasserted

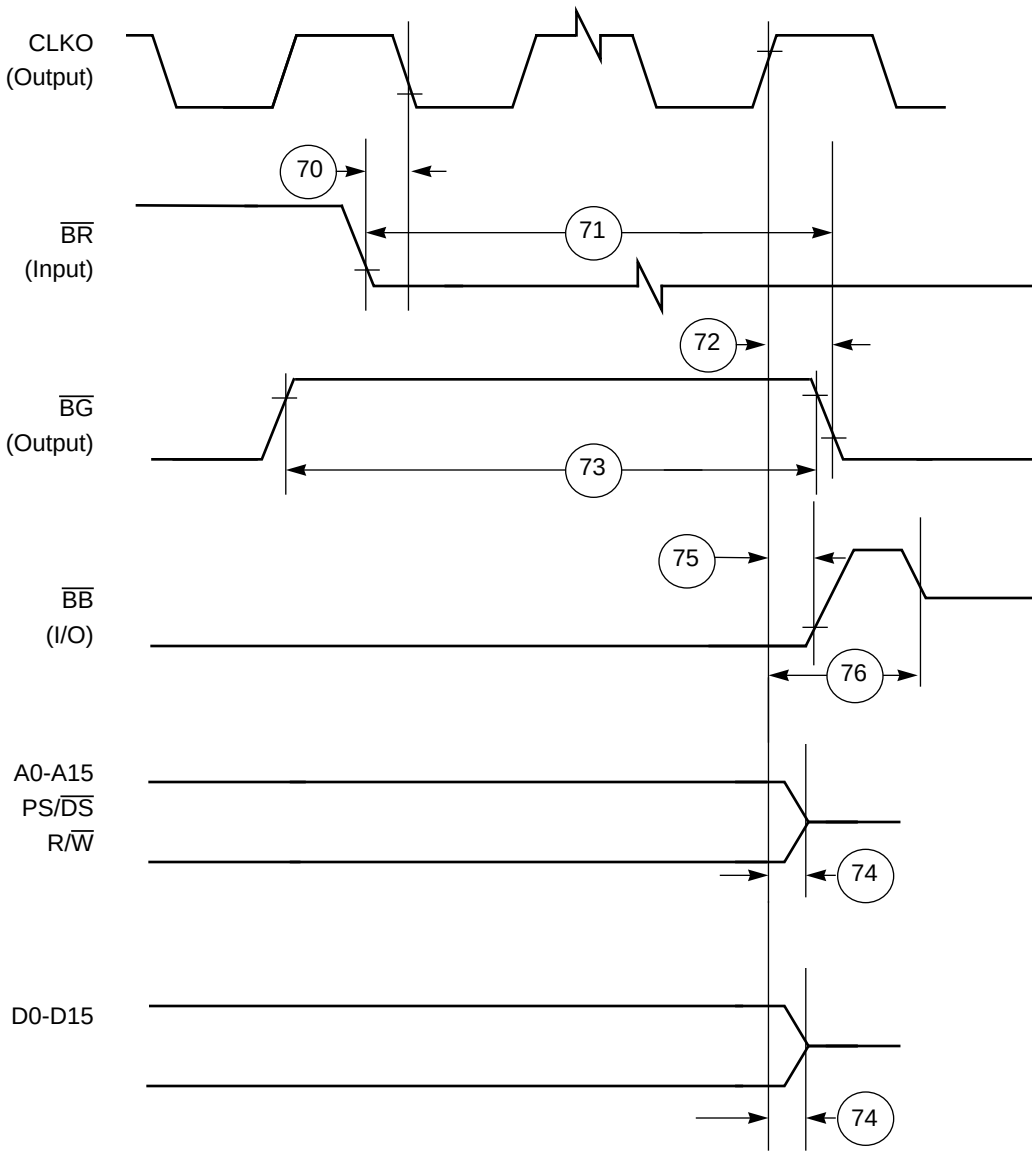


Figure 20 Bus Arbitration Timing — Slave Mode — Bus Release

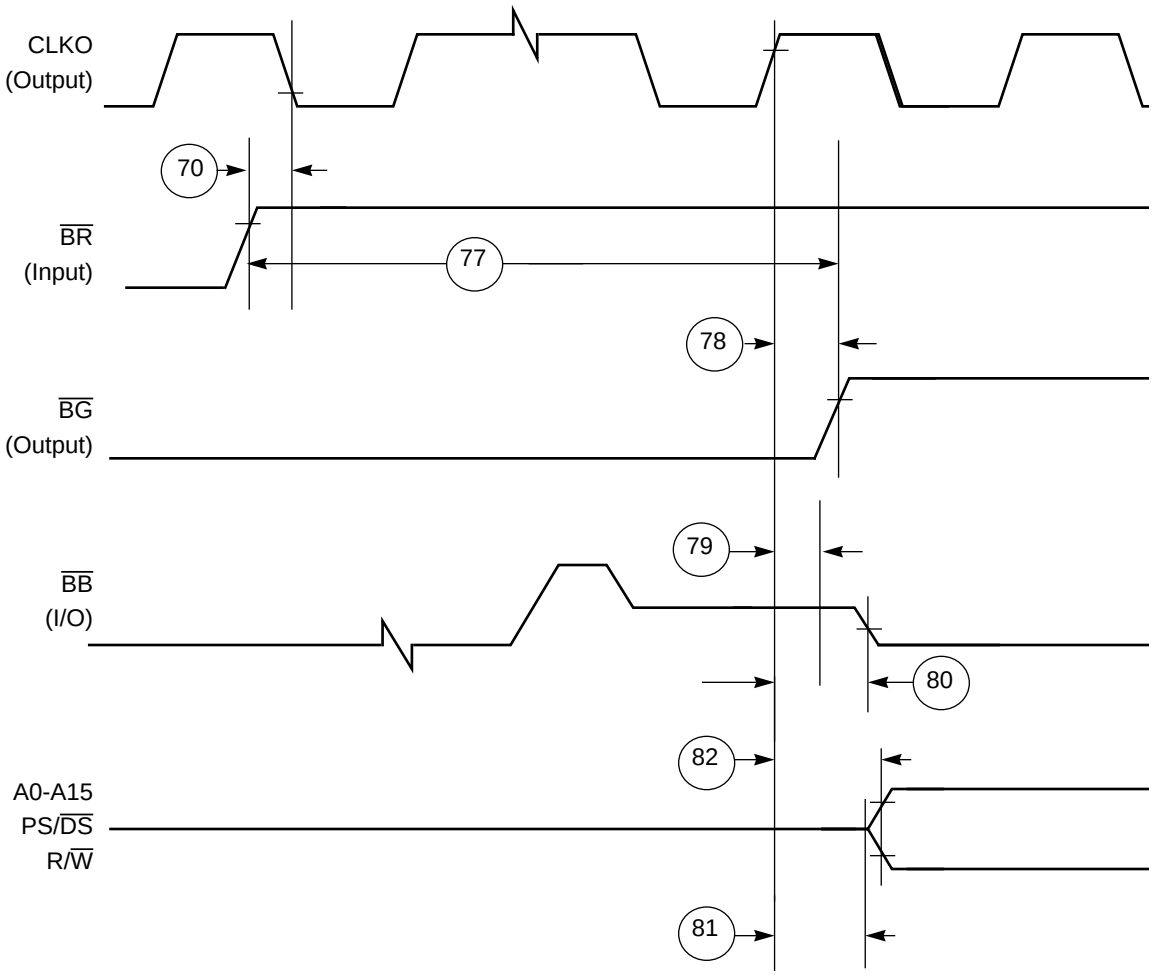


Figure 21 Bus Arbitration Timing — Slave Mode — Bus Acquisition

Bus Arbitration Timing — Master Mode

(V_{CC} = 5.0 V dc ± 10%, T_J = -40° to +125°C, C_L = 50 pF + 1 TTL Load)

Table 18 Master Mode

Num	Characteristic	40 MHz		50 MHz		60 MHz		Unit
		Min	Max	Min	Max	Min	Max	
85	CLKO High to $\overline{BR}$ Output Assertion CLKO High to $\overline{BR}$ Output Deassertion	4.7	12	4.7	12	4.7	12	ns
86	$\overline{BG}$ Input Asserted/ Deasserted to CLKO Low (Setup)	9.2	—	6.5	—	4.5	—	ns
87	CLKO Low to $\overline{BG}$ Input Invalid (Hold)	0	—	0	—	0	—	ns
88	$\overline{BB}$ Input Deasserted to CLKO Low (Setup)	9.2	—	6.5	—	4.5	—	ns
89	CLKO Low to $\overline{BB}$ Input Deasserted (Hold)	0	—	0	—	0	—	ns
90	CLKO High to $\overline{BB}$ Output Asserted	4.7	12	4.7	12	4.7	12	ns

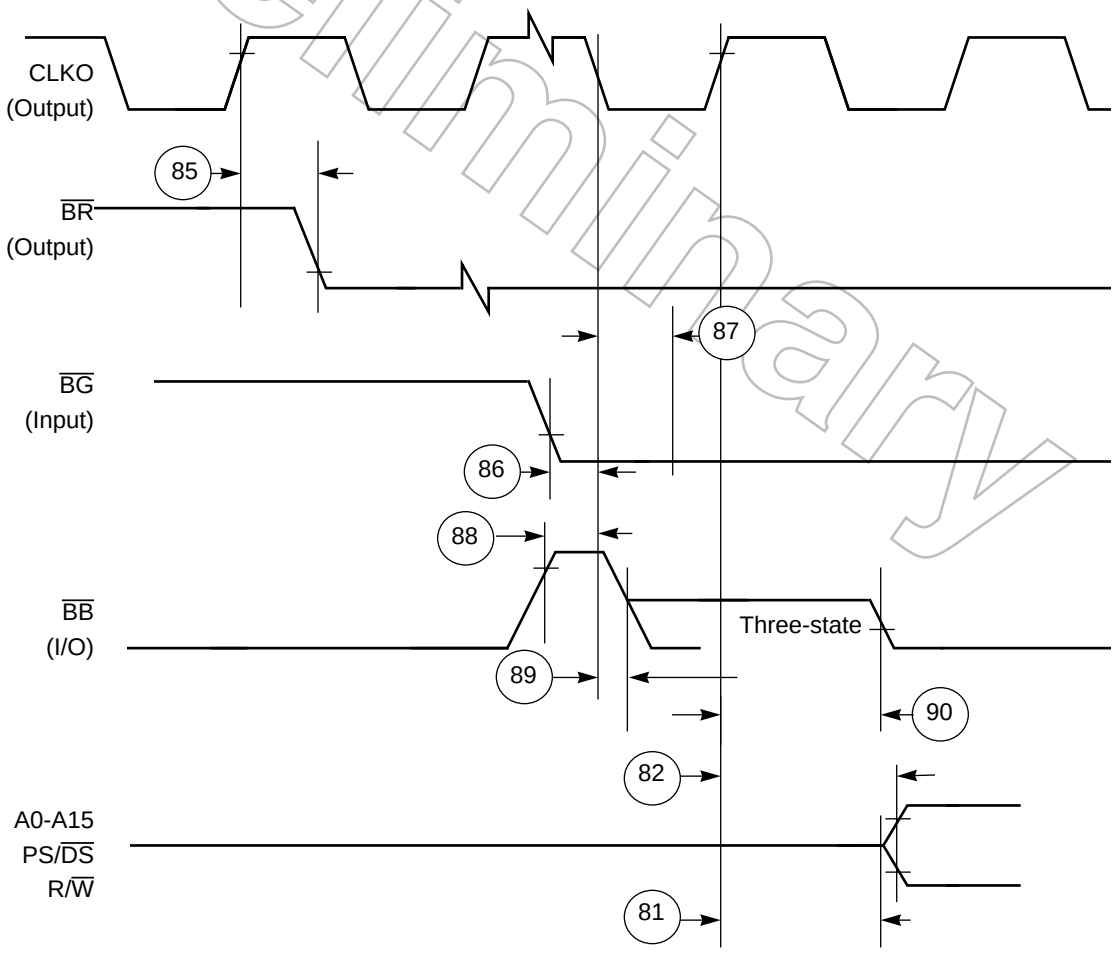


Figure 22 Bus Arbitration Timing — Master Mode — Bus Acquisition

Preliminary

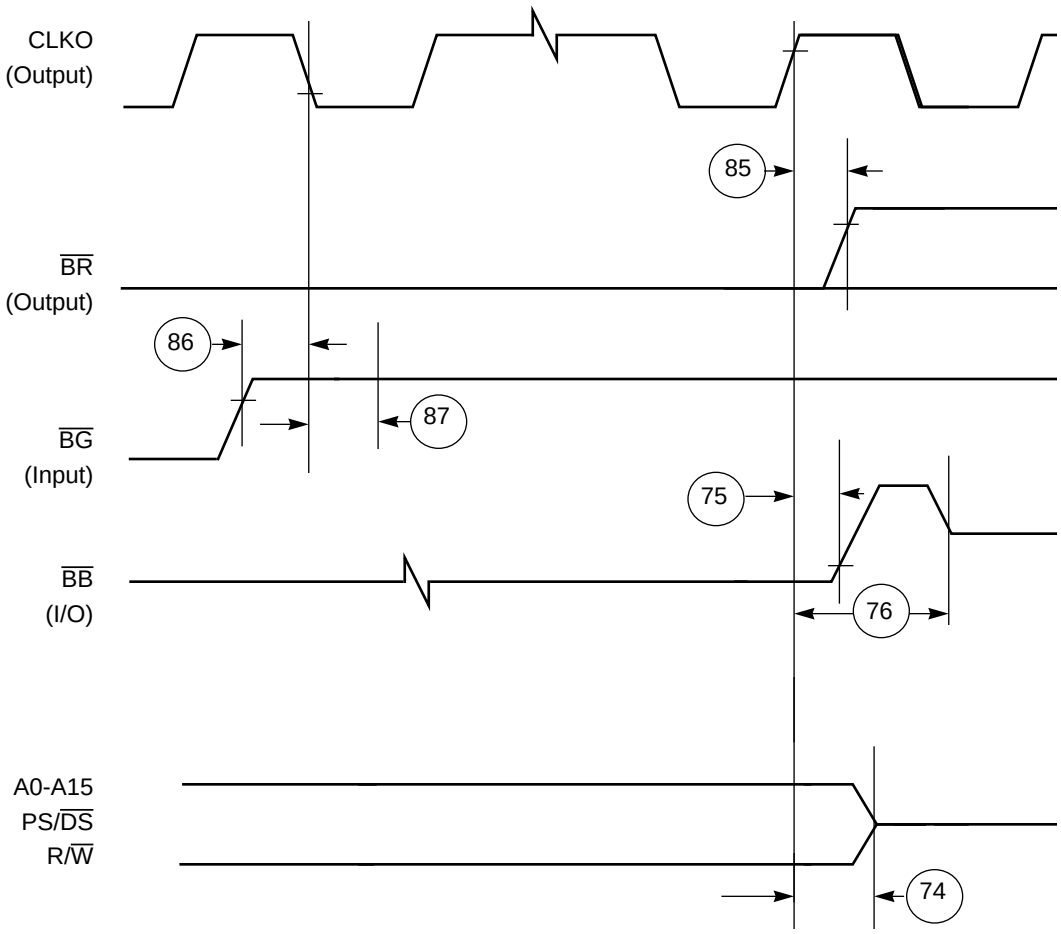


Figure 23 Bus Arbitration Timing — Master Mode — Bus Release

Host Port Timing

(V_{CC} = 5.0 V dc ± 10%, T_J = -40° to +125°C, C_L = 50 pF + 1 TTL Load)

T = I_{CYC} / 4
cyc = Clock cycle = $^1/_2$ instruction cycle= 2 T cycle
t_{HSDL} = Host Synchronization Delay Time (See Note 1)
t_{suh} = Host Processor Data Setup Time

Active low lines should be "pulled up" in a manner consistent with the AC and DC specifications.

Preliminary

Table 19 Host Port Timing

Num	Characteristic	40 MHz		50 MHz		60 MHz		Unit
		Min	Max	Min	Max	Min	Max	
100	tHSDL Host Synchronous Delay (See Note 1)	T	3T	T	3T	T	3T	ns
101	$\overline{HEN}/\overline{HACK}$ Assertion Width • CVR, ICR, ISR Read • Read • Write (See Notes 2, 4)	 2T+36 $32+t_{suh}$ 32	 — —	 2T+33 $29+t_{suh}$ 29	 — —	 2T+30 $26+t_{suh}$ 26	 — —	ns
102	$\overline{HEN}/\overline{HACK}$ Deassertion Width (See Note 2)	31	—	29	—	27	—	ns
103	Minimum Cycle Time Between Two $\overline{HEN}$ Assertion for Consecutive CVR, ICR, ISR Reads	4T+36	—	4T+33	—	4T+30	—	ns
104	Host Data Input Setup Time before $\overline{HEN}/\overline{HACK}$ Deassertion	5	—	4	—	3	—	ns
105	Host Data Input Hold Time after $\overline{HEN}/\overline{HACK}$ Deassertion	7	—	6	—	5	—	ns
106	$\overline{HEN}/\overline{HACK}$ Assertion to Output Data Active from High Impedance	0	—	0	—	0	—	ns
107	$\overline{HEN}/\overline{HACK}$ Assertion to Output Data Valid	—	32	—	29	—	26	ns
108	$\overline{HEN}/\overline{HACK}$ Deassertion to Output Data High Impedance	—	20	—	18.5	—	17	ns
109	Output Data Hold Time after $\overline{HEN}/\overline{HACK}$ Deassertion	5	—	5	—	4	—	ns

Table 19 Host Port Timing (continued)

Num	Characteristic	40 MHz		50 MHz		60 MHz		Unit
		Min	Max	Min	Max	Min	Max	
110	HR/$\overline{W}$ Low Setup Time before $\overline{HEN}$ Assertion	6	—	5	—	4	—	ns
111	HR/$\overline{W}$ Low Hold Time after $\overline{HEN}$ Deassertion	6	—	5	—	4	—	ns
112	HR/$\overline{W}$ High Setup Time to $\overline{HEN}$ Assertion	6	—	5	—	4	—	ns
113	HR/$\overline{W}$ High Hold Time after $\overline{HEN}$/$\overline{HACK}$ Deassertion	5	—	4	—	3	—	ns
114	HA0-HA2 Setup Time before $\overline{HEN}$ Assertion	9	—	7.5	—	6	—	ns
115	HA0-HA2 Hold Time after $\overline{HEN}$ Deassertion	8	—	7	—	6	—	ns
116	DMA $\overline{HACK}$ Assertion to $\overline{HREQ}$ Deassertion (See Note 3)	5	2T +37	5	2T +36	4	2T +35	ns
117	DMA $\overline{HACK}$ Deassertion to $\overline{HREQ}$ Assertion (See Note 3)							
	for DMA RXL Read	t_{HSDL} +3T+5	—	t_{HSDL} 3T+5	—	t_{HSDL} +3T+4	—	ns
	for DMA TXL Write	t_{HSDL} +2T+5	—	t_{HSDL} +2T+5	—	t_{HSDL} +2T+4	—	ns
	for All Other Cases	5	—	5	—	4	—	ns
118	Delay from $\overline{HEN}$ Deassertion to $\overline{HREQ}$ Assertion for RXL Read (See Note 3)	t_{HSDL} +3T+5	—	t_{HSDL} +3T+5	—	t_{HSDL} +3T+4	—	ns
119	Delay from $\overline{HEN}$ Deassertion to $\overline{HREQ}$ Assertion for TXL Write (See Note 3)	t_{HSDL} +2T+5	—	t_{HSDL} +2T+5	—	t_{HSDL} +2T+4	—	ns
120	Delay from $\overline{HEN}$ Assertion to $\overline{HREQ}$ Deassertion for RXL Read, TXL Write (See Note 3)	5	2T +37	5	2T +36	5	2T +35	ns

NOTES:
1. "Host Synchronization Delay (tHSDL)" is the time period required for the DSP56156 to sample any external asynchronous input signal, determine whether it is high or low, and synchronize it to the internal clock.
2. See **Host Port Considerations**.
3. $\overline{HREQ}$ is pulled up by 1 kΩ.
4. Only if two consecutive reads from one of these registers are executed.

Preliminary

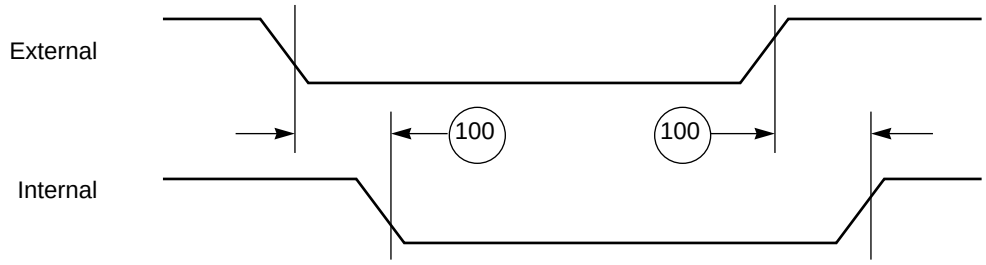


Figure 24 Host Synchronization Delay

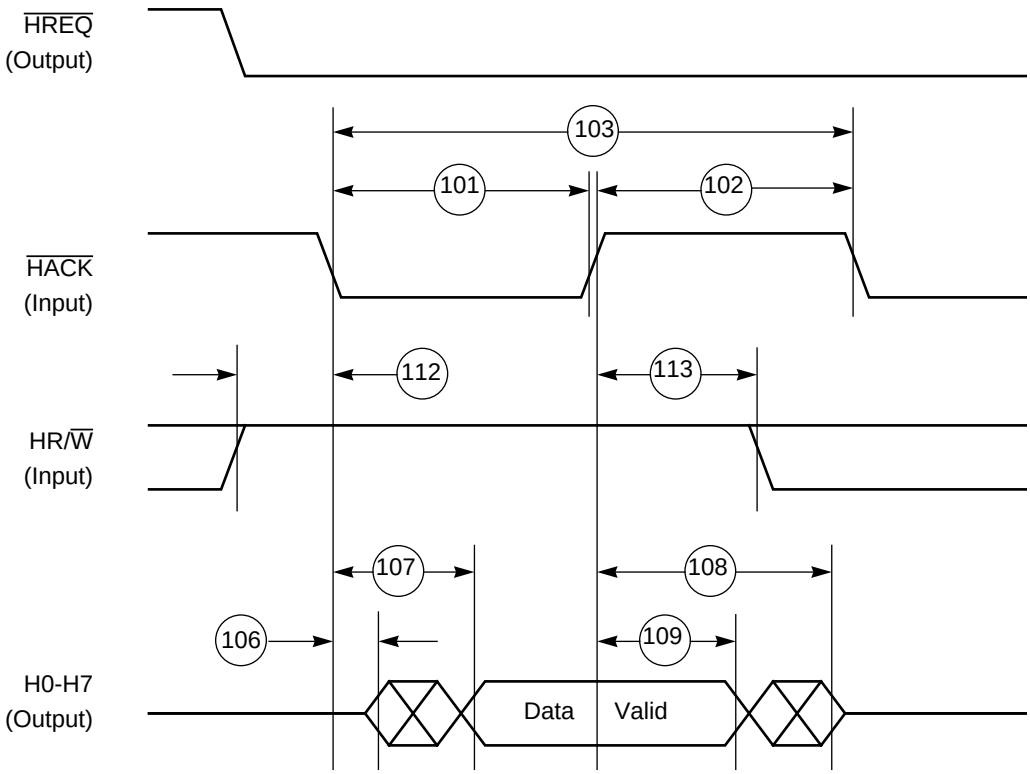


Figure 25 Host Interrupt Vector Register (IVR) Read

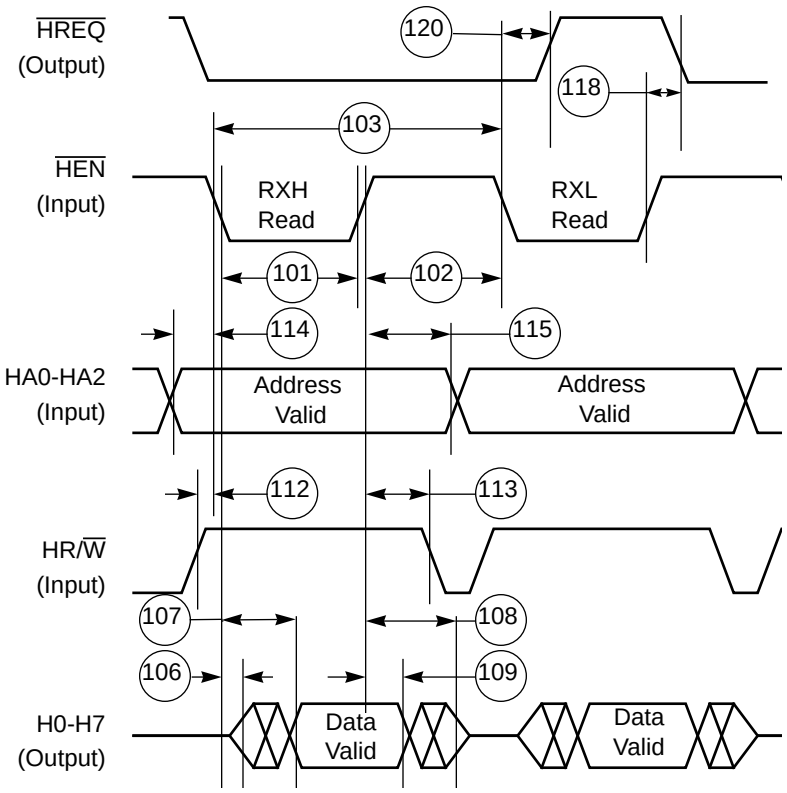


Figure 26 Host Read Cycle (Non-DMA Mode)

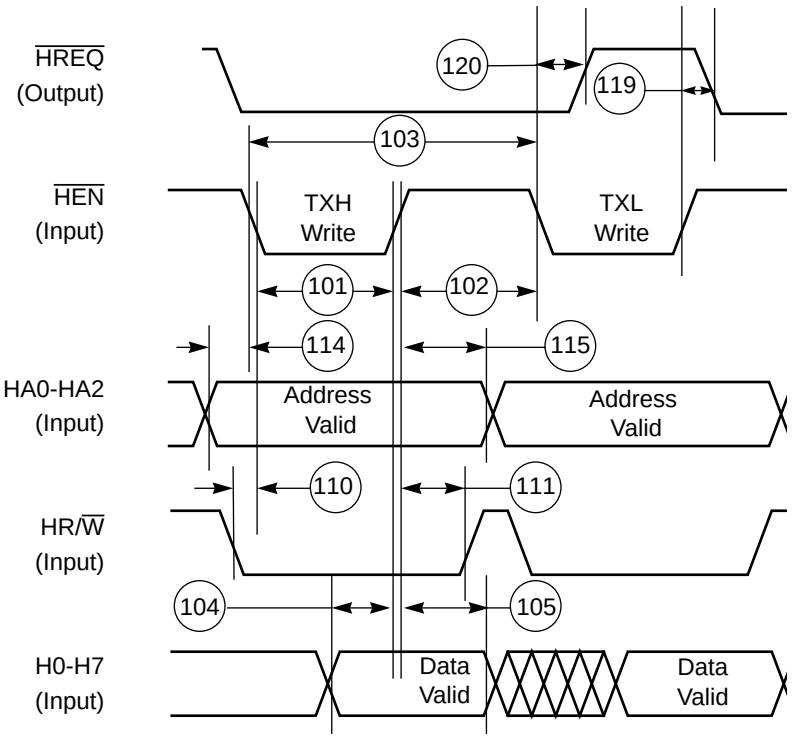


Figure 27 Host Write Cycle (Non-DMA Mode)

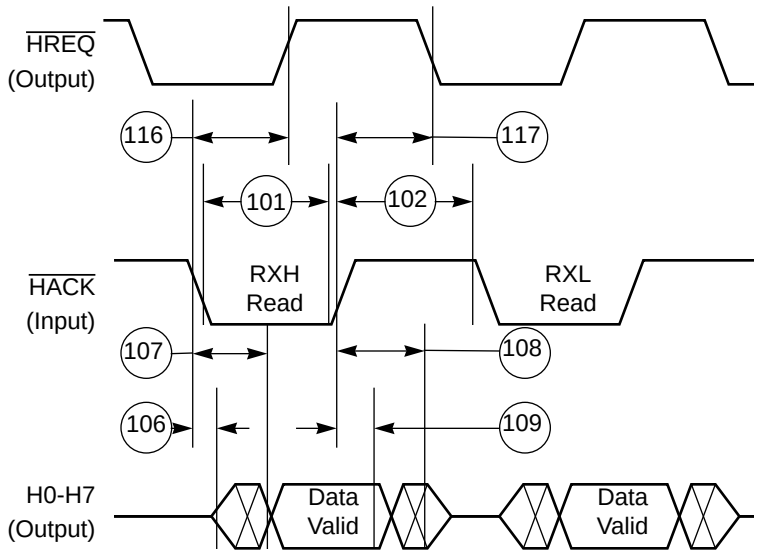


Figure 28 Host Read Cycle (DMA Mode)

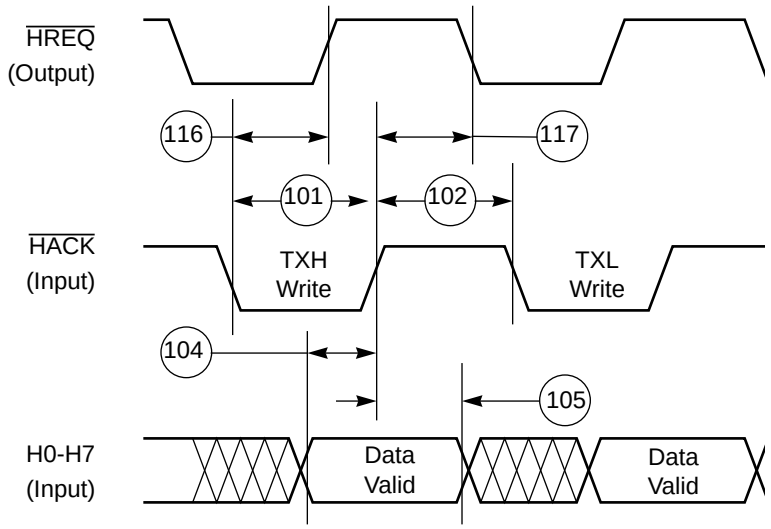


Figure 29 Host Write Cycle (DMA Mode)

Synchronous Serial Interfaces (SSI) Timing

(V_{CC} = 5.0 V dc ± 10%, T_J = -40° to + 125°C, C_L = 50 pF + 1 TTL Load)

T = I_{CYC} / 4
SCK = Serial Clock Pin
FST (Transmit Frame Sync) = SCx0 Pin
FSR (Receive Frame Sync) = SCx1 Pin
i ck = Internal Clock
x ck = External Clock
i ck a = Internal Clock, Asynchronous Mode (Asynchronous implies that FSR and FST are two different frame syncs)
i ck s = Internal Clock, Synchronous Mode (Synchronous implies that only one frame sync FS is used)
bl = bit length
wl = word length

Preliminary

Table 20 Synchronous Serial Interfaces Timing

Num	Characteristic	40/50/60 MHz		Case	Unit
		Min	Max		
130	Clock Cycle (See Note)	100	—	—	ns
131	Clock High Period	45	—	—	ns
132	Clock Low Period	45	—	—	ns
133	Output Clock Rise/Fall Time	—	7	—	ns
134	SCK Rising Edge to FSR Out (bl) High	— —	32 18	x ck i ck a	ns
135	SCK Rising Edge to FSR Out (bl) Low	— —	32 15	x ck i ck a	ns
136	SCK Rising Edge to FSR Out (wl) High	— —	32 15	x ck i ck a	ns
137	SCK Rising Edge to FSR Out (wl) Low	— —	32 15	x ck i ck a	ns
138	Data In Setup Time before SCK Falling Edge	30 40	— —	x ck i ck	ns
139	Data In Hold Time after SCK Falling Edge	25 12	— —	x ck i ck	ns

NOTE: All the timings for the SSI are given for a non-inverted serial clock polarity (SCKP=0 in CRB) and a non-inverted frame sync (FSI=0 in CRB). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal SCK and/or the frame sync FSR/FST in the tables and in the figures.

Table 20 Synchronous Serial Interfaces Timing (continued)

Num	Characteristic	40/50/60MHz		Case	Unit
		Min	Max		
140	FSR Input (bl) High before SCK Falling Edge	7 15	— —	x ck i ck a	ns
141	FSR Input (wl) High before SCK Falling Edge	7 15	— —	x ck i ck a	ns
142	FSR Input Hold Time after SCK Falling Edge	15 7	— —	x ck i ck a	ns
143	Flags Input Setup before SCK Falling Edge	7 15	— —	x ck i ck	ns
144	Flags Input Hold Time after SCK Falling Edge	15 7	— —	x ck i ck	ns
145	SCK Rising Edge to FST Out (bl) High	— —	33 15	x ck i ck	ns
146	SCK Rising Edge to FST Out (bl) Low	— —	30 15	x ck i ck	ns
147	SCK Rising Edge to FST Out (wl) High	— —	30 15	x ck i ck	ns
148	SCK Rising Edge to FST Out (wl) Low	— —	33 15	x ck i ck	ns
149	SCK Rising Edge to Data Out Enable from High Impedance	— —	30 12	x ck i ck	ns
150	SCK Rising Edge to Data Out Valid	— —	30 12	x ck i ck	ns
151	SCK Rising Edge to Data Out High Impedance	— —	30 20	x ck i ck	ns
152	FST Input (bl) Setup Time before SCK Falling Edge	6 16	— —	x ck i ck	ns
153	FST Input (wl) to Data Out Enable from High Impedance	—	36	—	ns
154	FST Input (wl) Setup Time before SCK Falling Edge	8 17	— —	x ck i ck	ns
155	FST Input Hold Time after SCK Falling Edge	15 4	— —	x ck i ck	ns
156	Flag Output Valid after SCK Rising Edge	— —	32 15	x ck i ck	ns

Preliminary

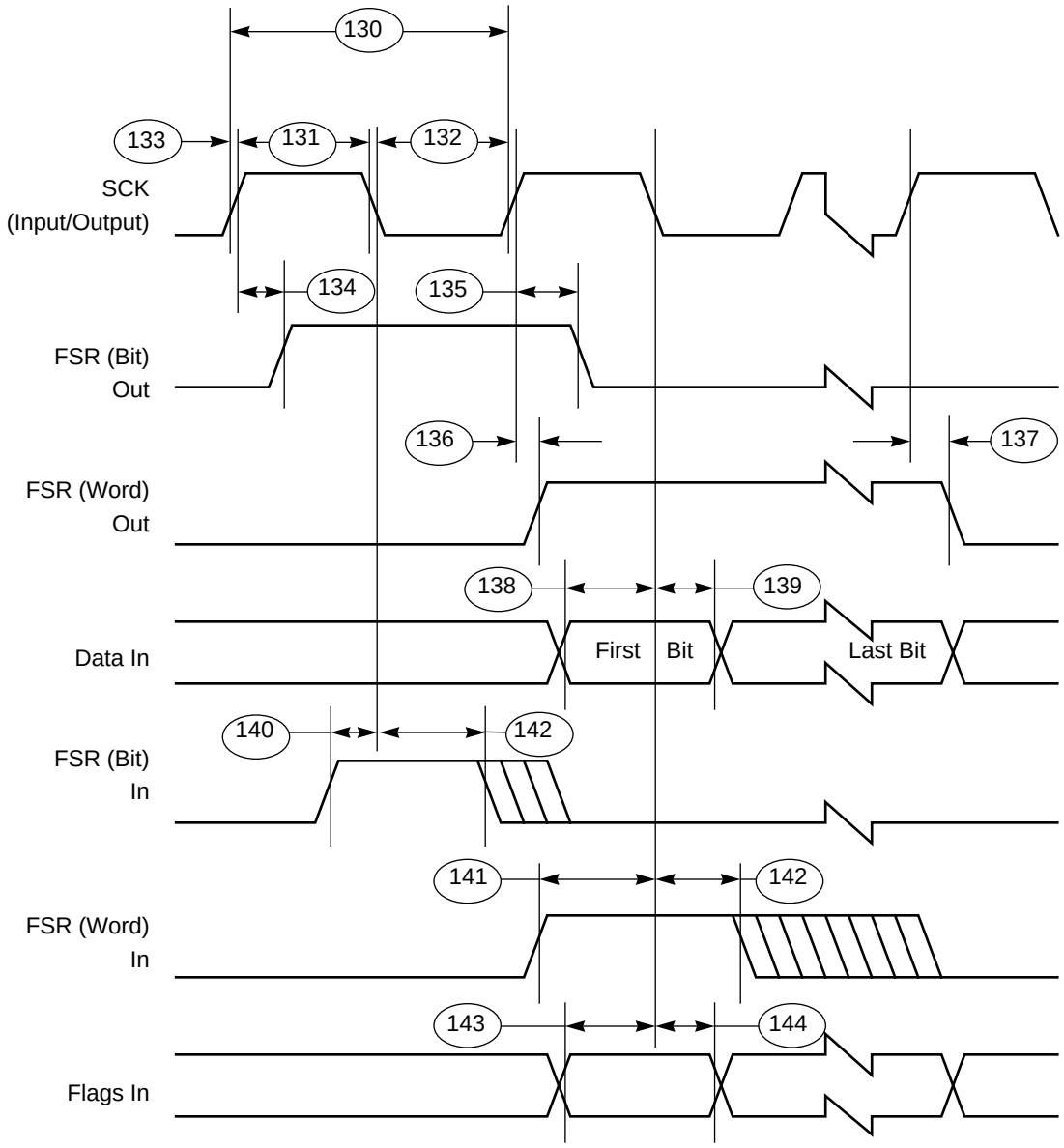


Figure 30 SSI Receiver Timing

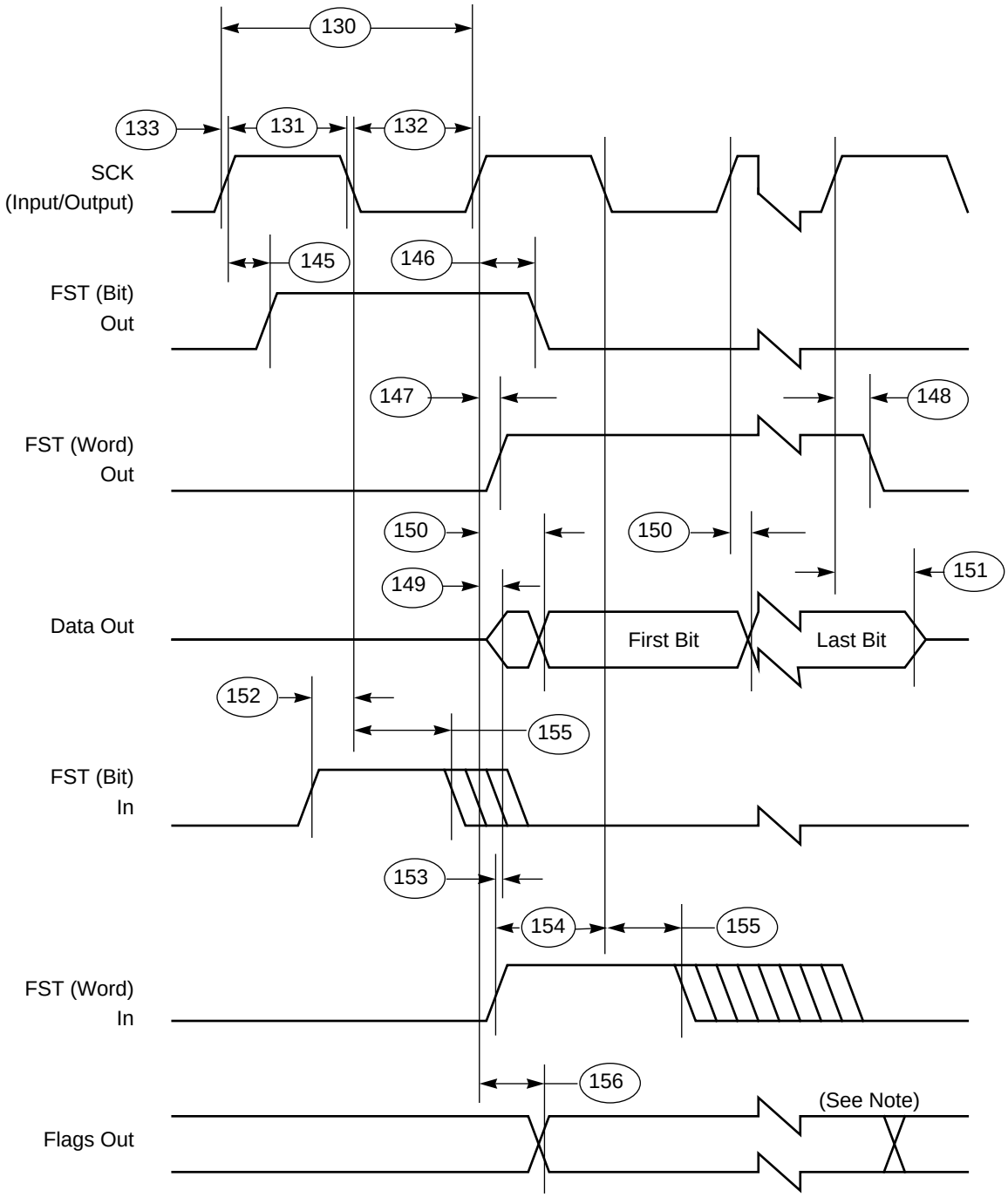


Figure 31 SSI Transmitter Timing

NOTE: In the Network mode, output flag transitions can occur at the start of each time slot within the frame. In the Normal mode, the output flag state is asserted for the entire frame period.

Timer Timing

(V_{CC} = 5.0 V dc ± 10%, T_J = -40° to +125°C, C_L = 50 pF + 1 TTL Load)

Table 21 Timer Timing

Num	Characteristic	40/50/60 MHz		Unit
		Min	Max	
170	TIN Valid to CLKO Low (Setup time)	6	—	ns
171	CLKO Low to TIN Invalid (Hold time)	0	—	ns
172	CLKO High to TOUT Asserted	3.5	14	ns
173	CLKO High to TOUT Deasserted	5.1	20.7	ns
174	TIN Period	8T	—	ns
175	TIN High/Low Period	4T	—	ns

Preliminary

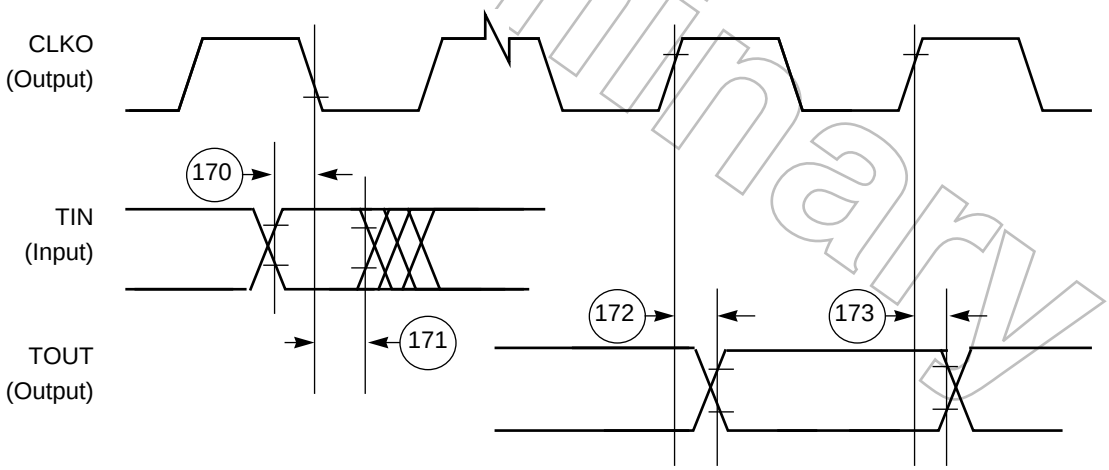


Figure 32 Timer Timing

OnCE™ Port Timing

(V_{CC} = 5.0 V dc ± 10%, T_J = -40° to +125°C, C_L = 50 pF + 1 TTL Load)

Table 22 OnCE Port Timing

Num	Characteristic	40/50/60 MHz		Unit
		Min	Max	
180	DSCK High to DSO Valid	—	37	ns
181	DSI Valid to DSCK Low (Setup)	5.2	—	ns
182	DSCK Low to DSI Invalid (Hold)	0	—	ns
183	DSCK High (See Note 1)	2Tc	—	ns
184	DSCK Low (See Note 1)	2Tc	—	ns
185	DSCK Cycle Time (See Note 1)	4Tc	—	ns
186	CLKO High to OS0-OS1 Valid		14.5	ns
187	CLKO High to OS0-OS1 Invalid	—	—	ns
188	Last DSCK High to OS0-OS1 (See Note 2) Last DSCK High to $\overline{ACK}$ Active (data) (See Note 2) Last DSCK High to $\overline{ACK}$ Active (command) (See Note 2)	10T+Td+14.5 10T+Td+13.5 21T+Td+13.5	— —	ns
189	DSO ($\overline{ACK}$) Asserted to OS0-OS1 Three-state	—	0	ns
190	DSO ($\overline{ACK}$) Asserted to First DSCK High	3Tc	—	ns
191	DSO ($\overline{ACK}$) Width Asserted: • when entering debug mode • when acknowledging command/data transfer	 3T-2 2Tc+0.5	 3T-5 2Tc+3	 ns ns
192	Last DSCK High of Read Register to First DSCK High of Next Command	6Tc	—	ns
193	DSCK High to DSO Invalid (See Note 2)	Td+11.2	—	ns
194	$\overline{DR}$ asserted to DSO ($\overline{ACK}$) Asserted	11T+19.5	—	ns

NOTES: 1. 45%-55% duty cycle
2. Td = DSCK High (Timing #183)

Preliminary

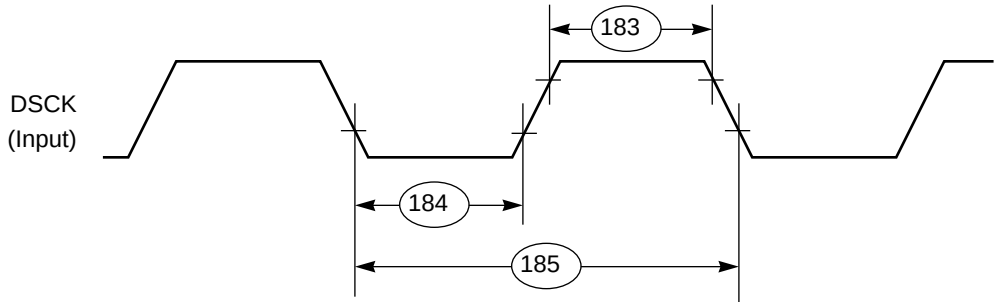


Figure 33 OnCE Port Serial Clock Timing

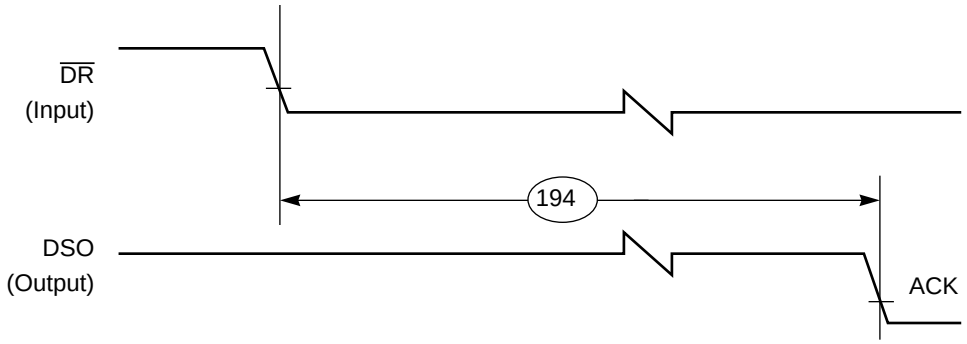
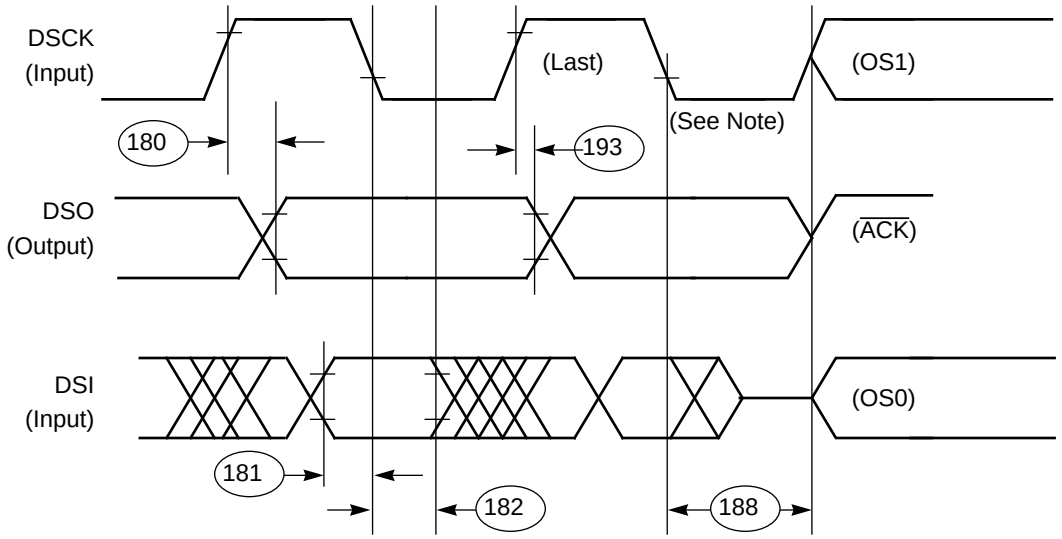
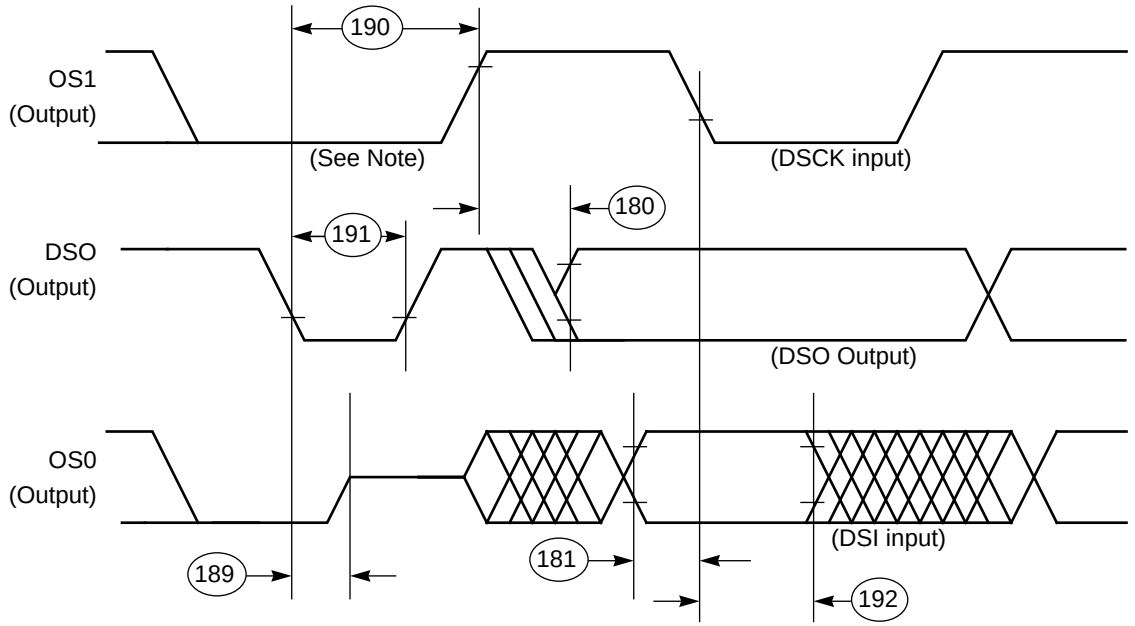


Figure 34 OnCE Port Acknowledge Timing



NOTE: Three-state, external pull-down resistor

Figure 35 OnCE Port Data I/O To Status Timing



NOTE: Three-state, external pull-down resistor

Figure 36 OnCE Port Data I/O to Status Timing

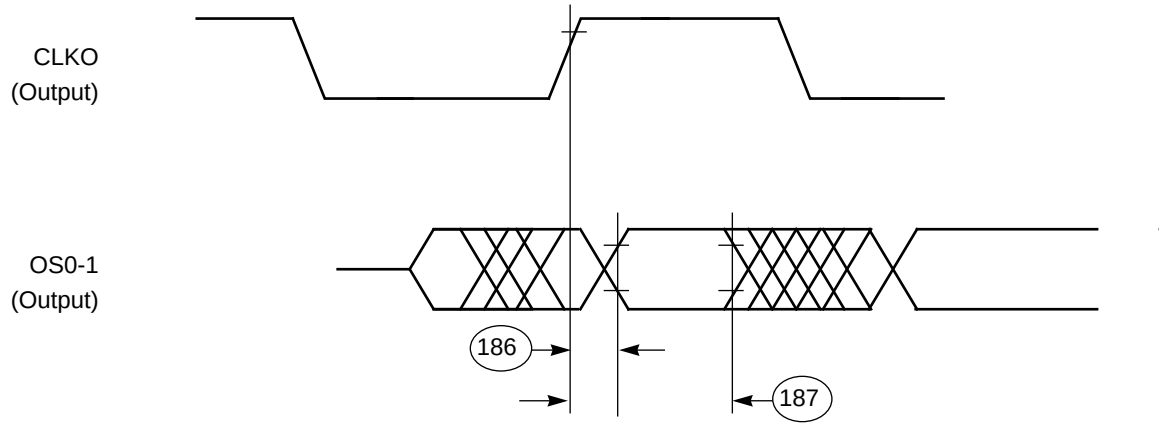


Figure 37 CLK to OnCE Port Status Timing

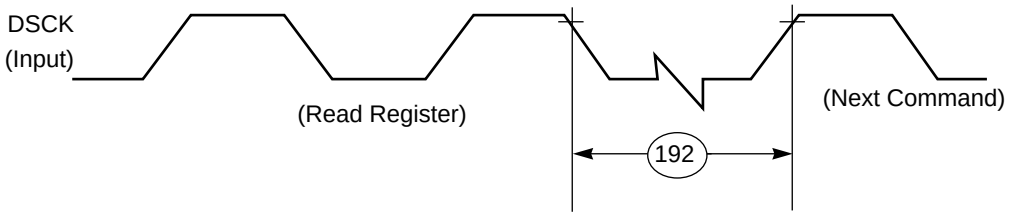
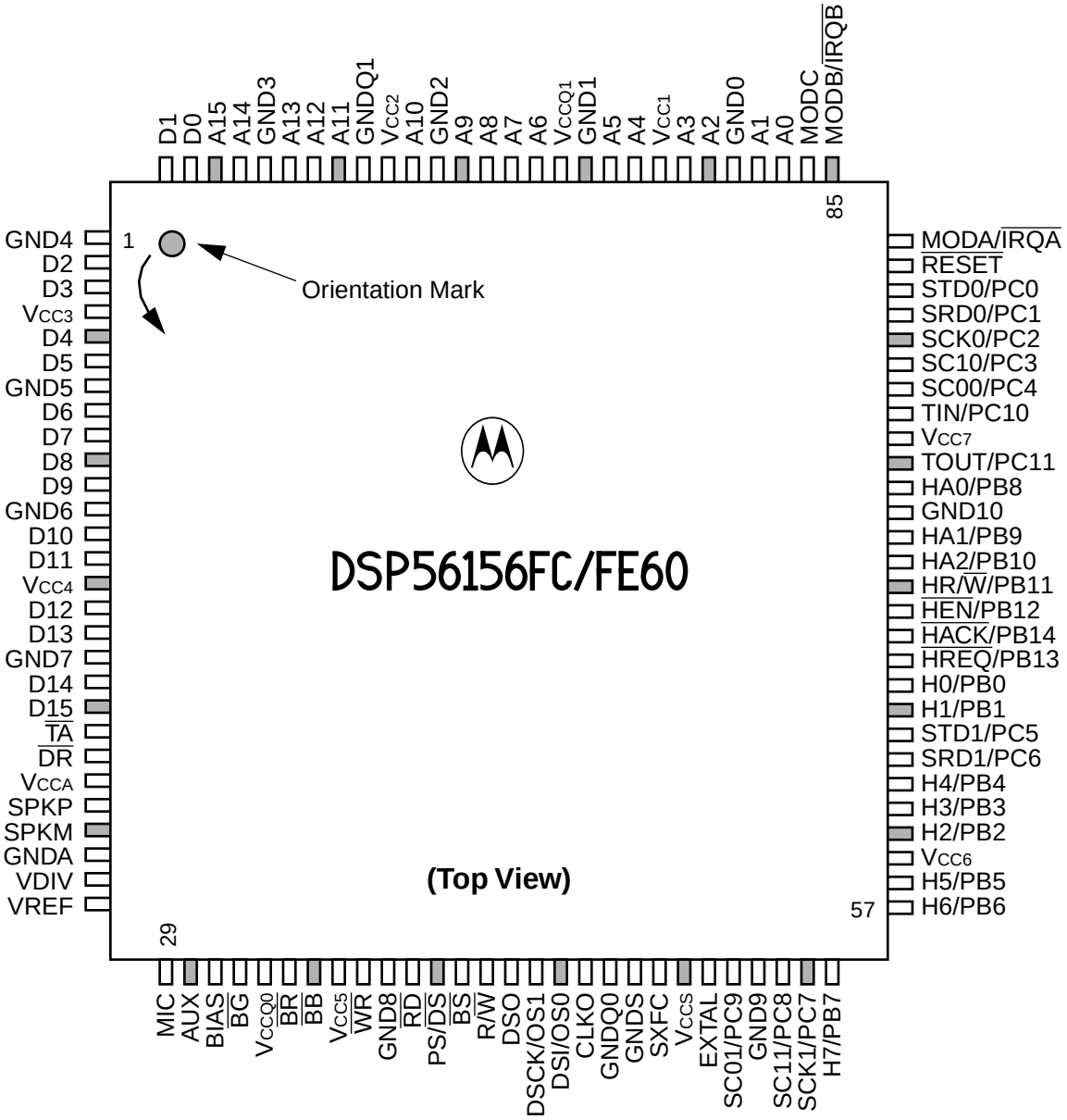


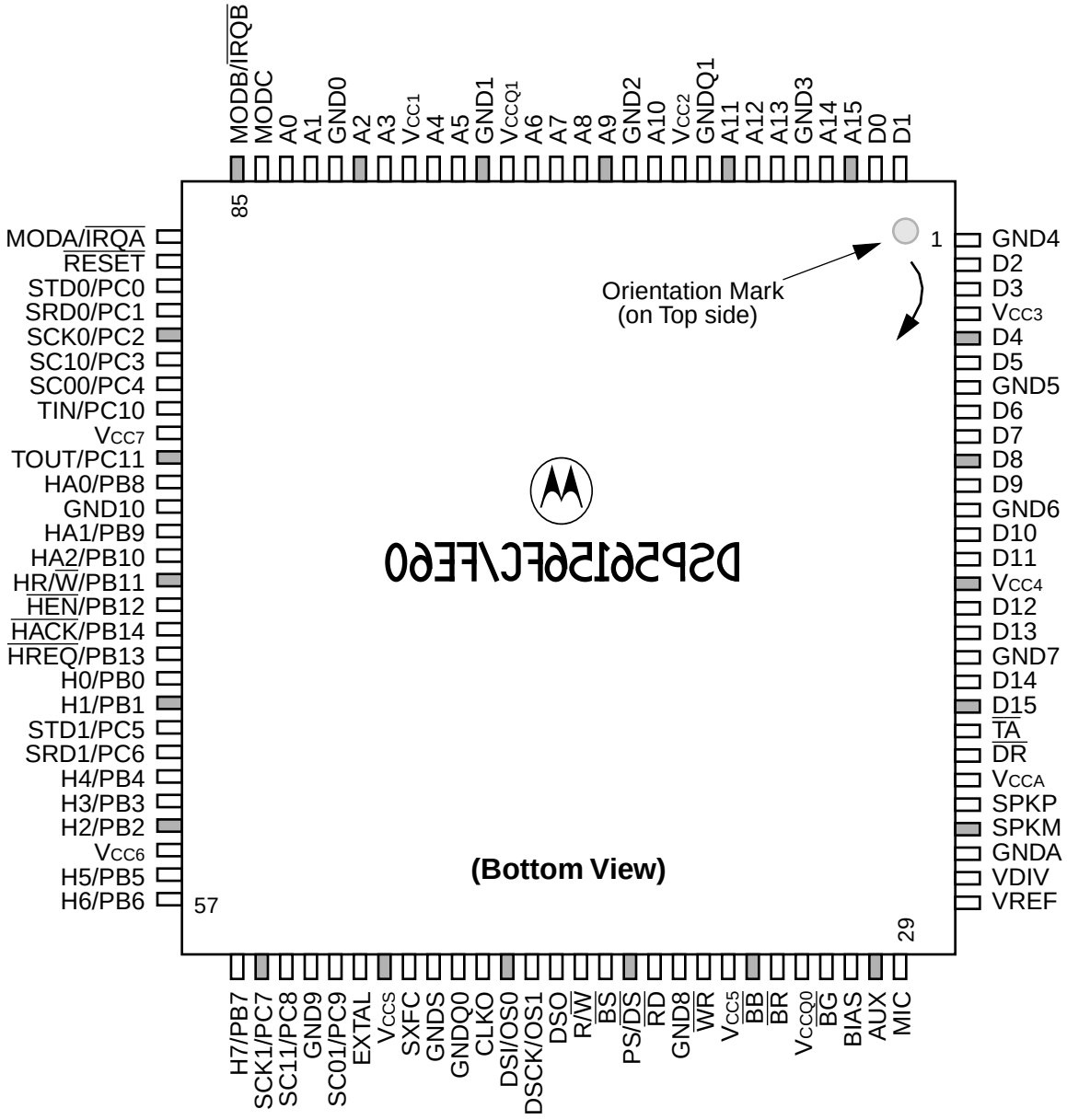
Figure 38 OnCE Port DSCK Next Command After Read Register Timing

Pin-out and Package Information



NOTE: An OVERBAR indicates the signal is asserted when the voltage = ground (active low).

Figure 39 Top View of the DSP56156 112-pin Plastic (FC) and Ceramic (FE) Quad Flat Packages



NOTE: An OVERBAR indicates the signal is asserted when the voltage = ground (active low).

Figure 40 Bottom View of the DSP56156 112-pin Plastic (FC) and Ceramic (FE) Quad Flat Packages

Table 23 DSP56156 General Purpose I/O Pin Identification

112-pin Package Pin #	DSP56156 Primary Pin Function	DSP56156 General Purpose I/O ID
66	H0	PB0
65	H1	PB1
60	H2	PB2
61	H3	PB3
62	H4	PB4
58	H5	PB5
57	H6	PB6
56	H7	PB7
74	HA0	PB8
72	HA1	PB9
71	HA2	PB10
70	HR/$\overline{W}$	PB11
69	$\overline{HEN}$	PB12
67	$\overline{HREQ}$	PB13
68	$\overline{HACK}$	PB14
82	STD0	PC0
81	SRD0	PC1
80	SCK0	PC2
79	SC10	PC3
78	SC00	PC4
64	STD1	PC5
63	SRD1	PC6
55	SCK1	PC7
54	SC11	PC8
52	SC01	PC9
77	TIN	PC10
75	TOUT	PC11

NOTES: 1. In Tables 23, 24, and 25, $\overline{OVERBAR}$ indicates the signal is asserted when the voltage = ground (active low).

2. For more information on power and ground, see Table 26 under Design Considerations.

Pin Number

Table 24 DSP56156 Pin Identification by Pin Number

112-pin Package Pin #	Signal Name	112-pin Package Pin #	Signal Name	112-pin Package Pin #	Signal Name
1	GND4	39	$\overline{RD}$	76	V_{CC7}
2	D2	40	PS/$\overline{DS}$	77	TIN/PC10
3	D3	41	$\overline{BS}$	78	SC00/PC4
4	V_{CC3}	42	R/$\overline{W}$	79	SC10/PC3
5	D4	43	DSO	80	SCK0/PC2
6	D5	44	DSCK/OS1	81	SRD0/PC1
7	GND5	45	DSI/OS0	82	STD0/PC0
8	D6	46	CLKO	83	$\overline{RESET}$
9	D7	47	GNDQ0	84	MODA/$\overline{IRQA}$
10	D8	48	GNDS	85	MODB/$\overline{IRQB}$
11	D9	49	SXFC	86	MODC
12	GND6	50	V_{CCS}	87	A0
13	D10	51	EXTAL	88	A1
14	D11	52	SC01/PC9	89	GND0
15	V_{CC4}	53	GND9	90	A2
16	D12	54	SC11/PC8	91	A3
17	D13	55	SCK1/PC7	92	V_{CC1}
18	GND7	56	H7/PB7	93	A4
19	D14	57	H6/PB6	94	A5
20	D15	58	H5/PB5	95	GND1
21	$\overline{TA}$	59	V_{CC6}	96	V_{CCQ1}
22	$\overline{DR}$	60	H2/PB2	97	A6
23	V_{CCA}	61	H3/PB3	98	A7
24	SPKP	62	H4/PB4	99	A8
25	SPKM	63	SRD1/PC6	100	A9
26	GNDA	64	STD1/PC5	101	GND2
27	VDIV	65	H1/PB1	102	A10
28	VREF	66	H0/PB0	103	V_{CC2}
29	MIC	67	$\overline{HREQ}$/PB13	104	GNDQ1
30	AUX	68	$\overline{HACK}$/PB14	105	A11
31	BIAS	69	$\overline{HEN}$/PB12	106	A12
32	$\overline{BG}$	70	HR/$\overline{W}$/PB11	107	A13
33	V_{CCQ0}	71	HA2/PB10	108	GND3
34	$\overline{BR}$	72	HA1/PB9	109	A14
35	$\overline{BB}$	73	GND10	110	A15
36	V_{CC5}	74	HA0/PB8	111	D0
37	$\overline{WR}$	75	TOUT/PC11	112	D1
38	GND8				

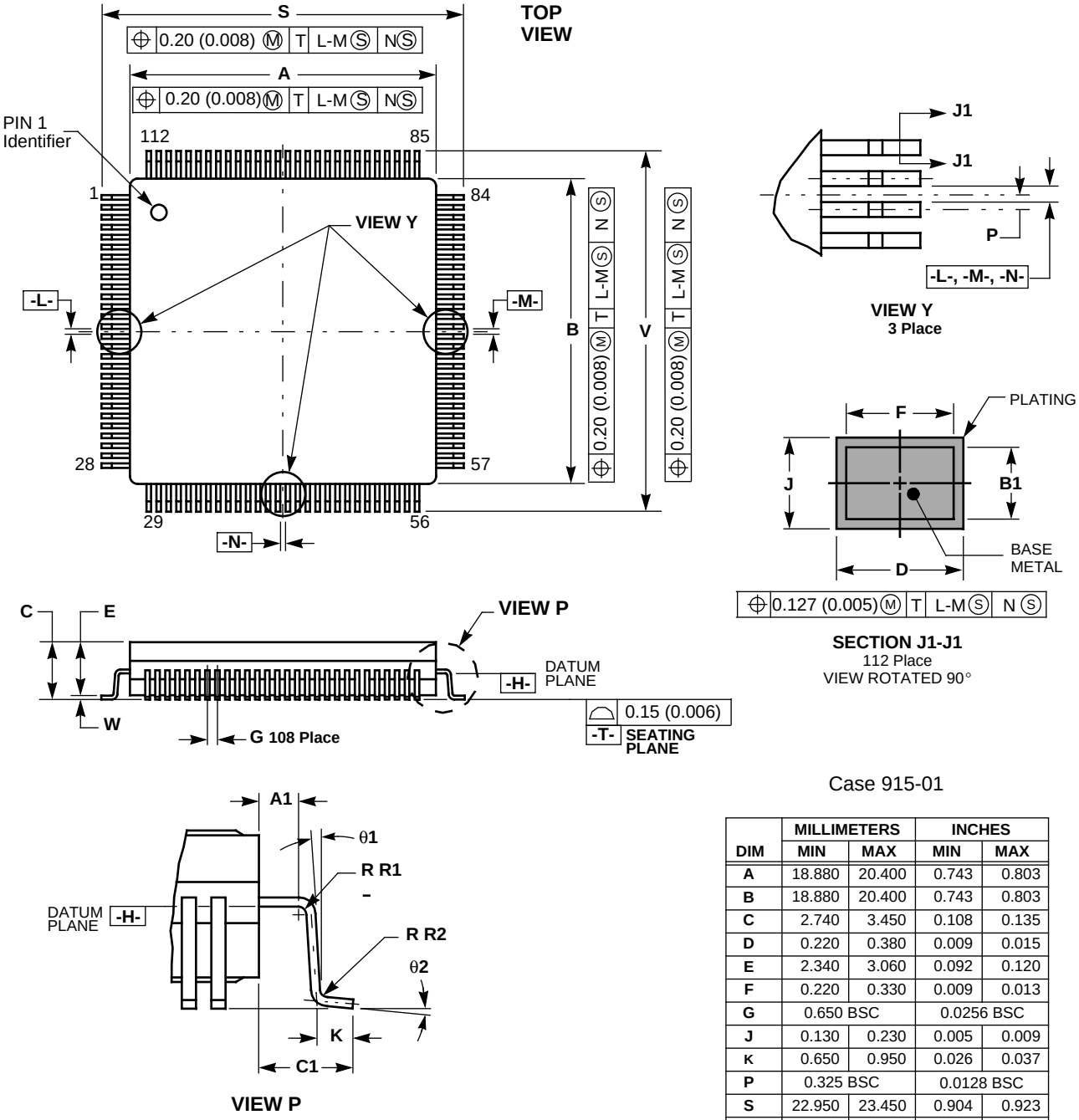
Table 25 DSP56156 Pin Identification by Signal Name

112-pin Package Pin #	Signal Name	112-pin Package Pin #	Signal Name	112-pin Package Pin #	Signal Name
87	A0	6	D5	47	GNDQ0
88	A1	8	D6	104	GNDQ1
90	A2	9	D7	48	GNDS
91	A3	10	D8	66	H0
93	A4	11	D9	65	H1
94	A5	13	D10	60	H2
97	A6	14	D11	61	H3
98	A7	16	D12	62	H4
99	A8	17	D13	58	H5
100	A9	19	D14	57	H6
102	A10	20	D15	56	H7
105	A11	22	$\overline{DR}$	74	HA0
106	A12	44	DSCK	72	HA1
107	A13	45	DSI	71	HA2
109	A14	43	DSO	68	$\overline{HACK}$
110	A15	51	EXTAL	69	$\overline{HEN}$
30	AUX	89	GND0	70	HR/$\overline{W}$
35	$\overline{BB}$	95	GND1	67	$\overline{HREQ}$
32	$\overline{BG}$	101	GND2	84	$\overline{IRQA}$
31	BIAS	108	GND3	85	$\overline{IRQB}$
34	$\overline{BR}$	1	GND4	29	MIC
41	$\overline{BS}$	7	GND5	84	MODA
46	CLKO	12	GND6	85	MODB
111	D0	18	GND7	86	MODC
112	D1	38	GND8	45	OS0
2	D2	53	GND9	44	OS1
3	D3	73	GND10	66	PB0
5	D4	26	GNDA	65	PB1

Table 25 DSP56156 Pin Identification by Signal Name (continued)

112-pin Package Pin #	Signal Name	112-pin Package Pin #	Signal Name	112-pin Package Pin #	Signal Name
60	PB2	55	PC7	64	STD1
61	PB3	54	PC8	49	SXFC
62	PB4	52	PC9	21	$\overline{TA}$
58	PB5	77	PC10	77	TIN
57	PB6	75	PC11	75	TOUT
56	PB7	40	PS/$\overline{DS}$	92	V_{CC1}
74	PB8	42	R/$\overline{W}$	103	V_{CC2}
72	PB9	39	$\overline{RD}$	4	V_{CC3}
71	PB10	83	$\overline{RESET}$	15	V_{CC4}
70	PB11	78	SC00	36	V_{CC5}
69	PB12	52	SC01	59	V_{CC6}
67	PB13	79	SC10	76	V_{CC7}
68	PB14	54	SC11	23	V_{CCA}
82	PC0	80	SCK0	33	V_{CCQ0}
81	PC1	55	SCK1	96	V_{CCQ1}
80	PC2	25	SPKM	50	V_{CCS}
79	PC3	24	SPKP	27	VDIV
78	PC4	81	SRD0	28	VREF
64	PC5	63	SRD1	37	$\overline{WR}$
63	PC6	82	STD0		

112 CQFP



Case 915-01

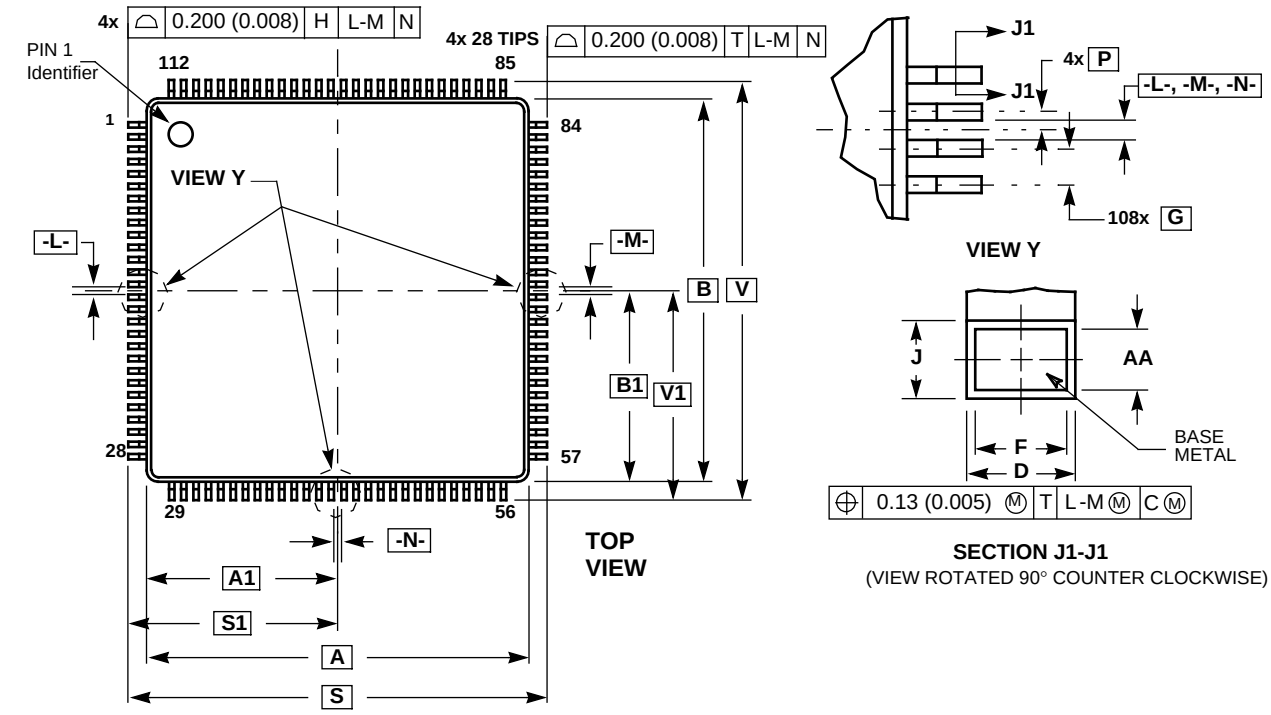
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.880	20.400	0.743	0.803
B	18.880	20.400	0.743	0.803
C	2.740	3.450	0.108	0.135
D	0.220	0.380	0.009	0.015
E	2.340	3.060	0.092	0.120
F	0.220	0.330	0.009	0.013
G	0.650 BSC		0.0256 BSC	
J	0.130	0.230	0.005	0.009
K	0.650	0.950	0.026	0.037
P	0.325 BSC		0.0128 BSC	
S	22.950	23.450	0.904	0.923
V	22.950	23.450	0.904	0.923
W	0.300	—	0.012	—
A1	0.200	0.600	0.008	0.024
B1	0.120	0.132	0.0047	0.0052
C1	1.800 REF		0.070 REF	
R1	0.200 REF		0.008 REF	
R2	0.200 REF		0.008 REF	
θ1	0°	8°	0°	8°
θ2	0°	8°	0°	8°

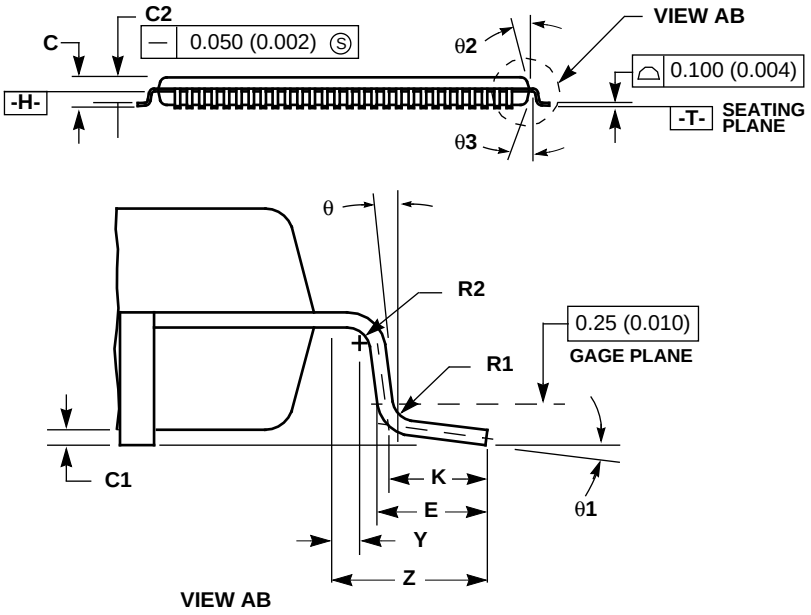
NOTE: BSC = Between Statistical Center (i.e., typical)

NOTES:
1. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
2. Controlling dimension: millimeter.
3. Datum plane -H- is coincident with the bottom of the lead where the lead exits the ceramic body.
4. Datums -L-, -M- and -N- to be determined at datum plane -H-.
5. Dimensions S and V to be determined at seating plane -T-.
6. Dimensions A and B define maximum ceramic body dimensions including glass protrusion and mismatch.

Figure 41 DSP56156 112-pin Ceramic Quad Flat Pack (CQFP) Mechanical Information

112 TQFP





Case 987-01

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.000 BSC		0.790 BSC	
A1	10.000 BSC		0.395 BSC	
B	20.000 BSC		0.790 BSC	
B1	10.000 BSC		0.395 BSC	
C	1.400	1.600	0.055	0.063
C1	0.050	0.150	0.002	0.006
C2	1.350	1.450	0.053	0.057
D	0.270	0.370	0.011	0.014
E	0.450	0.750	0.018	0.030
F	0.270	0.330	0.011	0.013
G	0.650 BSC		0.0256 BSC	
J	0.115	0.175	0.006	0.007
K	0.500 BSC		0.020 BSC	
P	0.325 BSC		0.013 BSC	
R1	0.100	0.200	0.004	0.008
R2	0.100	0.200	0.004	0.008
S	22.000 BSC		0.866 BSC	
S1	11.000 BSC		0.433 BSC	
V	22.000 BSC		0.866 BSC	
V1	11.000 BSC		0.433 BSC	
Y	0.250 REF		0.010 REF	
Z	1.000 REF		0.039 REF	
AA	0.115	0.135	0.004	0.005
θ	0°	8°	0°	8°
θ1	3°	7°	3°	7°
θ2	11°	13°	11°	13°
θ3	11°	13°	11°	13°

NOTE: BSC = Between Statistical Center (i.e., typical)

NOTES:
1. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
2. Controlling dimension: Millimeter.
3. Datum plane -H- is located at bottom of lead and is coincident with the lead where the lead exits the plastic body at the bottom of the parting line.
4. Datums -L-, -M- and -N- to be determined at datum plane -H-.
5. Dimensions S and V to be determined at seating plane -T-.
6. Dimensions A and B do not include mold protrusion. Allowable protrusion is 0.25 (0.010) per side. Dimensions A and B do include mold mismatch and are determined at datum plane -H-.
7. Dimension D does not include dambar protrusion. Allowable dambar protrusion shall not cause the D dimension to exceed 0.43 (0.017).

Figure 42 DSP56156 112-pin Plastic Thin Quad Flat Pack (TQFP) Mechanical Information

Design Considerations

Heat Dissipation

The average chip junction temperature, T_J, in °C, can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JA}) \quad (1)$$

Where:

T_A = ambient temperature, °C
Θ_{JA} = package thermal resistance, junction-to-ambient, °C/W
P_D = $P_{INT} + P_{I/O}$
P_{INT} = $I_{CC} \times V_{CC}$ watts — chip internal power
$P_{I/O}$ = power dissipation on input and output pins — user determined

For most applications $P_{I/O} < P_{INT}$ and $P_{I/O}$ can be neglected. An appropriate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K/(T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \times (T_A + 273) + P_D \times \Theta_{JA} \quad (3)$$

Where K is a constant pertaining to the particular package. K can be determined from equation (2) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A. The total thermal resistance of a package (Θ_{JA}) can be separated into two components, Θ_{JC} and Θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case) surface (Θ_{JC}) and from the case to the outside ambient (Θ_{CA}). These terms are related by the equation:

$$\Theta_{JA} = \Theta_{JC} + \Theta_{CA} \quad (4)$$

Θ_{JC} is device-related and cannot be influenced by the user. However, Θ_{CA} is user-dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling, and thermal convection. Thus, good thermal management on the part of the user can significantly reduce Θ_{CA} so that Θ_{JA} approximately equals Θ_{JC}. Substitution of Θ_{JC} for Θ_{JA} in equation (1) will result in a lower semiconductor junction temperature. Values for thermal resistance presented in this document, unless estimated, were derived using the procedure described in Motorola Reliability Report 7843, "Thermal Resistance Measurement Method for MC68XX Microcomponent Devices", and are provided for design purposes only. Thermal measurements are complex and dependent on procedure and setup. User-derived values for thermal resistance may differ.

Power, Ground, and Noise

Each DSP56156 V_{CC} pin should be provided with a low-impedance path to +5 volts. Each DSP56156 GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip as shown in Table 26.

The V_{CC} power supply should be bypassed to GND ground using at least six 0.01 – 0.1 µF bypass capacitors located either underneath the chip's socket or as close as possible to the four sides of the package. The capacitor leads and the associated printed circuit traces connecting to chip V_{CC} and GND should be kept to less than

0.5″ per capacitor lead. The use of at least a four layer board is recommended, employing two inner layers as V_{CC} and GND planes. All output pins on this DSP have fast rise and fall times. Printed Circuit Board (PCB) trace length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses as well as the PS/$\overline{DS}$, $\overline{BS}$, $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, interrupt, and $\overline{HEN}$ pins. Maximum PCB trace lengths on the order of 6" are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to PCB traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits.

Clock signals should not be run across many signals and should be kept away from analog power and ground traces as well as any analog signals. See Figure 44 for more details.

Table 26 Power and Ground Connections

Circuitry	Power		Ground	
	Signal Name	Pin #	Signal Name	Pin #
Address Bus Buffers	V_{CC1} V_{CC2}	92 103	GND0 GND1 GND2 GND3	89 95 101 108
Data Bus Buffers	V_{CC3} V_{CC4}	4 15	GND4 GND5 GND6 GND7	1 7 12 18
Bus Control Buffers	V_{CC5}	36	GND8	38
Codec	V_{CCA}	23	GNDA	26
Digital Peripherals	V_{CC6} V_{CC7}	59 76	GND9 GND10	53 73
Internal logic	V_{CCQ0} V_{CCQ1}	33 96	GNDQ0 GNDQ1	47 104
Phase-Locked Loop (PLL)	V_{CCS}	50	GNDS	48

Power Consumption

(V_{CC} = 5.0 V dc ± 10%, T_J = -40° to +125°C, C_L = 50 pF + 1 TTL Load)

The DC electrical characteristics of this device are shown in Table 27. Power consumption is application dependant. The data in Table 27 is collected by running the following code using internal memory after having programmed all pins of port B and C as input and after having three-stated the data bus (MC = 0 in OMR) and pulled high:

```
        move        #0,r0
        move        #0,r3
        move        #$100,r2
        move        #$00ff,m0
loop    clr         a
        move        x:(r0)+,a                   ;initial value to accumulator
        move        a1,a0
        rep         #30
        mac         x0,y0,a     x:(r3)+,x0      ;mac on typical data
        move        a,p:(r2)                    ;store the mac result
        move        #0,r3
        jmp         loop
```

Table 27 DC Electrical Characteristics

Conditions	Symbol	Typical			Unit
		40 MHz	50 MHz	60 MHz	
Digital current with Codec and PLL disabled	I_{CC}	91	112	133	mA
Digital current Wait Mode with Codec and PLL disabled	I_{CC}	12	14	17	mA
Digital current Wait Mode with Codec Enabled and PLL disabled	I_{CC}	92	113	134	mA
Stop mode with PLL and CLKO disabled	I_{CC}	—	250	—	µA
Digital current drawn by the PLL when active	I_{CC}	—	1	—	mA
Digital current drawn by CLKO when active	I_{CC}	—	3.6	—	mA
Analog current with Codec enabled	I_{CCA}	—	12	—	mA
Analog current with Codec disabled	I_{CCA}	—	70	—	µA

To minimize the power dissipation, all unused digital input pins should be tied inactive to ground or power; and all unused I/O pins should be tied inactive through a 10KΩ resistor to ground or power. When the codec is not used, GNDA should be connected to GND; and V_{CCA} should be connected to V_{CC}. Also, all codec pins should be left floating, except VREF which should still be decoupled.

Preliminary

Host Port Considerations

Careful synchronization is required when reading multi-bit registers that are written by another asynchronous system. This is a common problem when two asynchronous systems are connected. The situation exists in the host interface. The considerations for proper operation are discussed below.

Host Programming Considerations

1. Unsynchronized Reading of Receive Byte Registers
   When reading receive byte registers, RXH or RXL, the host program should use interrupts or poll the RXDF flag which indicates that data is available. This assures that the data in the receive byte registers will be stable.

2. Overwriting Transmit Byte Registers
   The host program should not write to the transmit byte registers, TXH or TXL, unless the TXDE bit is set indicating that the transmit byte registers are empty. This guarantees that the transmit byte registers will transfer valid data to the HRX register.

3. Synchronization of Status Bits from DSP to Host
   HC, HREQ, DMA, HF3, HF2, TRDY, TXDE, and RXDF status bits are set or cleared from inside the DSP and read by the host processor (refer to *DSP56156 User's Manual*, I/O Interface section, Host/DMA Interface Programming Model for descriptions of these status bits). The host can read these status bits very quickly without regard to the clock rate used by the DSP, but the possibility exists that the state of the bit could be changing during the read operation. This is generally not a system problem, since the bit will be read correctly in the next pass of any host polling routine.

   However, if the host asserts $\overline{\text{HEN}}$ for more than timing number 101 (T101), with a minimum cycle time of timing number 103 (T103), then these status bits are guaranteed to be stable. Care must be exercised when reading status bits HF3 and HF2 as an encoded pair. If the DSP changes HF3 and HF2 from 00 to 11, there is a small probability that the host could read the bits during the transition and receive 01 or 10 instead of 11. If the combination of HF3 and HF2 has significance, the host could read the wrong combination. Therefore, read the bits twice and check for consensus.

4. Overwriting the Host Vector
   The host program should change the Host Vector register only when the Host Command bit (HC) is clear. This change will guarantee that the DSP interrupt control logic will receive a stable vector.

5. Cancelling a Pending Host Command Exception
   The host processor may elect to clear the HC bit to cancel the host command exception request at any time before it is recognized by the DSP. Because the host does not know exactly when the exception will be recognized (due to exception processing synchronization and pipeline delays), the DSP may execute the host command exception after the HC bit is cleared. For these reasons, the HV bits must not be changed at the same time that the HC bit is cleared.

DSP Programming Considerations

1. Synchronization of Status Bits from Host to DSP
   DMA, HF1, HF0, and HCP, HTDE, and HRDF status bits are set or cleared by the host processor side of the interface. These bits are individually synchronized to the DSP clock. (Refer to the *DSP56156 User's Manual*, I/O Interface section, Host/DMA Interface Programming Model for descriptions of these status bits.)

2. Reading HF0 and HF1 as an Encoded Pair
   Care must be exercised when reading status bits HF0 and HF1 as an encoded pair, i.e., the four combinations 00, 01, 10, and 11 each have significance. A very small probability exists that the DSP will read the status bits synchronized during transition. Therefore, HF0 and HF1 should be read twice and checked for consensus.

Bus Operation

Figure 43 depicts the operation of the external memory interface with multiple wait states.

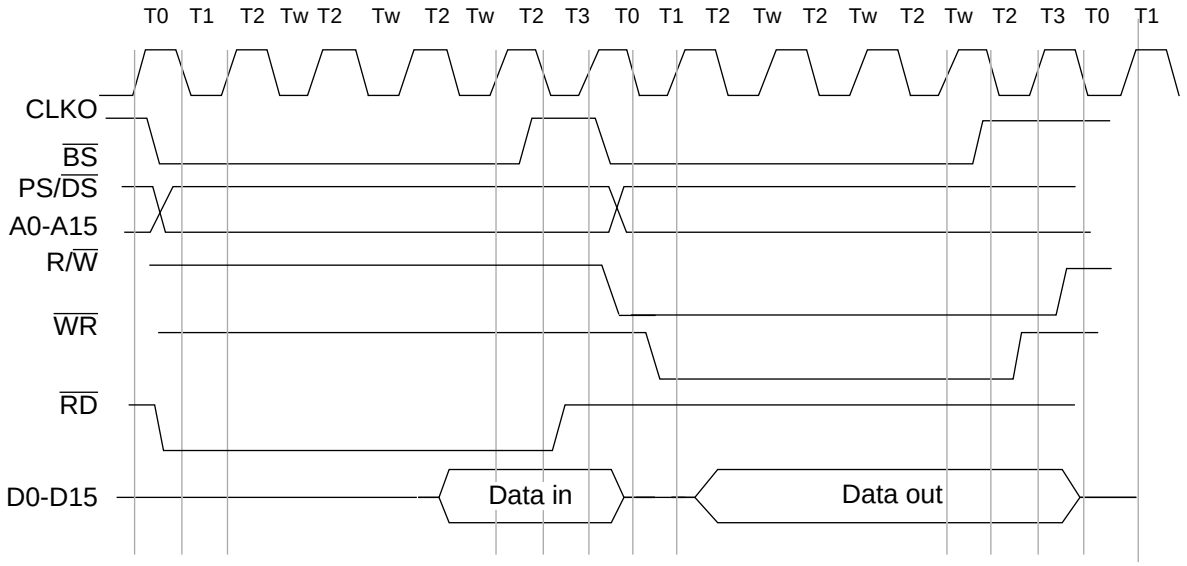


Figure 43 Read and Write Bus Operation (3 Wait States)

Analog I/O Considerations

Figure 44 describes the recommended analog I/O and power supply configurations. The two analog inputs are electrically identical. When one is not used, it can be left floating. When used, an AC coupling capacitor is required. The value of the capacitor along with the input impedance of the pin determine the cut off frequency of a high pass filter. The input impedance of the MIC and AUX varies as a function of the sigma-delta (∑Δ) modulator master clock. 78 kΩ is a typical value at 2 MHz. An AC capacitor of 1µF defines a high pass filter pole of 2 Hz. A smaller capacitor value will move this pole higher in frequency.

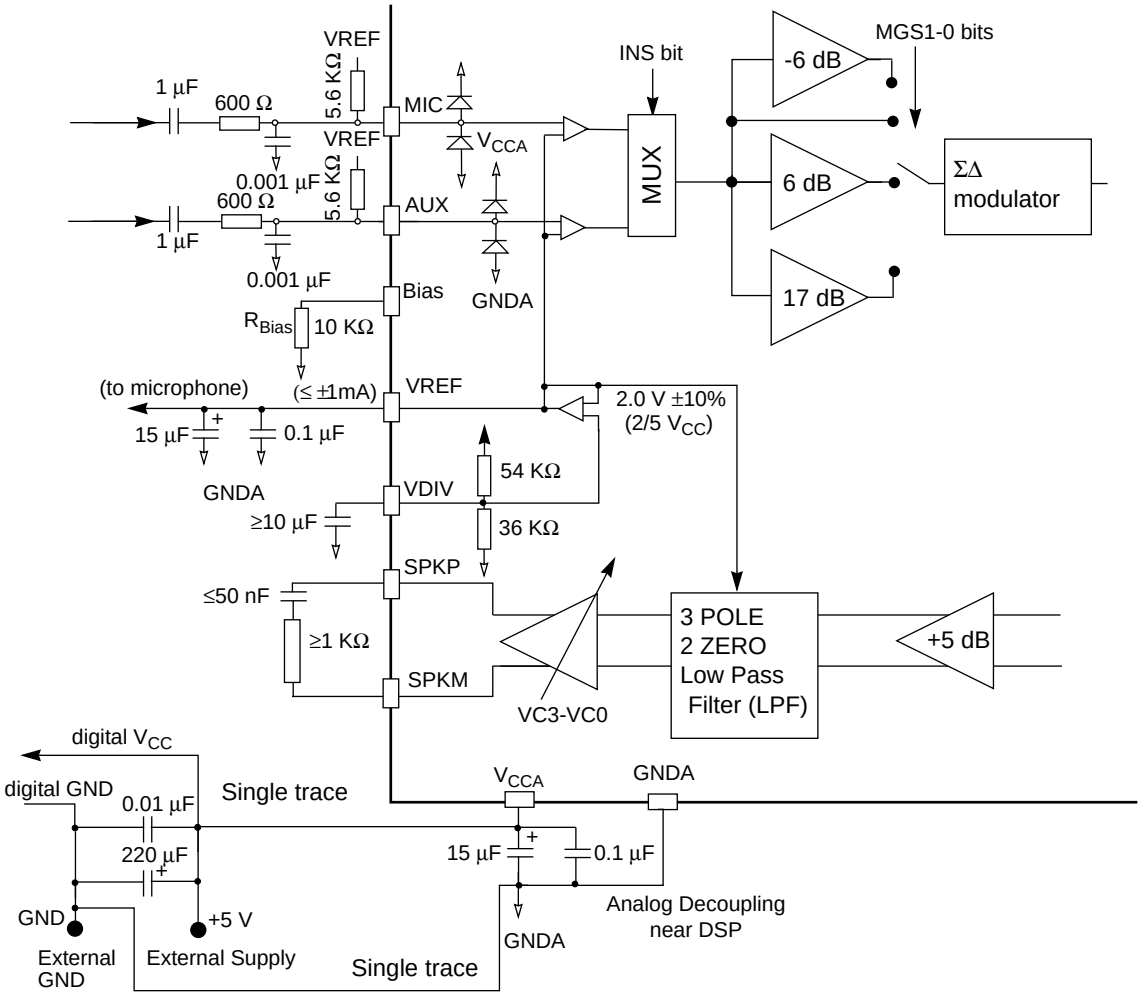


Figure 44 Recommended Analog I/O Configuration

Figure 45 shows three possible single-ended output configurations. Configuration (a) is highly recommended. For configurations (b) and (c), an AC coupling capacitor is required since the load resistor is tied to GNDA.

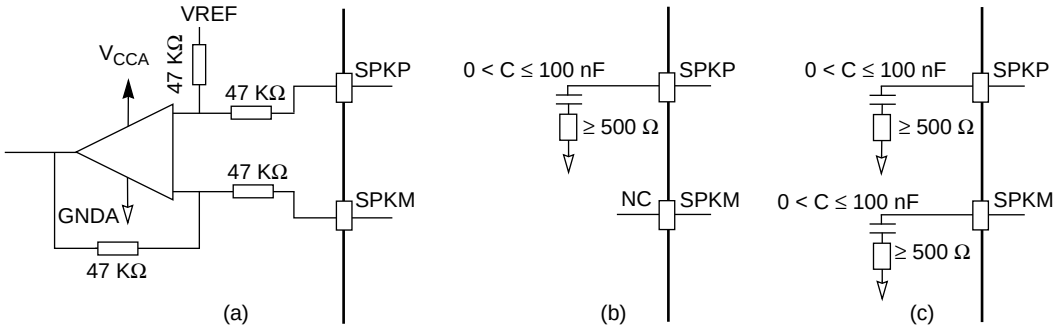


Figure 45 Single-ended Output Configurations

Figure 46 shows a recommended layout for power and ground planes.

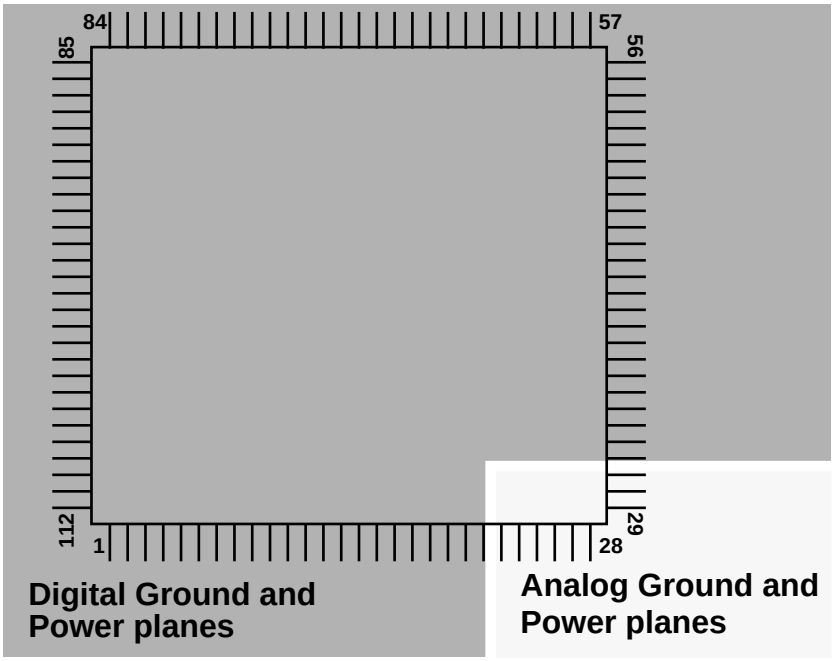


Figure 46 Ground and Power planes

A four level board is recommended. The top layer (directly under the parts) and the bottom layer should be interconnect layers. The two center layers should be power and ground. Ground and power planes should be completely separated. The digital and analog power/ground planes should not overlap. All codec pins should be over the analog planes. The analog planes should not encompass any digital pins. All codec signal traces should be over the analog planes.

Figure 47 shows that 0.1 µF bypass caps should be located as close to the pins being bypassed as possible. The ground side of these caps should be connected as close as possible to the V_{CCA} pin. The ground side of the bypass cap should be connected to the V_{CCA} pin by short traces.

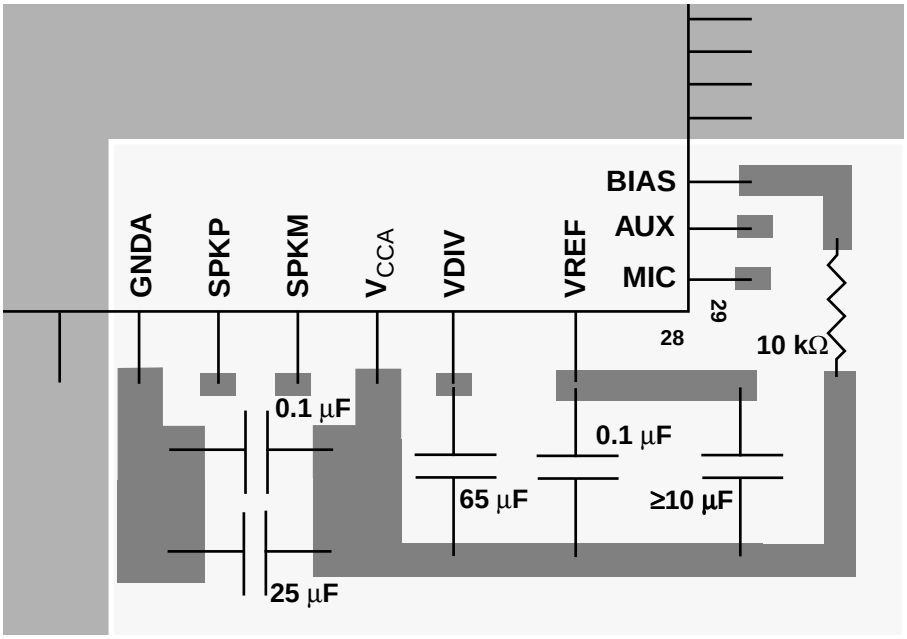


Figure 47 Suggested Top Layer Bypassing

The pins with 0.1 µF bypass caps are VREF and GNDA. The largest size practical bypass caps should also be added for each of these pins as well as for the VDIV pin; 10 µF bypass caps should be considered a minimum value for the larger caps (65 µF on VDIV may be used). These caps should be near the package but do not have to be right next to the pins.

The DAC outputs (SPKP and SPKM) should be run right next to each other as shown on Figure 48.

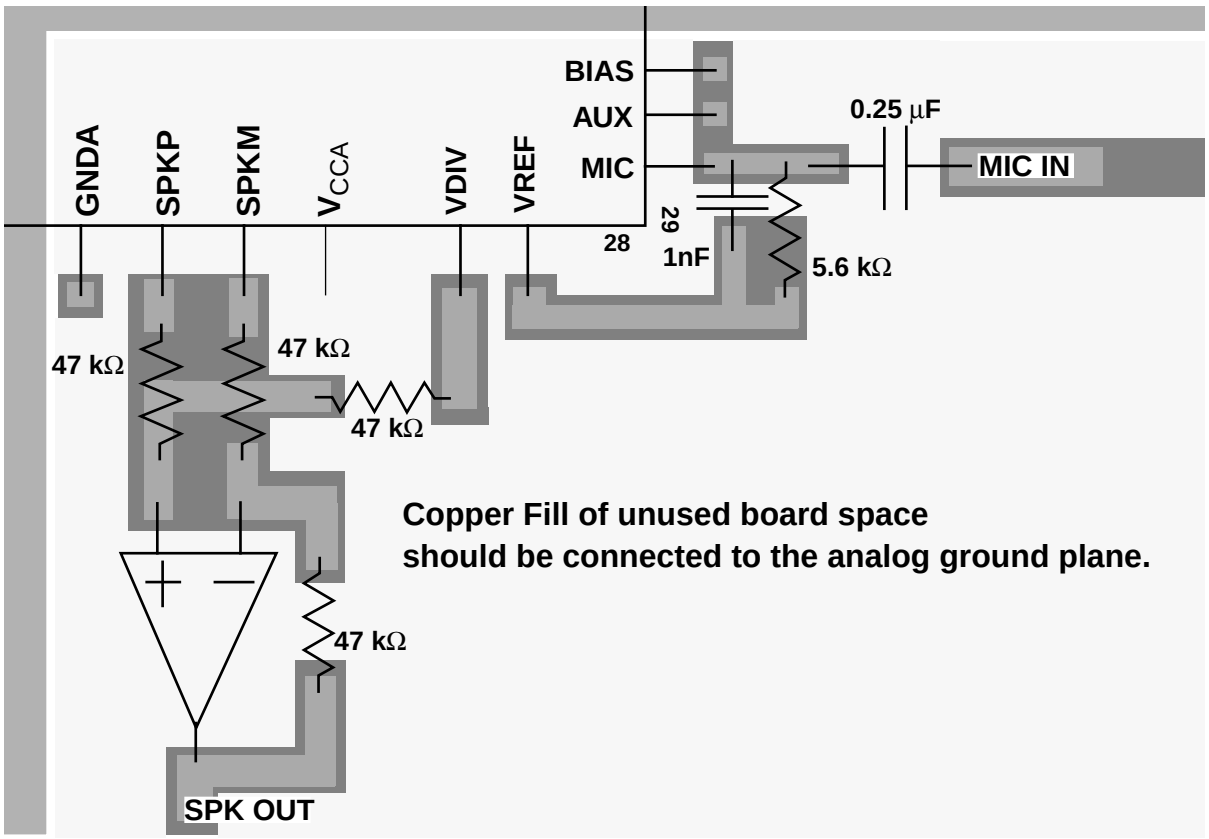
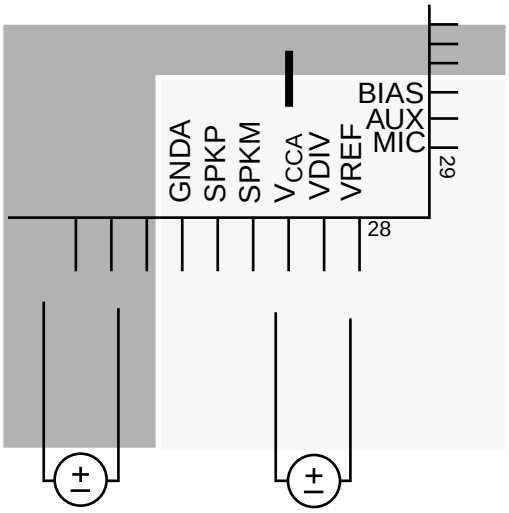


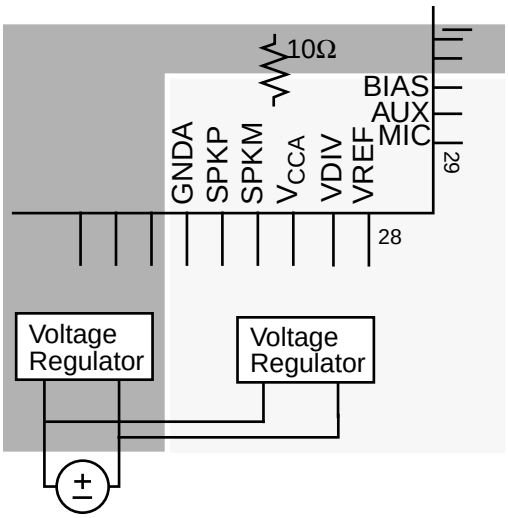
Figure 48 Suggested Bottom Layer Routing

The output should be used differentially if at all possible. Analog signal traces should be shielded by running traces connected to analog ground next to them. Unused board area on both interconnect levels should be copper filled and connected to analog ground. The copper fill is only shown on this page for clarity and simplicity. The ADC input anti-aliasing should be done with respect to VREF.

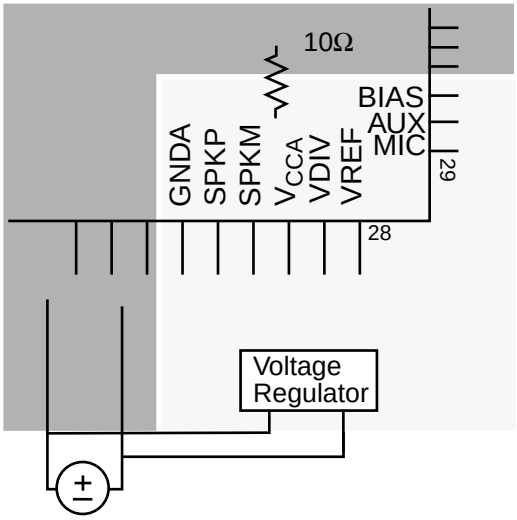
Figure 49 presents four options for good power supply connections.



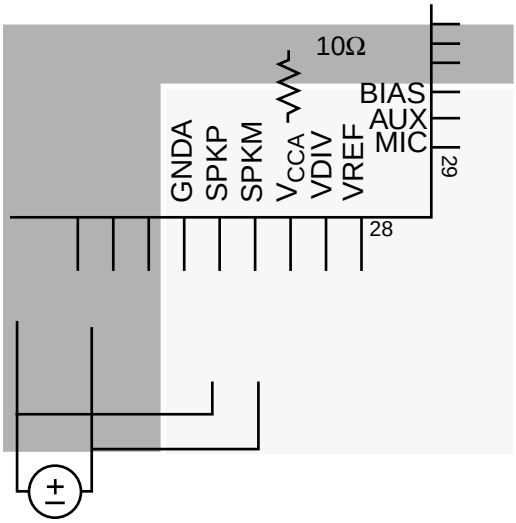
Ideal Choice — Two separate power supplies. Ground planes connected with a single trace as close as possible to the V_{CCA} pin on the codec.



Second Choice — One power supply. Two regulators, one for the digital supply, one for the analog supply. Ground planes connected with a 10 Ω resistor as close as possible to the V_{CCA} pin on the codec.



Third Choice — One power supply. One regulator for the analog supply. Digital supplies driven directly by voltage source. Ground planes connected with a 10 Ω resistor as close as possible to the V_{CCA} pin on the codec.



Fourth Choice — One power supply. Ground planes connected at source. Ground planes connected with a 10 Ω resistor as close as possible to the V_{CCA} pin on the codec.

Figure 49 Four Possible Power Supply Connections

Ordering Information

Table 28 lists information for ordering parts.

Table 28 DSP56156 Ordering Information

Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Order Number
5 V	Ceramic Quad Flat Pack (CQFP)	112	40	DSP56156FE40
			60	DSP56156FE60
5 V	Plastic Thin Quad Flat Pack (TQFP)	112	40	DSP56156FV40
			60	DSP56156FV60

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