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PRODUCT INFORMATION

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DSP56156
DSP56156ROM

Product Brief

16-bit Digital Signal Processor

The DSP56156 is a general-purpose MPU-style Digital Signal Processor (DSP). On a single semiconductor chip, the DSP56156 comprises a very efficient 16-bit digital signal processing core, program and data memories, a number of peripherals, and system support circuitry. Unique features of the DSP56156 include a built-in sigma-delta (ΣΔ) codec and phase-locked loop (PLL). This combination of features makes the DSP56156 a cost-effective, high-performance solution for many DSP applications, especially speech coding, digital communications, and cellular base stations.

The central processing unit of the DSP56156 is the DSP56100 core processor. Like all DSP56100-based DSPs, the DSP56156 consists of three execution units operating in parallel, allowing up to six operations to be performed during each instruction cycle. This parallelism greatly increases the effective processing speed of the DSP56156. The MPU-style programming model and instruction set allow straightforward generation of efficient, compact code. The basic architectures and development tools of Motorola's 16-bit, 24-bit, and 32-bit DSPs are so similar that understanding how to design and program one greatly reduces the time needed to learn the others.

On-Chip Emulation (OnCE™ port) circuitry provides convenient and inexpensive debug facilities normally available only through expensive external hardware. Development costs are reduced and in-field testing is greatly simplified using the OnCE™ port. Figure 1 illustrates the DSP56156 in detail.

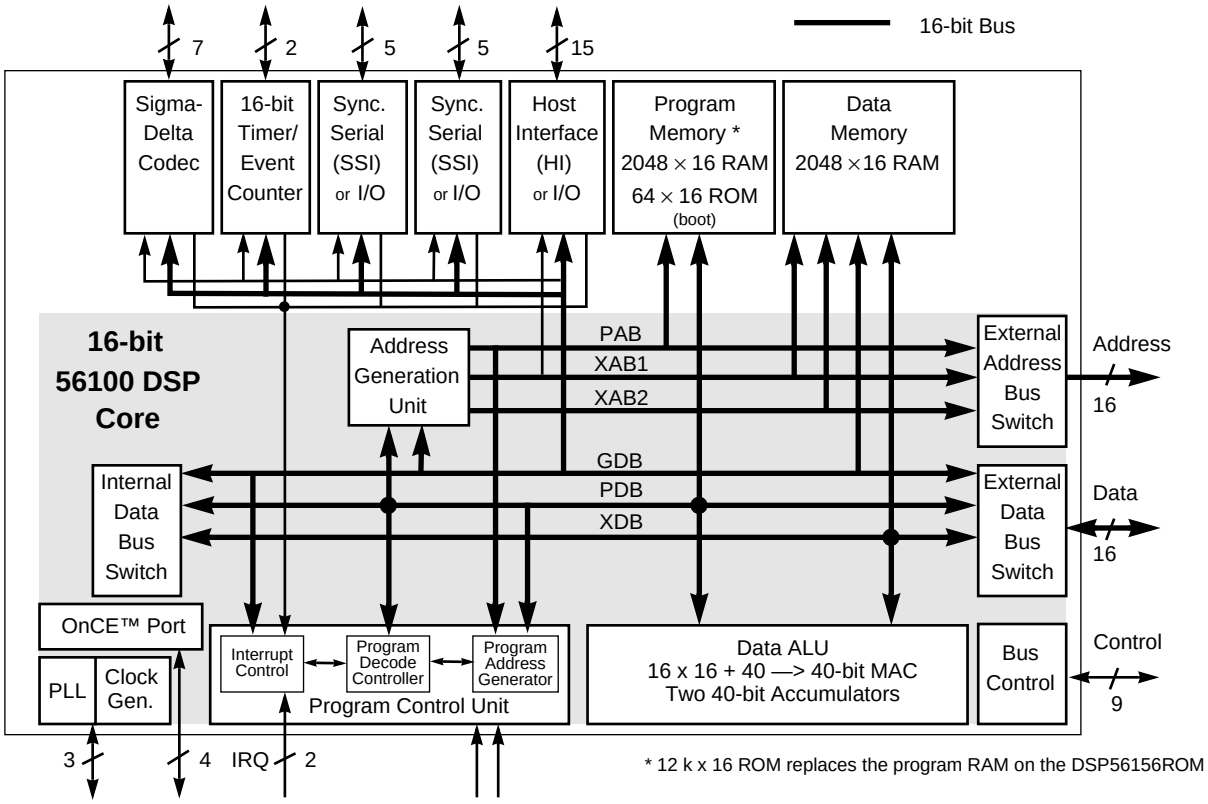

Figure 1 DSP56156 Block Diagram

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DSP56156 Features

Digital Signal Processing Core

- Efficient, object code compatible, 16-bit 56100-Family DSP engine
  - — Up to 30 Million Instructions Per Second (MIPS) – 33 ns instruction cycle at 60 MHz
  - — Up to 180 Million Operations Per Second (MOPS) at 60 MHz
  - — Highly parallel instruction set with unique DSP addressing modes
  - — Two 40-bit accumulators including extension byte
  - — Parallel 16 × 16-bit multiply-accumulate in 1 instruction cycle (2 clock cycles)
  - — Double precision 32 × 32-bit multiply with 72-bit result in 6 instruction cycles
  - — Least Mean Square (LMS) adaptive loop filter in 2 instructions
  - — 40-bit Addition/Subtraction in 1 instruction cycle
  - — Fractional and integer arithmetic with support for multiprecision arithmetic
  - — Hardware support for block-floating point FFT
  - — Hardware-nested DO loops including infinite loops
  - — Zero-overhead fast interrupts (2 instruction cycles)
  - — Three 16-bit internal data buses and three 16-bit internal address buses for maximum information transfer on-chip

Memory

- On-chip Harvard architecture permitting simultaneous accesses to program and memories
- 2048 × 16-bit on-chip program RAM and 64 ×16-bit bootstrap ROM (or 12 k × 16-bit on-chip program ROM on the DSP56156ROM)
- 2048 × 16-bit on-chip data RAM
- External memory expansion with 16-bit address and data buses
- Bootstrap loading from external data bus, Host Interface, or Synchronous Serial Interface

Peripheral and Support Circuits

- Byte-wide Host Interface (HI) with Direct Memory Access support
- Two Synchronous Serial Interfaces (SSI) to communicate with codecs and synchronous serial devices
  - — Built in μ-law and A-law compression/expansion
  - — Up to 32 software-selectable time slots in network mode
- 16-bit Timer/Event Counter also generates and measures digital waveforms
- On-chip sigma-delta voice band Codec:
  - — Sampling clock rates between 100 kHz and 3 MHz
  - — Four software-programmable decimation/interpolation ratios
  - — Internal voltage reference ($^2/_5$ of positive power supply)
  - — No external components required

- On-chip peripheral registers memory mapped in data memory space
- Double buffered peripherals
- Up to 27 general purpose I/O pins
- Two external interrupt request pins
- On-Chip Emulation (OnCE™) port for unobtrusive, processor speed-independent debugging
- Software-programmable, Phase-Locked Loop-based (PLL) frequency synthesizer for the core clock

Miscellaneous Features

- Power-saving Wait and Stop modes
- Fully static, HCMOS design for operating frequencies from 40 or 60 MHz down to DC
- 112-pin Ceramic Quad Flat Pack (CQFP) surface-mount package; 20 ×20 × 3 mm
- 112-pin Plastic Thin Quad Flat Pack (TQFP) surface-mount package; 20 × 20 × 1.4 mm
- 5 V power supply

Product Documentation

The data sheet plus the two manuals listed in Table 1 are required for a complete DSP56156 description and are necessary to properly design with the part. Documentation is available from a local Motorola distributor, a semiconductor sales office, or through a Motorola Literature Distribution Center.

Table 1 DSP56156 Documentation

Topic	Description	Order Number
DSP56100 Family Manual	Detailed description of the 56000-family architecture and the 16-bit core processor and instruction set	DSP56100FAMUM/AD
DSP56156 User's Manual	Detailed description of memory, peripherals, and interfaces	DSP56156UM/AD
DSP56156 Data Sheet	Pin and package descriptions, and electrical and timing specifications	DSP56156/D

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