DSP56007EVM

24-BIT
DIGITAL SIGNAL PROCESSOR
EVALUATION MODULE

USER'S GUIDE

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MOTOROLA

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SECTION 1

INTRODUCTION

This document describes the basic structure, theory, and operation of the DSP56007EVM Evaluation Module (Evaluation Module), the equipment required to use the Evaluation Module, and the specifications of the key components on the Evaluation Module. Code samples and self-test code are provided on the accompanying software diskette. Evaluation Module schematic diagrams and a parts list are included as well.

1.1 EVALUATION MODULE DESCRIPTION AND FEATURES

The DSP56007EVM is a low-cost platform for multichannel digital audio applications design, prototyping, and development. The fully assembled and tested circuit board contains:

- 24-bit DSP56007 Digital Signal Processor operating at 66 MHz
- 8192 bytes of off-chip SRAM and 8192 bytes of nonvolatile RAM
- Standard 30-pin SIMM slot for easy, inexpensive DRAM expansion
- One 20-bit stereo analog-to-digital converter (ADC), three 18-bit stereo digital-to-analog converters (DACs)
- Programmable analog-domain attenuators on the digital-to-analog outputs
- RCA jacks for all analog audio input/output

Evaluation Module Description and Features

- Optical and transformer-isolated electrical SPDIF / CP340 stereo digital audio inputs and outputs
- 50-pin expansion connector to provide the capability for expansion and / or substitution of other input / output peripherals, as well as easy interprocessor communication between Motorola Evaluation Modules
- Socketed MC68HC11E9 (52-pin CLCC microcontroller) to allow the user to substitute user-programmed microprocessor and prototype custom 68HC11 code (allows connection to MC68HC11 emulation systems)
- 2 × 16 character liquid crystal display (LCD) and four softswitches for user interface
- Connector provides capability to use optional standard 4 × 4 keypad matrix
- MC68705K1 microcontroller performing RS-232-to-OnCE™ port command conversions

SECTION 2

EQUIPMENT

The following section gives a brief summary of the equipment required to use the Evaluation Module, some of which is supplied with the Evaluation Module, and some of which will have to be supplied by the user.

2.1 WHAT YOU GET WITH THE EVALUATION MODULE

- Evaluation Module board (See Figure 2-1)
- 3.5” disk titled ‘Debug - Evaluation Module’
- 3.5” disk titled ‘Evaluation Module Software’
- Debug - Evaluation Module manual
- DSP56000 Family Manual
- DSP56007 User’s Manual
- DSP56007 Data Sheet
- DSP56007EVM User’s Guide (this document), including Evaluation Module Schematics
- Additional relevant documentation may be included in the form of a READ.ME file on the Evaluation Module Software disk.

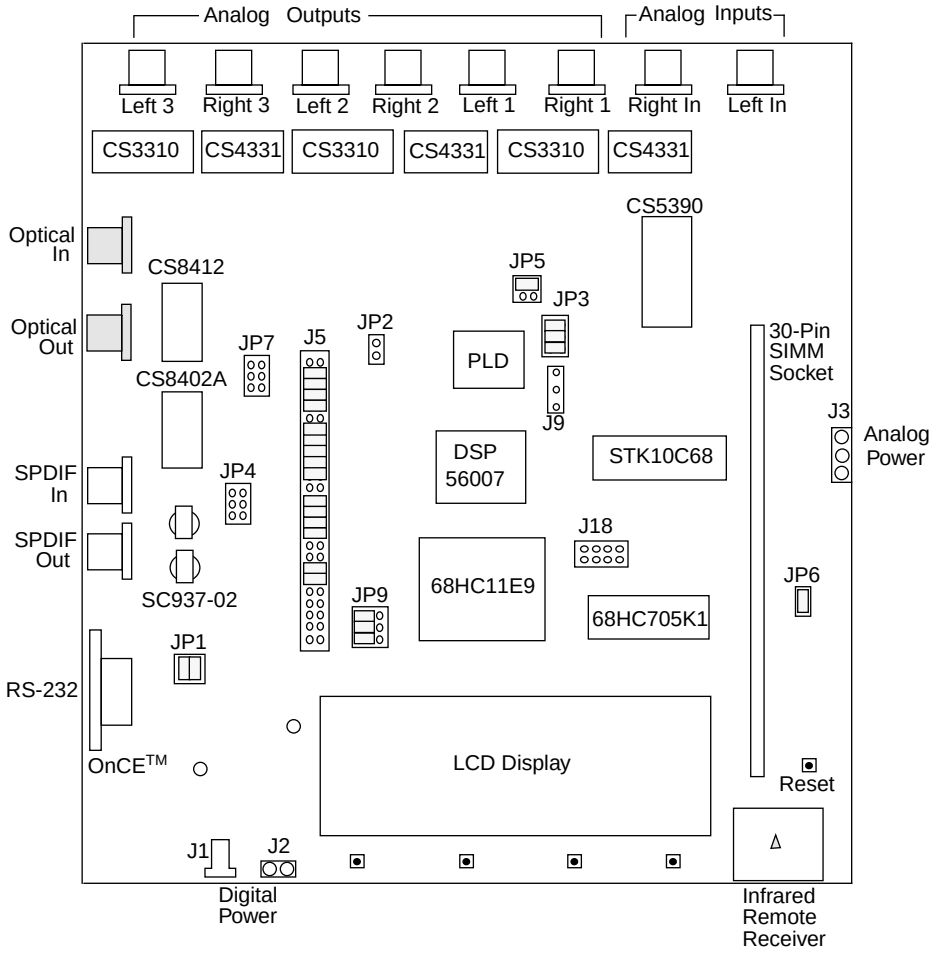


Figure 2-1 Evaluation Module Component Layout

2.2 WHAT YOU NEED TO SUPPLY

- A PC (-386 or higher) with minimum 2 Mbytes of memory, a 3.5” floppy disk drive, and a serial port capable of at least 19,200 bits-per-second data transfer rate.
- An RS-232 cable (DB9 male to DB9 female)
- Power supplies: dual 8-12V DC (for analog circuits), 8-15V AC or DC (for digital circuits)

- An audio source, an audio amplifier driving headphones or speakers, and cables with RCA / phono connectors are required to use the demo software

SECTION 3

EVALUATION MODULE THEORY OF OPERATION

Refer to **Section 7, 56007EVM Schematics**, for reference to pinouts and jumper configurations.

3.1 INPUTS AND OUTPUTS

Analog signals connected to the Evaluation Module inputs are converted to 20 bit-data at the ADC. U19 and U20 attenuate the signal and convert it to balanced mode.

The ADC has the Select Serial I/O Mode (SMODE) pin pulled high to make the ADC the SAI receive clock master. In master mode, the ADC's Serial Data Clock (SCLK) and Left/Right Select (L/$\overline{R}$) word clock pins are outputs. The L/$\overline{R}$ word clock output is the opposite polarity of I^2S. It is inverted in the programmable logic device (PLD) to create true I^2S. The ADC receives its oversampling clock on the Digital Section Clock Input (ICLKD), which is then internally divided by two, and this signal is provided to the Analog Section Clock Input (ICLKA). ICLKD can be driven from the 11.2896 MHz clock, the 12.288 MHz clock, or the $256 \times F_s$ clock produced by the CS8412 AES/EBU Receiver. The Audio Power Down Input (APD) and Digital Power Down Input (DPD) pins are wired to the $\overline{\text{Cntl\_Mute}}$ signal of the PLD. When pulled high, the ADC will be muted. When first pulled low, the ADC will be reset, then it will be enabled.

The other possible input source comes from the SPDIF inputs (J14 for electrical input and J17 for optical input). Jumper JP4 selects the source (see Table 1 below). When receiving valid SPDIF input, the SPDIF Receiver drives the Master Clock (MCK) output that is 256 times the Frame Sync frequency of the received data. The CS8412 operates in Mode 3, the I^2S slave mode.

Table 3-1 Digital Audio Input Selection

Selection	Jumper Settings
Electric SPDIF	JP4.1 to JP4.3 JP4.2 to JP4.4
Optical SPDIF	JP4.3 to JP4.5 JP4.4 to JP4.6

3.1.1 Clock Select

The Evaluation Module provides a means for the user to select which clock controls the reception and transmission of digital audio (see Table 3-2 below). JP2 selects the ADC and DAC clocks which, when jumpered, are set at 44.1 KHz and, when not jumpered, at 48 KHz. The expansion connector, J5, can be used to directly access the DSP. The receive SAI bus may be clocked by the selection made at JP2 (44.1 KHz or 48 KHz) or be clocked by the received SPDIF signal. The transmit SAI bus may be clocked by either the clock selected at JP2 or by the data and word clocks output from the DSP when it is in master mode. It is the user's responsibility to ensure that data is output at the desired rate. See Table 3-2, below.

Table 3-2 Digital Audio Receive/Transmit Jumper Configuration

Receive/ Transmit	Jumper JP5.1 to JP5.2	Jumper JP5.3 to JP5.4	No Jumper
Rx	Clocked by crystal	–	Clocked by received SPDIF
Tx	–	Clocked by crystal	Clocked by DSP

3.1.2 Serial Audio Interface (SAI)

The DSP56007 SAI transmitter drives the six analog outputs and the SPDIF output. I^2S is the default mode for the DACs. The Master Clock (MCLK) rate for the DACs is 256 $\times F_s$. The dual RC networks after the DACs serve as AC couplers for audio data and as low-pass filters to convert the delta-sigma digital output pulses to analog waveforms.

The digitally controlled analog domain attenuators receive the audio data and attenuate or amplify the data as determined by the microcontroller. The attenuators receive the Serial Clock Input (SCLK), Serial Data Input (SDATAI), and the Chip Select / Latch ($\overline{CS}$) from the microcontroller.

3.1.3 Sony-Philips Digital Interface Format (SPDIF)

The SPDIF transmitter receives data from the DSP through the Serial Data Input (SDATA) using the Frame Sync (FSYNC) and the Serial Data Clock (SCK). The transmitter outputs SPDIF audio signals through J15 (electrical) and J16 (optical). Fs_sens from the clock select appears at the expansion connector in order to read the sampling rate with the DSP's General Purpose I / O (GPIO1) at J5.41 and also at U21-2 to select the state of the 'sample-rate' bits transmitted within the channel status block. See the SPDIF specification for more information. The channel status bits and block sync signals (DRcv_Blk, DTrn_Blk, DRcv_CS, and DTrn_CS) are available at J5.43 to allow the DSP to read one of them as well. Isolation transformers are used on both input and output, although they are not strictly required for SPDIF, because this Evaluation Module is intended to be used as a development system.

3.1.4 Other Inputs and Outputs

The infrared remote receiver connects directly to the MC68HC711E9 and receives its commands from an infrared remote (though not currently implemented, this feature is planned for a future software release). The clock master is derived from one of two sources: the 11.2896 MHz clock or the 12.288 MHz clock. The microcontroller also receives commands from either the soft switches (S1, S2, S3, or S4) or from the Keypad Expansion Port, J18. The current user screen or the results of these commands are then displayed by a modular LCD panel with a 2 × 16 character display. The

microcontroller code is capable of driving larger LCD displays, but all user screens are designed for a 2×16 character display.

The MC68HC711E9 communicates with the DSP via the Serial Host Interface (SHI) port in SPI mode. When $\overline{SS}$ is pulled low, the microcontroller can write to the DSP. The MOSI and MISO lines pass control data through the DSP SHI in 24-bit mode. SCK is the SPI Shift Clock from the DSP. Again, the expansion connector, J5, can be used to access or intercept host port communications.

The Control_Data, Control_Clock, and Control_Latch lines from the microcontroller control the digitally controlled analog domain attenuators. The Control_Mute line mutes the ADC and the DACs; low is muted, high is enabled.

3.2 OPERATING MODE SELECTION

DSP56007EVM modes can be selected at JP3 as shown in Table 3-3. Once the mode has been selected, the PLD can receive interrupts from the network attached to J19.

Table 3-3 Mode Select Jumpers

Mode	JP3.5 to JP3.6	JP3.3 to JP3.4	JP3.1 to JP3.2
0	X	X	X
1	X	X	-
2	X	-	X
3	X	-	-
4	-	X	X
5	-	X	-
6	-	-	X
7	-	-	-

X = jumper installed; - = no jumper

3.3 BOOTSTRAP CONFIGURATION USING JP9

In the SHI bootstrap mode, JP9 can be configured to bootstrap the DSP by setting the jumpers according toTable 3-4. The first code-set contains the pass-through code included on the 56007EVM software disk. The second code-set currently contains shell

code to be replaced by Dolby ProLogic code in a future software release. JP9's pinout is shown in Figure 3-1.

Table 3-4 JP9 Configuration

JP3.1 to JP3.4 Do not send bootstrap code from HC11 to DSP		
JP3.4 to JP3.1 Send bootstrap code from HC11 to DSP	JP3.2 to JP3.5 Send 1st code-set in higher memory	JP3.3 to JP3.6 Send peripheral changes as if running ProLogic/THX out of ROM
	JP3.5 to JP3.1 Send 2nd code-set in higher memory	JP3.6 to JP3.1 Do not send peripheral changes

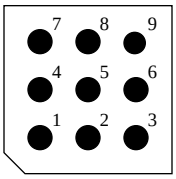


Figure 3-1 JP9 Pinout

3.4 ONCE™ PORT

The OnCE™ port interface operates by receiving the serial data from the RS-232 Transceiver and executing commands sent by the host computer. These commands can reset the DSP, put the DSP in debug mode, release the DSP from debug mode, read and write to the OnCE™ port, and read and write to the DSP itself. The serial bit rate is 19,200 bits / second. The RS-232 serial communications are performed in software on the MC68705K1. Port A of the MC68705K1 communicates with the DSP, and port B communicates with the host computer. The acknowledge signal from the OnCE™ port is a low-going pulse on DS0. Since the 68705K1 is too slow to reliably catch this very narrow pulse, the pulse is latched in the PLD and the output of the latch appears on the ACK pin (PA2). When this occurs, the 68705K1 illuminates red LED D5 to indicate that the DSP is in the debug mode. For more information on the OnCE™ port, see the DSP56000 Family Manual. The reset switch will reset the microcontroller,

which will subsequently reset the DSP56007. The MC68705K1 source and object code are available from the Motorola DSP Division; contact your local Motorola FAE.

3.5 RS-232 CONNECTIONS AND JP1

RS-232 is an often-abused standard, and the direction of the signals present on pins 2 and 3 of the DB9 connectordo not always conform to the standard. JP1 provides the user with the ability to reverse these two pin connections without resorting to NULL Modem adapters or rewiring cable connectors. As shipped, JP1.1 is connected via shorting jumpers to JP1.3 and JP1.2 is connected to JP1.4. This connects J4.2 to the OUTPUT of the Evaluation Module's RS-232 level converter (U4) and J4.3 to the INPUT of the board's RS-232 receiver. These directions can be reversed by reorienting the shorting jumpers and turning them 90 degrees (one-quarter turn), thereby connecting JP1.1 to JP1.2 and JP1.3 to JP1.4. The user should never need to rewire an RS-232 connector in order to establish Evaluation Module communications with a host computer.

3.6 OPERATING MODES AND SRAM REFRESH IN THE 56007

In modes 0, 1, 2, and 3 the SRAM is refreshed from the nvRAM and the DSP can bootstrap from the SRAM via the EMI if a valid bootstrap mode is used. When in modes 4, 5, 6, and 7 the SRAM is not refreshed. Refreshes are not affected by jumpers on the expansion connector, J5. Jumpers J5.37 and J5.39 must be inserted to have full DSP control of the SRAM and nvRAM after bootstrap.

3.7 EVALUATION MODULE PARTS LIST

The parts list of the DSP56007EVM is shown in **Section 8**.

3.8 POWER SUPPLIES

The Evaluation Module requires power sources, for both analog and digital circuits, in order to operate. Bipolar analog power (use a linear power supply for best results)

is received through screw terminals at J3. Digital power is received through screw terminals at J2 or via a 2.1mm connector (J1). When the power is on, D6 (green LED) is illuminated. Analog power input may be 8 to 12 volts and digital power input may be 8 to 15 volts. While the voltage regulator can accommodate higher input voltage potentials, the added heat dissipation required at these input voltage levels will result in the regulator becoming dangerously warm and it is not recommended that the user subject the board to power inputs in excess of the maximum levels listed.

Note: Always supply the Evaluation Module with analog power prior to or simultaneous with the application of digital power. If digital power is supplied before the analog power, the DACs may go into one of three possible error modes (no long-term damage to the device will occur) and will not function correctly. If analog power is supplied first, or if both analog power and digital power are applied simultaneously, these problems do not appear and the DACs are properly initialized.

3.9 MEMORY

The Evaluation Module has 8K (8192) bytes each of fast Static RAM (SRAM) and of nonvolatile RAM (nvRAM). The SRAM operates at zero wait states at a 40 MHz DSP clock speed and with one wait state at 50 and 66 MHz. The contents of the SRAM may be block-loaded into nvRAM and the contents of the nvRAM may be block- loaded into the SRAM. The lowest 3072 bytes of the nvRAM may also be used to store code to load into the DSP via EMI bootstrap.

On-chip DSP56007 memory includes:

- 6348 × 24-bit on-chip program ROM and 52 × 24-bit bootstrap ROM
- 1024 × 24-bit on-chip X-data RAM plus 512 × 24-bit on-chip X-data ROM
- 2176 × 24-bit on-chip Y-data RAM plus 512 × 24-bit on-chip Y-data ROM
- 1024 × 24- bits of the Y-data RAM can be configured as program RAM, replacing 1280 × 24 bits of program ROM

Table 3-5 DSP56007 Internal Memory Configurations

	PE=0	PE=1
P_RAM	0	1.024K
X_RAM	2.176K	1.024K

Table 3-5 DSP56007 Internal Memory Configurations (Continued)

	PE=0	PE=1
Y_RAM	1.024K	1.152K
P_ROM	6.348K	5.12K
X_ROM	512	512
Y_ROM	512	512

3.10 DIGITAL SIGNAL PROCESSOR OPERATING FREQUENCY

The DSP56007 is clocked at 768 kHz by a 12.288 MHz crystal divided by 16. The DSP56007 PLL is then used to multiply this frequency up to the desired operating frequency. Table 3-6 shows the frequency multiplication factors and the resulting DSP clock rates:

Table 3-6 Frequency Products

2	1.536 MHz	16	12.288 MHz	30	23.040 MHz	44	33.792 MHz	58	44.544 MHz	72	55.296 MHz
3	2.304 MHz	17	13.056 MHz	31	23.808 MHz	45	34.560 MHz	59	45.312 MHz	73	56.064 MHz
4	3.072 MHz	18	13.824 MHz	32	24.576 MHz	46	35.328 MHz	60	46.080 MHz	74	56.832 MHz
5	3.840 MHz	19	14.592 MHz	33	25.344 MHz	47	36.096 MHz	61	46.848 MHz	75	57.600 MHz
6	4.608 MHz	20	15.360 MHz	34	26.112 MHz	48	36.864 MHz	62	47.616 MHz	76	58.368 MHz
7	5.376 MHz	21	16.128 MHz	35	26.880 MHz	49	37.632 MHz	63	48.384 MHz	77	59.136 MHz
8	6.144 MHz	22	16.896 MHz	36	27.648 MHz	50	38.400 MHz	64	49.152 MHz	78	59.904 MHz
9	6.912 MHz	23	17.664 MHz	37	28.416 MHz	51	39.168 MHz	65	49.920 MHz	79	60.672 MHz
10	7.680 MHz	24	18.432 MHz	38	29.184 MHz	52	39.936 MHz	66	50.688 MHz	80	61.440 MHz
11	8.448 MHz	25	19.200 MHz	39	29.952 MHz	53	40.704 MHz	67	51.456 MHz	81	62.208 MHz
12	9.216 MHz	26	19.968 MHz	40	30.720 MHz	54	41.472 MHz	68	52.224 MHz	82	62.976 MHz
13	9.984 MHz	27	20.736 MHz	41	31.488 MHz	55	42.240 MHz	69	52.992 MHz	83	63.744 MHz
14	10.752 MHz	28	21.504 MHz	42	32.256 MHz	56	43.008 MHz	70	53.760 MHz	84	64.512 MHz
15	11.520 MHz	29	22.272 MHz	43	33.024 MHz	57	43.776 MHz	71	54.528 MHz	85	65.280 MHz

3.11 EXTERNAL INTERRUPT REQUESTS

J19 allows the user to externally initiate the External Interrupt Request A ($\overline{\text{IRQA}}$), the External Interrupt Request B ($\overline{\text{IRQB}}$), and/or the Non-Maskable Interrupt Request ($\overline{\text{NMI}}$). These pins are pulled high by 10k resistors to assure that false interrupts are not generated by floating inputs.

SECTION 4

PERIPHERAL SPECIFICATIONS

The following section describes the various peripheral devices used on the DSP56007EVM and includes any necessary equations and information. Contact information for the manufacturers of significant peripheral devices is included along with the parts listing in Section 8.

4.1 CS5390 STEREO ADC

The CS5390 is a complete analog-to-digital converter (ADC) for stereo digital audio systems. It performs sampling, analog-to-digital conversion and anti-alias filtering, generating 20-bit values for both left and right inputs in serial form. The output word rate can be up to 50 kHz per channel.

The CS5390 uses fifth-order, delta-sigma modulation with 64 times oversampling followed by digital filtering and decimation, which removes the need for an external anti-alias filter, beyond the simple balanced RC filter formed by R25, R26, and C8 (R31, R32, and C20 for the right channel).

The ADC uses a differential architecture that provides excellent noise rejection. The CS5390 has a filter passband of DC to 21.7kHz. The filters are linear phase, have 0.005 dB passband ripple, and greater than 100 dB stopband rejection. The operating temperature range is 0^o to 70^o.

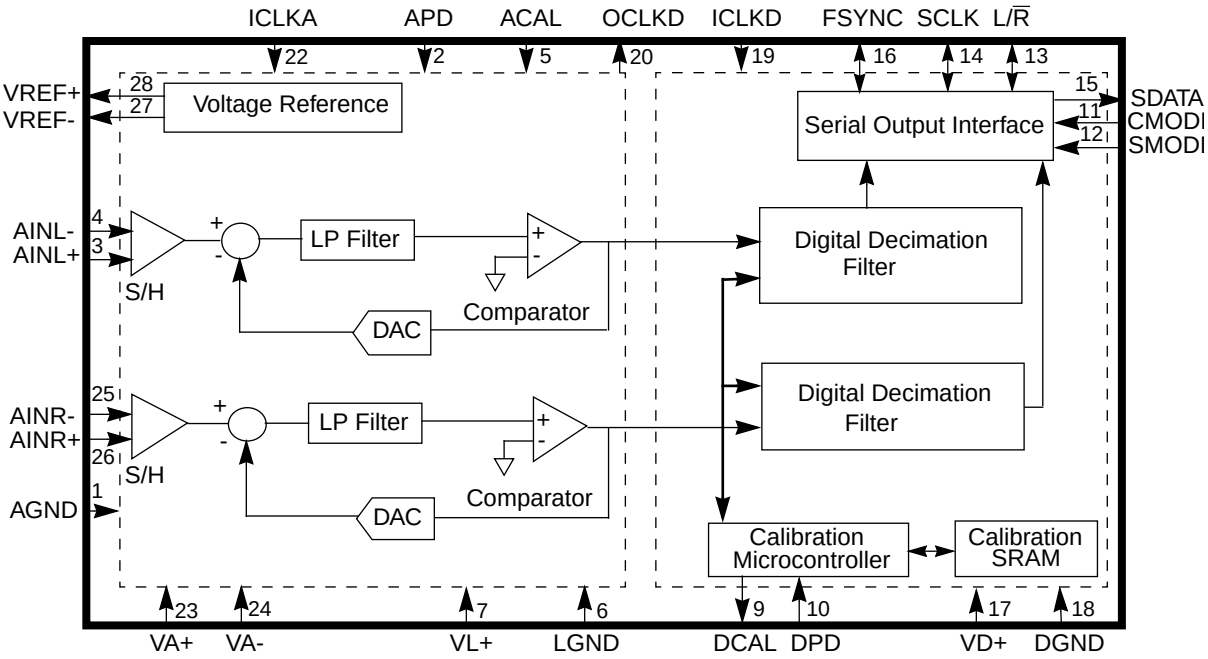


Figure 4-1 CS5390 ADC

4.2 CS4331 STEREO DAC

The CS4331 is a complete stereo digital-to-analog converter (DAC) with 18-bit resolution, including interpolation, 1-bit digital-to-analog conversion, and output analog filtering in an 8-pin package. The CS4331 is based on delta-sigma modulation where the modulator output controls the reference voltage input to an ultra-linear analog low-pass filter. This architecture allows for infinite adjustment of sample rate between 1 kHz and 50 kHz while maintaining linear phase response, simply by changing the master clock frequency. The CS4331 contains optional on-chip de-emphasis and operates from a single +5V power supply.

The CS4331 has a 96 dB dynamic range, less than 0.003% THD, low clock jitter sensitivity and completely filtered line level outputs that use linear-phase filtering.

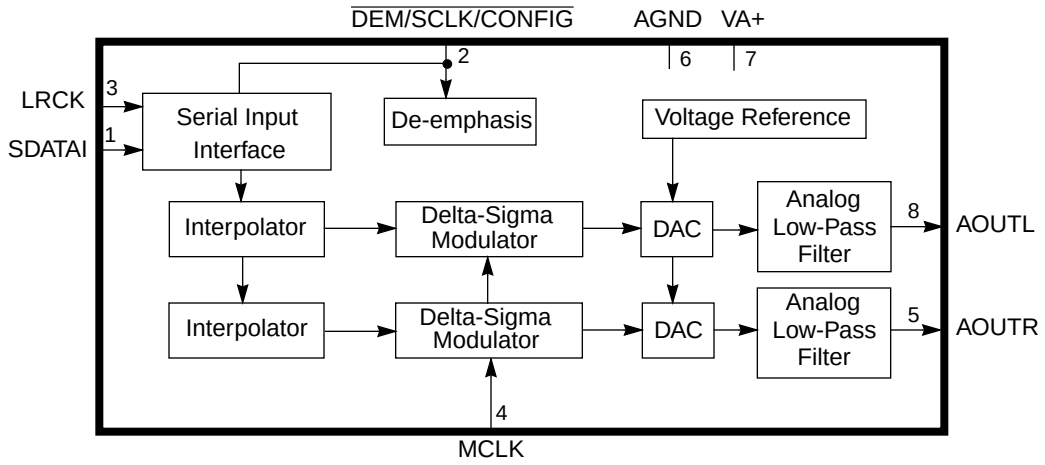


Figure 4-2 CS4331 DAC

4.3 CS3310 STEREO DIGITAL VOLUME CONTROL

The CS3310 is a complete stereo digital volume control designed specifically for audio systems. It features a 16-bit serial interface that controls two independent, low distortion (0.001% THD + N) audio channels.

The CS3310 includes an array of well-matched resistors and a low-noise active output stage that is capable of driving a 600 Ω load. A total adjustable range of 127 dB, in 0.5 dB steps, is achieved through 95.5 dB of attenuation and 31.5 dB of gain. The simple 3-wire interface provides daisy-chaining of multiple CS3310s for multi-channel audio systems. The device operates from ±5V supplies and has an input/output voltage range of ±3.75V.

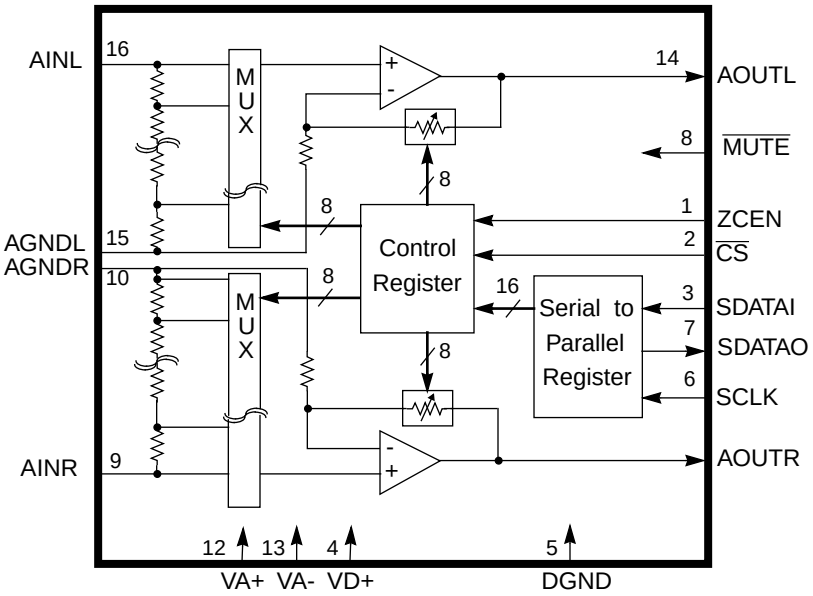


Figure 4-3 CS3310 Stereo Digital Volume Control

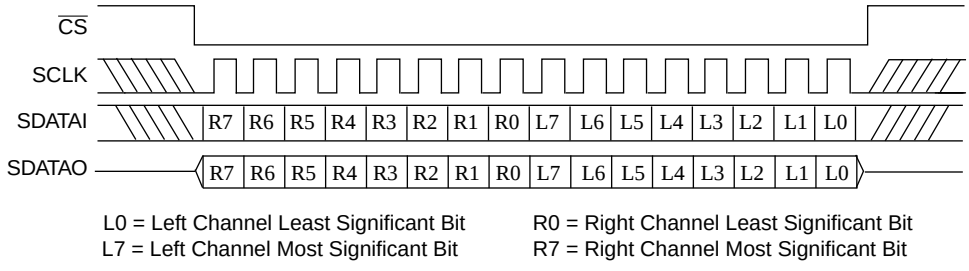


Figure 4-4 Serial Port Timing for the CS3310

4.4 CS8412 DIGITAL AUDIO INTERFACE RECEIVER

The CS8412 is a monolithic CMOS device that receives and decodes audio data according to the AES 3 - 1992, EBU Tech. 3250-E, IEC 958, SPDIF, and EIAJ CP-340 interface standards. The CS8412 receives data from a transmission line, recovers the clock and synchronization signals, and de-multiplexes the audio and non-audio data. Either differential or single-ended inputs can be decoded. The CS8412 de-multiplexes the channel, user, and validity data directly to dedicated output pins for the most commonly needed channel status bits.

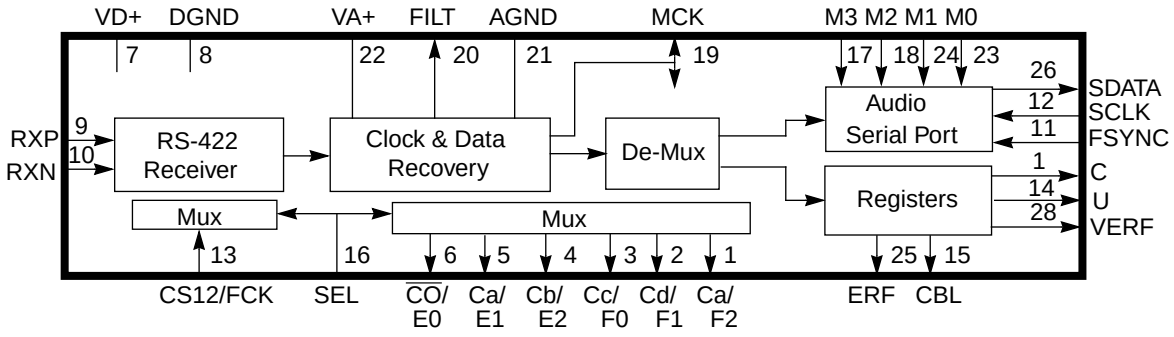


Figure 4-5 CS8412 Digital Audio Interface Receiver

4.5 CS8402A DIGITAL AUDIO INTERFACE TRANSMITTER

The CS8402A is a monolithic CMOS device that encodes and transmits audio data according to the AES 3 - 1992, EBU Tech. 3250-E, IEC 958, SPDIF, and EIAJ CP-340 interface standards. The CS8402A accepts audio and non-audio data and multiplexes and encodes the data. The audio serial port is double-buffered and capable of supporting a wide variety of formats. The CS8402A multiplexes the channel, user, and validity data directly from dedicated input pins for the most commonly needed channel status bits.

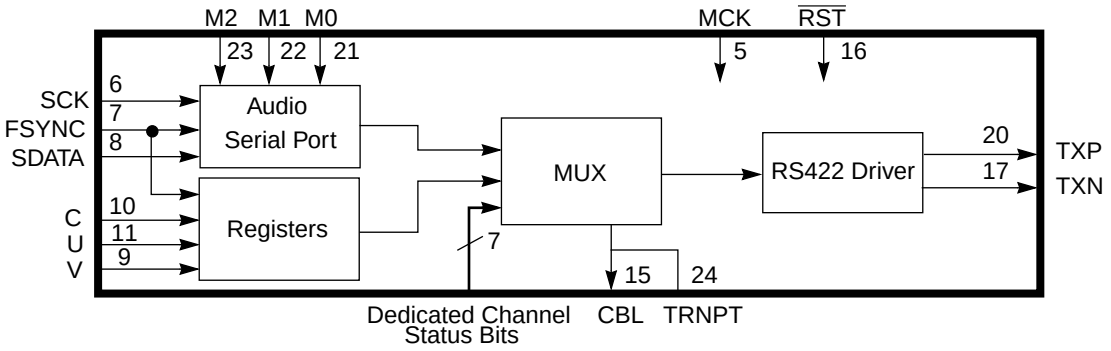


Figure 4-6 CS8402 Digital Audio Interface Transmitter

4.6 STK10C68 CMOS 2K X 8 NVSRAM

The Simtek STK10C68 is a fast static RAM (25, 30, 35, and 45ns), with a nonvolatile electrically-erasable PROM (EEPROM) element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times while independent, nonvolatile data resides in EEPROM. Data may easily be transferred from the SRAM to the EEPROM (STORE cycle), or from the EEPROM to the SRAM (RECALL cycle) using the $\overline{NE}$ pin (nonvolatile enable). It combines the high performance and ease of use of a fast SRAM with nonvolatile data integrity.

The STK10C68 features 12, 15, 20, and 25ns output enable access times, hardware STORE and RECALL initiation, automatic STORE and RECALL timing, 10^4 or 10^5 STORE cycles to EEPROM, unlimited RECALL cycles from EEPROM, and 10-year data retention in EEPROM. The STK10C68 requires a single +5V power supply.

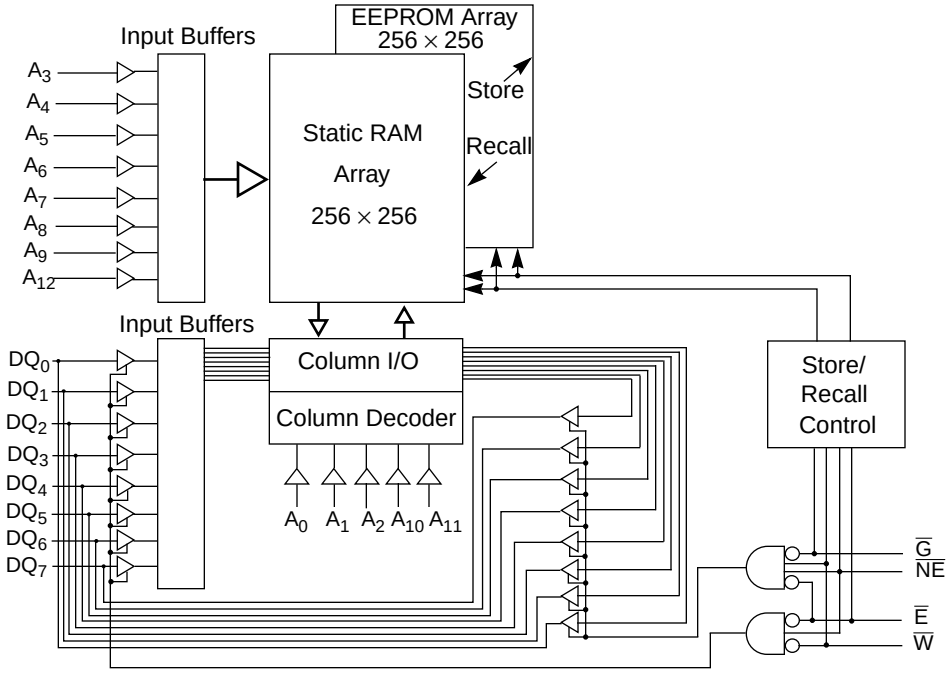


Figure 4-7 STK10C68 8K × 8 nvSRAM

4.7 SC937-02 AES/EBU TRANSFORMER

The AES/EBU circuit incorporates a transformer to reject common mode interference while transmitting the signal with fast rise time and minimum aberration. The SC937-02 is a surface mount, low capacitance, wide-band AES/EBU transformer. The SC937-02 has a very low capacitance shielded winding that reduces both radiated and received noise coupling and provides decreased jitter and improved audio quality, especially in noisy environments. EMI compliance and EMI susceptibility are improved by the use of this type of transformer. The transformer's ratio is 1:1, primary inductance is 600µH, inter-winding capacitance is 1.1pF, bandwidth is 16kHz to 100MHz, and rise-time is 3ns.

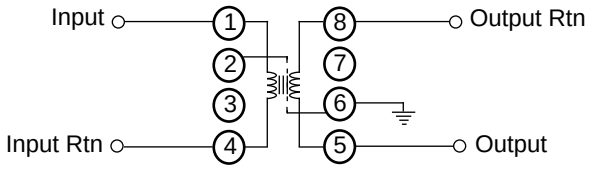
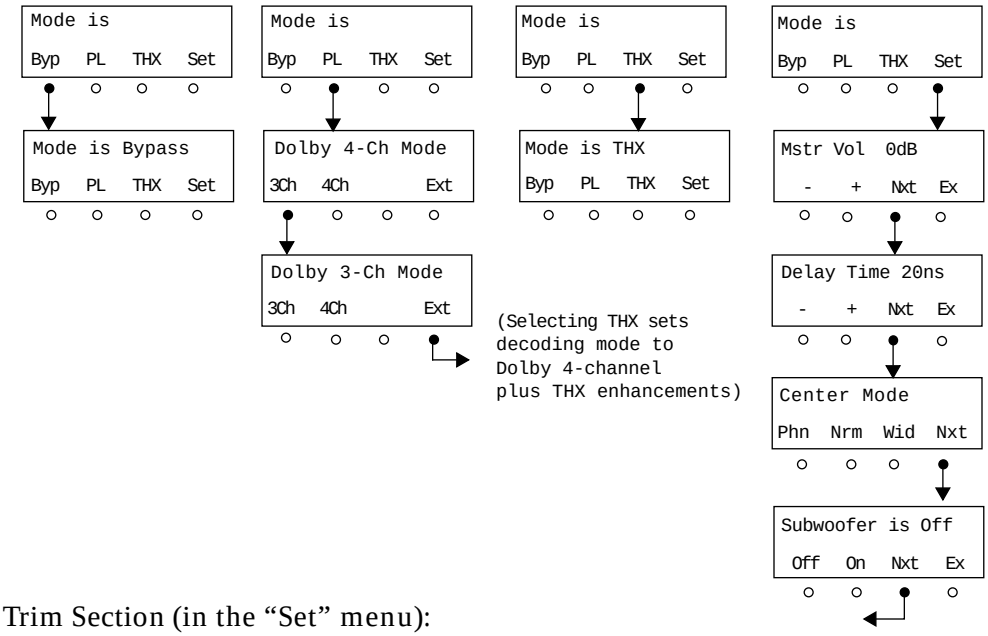


Figure 4-8 SC937-02 AES/EBU Transformer

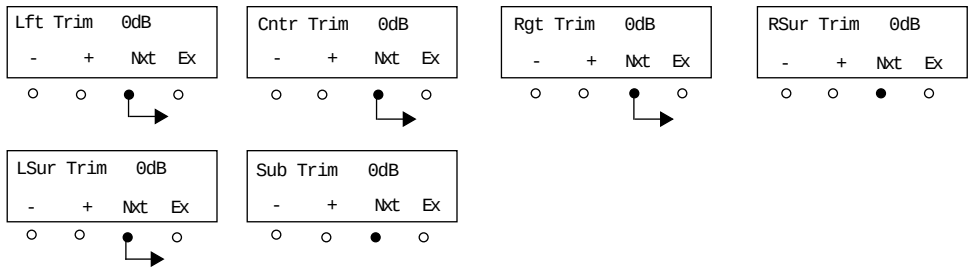
4.8 LCD PANEL

Figure 4-9 illustrates the different screens of the LCD panel and the corresponding actions of the soft switches. Note that ProLogic and THX functionality is not available on the generic DSP56007EVM. The attenuator trim functions (shown in the trim section in Figure 4-9) are fully functional on the generic 56007EVM.

Figure 4-10 illustrates the different screens of the LCD with respect to the 4×4 keypad matrix.



Trim Section (in the “Set” menu):



Re-equalization (Dolby 4-channel mode and THX mode must be active):

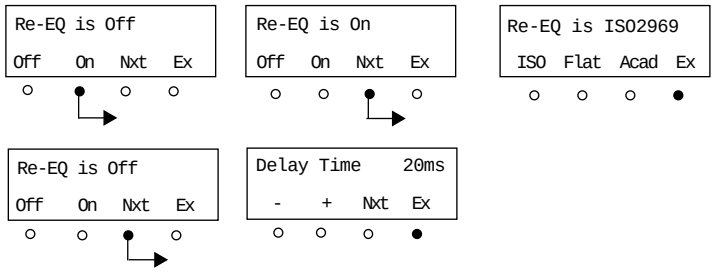


Figure 4-9 LCD Softswitch Screens

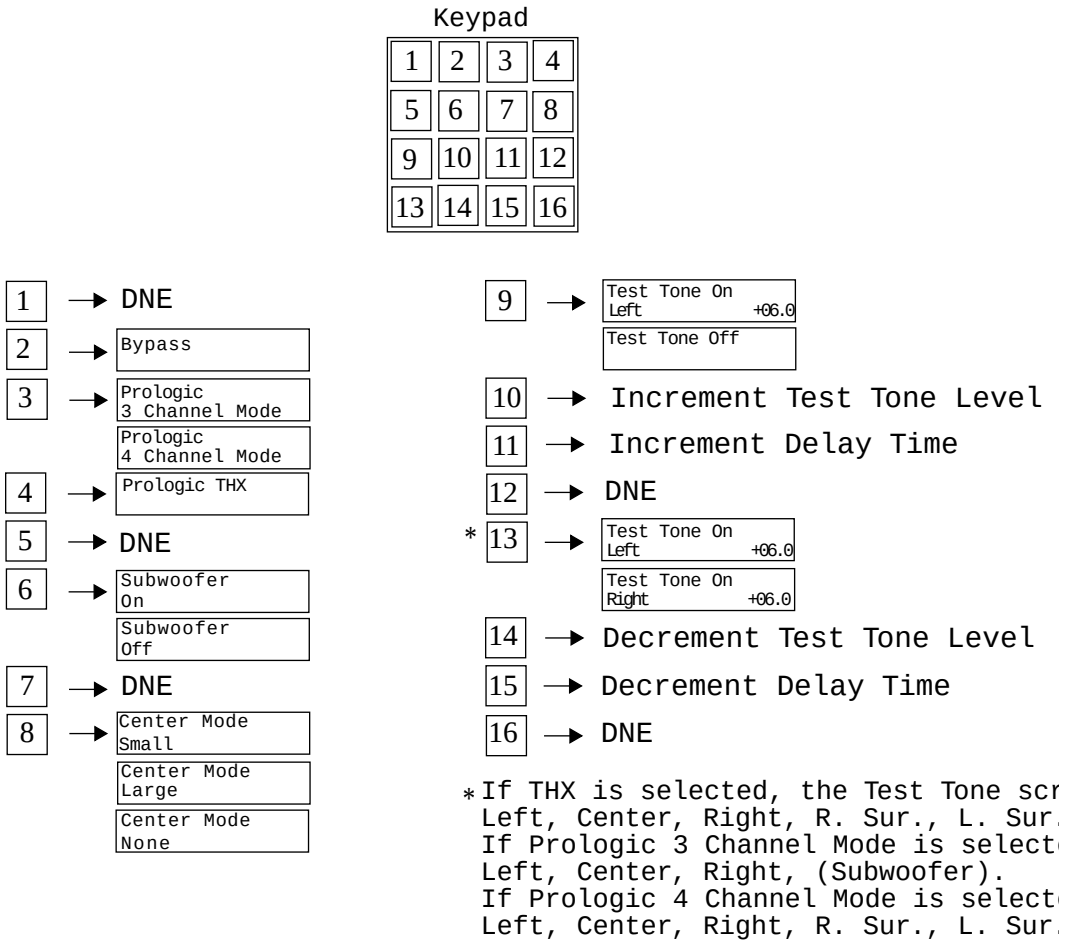


Figure 4-10 LCD Keypad Screens

4.9 WIRING FOR KEYPAD

A wiring diagram for a generic keypad is shown in Figure 4-11.

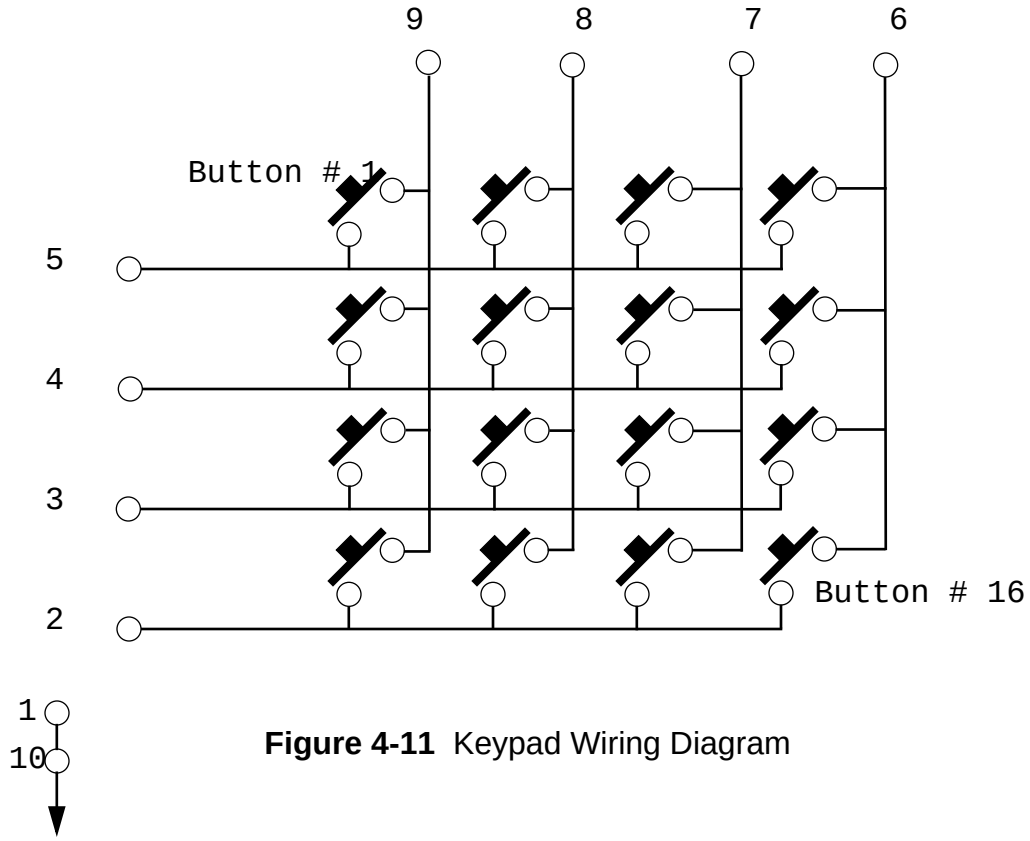


Figure 4-11 Keypad Wiring Diagram

SECTION 5

EPM7032 PLD EQUATIONS

The following data represents the PLD equations for the DSP56007EVM:

```
ACK_RST  : INPUT;
ClkSelA  : INPUT;
CLKSELB  : INPUT;
CNTL_MUTE : INPUT;
DSO      : INPUT;
DSP_RST  : INPUT;
EMI_MRD  : INPUT;
EXP2_~WSR : INPUT;
FS_SENS  : INPUT;
IRQA     : INPUT;
IRQB     : INPUT;
IRQC     : INPUT;
MODA_SEL : INPUT;
MODB_SEL : INPUT;
MODC_SEL : INPUT;
RCVMASTER_SEL : INPUT;
TXMASTER_SEL : INPUT;
11MHZ_CLK : INPUT;
12MHZ_CLK : INPUT;
8412_MCK : INPUT;

% ACK      = _LC031 %
 ACK     = LCELL( _EQ001 $  GND);
  _EQ001 =  _X001;
```

```
  _X001  = EXP( DSO &  _X002);
  _X002  = EXP( ACK_RST &  _X001);

% ADA_CLK  = _LC006 %
 ADA_CLK = LCELL( _EQ002 $  GND);
  _EQ002 =  FS_SENS &  _LC026
         # !FS_SENS &  _LC025;

% ADA_Clk/2 = _LC019 %
% ADA_Clk/2 = |74393:15|Q1A %
 ADA_Clk/2 = TFFE( VCC,  _EQ003,  VCC,  VCC,  VCC);
  _EQ003 =  _X003 &  _X004;
  _X003  = EXP(!FS_SENS &  _LC025);
  _X004  = EXP( FS_SENS &  _LC026);

% DSP_CLK  = _LC020 %
% DSP_CLK  = |74393m:82|QD %
 DSP_CLK = TFFE( _EQ004, !_LC026,  VCC,  VCC,  VCC);
  _EQ004 =  _LC009 &  _LC013 &  _LC027;

% DSP_MODA = _LC010 %
 DSP_MODA = LCELL( _EQ005 $  GND);
  _EQ005 =  DSP_RST &  IRQA
         # !DSP_RST &  MODA_SEL;

% DSP_MODB = _LC011 %
 DSP_MODB = LCELL( _EQ006 $  GND);
  _EQ006 =  DSP_RST &  IRQB
         # !DSP_RST &  MODB_SEL;

% DSP_MODC = _LC012 %
 DSP_MODC = LCELL( _EQ007 $  GND);
  _EQ007 =  DSP_RST &  IRQC
         # !DSP_RST &  MODC_SEL;

% EXP2_GPIO2 = _LC016 %
EXP2_GPIO2 = TRI(_LC016, GLOBAL(!DSP_RST));
_LC016   = LCELL( GND $  GND);

% EXP2_GPIO3 = _LC021 %
EXP2_GPIO3 = TRI(_LC021, GLOBAL(!DSP_RST));
_LC021   = LCELL( GND $  GND);
```

```
% EXP2_SCKT = |74393:15|Q1B %
EXP2_SCKT = TRI(_LC002, GLOBAL(!TXMASTER_SEL));
_LC002   = TFFE( ADA_Clk/2,  _EQ008,  VCC,  VCC,  VCC);
  _EQ008 =  _X003 &  _X004;

% EXP2_WSR = _LC003 %
 EXP2_WSR = LCELL(!EXP2_~WSR $  GND);

% EXP2_WST = |74393:15|Q2D %
EXP2_WST = TRI(_LC017, GLOBAL(!TXMASTER_SEL));
_LC017   = TFFE( _EQ009, !_LC015,  VCC,  VCC,  VCC);
  _EQ009 =  _LC004 &  _LC014 &  _LC024;

% NVRAM_G  = _LC001 %
 NVRAM_G = LCELL( _EQ010 $  GND);
  _EQ010 =  DSP_RST &  EMI_MRD
         # !DSP_RST &  MODC_SEL;

% 5390_CLK = _LC023 %
 5390_CLK = LCELL( _EQ011 $  GND);
  _EQ011 =  FS_SENS &  _LC026 & !RCVMASTER_SEL
         # !FS_SENS &  _LC025 & !RCVMASTER_SEL
         #  RCVMASTER_SEL &  8412_MCK;

% |clockpr4:111|:26 %
_LC026   = TFFE( VCC,  12MHZ_CLK,  VCC,  VCC,  VCC);

% |clockpr4:111|:28 %
_LC025   = TFFE( VCC,  11MHZ_CLK,  VCC,  VCC,  VCC);

% |74393:15|Q1C = |74393:15|:5 %
_LC007   = TFFE( _EQ012,  _EQ013,  VCC,  VCC,  VCC);
  _EQ012 =  ADA_Clk/2 &  _LC002;
  _EQ013 =  _X003 &  _X004;

% |74393:15|Q1D = |74393:15|:9 %
_LC015   = TFFE( _EQ014,  _EQ015,  VCC,  VCC,  VCC);
  _EQ014 =  ADA_Clk/2 &  _LC002 &  _LC007;
  _EQ015 =  _X003 &  _X004;

% |74393:15|Q2A = |74393:15|:28 %
_LC004   = TFFE( VCC, !_LC015,  VCC,  VCC,  VCC);
```

```
% |74393:15|Q2B = |74393:15|:29 %
_LC014   = TFFE( _LC004, !_LC015,  VCC,  VCC,  VCC);

% |74393:15|Q2C = |74393:15|:30 %
_LC024   = TFFE( _EQ016, !_LC015,  VCC,  VCC,  VCC);
  _EQ016 =  _LC004 &  _LC014;

% |74393m:82|QA = |74393m:82|:1 %
_LC009   = TFFE( VCC, !_LC026,  VCC,  VCC,  VCC);

% |74393m:82|QB = |74393m:82|:3 %
_LC013   = TFFE( _LC009, !_LC026,  VCC,  VCC,  VCC);

% |74393m:82|QC = |74393m:82|:5 %
_LC027   = TFFE( _EQ017, !_LC026,  VCC,  VCC,  VCC);
  _EQ017 =  _LC009 &  _LC013;

% ~CNTL_MUTE = _LC029 %
 ~CNTL_MUTE = LCELL(!CNTL_MUTE $  GND)
```

SECTION 6

INTRODUCTION TO THE GUI

This section will give an introduction to the Graphical User Interface (GUI), detailing only that which is required to work through the brief example below. Full details of the GUI can be found in the Debug - Evaluation Module manual.

6.1 STARTING THE GUI

To start up the GUI, type '**evm56K**'. The display you see will be similar to that shown in Figure 6-1.

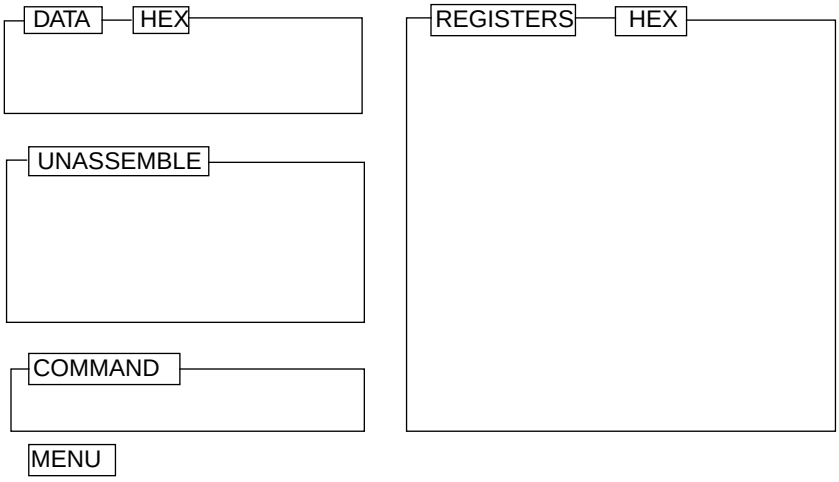


Figure 6-1 The GUI

6.2 THE GUI WINDOWS

The DATA window, shown in the top left corner, displays the data. To display the contents of X data memory, starting at location x:0, position the pointing device cursor in the COMMAND window, click once, and type: **display x:0**. The radix in which the data is shown can be changed by clicking in the box that contains the word HEX in the diagram above. Data can also be displayed in a graphical form. To do this type: **display x:0 -graph**. To change back to text type: **display x:0 -text**.

The UNASSEMBLE window shows an unassembled version of the contents of program memory. The next instruction to be executed will be highlighted.

The COMMAND window is where OnCE commands (i.e., the controlling commands) are entered.

The REGISTERS window shows the contents of the registers of the ALU (Arithmetic Logic Unit) and the AGU (Address Generation Unit)

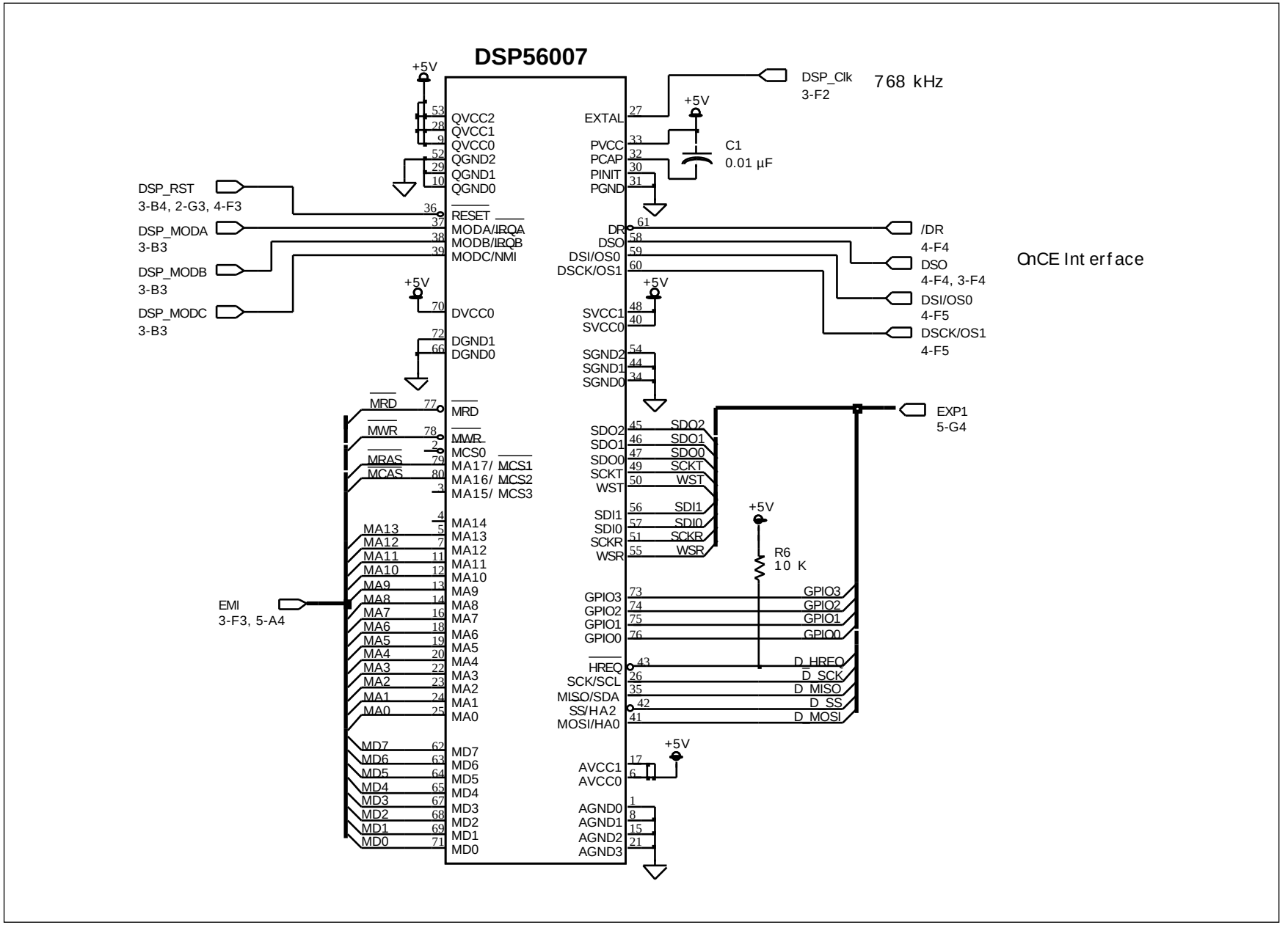


Figure 7-1 DSP56007

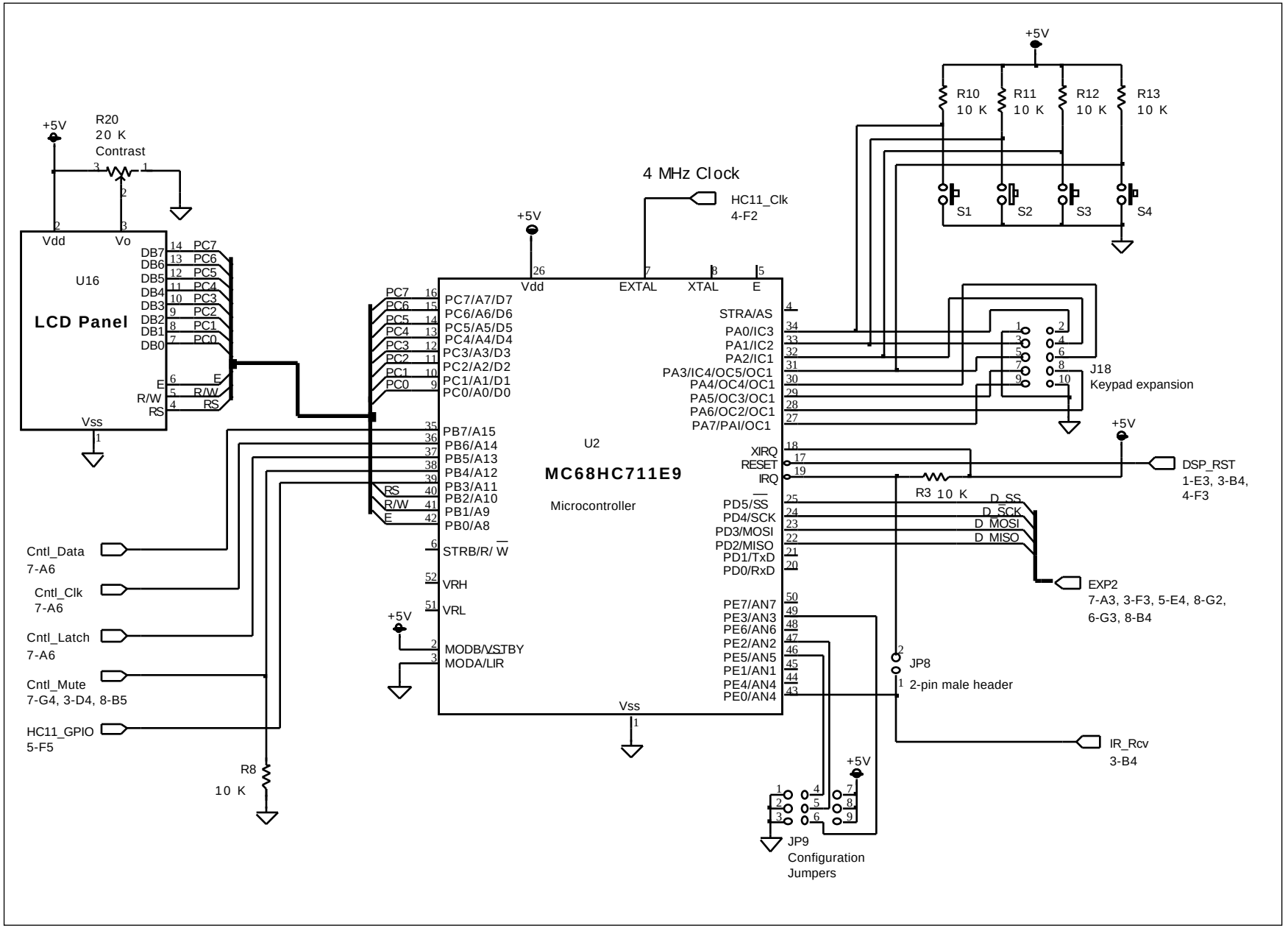


Figure 7-2 Microcontroller and LCD

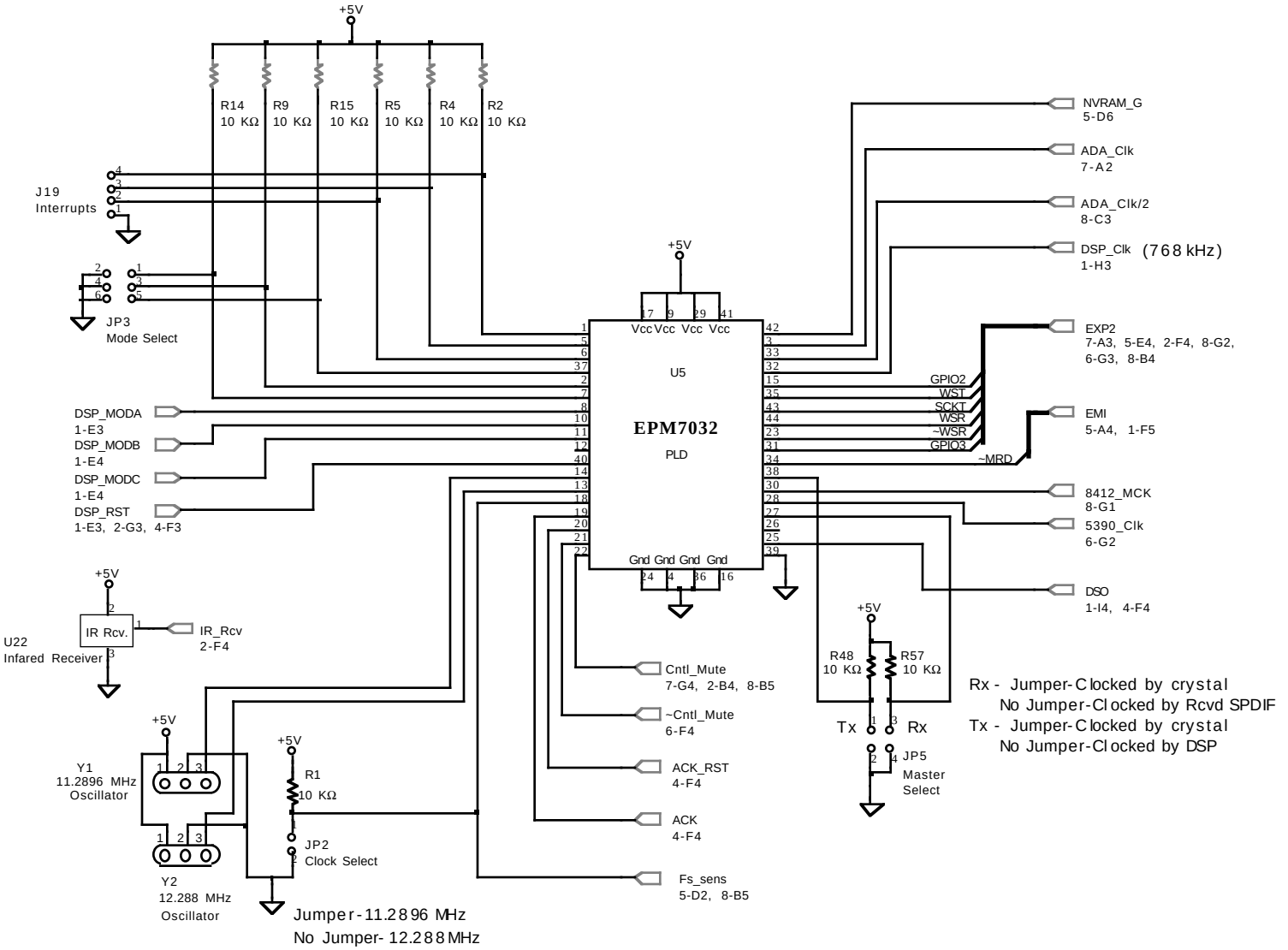


Figure 7-3 Programmable Logic Device

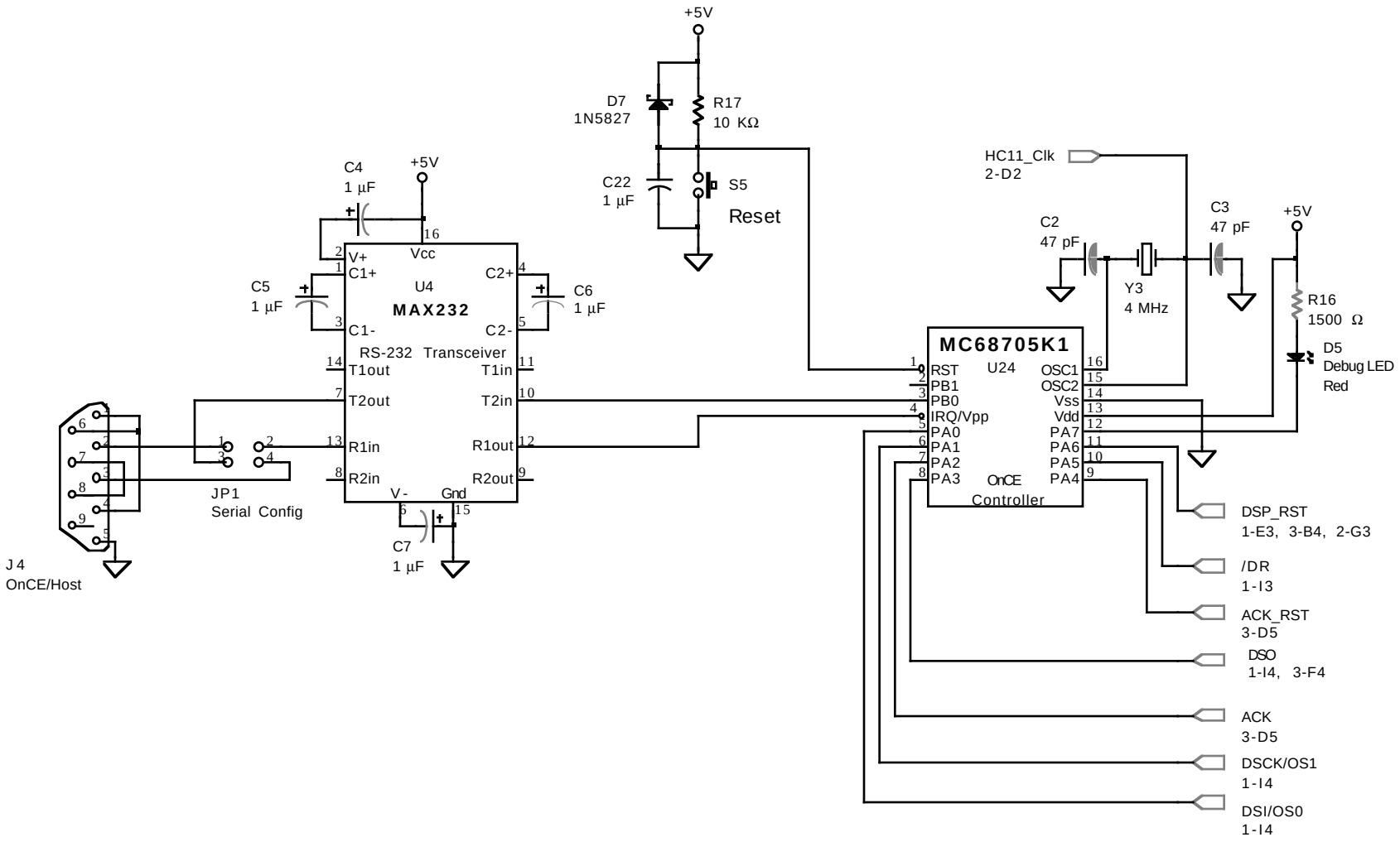


Figure 7-4 RS-232 and OnCE Port Interface

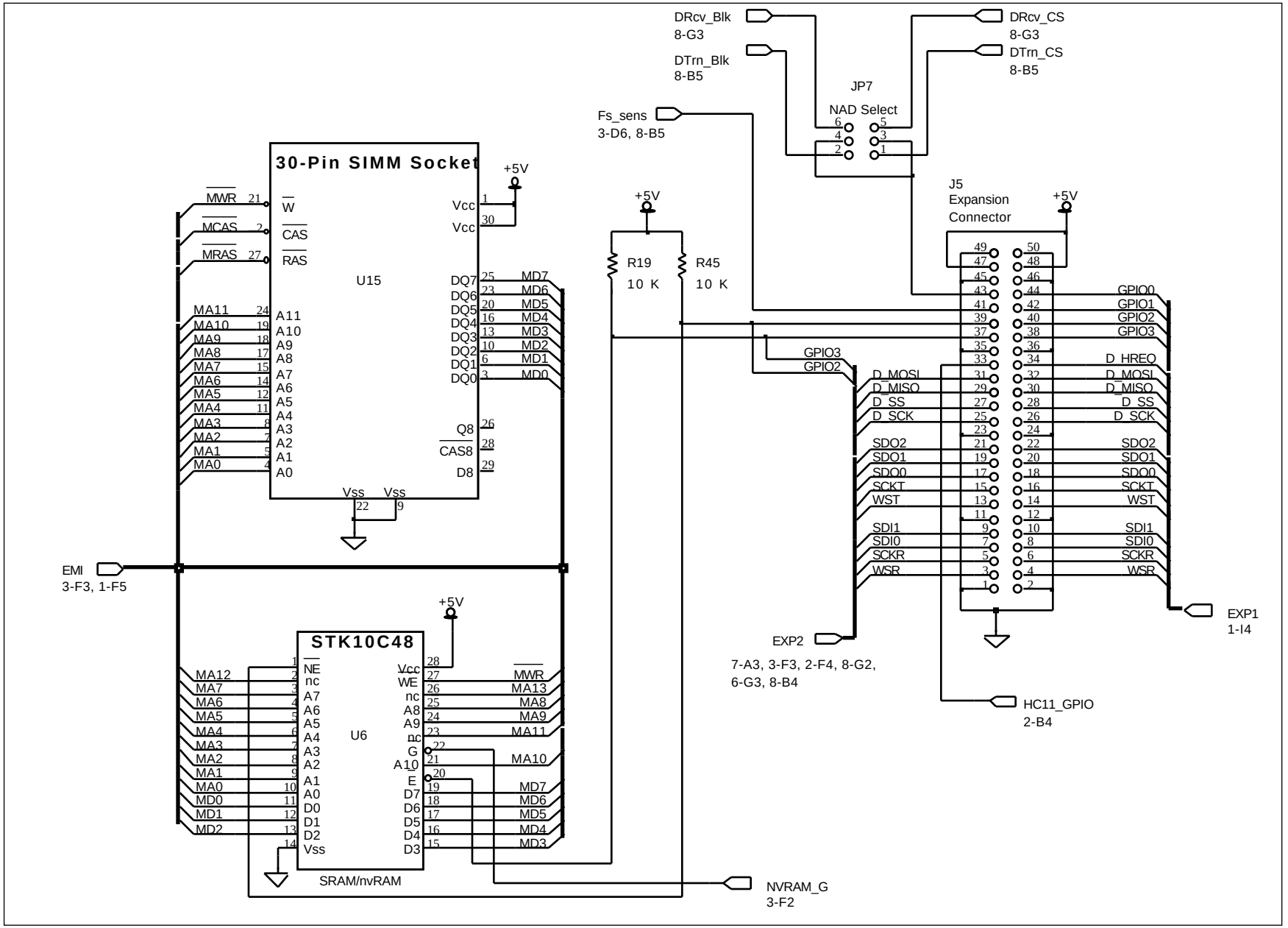


Figure 7-5 Memory and Expansion Connector

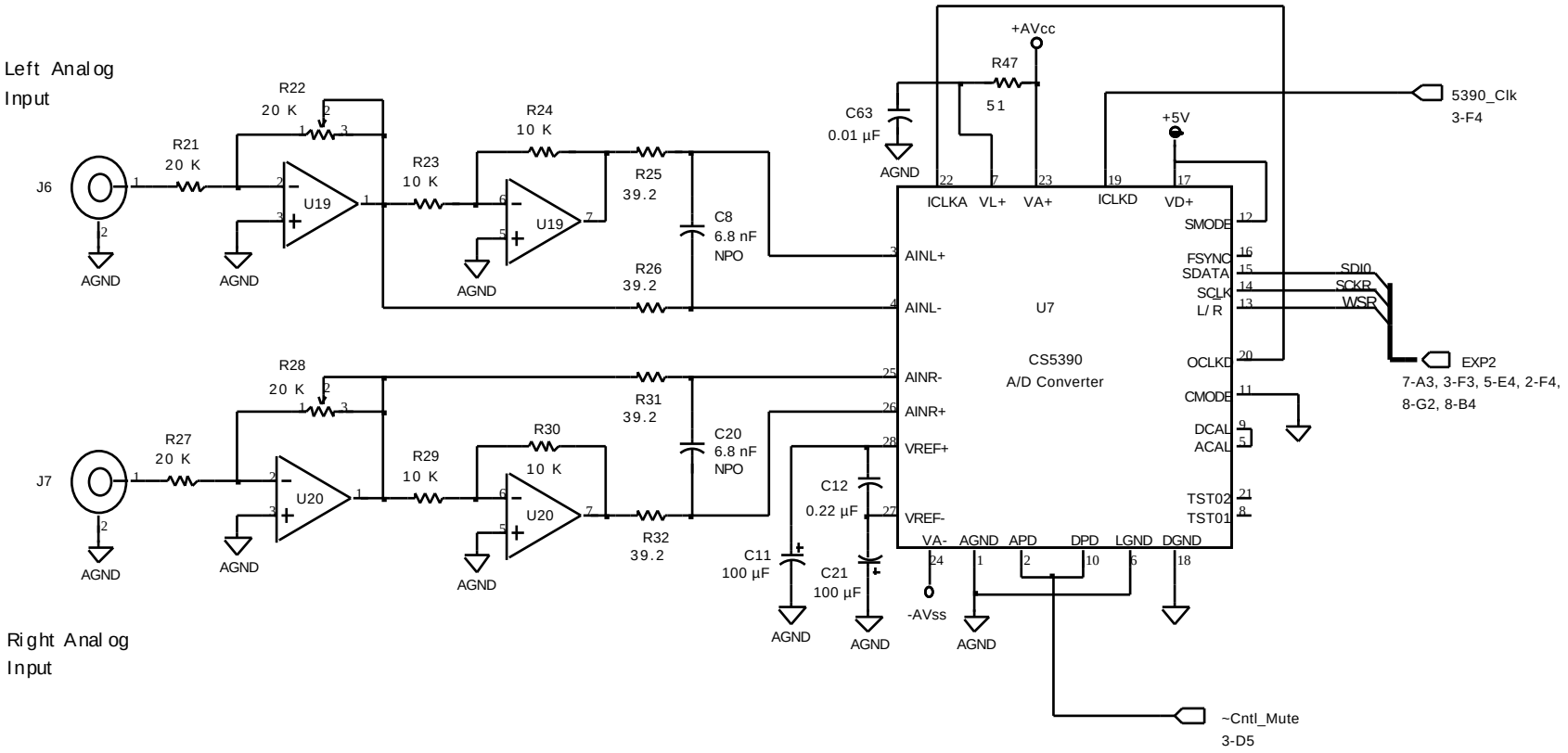


Figure 7-6 Analog-to-Digital Converter

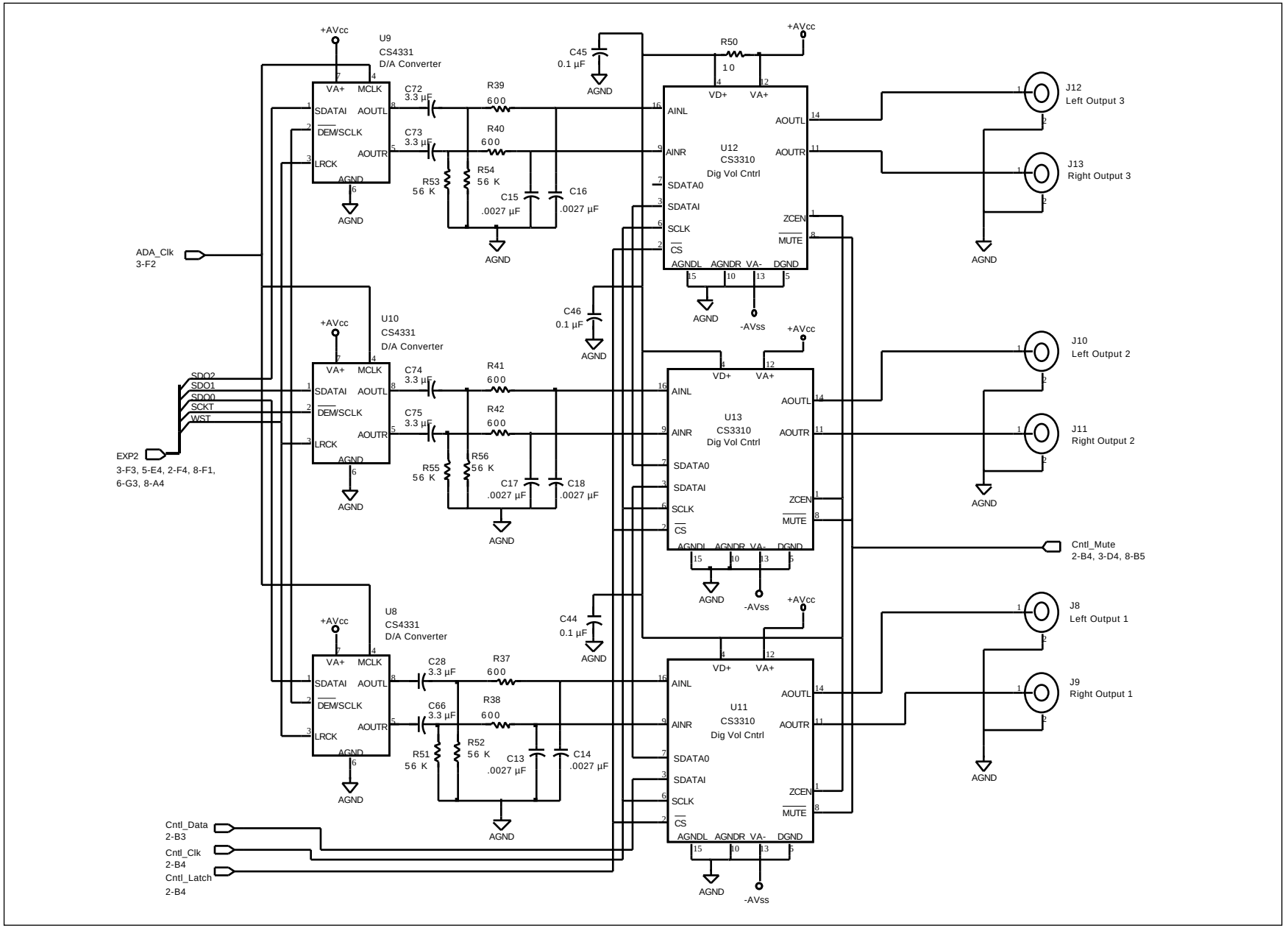


Figure 7-7 Digital-to-Analog Converter

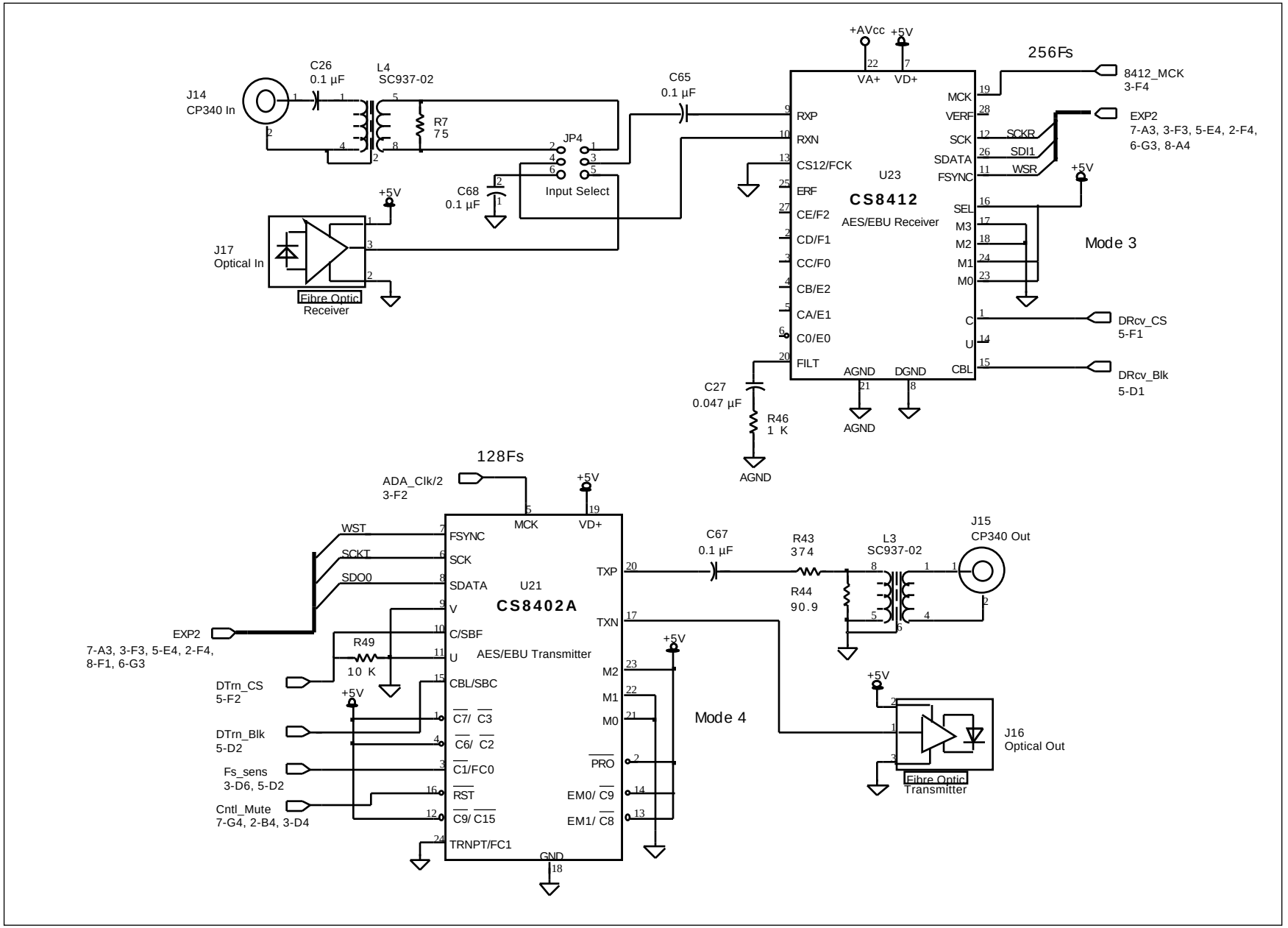


Figure 7-8 SPDIF I/O

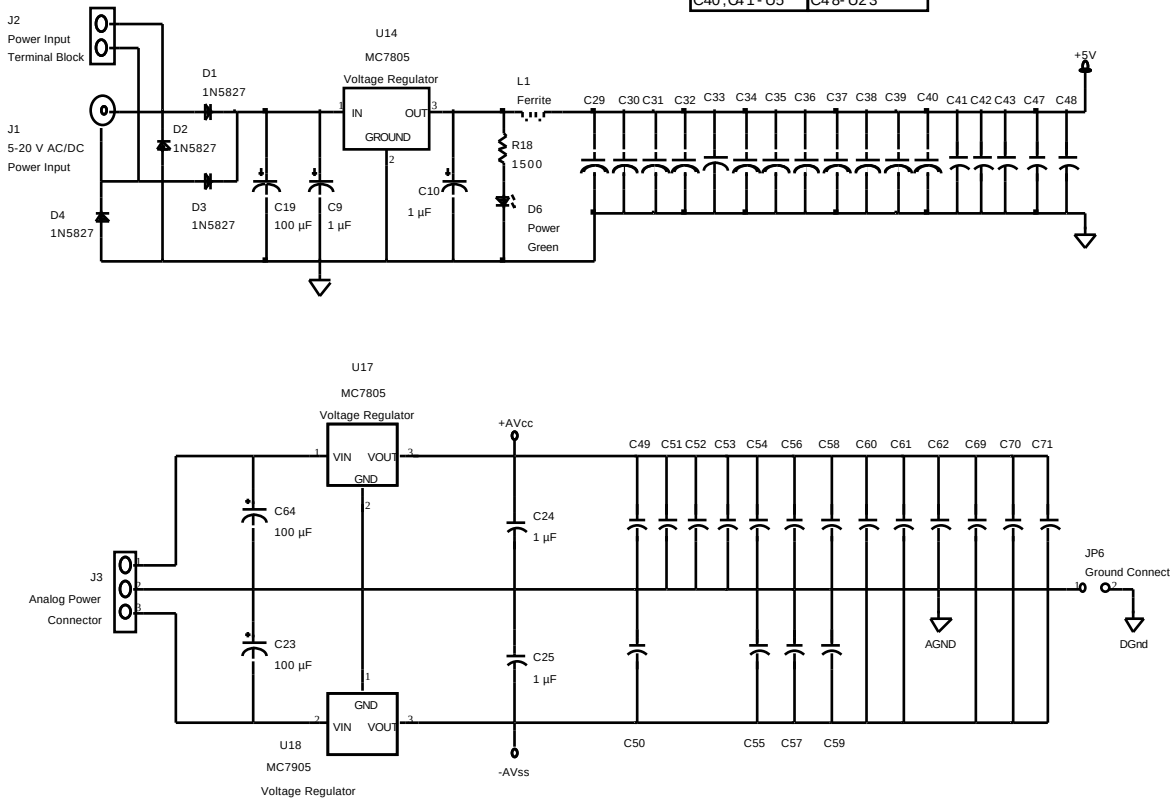


Figure 7-9 Power Supply

SECTION 8

EVALUATION MODULE PARTS LIST

8.1 PARTS LISTING

The following four pages contain, in table form, information on the parts and devices on the Evaluation Module. Contact information for suppliers of key devices, as indicated by footnote, is also included at the end of the table.

Table 8-1 DSP56007EVM Parts List

Part Designator	Manufacturer	Part Number	Description
U1	Motorola	DSP56007	DSP
U2	Motorola	MC68HC711E9	Microcontroller
U24	Motorola	MC68HC705K1	Microcontroller (OnCE)
U7	Crystal [a]	CS5390-KS	ADC
U8 U9 U10	Crystal [a]	CS4331-KS	DAC
U21	Crystal [a]	CS8402-CS	AES/EBU Transmitter
U23	Crystal [a]	CS8412-CS	AES/EBU Receiver
U11 U12 U13	Crystal [a]	CS3310-KS	Digital Volume Controller
L3 L4	Scientific Conversion [b]	SC937-02	Audio Isolation Transformer
U6	Simtek [c]	STK1068-S45	SRAM/nVRAM
U16	Hitachi	LM052L	LCD Module
U14 U17	Motorola	MC7805	Voltage Regulator
U18	Motorola	MC7905	Voltage Regulator
U19 U20	Motorola	MC33078	Op-Amp
U5	Altera	EPM7032TC44-12	PLD
D1 D2 D3 D4 D7	Rectron	FM4001	Rectifier, SMD
U4	Maxim	MAX232CSE	RS232 Transceiver
C4 C5 C6 C7 C9 C10 C22 C24 C25	Murata	GRM42-6Y5V105Z16BL	1.0µF capacitor
C28 C66 C72 C73 C74 C75	TDK	CC1206CY5V335ZTR	3.3 µF capacitor
C1 C63	Murata	GRM42-6XR103K050BD	0.01µF capacitor
C8 C20	Venkel	C1210C0G500-682JNE	6.8nF capacitor
C11 C19 C21 C23 C64	Future	SME25T101M6X16LL	100µF Aluminum Electro-lytic capacitor

Table 8-1 DSP56007EVM Parts List (Continued)

Part Designator	Manufacturer	Part Number	Description
C2 C3	Murata	GRM42-6C0G470J050BD	47pF capacitor
C26 C29 C30 C31 C33 C34 C35 C36 C37 C38 C39 C40 C41 C42 C43 C44 C45 C46 C47 C48 C49 C50 C51 C52 C53 C54 C55 C56 C57 C58 C59 C60 C61 C62 C65 C67 C68 C69 C70 C71	Murata	GRM42-6X7R104K050BL	0.1µF capacitor
C27	Venkel	C1206X7R500-473KNE	0.047µF capacitor
C13 C14 C15 C16 C17 C18	Venkel	C1206X7R500-272KNE	0.0027µF capacitor
C12	Venkel	C1206X7R500-224KNE	0.22µF capacitor
R50			10Ω 1/4W resistor
R25 R26 R31 R32	Venkel	CR1206-8W-39R2FT	39.2Ω 1/4W resistor
R47	Venkel	CR1206-8W-51R1FT	51Ω 1/4W resistor
R7			75Ω 1/4W resistor
R44	Venkel	CR1206-8W-90R9FT	90.9Ω 1/4W resistor
R43	Venkel	CR1206-8W-3740FT	374Ω 1/4W resistor
R37 R38 R39 R40 R41 R42	Future	NRC12F604OTR	604Ω 1/4W resistor
R46	Future	CRCW1206-102JRT1	1.0KΩ 1/4W resistor
R16 R18	Newark	44F6300-1.5K	1.5KΩ 1/4W resistor
R1 R2 R3 R4 R5 R6 R8 R9 R10 R11 R12 R13 R14 R15 R17 R19 R23 R24 R29 R30 R45 R48 R49 R57	Future	CR32-1002F-T	10KΩ 1/4W resistor
R21 R27			20kΩ 1/4W resistors
R51 R52 R53 R54 R55 R56			56KΩ 1/4W resistors

Table 8-1 DSP56007EVM Parts List (Continued)

Part Designator	Manufacturer	Part Number	Description
R20 R22 R28	Digikey	D4AA24-ND	20KΩ 1/4W trimpot thru-hole
Y1	MMD	MB100HA-11.2896MHz	11.2896MHz Clock Oscillator
Y2	MMD	MB100HA-12.288MHz	12.288MHz Clock Oscillator
Y3	Ecliptek	EC2-040-4.000MHz-I	4.0MHz Crystal
JP2 JP6 JP8			2-pin single row header
J19			4-pin single row header
JP1 JP5			4-pin double row header
JP3 JP4 JP7			6-pin double row header
J18			10-pin double row header
on PC board for U16			14-pin single row female header
on PC board for U16			14-pin single row male header
J5			50-pin double row male header
on PC board for U15			SIMM socket
J17	Sharp	GP1F32R	Optical Connector-Receive
J16	Sharp	GP1F32T	Optical Connector-Transmit
J1	Mouser	16PJ031	2.1mm DIN power connector
J4	Mouser	152-3409	PC mount DB9 female connector
J7 J9 J11 J13 J6 J8 J10 J13 J14 J15	Mouser	161-4215	RCA Jack
on PC board for U2	McKensie	PLCC-52P-T	52-pin PLCC socket
J2			2-position terminal block
J3			3-position terminal block
S1 S2 S3 S4 S5			6mm pushbutton switch

Table 8-1 DSP56007EVM Parts List (Continued)

Part Designator	Manufacturer	Part Number	Description
D6	Future	HLMP1790	Green LED 2mA, 1.8V
D5	Future	HLMP1700	Red LED 2mA, 1.8V
U22	Sharp	GP1U56Y	Infrared receiver
L1	Future	BL01RN1-A62	Ferrite
on PC board for U14			TO-220 0.5” compact heat sink

a.Crystal Semiconductor Corporation, P.O. Box 17847, Austin, TX 78760, (512) 445-7222 Fax:
b.Scientific Conversion, Inc., 42 Truman Drive, Novato, CA 94947,(415) 892-2323, Fax: (415
c.Simtek Corporation, 1465 Kelly Johnson Blvd., Colorado Springs, CO 80920, (800) 637-1667,
9481

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