

DSP56302

Advance Information 24-BIT DIGITAL SIGNAL PROCESSOR

The DSP56302 is a member of the DSP56300 core family of programmable CMOS Digital Signal Processors (DSPs). This family uses a high performance, single clock cycle per instruction engine providing a twofold performance increase over Motorola's popular DSP56000 core family, while retaining code compatibility. Significant architectural enhancements to the DSP56300 core family include a barrel shifter, 24 bit addressing, instruction cache, and DMA. The DSP56302 offers 66 MIPS using an internal 66 MHz clock at 3.0–3.6 volts. The DSP56300 core family offers a new level of performance in speed and power provided by its rich instruction set and low power dissipation, enabling a new generation of wireless, telecommunications, and multimedia products.

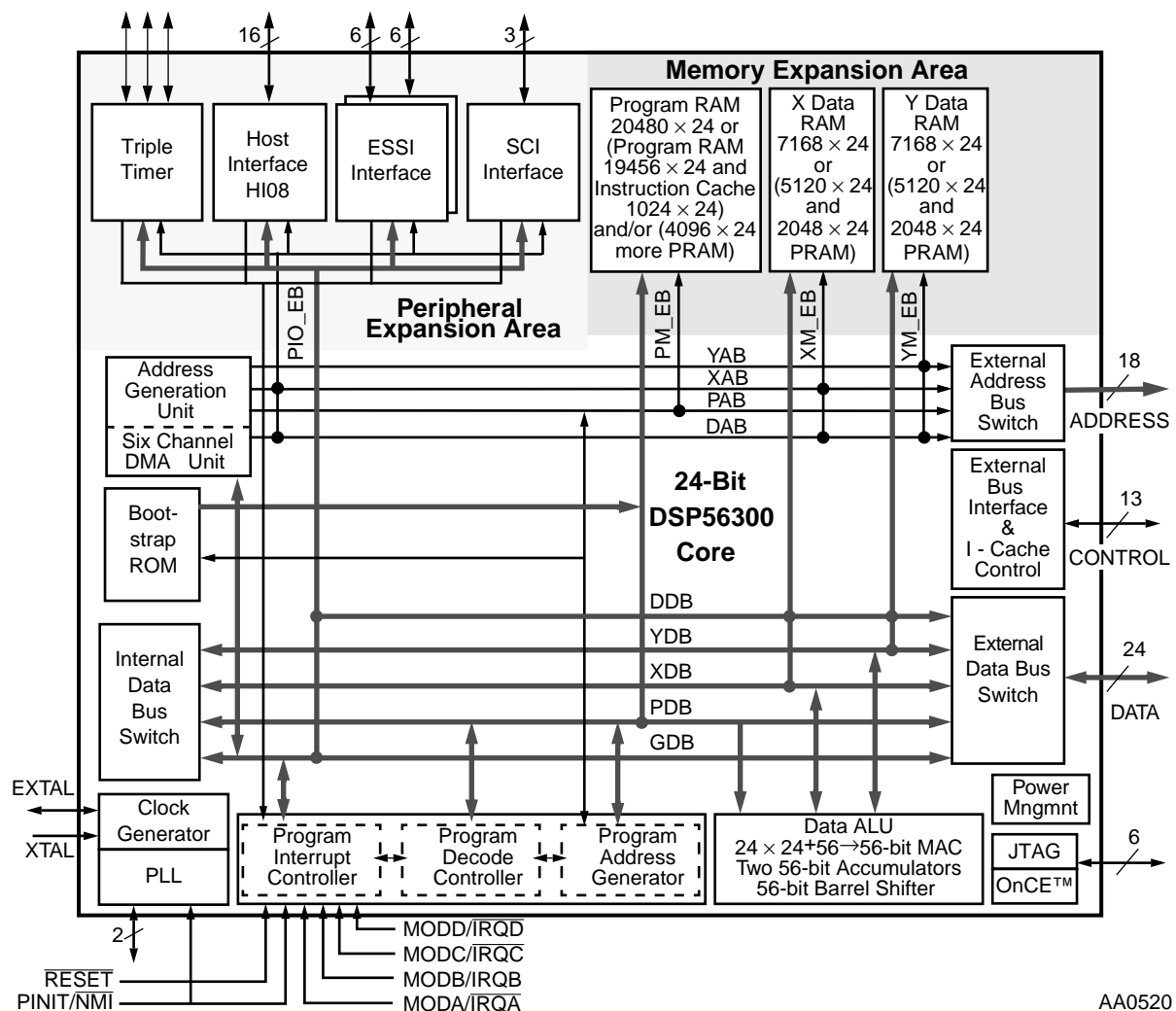


Figure 1 DSP56302 Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

DSP56302 FEATURES

- High performance DSP56300 core
 - 66 Million Instructions Per Second (MIPS) with a 66 MHz clock
 - Object code compatible with the DSP56000 core
 - Highly parallel instruction set
 - Fully pipelined 24 x 24-bit parallel multiplier-accumulator
 - 56-bit parallel barrel shifter
 - 24-bit or 16-bit arithmetic support under software control
 - Position independent code support
 - Addressing modes optimized for DSP applications
 - On-chip instruction cache controller
 - On-chip memory-expandable hardware stack
 - Nested hardware DO loops
 - Fast auto-return interrupts
 - On-chip concurrent six-channel DMA controller
 - On-chip Phase Lock Loop (PLL) and clock generator
 - On-Chip Emulation (OnCE™) module
 - JTAG Test Access Port (TAP)
 - Address tracing mode reflects internal accesses at the external port
- On-chip memories
 - Program RAM, Instruction Cache, X data RAM, and Y data RAM size is programmable:

Instruction Cache	Switch Mode	Program RAM Size	Instruction Cache Size	X Data RAM Size	Y Data Ram Size
disabled	disabled	20480 × 24-bit	0	7168 × 24-bit	7168 × 24-bit
enabled	disabled	19456 × 24-bit	1024 × 24-bit	7168 × 24-bit	7168 × 24-bit
disabled	enabled	25576 × 24-bit	0	5120 × 24-bit	5120 × 24-bit
enabled	enabled	24552 × 24-bit	1024 × 24-bit	5120 × 24-bit	5120 × 24-bit

- 192 × 24-bit bootstrap ROM

- Off-chip memory expansion
 - Data memory expansion to two 256 K x 24-bit word memory spaces
 - Program memory expansion to one 256 K x 24-bit word memory space
 - External memory expansion port
 - Chip select logic requires no additional circuitry to interface to SRAMs and SSRAMs
 - On-chip DRAM controller requires no additional circuitry to interface to DRAMs
- On-chip peripherals
 - 8-bit parallel Host Interface (HI08), ISA-compatible bus interface, providing a cost-effective solution for applications not requiring the PCI bus
 - Two Enhanced Synchronous Serial Interfaces (ESSI)
 - Serial Communications Interface (SCI) with baud rate generator
 - Triple timer module
 - Up to thirty-four programmable General Purpose I/O pins (GPIO), depending on which peripherals are enabled
- Reduced power dissipation
 - Very low power CMOS design
 - Wait and Stop low power standby modes
 - Fully-static logic, operation frequency down to DC
 - Optimized power management circuitry

TARGET APPLICATIONS

The DSP56302 is intended for applications requiring a large amount of on-chip memory, such as wireless infrastructure applications. It is also intended as a RAM-based emulation part for low-cost ROM-based solutions.

PRODUCT DOCUMENTATION

The three manuals listed in **Table 1** are required for a complete description of the DSP56302 and are necessary to design with the part properly. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or the Motorola DSP home page on the Internet, which will have the latest information (see its address below).

Table 1 DSP56302 Documentation

Document Name	Contents	Order Number
DSP56300 Family Manual	Detailed description of the DSP56300 family architecture and the 24-bit core processor and instruction set	DSP56300FM/AD
DSP56302 User's Manual	Detailed description of DSP56302 memory, peripherals, and interfaces	DSP56302UM/AD
DSP56302 Technical Data	DSP56302 pin and package descriptions, and electrical and timing specifications	DSP56302/D

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