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DSP56305ADSP/D

DSP56305ADS

Advance Information

DSP56305 Applications Development System

The DSP56305 Applications Development System (ADS) is designed as a full-featured platform for developing real-time software and hardware products to support a new generation of applications in digital telecommunications such as Global System for Mobile (GSM) communications. The DSP56305 combines three dedicated on-chip hardware co-processors (filter, Viterbi, and cyclic code) with a DSP56300 core to perform all the complex signal processing required by a single Radio Frequency (RF) carrier in one chip. The DSP56305 also includes an on-chip PLL, a Data ALU, an instruction cache, on-chip debugging modules, on-chip program and data memory, six DMA channels, and an external memory expansion port. In addition, the DSP56305 provides two types of serial ports, a PCI/Universal bus 32-bit Host Interface, and timers. The versatile DSP56305ADS provides access to all these features and interfaces of the DSP56305 chip, making it ideal for developing and implementing the algorithms required for GSM implementations, such as channel equalization, channel coding, and speech coding. The DSP56305ADS is available for IBM-PC-compatible hosts, and includes a host interface card for ISA interfaces. The DSP56305ADS can also be operated as a stand-alone card or installed in a PCI slot. The Motorola Development Tools software package is included. **Figure 1** shows the functional block diagram for the DSP56305ADS.

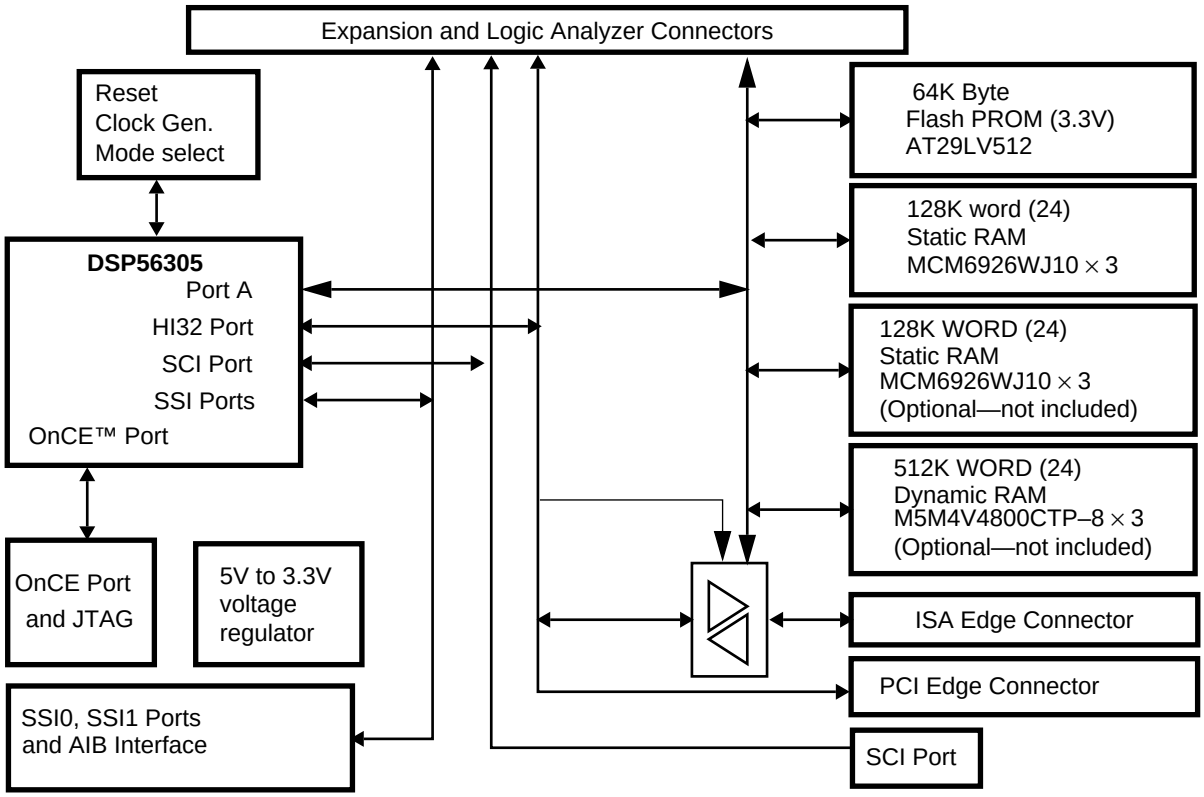

Figure 1 DSP56305ADS Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

DSP56305 FEATURES

- High performance DSP56300 core
  - 80 Million Instructions Per Second (MIPS) with an 80 MHz clock at 3.3 v
  - Highly parallel instruction set
  - Fully pipelined 24 x 24-bit parallel Multiplier-Accumulator (MAC)
  - 56-bit parallel barrel shifter
  - 24-bit or 16-bit arithmetic support under software control
  - On-chip concurrent six-channel Direct Memory Access (DMA) controller
  - Pin-compatible in 252-pin PBGA package with the DSP56301
- On-chip memory
  - Programmable partitions for on-chip X data RAM, Y data RAM, program RAM, and instruction cache
  - 6144 × 24-bit program ROM
  - 3072 × 24-bit Y data ROM
  - 192 × 24-bit bootstrap ROM
- Off-chip memory expansion
  - Data memory expansion to two 16 M x 24-bit word memory spaces
  - Program memory expansion to one 16 M x 24-bit word memory space
  - On-chip DRAM controller provides glueless interface to DRAMs
- On-chip peripherals
  - 32-bit PCI Rev. 2.1-compliant interface and ISA interface
  - Two Enhanced Synchronous Serial Interfaces (ESSI)
  - Serial Communications Interface (SCI) with baud rate generator
  - Triple timer module
  - As many as 42 programmable General Purpose Input/Output pins (GPIO)
- On-chip co-processors
  - Filter Co-Processor (FCOP) implements a wide variety of convolution and correlation filtering algorithms.
  - Viterbi Co-Processor (VCOP) implements Maximum Likelihood Sequential Estimation (MLSE) algorithm for channel decoding and equalization (uplink) and channel convolution coding (downlink).
  - Cyclic-code Co-Processor (CCOP) executes cyclic code calculations for data ciphering and deciphering, as well as parity code generation and check.

DSP56305ADS FEATURES

The DSP56305ADS kit contains the following components:

- DSP56305 Application Development Module (ADM) board
  - DSP56305 processor running at 80 MHz on board (socketed BGA package)
  - 128K fast static memory, with one wait state access at 80 MHz (3.3 v)
  - Option to add 128K fast static memory and 512K dynamic memory
  - ISA/EISA bus-compatible edge connector (for slave-only operation)
  - PCI bus-compatible edge connector (for master or slave operation)
  - All DSP signal lines accessible through on- board connectors
  - Integrated expansion and logic-analyzer connectors
  - Two dedicated SSI port connectors
  - Dedicated SCI port connector
  - JTAG/OnCE port connector
  - User-replaceable oscillator clock chip for custom clocking requirements
- Command Converter card
- ISA bus interface card
- Power supply and data connecting cables
- Motorola Development Tools software including the CLAS package
  - Graphical User Interface (GUI) simplifies code development
  - Compiler, Linker, and Assembler provide optimized code
- Supporting chip, software, and ADS documentation on CD-ROM

SYSTEM REQUIREMENTS

Users of the DSP56305ADS need to provide the following:

- IBM-PC-compatible computer (486 class or higher) running Windows 3.1 and DOS 6.0 (or higher), or Windows 95, open ISA slot, at least 8 Mbytes RAM, 3-1/2 inch diskette drive, CD-ROM drive, hard drive with at least 4 Mbytes of free disk space, and a mouse

Or

- HP 7xx workstation running HP-UX version 9.*x* with at least 32 Mbytes RAM, CD-ROM drive, and a hard drive with at least 40 Mbytes of free disk space

ORDERING INFORMATION

Table 1 provides the ordering information for the DSP56305ADS.

Table 1 DSP56305ADS Ordering Information

Description	Order Number
DSP56305ADS with ISA Host Interface adapter card for use with IBM-PC-compatible systems	DSP56305ADSA

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