DSP56002

24-BIT DIGITAL SIGNAL PROCESSOR

The DSP56002 is a MPU-style general purpose Digital Signal Processor (DSP) composed of an efficient 24-bit DSP core, program and data memories, various peripherals, and support circuitry. The DSP56000 core is fed by on-chip Program RAM, and two independent data RAMs. The DSP56002 contains a Serial Communication Interface (SCI), Synchronous Serial Interface (SSI), parallel Host Interface (HI), Timer / Event Counter, Phase Lock Loop (PLL), and an On-Chip Emulation (OnCE™) port. This combination of features, illustrated in **Figure 1**, makes the DSP56002 a cost-effective, high-performance solution for high-precision general purpose digital signal processing.

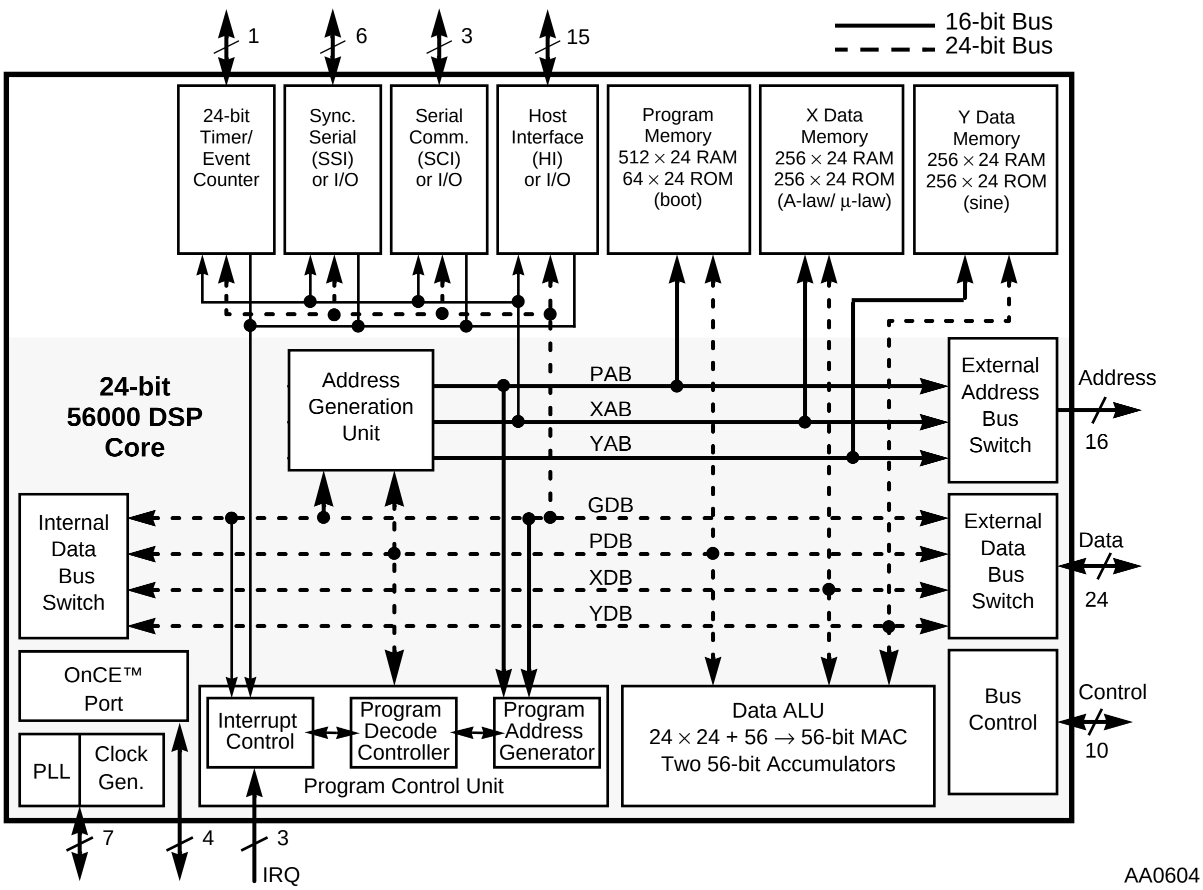

Figure 1 DSP56002 Block Diagram

MOTOROLA

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Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	Used to indicate a signal that is active when pulled low (For example, the $\overline{\text{RESET}}$ pin is active when low.)
"asserted"	Means that a high true (active high) signal is high or that a low true (active low) signal is low
"deasserted"	Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:

Signal/Symbol	Logic State	Signal State	Voltage[1]
$\overline{\text{PIN}}$	True	Asserted	V_{IL} / V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH} / V_{OH}
PIN	True	Asserted	V_{IH} / V_{OH}
PIN	False	Deasserted	V_{IL} / V_{OL}

Note: Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

FEATURES

Digital Signal Processing Core

- Efficient 24-bit DSP56000 core
- Up to 40 Million Instructions Per Second (MIPS), 25 ns instruction cycle at 80 MHz; up to 33 MIPS, 30.3 ns instruction cycle at 66 MHz
- Up to 240 Million Operations Per Second (MOPS) at 80 MHz; up to 198 MOPS at 66 MHz
- Performs a 1024-point complex Fast Fourier Transform (FFT) in 59,898 clocks
- Highly parallel instruction set with unique DSP addressing modes
- Two 56-bit accumulators including extension bits
- Parallel 24×24-bit multiply-accumulate in 1 instruction cycle (2 clock cycles)
- Double precision 48×48-bit multiply with 96-bit result in 6 instruction cycles
- 56-bit addition / subtraction in 1 instruction cycle
- Fractional and integer arithmetic with support for multiprecision arithmetic
- Hardware support for block-floating point FFT
- Hardware nested DO loops
- Zero-overhead fast interrupts (2 instruction cycles)
- Four 24-bit internal data buses and three 16-bit internal address buses for maximum information transfer on-chip

Memory

- On-chip Harvard architecture permitting simultaneous accesses to program and two data memories
- 512×24-bit on-chip Program RAM and 64×24-bit bootstrap ROM
- Two 256×24-bit on-chip data RAMs
- Two 256×24-bit on-chip data ROMs containing sine, A-law, and μ-law tables
- External memory expansion with 16-bit address and 24-bit data buses
- Bootstrap loading from external data bus, Host Interface, or Serial Communications Interface

Peripheral and Support Circuits

- Byte-wide host interface (HI) with Direct Memory Access (DMA) support (or fifteen Port B GPIO lines)
- SSI support:
  - Supports serial devices with one or more industry-standard codecs, other DSPs, microprocessors, and Motorola-SPI-compliant peripherals
  - Asynchronous or synchronous transmit and receive sections with separate or shared internal/external clocks and frame syncs
  - Network mode using frame sync and up to 32 software-selectable time slots
  - 8-bit, 12-bit, 16-bit, and 24-bit data word lengths
- SCI for full duplex asynchronous communications (or three additional Port C GPIO lines)
- One 24-bit timer/event counter (or one additional GPIO line)
- Double-buffered peripherals
- Up to twenty-five General Purpose Input/Output (GPIO) pins
- One non-maskable and two maskable external interrupt/mode control pins
- On-Chip Emulation (OnCE™) port for unobtrusive, processor speed-independent debugging
- Software-programmable, Phase Lock Loop-based (PLL) frequency synthesizer for the DSP core clock with a wide input frequency range (12.2 KHz to 80 MHz)

Miscellaneous Features

- Power-saving Wait and Stop modes
- Fully static, HCMOS design for specified operating frequency down to dc
- Three packages available:
  - 132-pin Plastic Quad Flat Pack (PQFP); 1.1 × 1.1 × 0.19 inches
  - 144-pin Thin Quad Flat Pack (TQFP); 20 × 20 × 1.5 mm
  - 132-pin Ceramic Pin Grid Array (PGA); 1.36 × 1.35 × 0.125 inches

PRODUCT DOCUMENTATION

The three documents listed in the following table are required for a complete description of the DSP56002 and are necessary to design properly with the part. Documentation is available from one of the following locations (see back cover for detailed information):

- A local Motorola distributor
- A Motorola semiconductor sales office
- A Motorola Literature Distribution Center
- The World Wide Web (WWW)

Table 1 DSP56002 Documentation

Name	Description	Order Number
DSP56000 Family Manual	Detailed description of the DSP56000 family processor core and instruction set	DSP56KFAMUM/AD
DSP56002 User's Manual	Detailed functional description of the DSP56002 memory configuration, operation, and register programming	DSP56002UM/AD
DSP56002 Technical Data	DSP56002 features list and physical, electrical, timing, and package specifications	DSP56002/D

SECTION 1

SIGNAL/PIN DESCRIPTIONS

INTRODUCTION

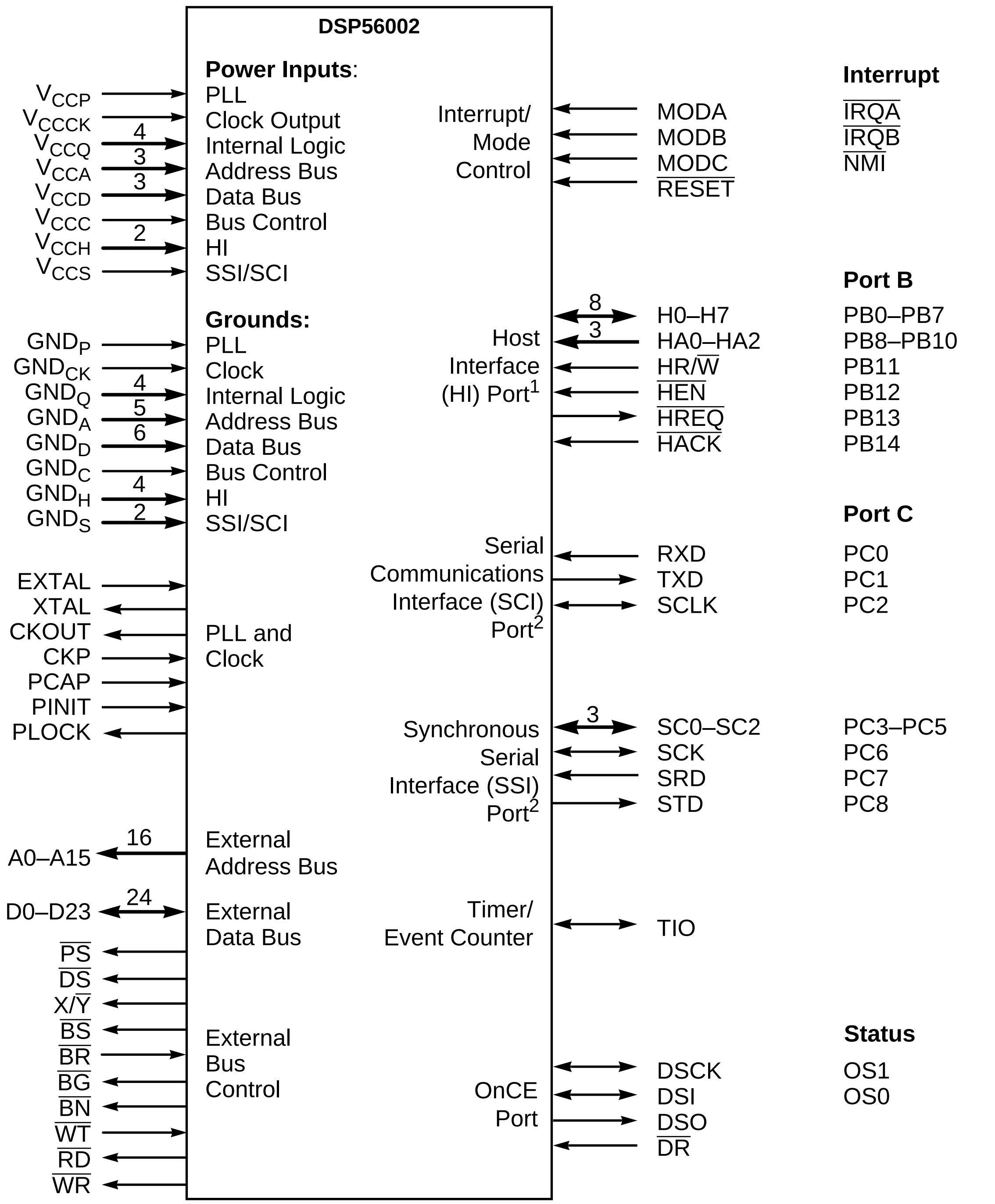
DSP56002 signals are organized into twelve functional groups, as summarized in **Table 1-1**.

Table 1-1 Signal Functional Group Allocations

Functional Group		**Number of Signals**	**Detailed Description**
Power (V_{CCX})		16	**Table 1-2**
Ground (GND_X)		24	**Table 1-3**
PLL and Clock		7	**Table 1-4**
Address Bus	Port A[1]	16	**Table 1-5**
Data Bus	Port A[1]	24	**Table 1-6**
Bus Control	Port A[1]	10	**Table 1-7**
Interrupt and Mode Control		4	**Table 1-8**
Host Interface (HI) Port	Port B[2]	15	**Table 1-9**
Serial Communications Interface (SCI) Port	Port C[3]	3	**Table 1-10**
Synchronous Serial Interface (SSI) Port	Port C[3]	6	**Table 1-11**
Timer / Event Counter or General Purpose Input / Output (GPIO)		1	**Table 1-12**
On-Chip Emulation (OnCE) Port		4	**Table 1-13**

Note:
1. Port A signals define the External Memory Interface port.
2. Port B signals are the HI signals multiplexed on the external pins with the GPIO signals.
3. Port C signals are the SCI and SSI signals multiplexed on the external pins with the GPIO signals.

Figure 1-1 is a diagram of DSP56002 signals by functional group.



Note:
1. The Host Interface port signals are multiplexed with the Port B GPIO signals (PB0–PB15).
2. The SCI and SSI signals are multiplexed with the Port C GPIO signals (PC0–PC8).
3. Power and Ground lines are indicated for the 144-pin TQFP package.

AA1081G

Figure 1-1 Signals Identified by Functional Group

POWER

Table 1-2 Power

Power Names	Description
V_{CCP}	**Analog PLL Circuit Power**—This line is dedicated to the analog PLL circuits and must remain noise-free to ensure stable PLL frequency and performance. Ensure that the input voltage to this line is well-regulated and uses an extremely low impedance path to tie to the V_{CC} power rail. Use a 0.1 μF capacitor and a 0.01 μF capacitor located as close as possible to the chip package to connect between the V_{CCP} line and the GND_P line.
V_{CCCK}	**Clock Output Power**—This line supplies a quiet power source for the CKOUT output. Ensure that the input voltage to this line is well-regulated and uses an extremely low impedance path to tie to the V_{CC} power rail. Use a 0.1 μF bypass capacitor located as close as possible to the chip package to connect between the V_{CCCK} line and the GND_{CK} line.
V_{CCQ} (4)	**Oscillator Power**—These lines supply a quiet power source to the oscillator circuits and the mode control and interrupt lines. Ensure that the input voltage to this line is well-regulated and uses an extremely low impedance path to tie to the V_{CC} power rail. Use a 0.1 μF bypass capacitor located as close as possible to the chip package to connect between the V_{CCQ} lines and the GND_Q lines.
V_{CCA} (3)	**Address Bus Power**—These lines supply power to the address bus.
V_{CCD} (3)	**Data Bus Power**—These lines supply power to the data bus.
V_{CCC}	**Bus Control Power**—This line supplies power to the bus control logic.
V_{CCH} (2)	**Host Interface Power**—These lines supply power to the Host Interface logic.
V_{CCS}	**Serial Interface Power**—This line supplies power to the serial interface logic (SCI and SSI).

GROUND

Table 1-3 Ground

Ground Names	Description
GND_P	**Analog PLL Circuit Ground**—This line supplies a dedicated quiet ground connection for the analog PLL circuits and must remain relatively noise-free to ensure stable PLL frequency and performance. Ensure that this line connects through an extremely low impedance path to ground. Use a 0.1 µF capacitor and a 0.01 µF capacitor located as close as possible to the chip package to connect between the V_{CCP} line and the GND_P line.
GND_{CK}	**Clock Output Ground**—This line supplies a quiet ground connection for the CKOUT output. Ensure that this line connects through an extremely low impedance path to ground. Use a 0.1 µF bypass capacitor located as close as possible to the chip package to connect between the V_{CCCK} line and the GND_{CK} line.
GND_Q (4)	**Oscillator Ground**—These lines supply a quiet ground connection for the oscillator circuits and the mode control and interrupt lines. Ensure that this line connects through an extremely low impedance path to ground. Use a 0.1 µF bypass capacitor located as close as possible to the chip package to connect between the V_{CCQ} line and the GND_Q line.
GND_A (5)	**Address Bus Ground**—These lines connect system ground to the address bus.
GND_D (6)	**Data Bus Ground**—These lines connect system ground to the data bus.
GND_C	**Bus Control Ground**—This line connects ground to the bus control logic.
GND_H (4)	**Host Interface Ground**—These lines supply ground connections for the Host Interface logic.
GND_S (2)	**Serial Interface Ground**—These lines supply ground connections for the serial interface logic (SCI and SSI).

PLL AND CLOCK

Table 1-4 PLL and Clock Signals

Signal Name	Signal Type	State during Reset	Signal Description
EXTAL	Input	Input	**External Clock/Crystal Input**—This input connects the internal oscillator input to an external crystal or to an external oscillator.
XTAL	Output	Chip-driven	**Crystal Output**—This output connects the internal crystal oscillator output to an external crystal. If an external oscillator is used, XTAL should be left unconnected.
CKOUT	Output	Chip-driven	**PLL Output Clock**—When the PLL is enabled and locked, this signal provides a 50% duty cycle output clock signal synchronized to the internal processor clock. When the PLL is enabled and the Multiplication Factor is less than or equal to 4, then CKOUT is synchronized to EXTAL. When the PLL is disabled, the output clock at CKOUT is derived from, and has the same frequency and duty cycle as, EXTAL. Note: For information about using the PLL Multiplication Factor, see the *DSP56002 User's Manual*.
CKP	Input	Input	**PLL Output Clock Polarity Control**—The value of this signal at reset defines the polarity of the CKOUT output relative to EXTAL. If CKP is pulled low by connecting through a resistor to ground, CKOUT and EXTAL have the same polarity. Pulling CKP high by connecting it through a resistor to V_{CC} causes CKOUT and EXTAL to be inverse polarities. The polarity of CKOUT is latched at the end of reset; therefore, any changes to CKP after deassertion of $\overline{\text{RESET}}$ do not affect CKOUT polarity.
PCAP	Input/Output	Indeter-minate	**PLL Capacitor**—This signal is used to connect the required external filter capacitor to the PLL filter. Connect one end of the capacitor to PCAP and the other to V_{CCP}. The value of the capacitor is specified in **Section 2** of this data sheet.

Table 1-4 PLL and Clock Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
PINIT	Input	Input	**PLL Initialization Source**—The value of this signal at reset defines the value written into the PLL Enable (PEN) bit in the PLL control register. If PINIT is pulled high during reset, the PEN bit is written as a 1, enabling the PLL and causing the DSP internal clocks to be derived from the PLL VCO. If PINIT is pulled low during reset, the PEN bit is written as a 0, disabling the PLL and causing DSP internal clocks to be derived from the clock connected to EXTAL. PEN is written only at the deassertion of $\overline{\text{RESET}}$ and; therefore, the value of PINIT is ignored after that time.
PLOCK	Output	Indeter-minate	**Phase and Frequency Lock**—This output is generated by an internal Phase Detector circuit. This circuit drives the output high when: • the PLL is disabled (the output clock is EXTAL and is therefore in phase with itself), or • the PLL is enabled and is locked onto the proper phase (based on the CKP value) and frequency of EXTAL. The circuit drives the output low (deasserted) whenever the PLL is enabled, but has not locked onto the proper phase and frequency. Note: PLOCK is a reliable indicator of the PLL lock state only after the chip has exited the Reset state. During hardware reset, the PLOCK state is determined by PINIT and the current PLL lock condition.

ADDRESS BUS

Table 1-5 Address Bus Signals

Signal Names	Signal Type	State during Reset	Signal Description
A0–A15	Output	Tri-stated	**Address Bus**—These signals specify the address for external program and data memory accesses. If there is no external bus activity, A0–A15 remain at their previous values to reduce power consumption. A0–A15 are tri-stated when the bus grant signal is asserted.

DATA BUS

Table 1-6 Data Bus Signals

Signal Names	Signal Type	State during Reset	Signal Description
D0–D23	Input/ Output	Tri-stated	**Data Bus**—These signals provide the bidirectional data bus for external program and data memory accesses. D0–D23 are tri-stated when the $\overline{\mathrm{BG}}$ or $\overline{\mathrm{RESET}}$ signal is asserted.

BUS CONTROL

Table 1-7 Bus Control Signals

Signal Name	Signal Type	State during Reset	Signal Description
$\overline{\text{PS}}$	Output	Tri-stated	**Program Memory Select**—$\overline{\text{PS}}$ is asserted low for external program memory access. $\overline{\text{PS}}$ is tri-stated when the $\overline{\text{BG}}$ or $\overline{\text{RESET}}$ signal is asserted.
$\overline{\text{DS}}$	Output	Tri-stated	**Data Memory Select**—$\overline{\text{DS}}$ is asserted low for external data memory access. $\overline{\text{DS}}$ is tri-stated when the $\overline{\text{BG}}$ or $\overline{\text{RESET}}$ signal is asserted.
X/$\overline{\text{Y}}$	Output	Tri-stated	**X/Y External Memory Select**—This output is driven low during external Y data memory accesses. It is also driven low during external exception vector fetches when operating in the Development mode. X/$\overline{\text{Y}}$ is tri-stated when the $\overline{\text{BG}}$ or $\overline{\text{RESET}}$ signal is asserted.
$\overline{\text{BS}}$	Output	Pulled high	**Bus Select—**$\overline{\text{BS}}$ is asserted when the DSP accesses the external bus, and it acts as an early indication of imminent external bus access by the DSP56002. It may also be used with the bus wait input $\overline{\text{WT}}$ to generate wait states. $\overline{\text{BS}}$ is pulled high when the $\overline{\text{BG}}$ or $\overline{\text{RESET}}$ signal is asserted.
$\overline{\text{BR}}$	Input	Input	**Bus Request**—When the Bus Request input ($\overline{\text{BR}}$) is asserted, it allows an external device, such as another processor or DMA controller, to become the master of the external address and data buses. While the bus is released, the DSP may continue internal operations using internal memory spaces. When $\overline{\text{BR}}$ is deasserted, the DSP56002 is the bus master.When $\overline{\text{BR}}$ is asserted, the DSP56002 will release Port A, including A0–A15, D0–D23, and the bus control signals ($\overline{\text{PS}}$, $\overline{\text{DS}}$, X/$\overline{\text{Y}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, and $\overline{\text{BS}}$) by placing them in the high-impedance state after execution of the current instruction has been completed. Note: To prevent erroneous operation, pull up the $\overline{\text{BR}}$ signal when it is not in use.
$\overline{\text{BG}}$	Output	Pulled high	**Bus Grant**—When this output is asserted, it grants an external device's request for access to the external bus. This output is deasserted during hardware reset.

Table 1-7 Bus Control Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
$\overline{\text{BN}}$	Output	Pulled low	**Bus Not Required**—The $\overline{\text{BN}}$ signal is asserted whenever the chip requires mastership of the external bus. During instruction cycles where the external bus is not required, $\overline{\text{BN}}$ is deasserted. If the $\overline{\text{BN}}$ signal is asserted when the DSP is not the bus master, processing has stopped and the chip is waiting to acquire bus ownership. An external arbiter may use this signal to help determine when to return bus ownership to the DSP. Note: The $\overline{\text{BN}}$ signal cannot be used as an early indication of imminent external bus access because it is valid later than the other bus control signals $\overline{\text{BS}}$ and $\overline{\text{WT}}$.
$\overline{\text{WT}}$	Input	Input	**Bus Wait**—An external device may insert wait states by asserting $\overline{\text{WT}}$ during external bus cycles. Note: To prevent erroneous operation, pull up the $\overline{\text{WT}}$ signal when it is not in use.
$\overline{\text{WR}}$	Output	Tri-stated	**Write Enable**—$\overline{\text{WR}}$ is asserted low during external memory write cycles. $\overline{\text{WR}}$ is tri-stated when the $\overline{\text{BG}}$ or $\overline{\text{RESET}}$ signal is asserted.
$\overline{\text{RD}}$	Output	Tri-stated	**Read Enable**—$\overline{\text{RD}}$ is asserted low during external memory read cycles. $\overline{\text{RD}}$ is tri-stated when the $\overline{\text{BG}}$ or $\overline{\text{RESET}}$ signal is asserted.

INTERRUPT AND MODE CONTROL

Table 1-8 Interrupt and Mode Control Signals

Signal Name	Signal Type	State during Reset	Signal Description
MODA/$\overline{\text{IRQA}}$	Input	Input	**Mode Select A/External Interrupt Request A**—This input has two functions: 1. to select the initial chip operating mode, and 2. after synchronization, to allow an external device to request a DSP interrupt. MODA is read and internally latched in the DSP when the processor exits the Reset state. MODA, MODB, and MODC select the initial chip operating mode. Several clock cycles (depending on PLL stabilization time) after leaving the Reset state, the MODA signal changes to external interrupt request $\overline{\text{IRQA}}$. The chip operating mode can be changed by software after reset. The $\overline{\text{IRQA}}$ input is a synchronized external interrupt request that indicates that an external device is requesting service. It may be programmed to be level-sensitive or negative-edge-sensitive. If level-sensitive triggering is selected, an external pull up resistor is required for wired-OR operation. If the processor is in the Stop state and $\overline{\text{IRQA}}$ is asserted, the processor will exit the Stop state.
MODB/$\overline{\text{IRQB}}$	Input	Input	**Mode Select B/External Interrupt Request B**—This input has two functions: 1. to select the initial chip operating mode, and 2. after internal synchronization, to allow an external device to request a DSP interrupt. MODB is read and internally latched in the DSP when the processor exits the Reset state. MODA, MODB, and MODC select the initial chip operating mode. Several clock cycles (depending on PLL stabilization time) after leaving the Reset state, the MODB signal changes to external interrupt request $\overline{\text{IRQB}}$. After reset, the chip operating mode can be changed by software. The $\overline{\text{IRQB}}$ input is an external interrupt request that indicates that an external device is requesting service. It may be programmed to be level-sensitive or negative-edge-triggered. If level-sensitive triggering is selected, an external pull up resistor is required for wired-OR operation.

Table 1-8 Interrupt and Mode Control Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
MODC / $\overline{\text{NMI}}$	Input	Input	**Mode Select C/Non-maskable Interrupt Request**—This input has two functions: 1. to select the initial chip operating mode, and 2. after internal synchronization, to allow an external device to request a non-maskable DSP interrupt. MODC is read and internally latched in the DSP when the processor exits the Reset state. MODA, MODB, and MODC select the initial chip operating mode. Several clock cycles (depending on PLL stabilization time) after leaving the Reset state, the MODC signal changes to the nonmaskable external interrupt request $\overline{\text{NMI}}$. After reset, the chip operating mode can be changed by software. The $\overline{\text{NMI}}$ input is an external interrupt request that indicates that an external device is requesting service. It may be programmed to be level-sensitive or negative-edge-triggered. If level-sensitive triggering is selected, an external pull up resistor is required for wired-OR operation.
$\overline{\text{RESET}}$	Input	Input	**Reset**—This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the DSP is initialized and placed in the Reset state. A Schmitt trigger input is used for noise immunity. When the $\overline{\text{RESET}}$ signal is deasserted, the initial chip operating mode is latched from the MODA, MODB, and MODC signals. The internal reset signal is deasserted synchronous with the internal clocks. In addition, the PINIT pin is sampled and written into the PEN bit of the PLL Control Register and the CKP pin is sampled to determine the polarity of the CKOUT signal.

HOST INTERFACE (HI) PORT

Table 1-9 HI Signals

Signal Name	Signal Type	State during Reset	Signal Description
H0–H7 PB0–PB7	Input or Output	Tri-stated	**Host Data Bus (H0–H7)**—This data bus transfers data between the host processor and the DSP56002. When configured as a Host Interface port, the H0–H7signals are tri-stated as long as $\overline{\text{HEN}}$ is deasserted. The signals are inputs unless HR/$\overline{\text{W}}$ is high and $\overline{\text{HEN}}$ is asserted, in which case H0–H7 become outputs, allowing the host processor to read the DSP56002 data. H0–H7 become outputs when $\overline{\text{HACK}}$ is asserted during $\overline{\text{HREQ}}$ assertion. **Port B GPIO 0–7 (PB0–PB7)**—These signals are General Purpose I/O signals (PB0–PB7) when the Host Interface is not selected. After reset, the default state for these signals is GPIO input.
HA0–HA2 PB8–PB10	Input Input or Output	Tri-stated	**Host Address 0—Host Address 2 (HA0–HA2)**—These inputs provide the address selection for each Host Interface register. **Port B GPIO 8–10 (PB8–PB10)**—These signals are General Purpose I/O signals (PB8–PB10) when the Host Interface is not selected. After reset, the default state for these signals is GPIO input.
HR/$\overline{\text{W}}$ PB11	Input Input or Output	Tri-stated	**Host Read/Write**—This input selects the direction of data transfer for each host processor access. If HR/$\overline{\text{W}}$ is high and $\overline{\text{HEN}}$ is asserted, H0–H7 are outputs and DSP data is transferred to the host processor. If HR/$\overline{\text{W}}$ is low and $\overline{\text{HEN}}$ is asserted, H0–H7 are inputs and host data is transferred to the DSP. HR/$\overline{\text{W}}$ must be stable when $\overline{\text{HEN}}$ is asserted. **Port B GPIO 11 (PB11)**—This signal is a General Purpose I/O signal called PB11 when the Host Interface is not being used. After reset, the default state for this signal is GPIO input.

Table 1-9 HI Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
$\overline{\text{HEN}}$ PB12	Input Input or Output	Tri-stated	**Host Enable**—This input enables a data transfer on the host data bus. When $\overline{\text{HEN}}$ is asserted and HR/$\overline{\text{W}}$ is high, H0–H7 become outputs and the host processor may read DSP56002/L002 data. When $\overline{\text{HEN}}$ is asserted and HR/$\overline{\text{W}}$ is low, H0–H7 become inputs. Host data is latched inside the DSP on the rising edge of $\overline{\text{HEN}}$. Normally, a chip select signal derived from host address decoding and an enable strobe are used to generate $\overline{\text{HEN}}$. **Port B GPIO 12 (PB12)**—This signal is a General Purpose I/O signal called PB12 when the Host Interface is not being used. After reset, the default state for this signal is GPIO input.
$\overline{\text{HREQ}}$ PB13	Open drain Output Input or Output	Tri-stated	**Host Request**—This signal is used by the Host Interface to request service from the host processor, DMA controller, or a simple external controller. Note: $\overline{\text{HREQ}}$ should always be pulled high when it is not in use. **Port B GPIO 13 (PB13)**—This signal is a General Purpose (not open-drain) I/O signal (PB13) when the Host Interface is not selected. After reset, the default state for this signal is GPIO input.
$\overline{\text{HACK}}$ PB14	Input Input or Output	Tri-stated	**Host Acknowledge**—This input has two functions. It provides a host acknowledge handshake signal for DMA transfers and it receives a host interrupt acknowledge compatible with MC68000 family processors. Note: $\overline{\text{HACK}}$ should always be pulled high when it is not in use. **Port B GPIO 14 (PB14)**—This signal is a General Purpose I/O signal (PB14) when the Host Interface is not selected. After reset, the default state for this signal is GPIO input.

SERIAL COMMUNICATIONS INTERFACE PORT

Table 1-10 Serial Communications Interface (SCI+) Signals

Signal Name	Signal Type	State during Reset	Signal Description
RXD PC0	Input Input or Output	Tri-stated	**Receive Data (RXD)**—This input receives byte-oriented data and transfers the data to the SCI receive shift register. Input data can be sampled on either the positive edge or on the negative edge of the receive clock, depending on how the SCI control register is programmed. **Port C GPIO 0 (PC0)**—This signal is a GPIO signal called PC0 when the SCI RXD function is not being used. After reset, the default state is GPIO input.
TXD PC1	Output Input or Output	Tri-stated	**Transmit Data (TXD)**—This output transmits serial data from the SCI transmit shift register. In the default configuration, the data changes on the positive clock edge and is valid on the negative clock edge. The user can reverse this clock polarity by programming the SCI control register appropriately. **Port C GPIO 1 (PC1)**—This signal is a GPIO signal called PC1 when the SCI TXD function is not being used. After reset, the default state is GPIO input.
SCLK PC2	Input or Output	Tri-stated	**SCI Clock (SCLK)—**This signal provides an input or output clock from which the receive or transmit baud rate is derived in the Asynchronous mode, and from which data is transferred in the Synchronous mode. The direction and function of the signal is defined by the RCM bit in the SCI+ Clock Control Register (SCCR). **Port C GPIO 2 (PC2)**—This signal is a GPIO signal called PC2 when the SCI SCLK function is not being used. After reset, the default state is GPIO input.

SYNCHRONOUS SERIAL INTERFACE PORT

Table 1-11 Synchronous Serial Interface (SSI) Signals

Signal Name	Signal Type	State during Reset	Signal Description
SC0 PC3	Input or Output	Tri-stated	**Serial Clock 0 (SC0)—**This signal's function is determined by whether the SCLK is in Synchronous or Asynchronous mode. • In Synchronous mode, this signal is used as a serial I/O flag. • In Asynchronous mode, this signal receives clock I/O. **Port C GPIO 3 (PC3)**—This signal is a GPIO signal called PC3 when the SSI SC0 function is not being used. After reset, the default state is GPIO input.
SC1 PC4	Input or Output	Tri-stated	**Serial Clock 1 (SC1)—**The SSI uses this bidirectional signal to control flag or frame synchronization. This signal's function is determined by whether the SCLK is in Synchronous or Asynchronous mode. • In Asynchronous mode, this signal is frame sync I/O. • For Synchronous mode with continuous clock, this signal is a serial I/O flag and operates like the SC0. SC0 and SC1 are independent serial I/O flags but may be used together for multiple serial device selection. **Port C GPIO 4 (PC4)**—This signal is a GPIO signal called PC4 when the SSI SC1 function is not being used. After reset, the default state is GPIO input.
SC2 PC5	Input or Output	Tri-stated	**Serial Clock 2 (SC2)—**The SSI uses this bidirectional signal to control frame synchronization only. As with SC0 and SC1, its function is defined by the SSI operating mode. **Port C GPIO 5 (PC5)**—This signal is a GPIO signal called PC5 when the SSI SC1 function is not being used. After reset, the default state is GPIO input.

Table 1-11 Synchronous Serial Interface (SSI) Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
SCK PC6	Input or Output	Tri-stated	**SSI Serial Receive Clock**—This bidirectional signal provides the serial bit rate clock for the SSI when only one clock is being used. **Port C GPIO 6 (PC6)**—This signal is a GPIO signal called PC6 when the SSI function is not being used. After reset, the default state is GPIO input.
SRD PC7	Input Input or Output	Tri-stated	**SSI Receive Data**—This input signal receives serial data and transfers the data to the SSI Receive Shift Register. **Port C GPIO 7 (PC7)**—This signal is a GPIO signal called PC7 when the SSI SRD function is not being used. After reset, the default state is GPIO input.
STD PC8	Output Input or Output	Tri-stated	**SSI Transmit Data (STD)**—This output signal transmits serial data from the SSI Transmitter Shift Register. **Port C GPIO 8 (PC8)**—This signal is a GPIO signal called PC8 when the SSI STD function is not being used. After reset, the default state is GPIO input.

TIMERS

Table 1-12 Timer Signals

Signal Name	Signal Type	State during Reset	Signal Description
TIO	Input or Output	Tri-stated	**Timer Input/Output**—The TIO signal provides an interface to the timer / event counter module. When the module functions as an external event counter or is used to measure external pulse width / signal period, the TIO is an input. When the module functions as a timer, the TIO is an output, and the signal on the TIO signal is the timer pulse. When not used by the timer module, the TIO can be programmed through the Timer Control / Status Register (TCSR) to be a General Purpose I / O signal. TIO is effectively disconnected upon leaving reset.

On-CHIP EMULATION PORT

Table 1-13 On-Chip Emulation (OnCE) Signals

Signal Name	Signal Type	State during Reset	Signal Description
DSI / OS0	Input or Output	Low Output	**Debug Serial Input/Chip Status 0**—Serial data or commands are provided to the OnCE controller through the DSI / OS0 signal when it is an input. The data received on the DSI signal will be recognized only when the DSP has entered the Debug mode of operation. Data is latched on the falling edge of the DSCK serial clock. Data is always shifted into the OnCE serial port Most Significant Bit (MSB) first. When the DSI / OS0 signal is an output, it works in conjunction with the OS1 signal to provide chip status information. The DSI / OS0 signal is an output when the processor is not in Debug mode. When switching from output to input, the signal is tri-stated. Note: Connect an external pull-down resistor to this signal.
DSCK / OS1	Input or Output	Low Output	**Debug Serial Clock/Chip Status 1**—The DSCK / OS1 signal supplies the serial clock to the OnCE when it is an input. The serial clock provides pulses required to shift data into and out of the OnCE serial port. (Data is clocked into the OnCE on the falling edge and is clocked out of the OnCE serial port on the rising edge.) The debug serial clock frequency must be no greater than $^1/_8$ of the processor clock frequency. When switching from input to output, the signal is tri-stated. When it is an output, this signal works with the OS0 signal to provide information about the chip status. The DSCK / OS1 signal is an output when the chip is not in Debug mode. Note: Connect an external pull-down resistor to this signal.

Table 1-13 On-Chip Emulation (OnCE) Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
DSO	Output	Pulled high	**Debug Serial Output**—Data contained in one of the OnCE controller registers is provided through the DSO output signal, as specified by the last command received from the external command controller. Data is always shifted out the OnCE serial port Most Significant Bit (MSB) first. Data is clocked out of the OnCE serial port on the rising edge of DSCK. The DSO signal also provides acknowledge pulses to the external command controller. When the chip enters the Debug mode, the DSO signal will be pulsed low to indicate (acknowledge) that the OnCE is waiting for commands. After the OnCE receives a read command, the DSO signal will be pulsed low to indicate that the requested data is available and the OnCE serial port is ready to receive clocks in order to deliver the data. After the OnCE receives a write command, the DSO signal will be pulsed low to indicate that the OnCE serial port is ready to receive the data to be written; after the data is written, another acknowledge pulse will be provided. Note: Connect an external pull-up resistor to this signal.
$\overline{\mathrm{DR}}$	Input	Input	**Debug Request**—The debug request input ($\overline{\mathrm{DR}}$) allows the user to enter the Debug mode of operation from the external command controller. When $\overline{\mathrm{DR}}$ is asserted, it causes the DSP to finish the current instruction being executed, save the instruction pipeline information, enter the Debug mode, and wait for commands to be entered from the DSI line. While in Debug mode, the $\overline{\mathrm{DR}}$ signal lets the user reset the OnCE controller by asserting it and deasserting it after receiving acknowledge. It may be necessary to reset the OnCE controller in cases where synchronization between the OnCE controller and external circuitry is lost. $\overline{\mathrm{DR}}$ must be deasserted after the OnCE responds with an acknowledge on the DSO signal and before sending the first OnCE command. Asserting $\overline{\mathrm{DR}}$ will cause the chip to exit the Stop or Wait state. Having $\overline{\mathrm{DR}}$ asserted during the deassertion of $\overline{\mathrm{RESET}}$ will cause the DSP to enter Debug mode. Note: Connect an external pull-up resistor to this signal.

SECTION 2

SPECIFICATIONS

GENERAL CHARACTERISTICS

The DSP56002 is fabricated in high-density HCMOS with TTL compatible inputs and outputs.

MAXIMUM RATINGS

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

Note: In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification will never occur in the same device that has a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2-1 Absolute Maximum Ratings (GND = 0 V)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.3 to +7.0	V
All Input Voltages	V_{IN}	(GND – 0.5) to (V_{CC} + 0.5)	V
Current Drain per Pin excluding V_{CC} and GND	I	10	mA
Operating Temperature Range	T_J	–40 to +105	°C
Storage Temperature	T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Table 2-2 Thermal Characteristics

Characteristic	Symbol	PQFP Value[3]	TQFP Value[3]	TQFP Value[4]	PGA Value[3]	Unit
Junction-to-ambient thermal resistance[1]	$R_{\theta JA}$ or θ_{JA}	50	48	40.6	22	°C / W
Junction-to-case thermal resistance[2]	$R_{\theta JC}$ or θ_{JC}	12.4	10.8	—	6.5	°C / W
Thermal characterization parameter	Ψ_{JT}	4.0	0.16	—	N / A	°C / W

Notes:
1. Junction-to-ambient thermal resistance is based on measurements on a horizontal-single-sided Printed Circuit Board per SEMI G38-87 in natural convection.(SEMI is Semiconductor Equipment and Materials International, 805 East Middlefield Rd., Mountain View, CA 94043, (415) 964-5111) Measurements were made with the parts installed on thermal test boards meeting the specification EIA / JEDECSI-3.
2. Junction-to-case thermal resistance is based on measurements using a cold plate per SEMI G30-88, with the exception that the cold plate temperature is used for the case temperature.
3. These are measured values. See note 1 for test board conditions.
4. These are measured values; testing is not complete. Values were measured on a non-standard four-layer thermal test board (two internal planes) at one watt in a horizontal configuration.

DC ELECTRICAL CHARACTERISTICS

Table 2-3 DC Electrical Characteristics

Characteristics	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage •EXTAL •$\overline{\text{RESET}}$ • MODA, MODB, MODC • All other inputs	 V_{IHC} V_{IHR} V_{IHM} V_{IH}	 4.0 2.5 3.5 2.0	 — — — —	 V_{CC} V_{CC} V_{CC} V_{CC}	 V V V V
Input Low Voltage • EXTAL • MODA, MODB, MODC • All other inputs	 V_{ILC} V_{ILM} V_{IL}	 –0.5 –0.5 –0.5	 — — —	 0.6 2.0 0.8	 V V V
Input Leakage Current EXTAL, $\overline{\text{RESET}}$, MODA / $\overline{\text{IRQA}}$, MODB / $\overline{\text{IRQB}}$, MODC / $\overline{\text{NMI}}$, $\overline{\text{DR}}$, $\overline{\text{BR}}$, $\overline{\text{WT}}$, CKP, PINIT, $\overline{\text{MCBG}}$, $\overline{\text{MCBCLR}}$, MCCLK, D20IN	I_{IN}	–1	—	1	µA
Tri-state (Off–state) Input Current (@ 2.4 V / 0.4 V)	I_{TSI}	–10	—	10	µA
Output High Voltage (I_{OH} = –0.4 mA)	V_{OH}	2.4	—	—	V
Output Low Voltage (I_{OL} = 3.0 mA) $\overline{\text{HREQ}}$ I_{OL} = 6.7 mA, TXD I_{OL} = 6.7 mA	V_{OL}	—	—	0.4	V
Internal Supply Current at 40 MHz[1] • In Wait mode[2] • In Stop mode[2]	I_{CCI} I_{CCW} I_{CCS}	— — —	90 12 2	105 20 95	mA mA µA
Internal Supply Current at 66 MHz[1] • In Wait mode[2] • In Stop mode[2]	I_{CCI} I_{CCW} I_{CCS}	— — —	95 15 2	130 25 95	mA mA µA
Internal Supply Current at 80 MHz[1] • In Wait mode[2] • In Stop mode[2]	I_{CCI} I_{CCW} I_{CCS}	— — —	115 18 2	160 30 95	mA mA µA
PLL Supply Current[3] • 40 MHz • 66 MHz • 80 MHz		 — — —	 1.0 1.1 1.2	 1.5 1.5 1.8	 mA mA mA
CKOUT Supply Current[4] • 40 MHz • 66 MHz • 80 MHz		 — — —	 14 28 34	 20 35 42	 mA mA mA
Input Capacitance[5]	C_{IN}	—	10	—	pF

Notes:
1. **Section 4 Design Considerations** describes how to calculate the external supply current.
2. In order to obtain these results all inputs must be terminated (i.e., not allowed to float).
3. Values are given for PLL enabled.
4. Values are given for CKOUT enabled.
5. Periodically sampled and not 100% tested

AC ELECTRICAL CHARACTERISTICS

The timing waveforms in the AC Electrical Characteristics are tested with a V_{IL} maximum of 0.5 V and a V_{IH} minimum of 2.4 V for all pins, except EXTAL, $\overline{\text{RESET}}$, MODA, MODB, and MODC. These pins are tested using the input levels set forth in the DC Electrical Characteristics. AC timing specifications that are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition. DSP56002 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.8 V and 2.0 V, respectively.

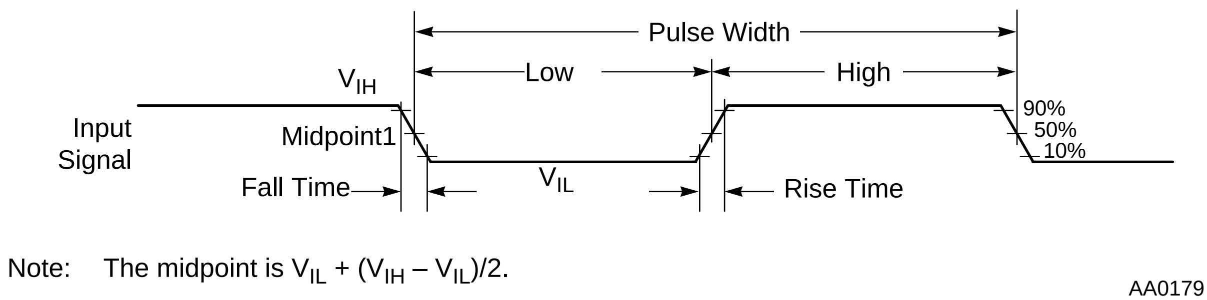


Figure 2-1 Signal Measurement Reference

INTERNAL CLOCKS

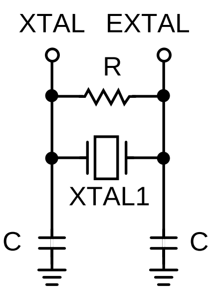
For each occurrence of T_H, T_L, T_C or I_{CYC}, substitute with the numbers in **Table 2-4**. DF and MF are PLL division and multiplication factors set in registers.

Table 2-4 Internal Clocks

Characteristics	Symbol	Expression
Internal Operation Frequency	f	
Internal Clock High Period • With PLL disabled • With PLL enabled and MF ≤ 4 • With PLL enabled and MF > 4	T_H	 ET_H (Min) $0.48 \times T_C$ (Max) $0.52 \times T_C$ (Min) $0.467 \times T_C$ (Max) $0.533 \times T_C$
Internal Clock Low Period • With PLL disabled • With PLL enabled and MF ≤ 4 • With PLL enabled and MF > 4	T_L	 ET_L (Min) $0.48 \times T_C$ (Max) $0.52 \times T_C$ (Min) $0.467 \times T_C$ (Max) $0.533 \times T_C$
Internal Clock Cycle Time	T_C	$ET_C \times DF / MF$
Instruction Cycle Time	I_{CYC}	$2 \times T_C$

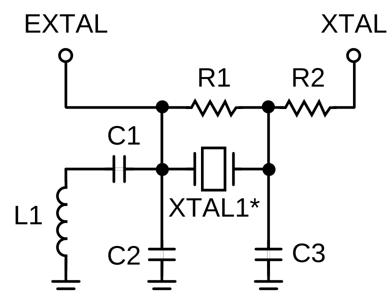
EXTERNAL CLOCK (EXTAL PIN)

The DSP56002 system clock may be derived from the on-chip crystal oscillator as shown in **Figure 2-2**, or it may be externally supplied. An externally supplied square wave voltage source should be connected to EXTAL, leaving XTAL physically unconnected to the board or socket. The rise and fall times of this external clock should be 4 ns maximum.



Fundamental Frequency Crystal Oscillator

Suggested Component Values
R = 680 kΩ ± 10%
C = 20 pf ± 20%



3rd Overtone Crystal Oscillator

Suggested Component Values
R1 = 470 kΩ ± 10%
R2 = 330 Ω ± 10%
C1 = 0.1 µf ± 20%
C2 = 26 pf ± 20%
C3 = 20 pf ± 10%
L1 = 2.37 µH ± 10%
XTAL = 40 MHz, AT cut, 20 pf load,
50 Ω max series resistance

Note:
1. The suggested crystal source is ICM, # 433163 - 4.00 (4 MHz fundamental, 20 pf load) or # 436163 - 30.00 (30 MHz fundamental, 20 pf load).
2. To reduce system cost, a ceramic resonator may be used instead of the crystal. Suggested source: Murata-Erie #CST4.00MGW040 (4 MHz with built-in load capacitors)

Note:
1. *3^{rd} overtone crystal.
2. The suggested crystal source is ICM, # 471163 - 40.00 (40 MHz 3^{rd} overtone, 20 pf load).
3. R2 limits crystal current.
4. Reference Benjamin Parzen, The Design of Crystal and Other Harmonic Oscillators, John Wiley & Sons, 1983.

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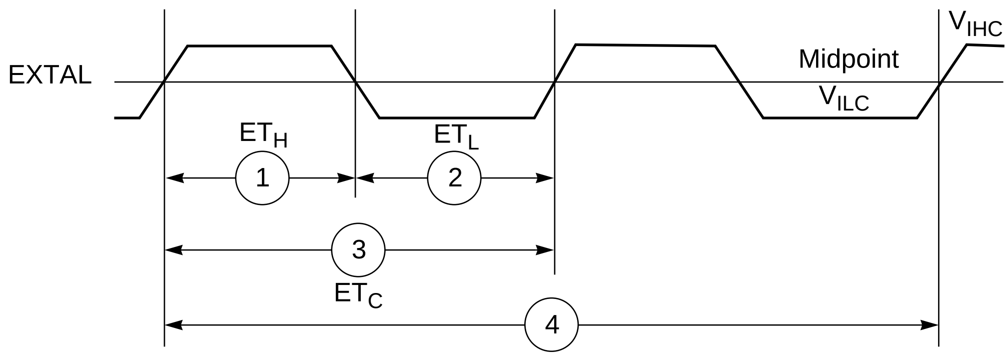
Figure 2-2 Crystal Oscillator Circuits



NOTE: The midpoint is $V_{ILC} + 0.5 (V_{IHC} – V_{ILC})$.

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Figure 2-3 External Clock Timing

Table 2-5 Clock Operation

Num	Characteristics	Symbol	40 MHz		66 MHz		80 MHz		Unit
			Min	Max	Min	Max	Min	Max	
	Frequency of Operation (EXTAL Pin)	E_f	0	40	0	66	0	80	MHz
1	Clock Input High • With PLL disabled (46.7% – 53.3% duty cycle) • With PLL enabled (42.5% – 57.5% duty cycle)	ET_H	11.7 10.5	∞ 235.5 µs	7.09 6.36	∞ 235.5 µs	5.8 5.3	∞ 235.5 µs	ns
2	Clock Input Low • With PLL disabled (46.7% – 53.3% duty cycle) • With PLL enabled (42.5% – 57.5% duty cycle)	ET_L	11.7 10.5	∞ 235.5 µs	7.09 6.36	∞ 235.5 µs	5.8 5.3	∞ 235.5 µs	ns
3	Clock Cycle Time • With PLL disabled • With PLL enabled	ET_C	25 25	∞ 409.6 µs	15.15 15.15	∞ 409.6 µs	12.5 12.5	∞ 409.6 µs	ns
4	Instruction Cycle Time = $I_{CYC} = 2T_C$ • With PLL disabled • With PLL enabled	I_{CYC}	50 50	∞ 819.2 µs	30.3 30.3	∞ 819.2 µs	25 25	∞ 819.2 µs	ns
Note: External Clock Input High and External Clock Input Low are measured at 50% of the input transition.									

PHASE LOCK LOOP (PLL) CHARACTERISTICS

Table 2-6 Phase Lock Loop (PLL) Characteristics

Characteristics	Expression	Min	Max	Unit
VCO frequency when PLL enabled[1,2,3]	$MF \times E_f$	10	f	MHz
PLL external capacitor[4] (PCAP pin to V_{CCP})	$MF \times Cpcap$ $@ MF \le 4$ $@ MF > 4$	 $MF \times 340$ $MF \times 380$	 $MF \times 480$ $MF \times 970$	 pF pF

Notes:
1. The E in ET_H, ET_L, and ET_C means external.
2. MF is the PCTL Multiplication Factor bits (MF0–MF11).
3. The maximum VCO frequency is limited to the internal operation frequency.
4. Cpcap is the value of the PLL capacitor (connected between PCAP pin and V_{CCP}) for MF = 1. The recommended value for Cpcap is: 400 pF for MF ≤ 4 and 540 pF for MF > 4.

RESET, STOP, MODE SELECT, AND INTERRUPT TIMING

C_L = 50 pF + 2 TTL loads
WS = number of Wait States (0–15) programmed into the external bus access using BCR
1 Wait State = T_C

Table 2-7 Reset, Stop, Mode Select, and Interrupt Timing (All Frequencies)

Num	Characteristics	Min	Max	Unit
9	Delay from $\overline{\text{RESET}}$ Assertion to Address High Impedance (periodically sampled and not 100% tested).	—	26	ns
10	Minimum Stabilization Duration • Internal Oscillator PLL Disabled[1] • External clock PLL Disabled[2] • External clock PLL Enabled[2]	 $75000T_C$ $25T_C$ $2500T_C$	 — — —	 ns ns ns
11	Delay from Asynchronous $\overline{\text{RESET}}$ Deassertion to First External Address Output (Internal Reset Deassertion)	$8T_C$	$9T_C + 20$	ns
12	Synchronous Reset Setup Time from $\overline{\text{RESET}}$ Deassertion to first CKOUT transition	8.5	T_C	ns
13	Synchronous Reset Delay Time from the first CKOUT transition to the First External Address Output	$8T_C$	$8T_C + 6$	ns
14	Mode Select Setup Time	21	—	ns
15	Mode Select Hold Time	0	—	ns
16	Minimum Edge-Triggered Interrupt Request Assertion Width	13	—	ns

Table 2-7 Reset, Stop, Mode Select, and Interrupt Timing (All Frequencies) (Continued)

Num	Characteristics	Min	Max	Unit
16a	Minimum Edge-Triggered Interrupt Request Deassertion Width	13	—	ns
17	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{NMI}}$ Assertion to External Memory Access Address Out Valid • Caused by First Interrupt Instruction Fetch • Caused by First Interrupt Instruction Execution	 $5T_C + T_H$ $9T_C + T_H$	 — —	 ns ns
18	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{NMI}}$ Assertion to General Purpose Transfer Output Valid caused by First Interrupt Instruction Execution	$11T_C + T_H$	—	ns
19	Delay from Address Output Valid caused by First Interrupt Instruction Execute to Interrupt Request Deassertion for Level Sensitive Fast Interrupts[3]	—	$2\ T_C + T_L +$ $(T_C \times WS) - 23$	ns
20	Delay from $\overline{\text{RD}}$ Assertion to Interrupt Request Deassertion for Level Sensitive Fast Interrupts[3]	—	$2T_C +$ $(T_C \times WS) - 21$	ns
21	Delay from $\overline{\text{WR}}$ Assertion to Interrupt Request Deassertion for Level Sensitive Fast Interrupts[3] • WS = 0 • WS > 0	 — —	 $2T_C - 21$ $T_C + T_L +$ $(T_C \times WS) - 21$	 ns ns
22	Delay from General-Purpose Output Valid to Interrupt Request Deassertion for Level Sensitive Fast Interrupts[3] —If Second Interrupt Instruction is: • Single Cycle • Two Cycles	 — —	 $T_L - 31$ $2T_C + T_L - 31$	 ns ns
23	Synchronous Interrupt Setup Time from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{NMI}}$ Assertion to the second CKOUT transition	10	T_C	ns
24	Synchronous Interrupt Delay Time from the second CKOUT transition to the First External Address Output Valid caused by the First Instruction Fetch after coming out of Wait State	$13T_C + T_H$	$13T_C + T_H + 6$	ns
25	Duration for $\overline{\text{IRQA}}$ Assertion to Recover from Stop State	12	—	ns
26	Delay from $\overline{\text{IRQA}}$ Assertion to Fetch of First Interrupt Instruction (when exiting 'Stop')[1] • Internal Crystal Oscillator Clock, OMR bit 6 = 0 • Stable External Clock, OMR Bit 6 = 1 • Stable External Clock, PCTL Bit 17 = 1	 $65548T_C$ $20T_C$ $13T_C$	 — — —	 ns ns ns
27	Duration of Level Sensitive $\overline{\text{IRQA}}$ Assertion to ensure interrupt service (when exiting 'Stop')[1] • Internal Crystal Oscillator Clock, OMR bit 6 = 0 • Stable External Clock, OMR Bit 6 = 1 • Stable External Clock, PCTL Bit 17 = 1	 $65534T_C + T_L$ $6T_C + T_L$ 12	 — — —	 ns ns ns

Table 2-7 Reset, Stop, Mode Select, and Interrupt Timing (All Frequencies) (Continued)

Num	Characteristics	Min	Max	Unit
28	Delay from Level Sensitive $\overline{IRQA}$ Assertion to Fetch of First Interrupt Instruction (when exiting 'Stop') [1]			
	• Internal Crystal Oscillator Clock, OMR bit 6 = 0	$65548T_C$	—	ns
	• Stable External Clock, OMR bit 6 = 1	$20T_C$	—	ns
	• Stable External Clock, PCTL bit 17= 1	$13T_C$	—	ns

Notes:
1. A clock stabilization delay is required when using the on-chip crystal oscillator in two cases:
   • after power-on reset, and
   • when recovering from Stop mode.
   During this stabilization period, T_C, T_H, and T_L will not be constant. Since this stabilization period varies, a delay of $75{,}000 \times T_C$ is typically allowed to assure that the oscillator is stable before executing programs.
2. Circuit stabilization delay is required during reset when using an external clock in two cases:
   • after power-on reset, and
   • when recovering from Stop mode.
3. When using fast interrupts and $\overline{IRQA}$ and $\overline{IRQB}$ are defined as level-sensitive, then timings 19 through 22 apply to prevent multiple interrupt service. To avoid these timing restrictions, the deasserted Edge-triggered mode is recommended when using fast interrupt. Long interrupts are recommended when using Level-sensitive mode.

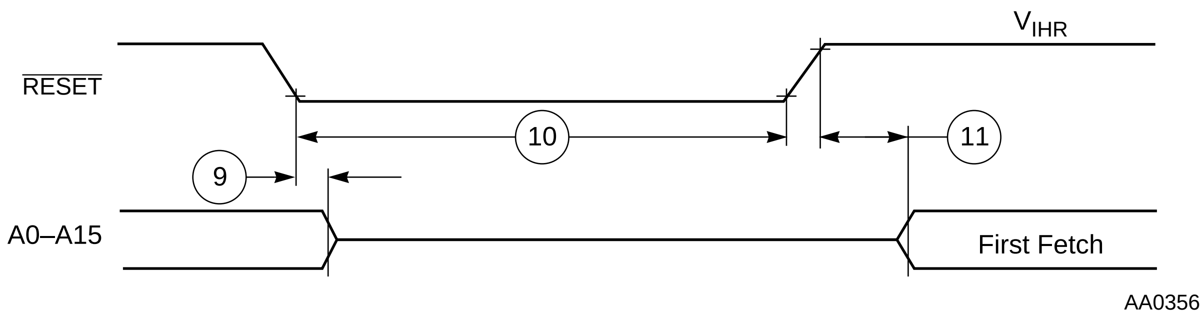


Figure 2-4 Reset Timing

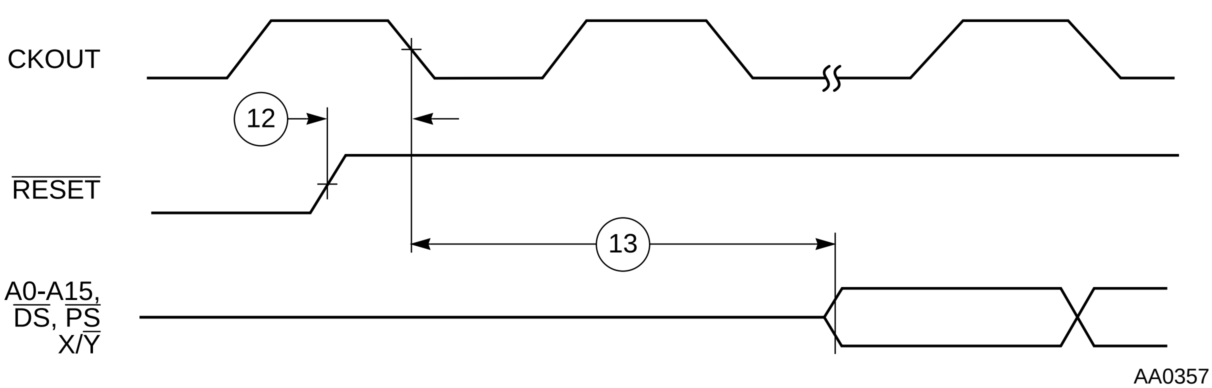


Figure 2-5 Synchronous Reset Timing

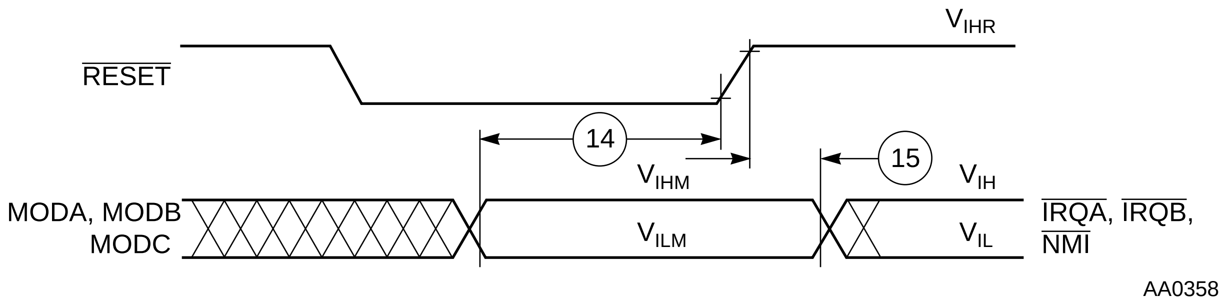


Figure 2-6 Operating Mode Select Timing

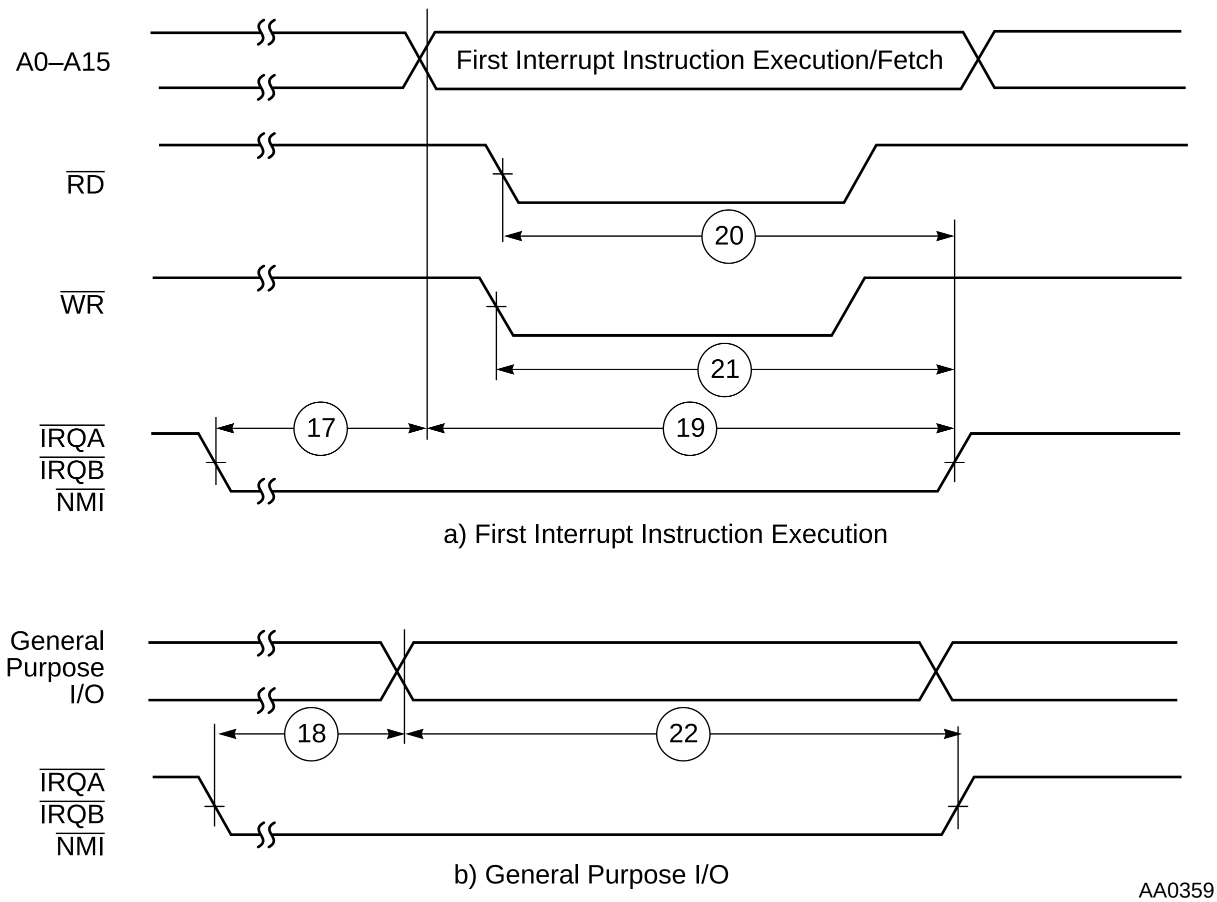


Figure 2-7 External Level-Sensitive Fast Interrupt Timing

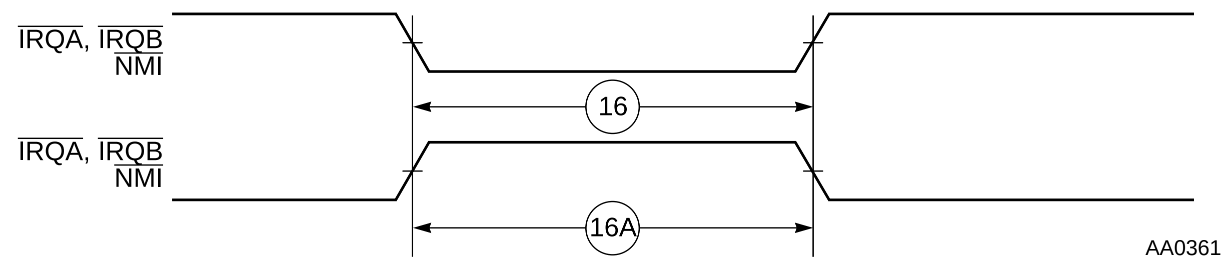


Figure 2-8 External Interrupt Timing (Negative Edge-Triggered)

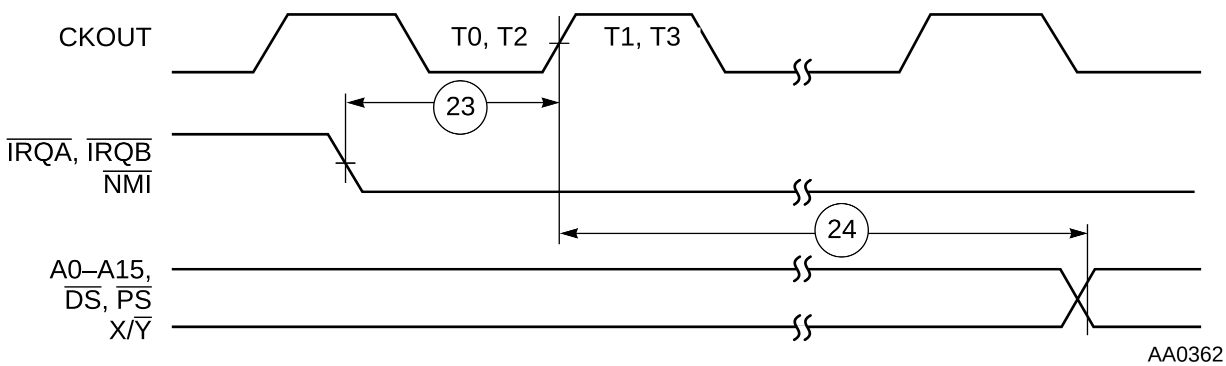


Figure 2-9 Synchronous Interrupt from Wait State Timing

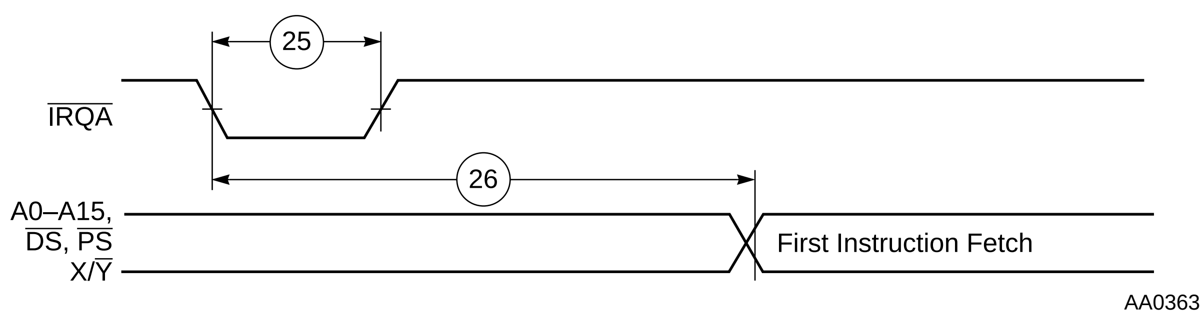


Figure 2-10 Recovery from Stop State Using $\overline{\text{IRQA}}$

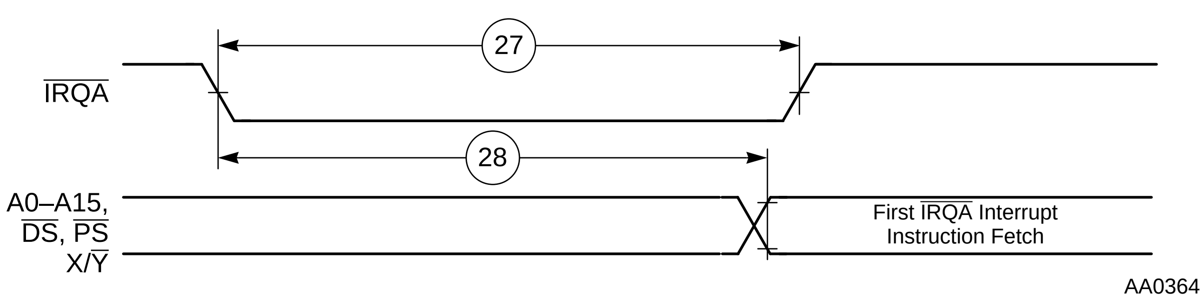


Figure 2-11 Recovery from Stop State Using $\overline{\text{IRQA}}$ Interrupt Service

HOST I/O (HI) TIMING

C_L = 50 pF + 2 TTL loads

Note: Active low lines should be “pulled up” in a manner consistent with the ac and dc specifications.

Table 2-8 Host I / O Timing (All Frequencies)

Num	Characteristics	Min	Max	Unit
31	$\overline{HEN}$ / $\overline{HACK}$ Assertion Width[1] • CVR, ICR, ISR, RXL Read • IVR, RXH / M Read • Write	 T_C + 31 26 13	 — — —	 ns
32	$\overline{HEN}$ / $\overline{HACK}$ Deassertion Width[1] • Between Two TXL Writes[2] • Between Two CVR, ICR, ISR, RXL Reads[3]	13 $2T_C$ + 31 $2T_C$ + 31	— — —	ns ns ns
33	Host Data Input Setup Time Before $\overline{HEN}$ / $\overline{HACK}$ Deassertion	4	—	ns
34	Host Data Input Hold Time After $\overline{HEN}$ / $\overline{HACK}$ Deassertion	3	—	ns
35	$\overline{HEN}$ / $\overline{HACK}$ Assertion to Output Data Active from High Impedance	0	—	ns
36	$\overline{HEN}$ / $\overline{HACK}$ Assertion to Output Data Valid	—	26	ns
37	$\overline{HEN}$ / $\overline{HACK}$ Deassertion to Output Data High Impedance[5]	—	18	ns
38	Output Data Hold Time After $\overline{HEN}$ / $\overline{HACK}$ Deassertion[6]	2.5	—	ns
39	HR / $\overline{W}$ Low Setup Time Before $\overline{HEN}$ Assertion	0	—	ns
40	HR / $\overline{W}$ Low Hold Time After $\overline{HEN}$ Deassertion	3	—	ns
41	HR / $\overline{W}$ High Setup Time to $\overline{HEN}$ Assertion	0	—	ns
42	HR / $\overline{W}$ High Hold Time After $\overline{HEN}$ / $\overline{HACK}$ Deassertion	3	—	ns
43	HA0–HA2 Setup Time Before $\overline{HEN}$ Assertion	0	—	ns
44	HA0–HA2 Hold Time After $\overline{HEN}$ Deassertion	3	—	ns
45	DMA $\overline{HACK}$ Assertion to $\overline{HREQ}$ Deassertion[4]	3	45	ns
46	DMA $\overline{HACK}$ Deassertion to $\overline{HREQ}$ Assertion[4,5] • For DMA RXL Read • For DMA TXL Write • All other cases	 $T_L + T_C + T_H$ $T_L + T_C$ 0	 — — —	 ns ns ns

Table 2-8 Host I/O Timing (Continued)(All Frequencies) (Continued)

Num	Characteristics	Min	Max	Unit
47	Delay from $\overline{\text{HEN}}$ Deassertion to $\overline{\text{HREQ}}$ Assertion for RXL Read[4,5]	$T_L + T_C + T_H$	—	ns
48	Delay from $\overline{\text{HEN}}$ Deassertion to $\overline{\text{HREQ}}$ Assertion for TXL Write[4,5]	$T_L + T_C$	—	ns
49	Delay from $\overline{\text{HEN}}$ Assertion to $\overline{\text{HREQ}}$ Deassertion for RXL Read, TXL Write [4,5]	3	58	ns

Notes:
1. See **Host Port Considerations** in **Section 4**.
2. This timing must be adhered to only if two consecutive writes to the TXL are executed without polling TXDE or $\overline{\text{HREQ}}$.
3. This timing must be adhered to only if two consecutive reads from one of these registers are executed without polling the corresponding status bits or $\overline{\text{HREQ}}$
4. $\overline{\text{HREQ}}$ is pulled up by a 1 kΩ resistor.
5. Specifications are periodically sampled and not 100% tested.
6. May decrease to 0 ns for future versions.

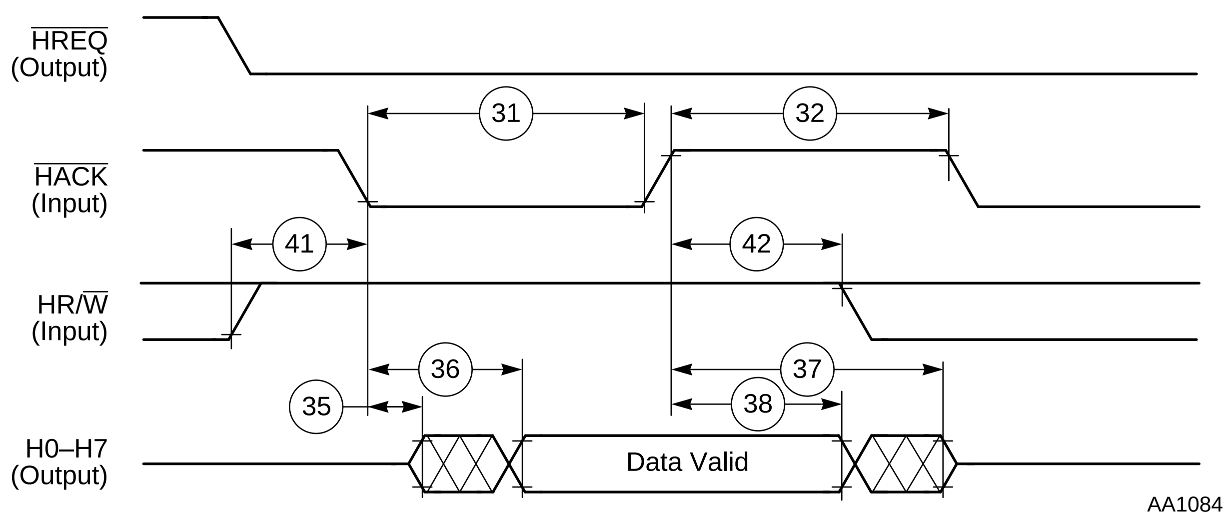


Figure 2-12 Host Interrupt Vector Register (IVR) Read

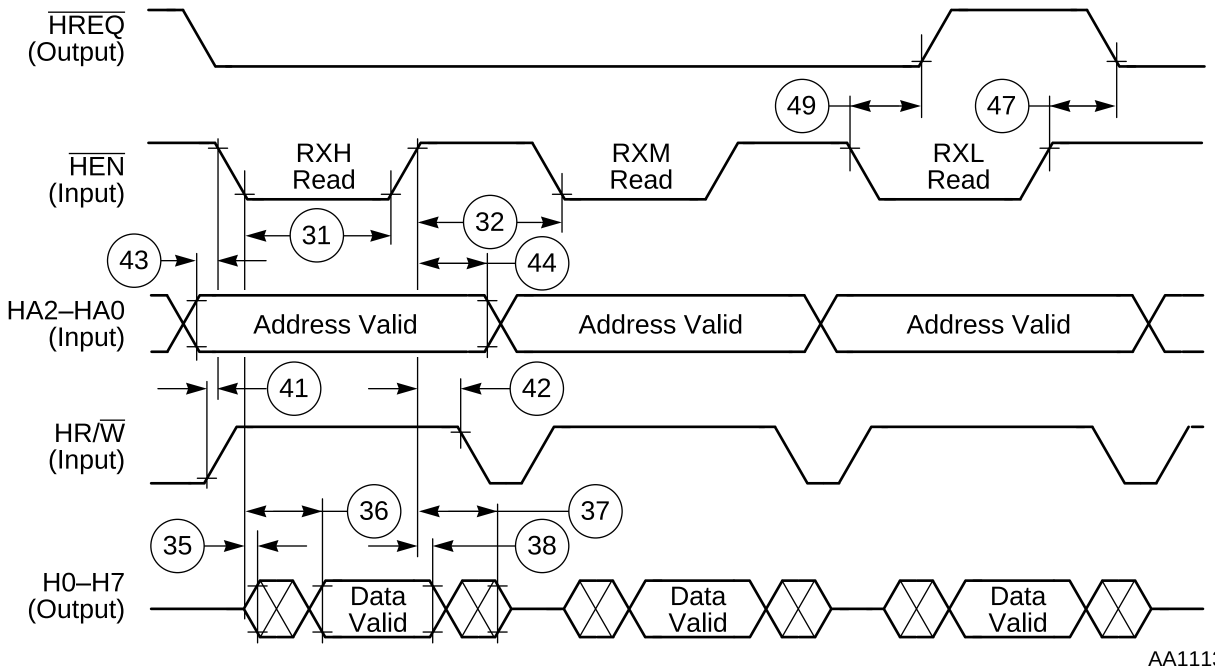


Figure 2-13 Host Read Cycle (Non-DMA Mode)

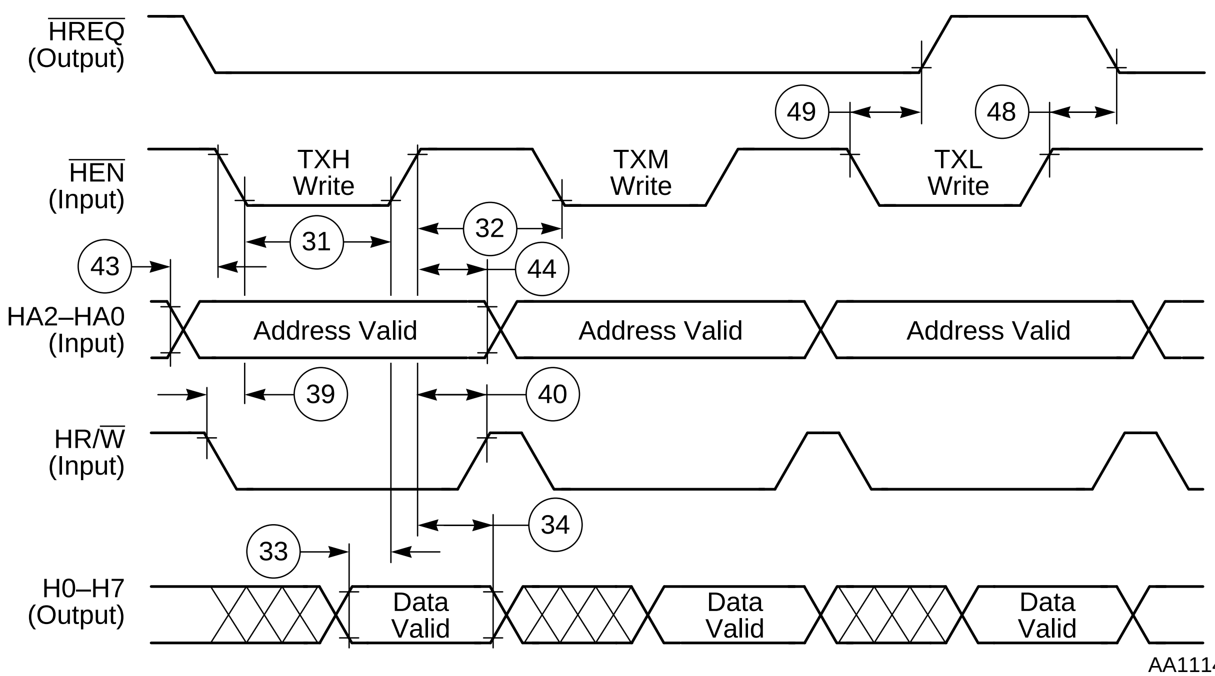


Figure 2-14 Host Write Cycle (Non-DMA Mode)

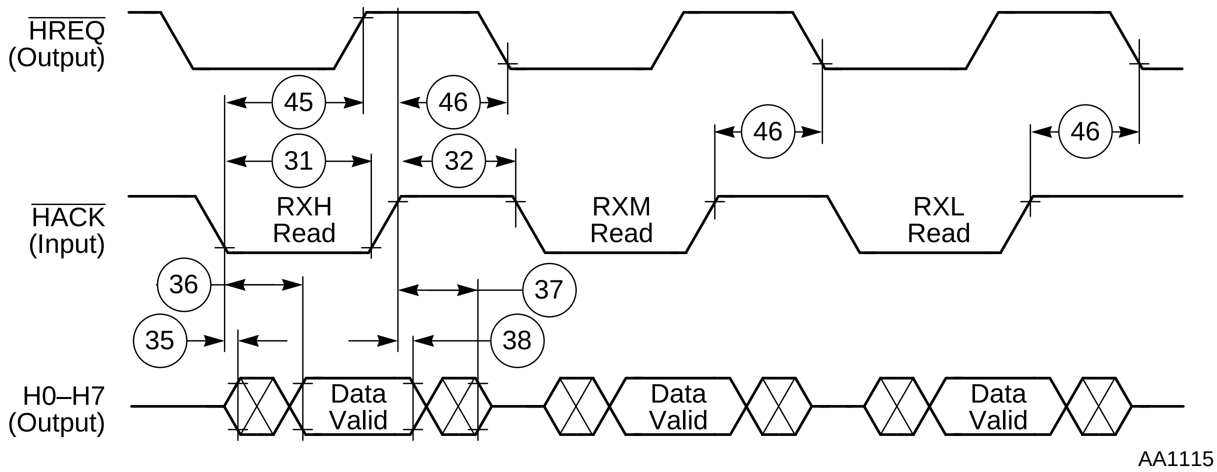


Figure 2-15 Host DMA Read Cycle

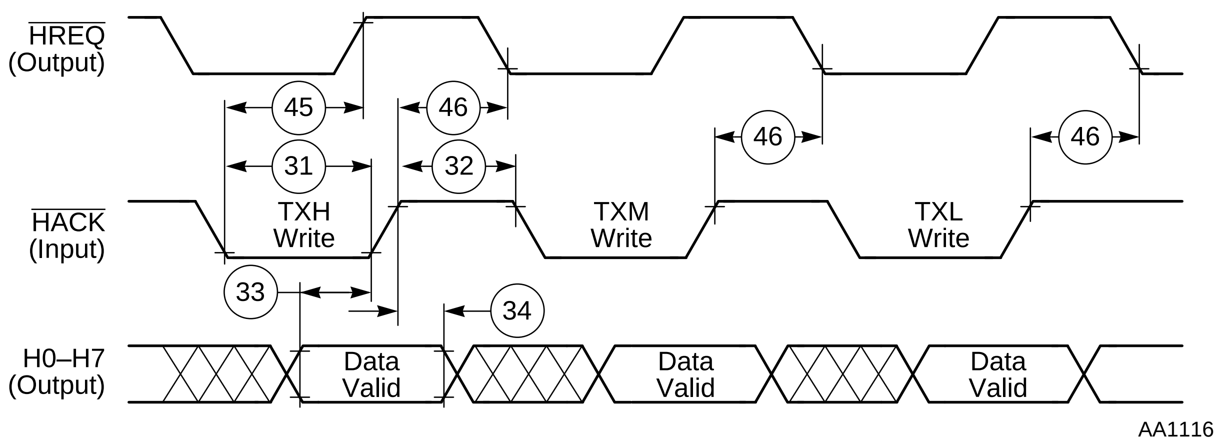


Figure 2-16 Host DMA Write Cycle

SERIAL COMMUNICATION INTERFACE (SCI) TIMING

C_L = 50 pF + 2 TTL loads
t_{SCC} = Synchronous Clock Cycle Time (For internal clock, t_{SCC} is determined by the SCI Clock Control Register and T_C.) The minimum t_{SCC} value is $8 \times T_C$.

Table 2-9 SCI Synchronous Mode Timing (All Frequencies)

Num	Characteristics	Min	Max	Unit
55	Synchronous Clock Cycle—t_{SCC}	$8T_C$	—	ns
56	Clock Low Period	$t_{SCC}/2 - 10.5$	—	ns
57	Clock High Period	$t_{SCC}/2 - 10.5$	—	ns
58	< intentionally blank >	—	—	—
59	Output Data Setup to Clock Falling Edge (Internal Clock)	$t_{SCC}/4 + T_L - 26$	—	ns
60	Output Data Hold After Clock Rising Edge (Internal Clock)	$t_{SCC}/4 - T_L - 8$	—	ns
61	Input Data Setup Time Before Clock Rising Edge (Internal Clock)	$t_{SCC}/4 + T_L + 23$	—	ns
62	Input Data Not Valid Before Clock Rising Edge (Internal Clock)	—	$t_{SCC}/4 + T_L - 5.5$	ns
63	Clock Falling Edge to Output Data Valid (External Clock)	—	32.5	ns
64	Output Data Hold After Clock Rising Edge (External Clock)	$T_C + 3$	—	ns
65	Input Data Setup Time Before Clock Rising Edge (External Clock)	16	—	ns
66	Input Data Hold Time After Clock Rising Edge (External Clock)	21	—	ns

Table 2-10 SCI Asynchronous Mode Timing—1X Clock

Num	Characteristics	Min	Max	Unit
67	Asynchronous Clock Cycle—t_{ACC}	$64T_C$	—	ns
68	Clock Low Period	$t_{ACC}/2 - 11$	—	ns
69	Clock High Period	$t_{ACC}/2 - 11$	—	ns
70	< intentionally blank >	—	—	—
71	Output Data Setup to Clock Rising Edge (Internal Clock)	$t_{ACC}/2 - 51$	—	ns
72	Output Data Hold After Clock Rising Edge (Internal Clock)	$t_{ACC}/2 - 51$	—	ns

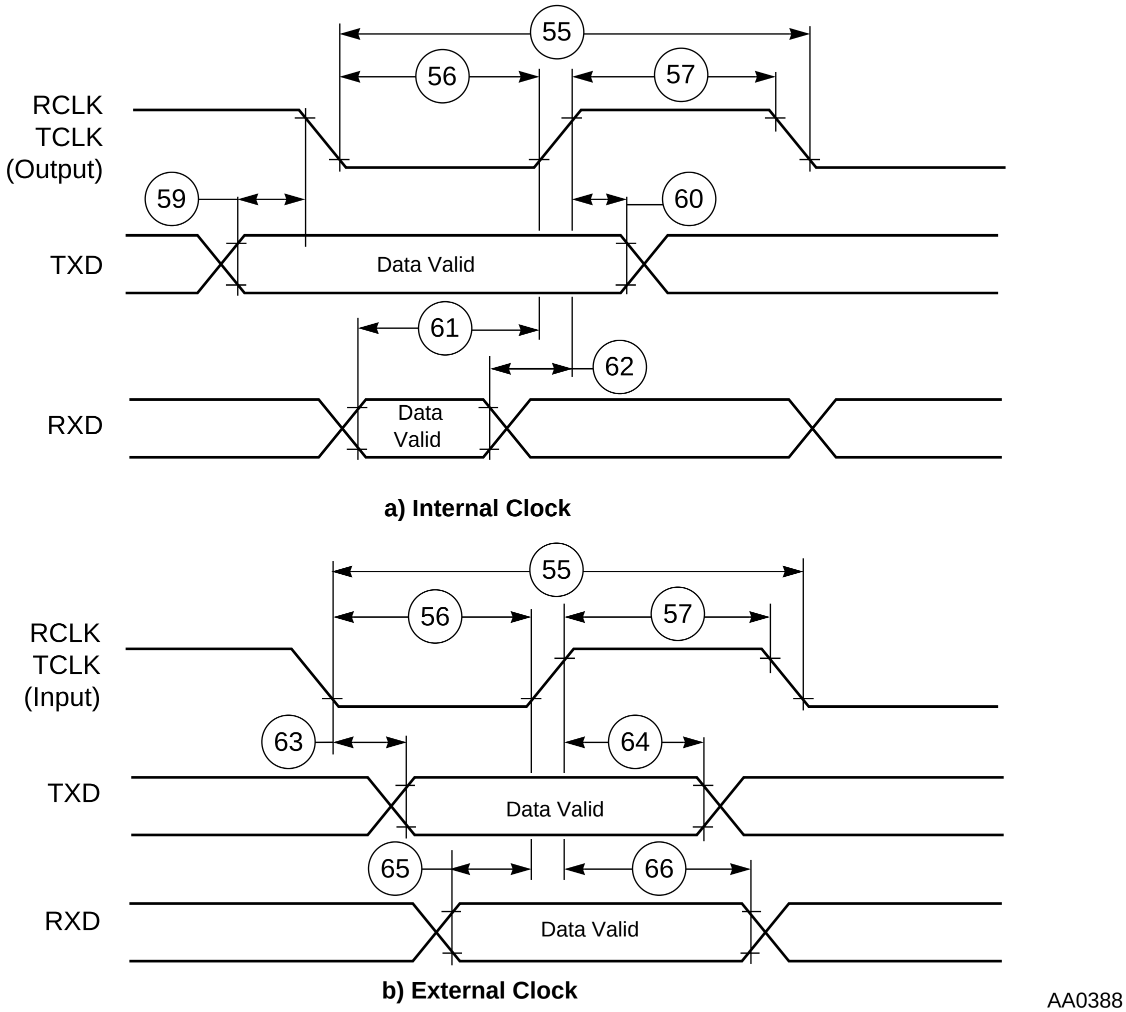


Figure 2-17 SCI Synchronous Mode Timing

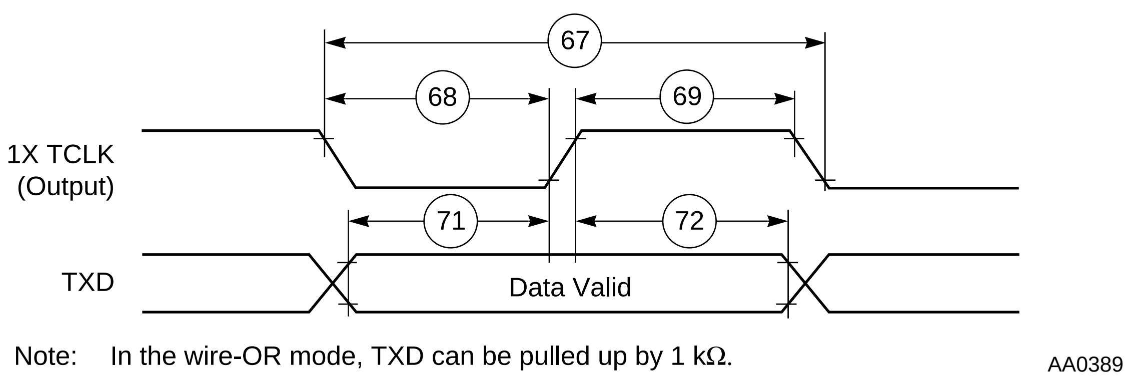


Figure 2-18 SCI Asynchronous Mode Timing

SYNCHRONOUS SERIAL INTERFACE (SSI) TIMING

C_L = 50 pF + 2 TTL loads
t_{SSICC} = SSI clock cycle time
TXC (SCK Pin) = Transmit Clock
RXC (SC0 or SCK Pin) = Receive Clock
FST (SC2 Pin) = Transmit Frame Sync
FSR (SC1 or SC2 Pin) = Receive Frame Sync
i ck = Internal Clock
x ck = External Clock
g ck = Gated Clock
i ck a = Internal Clock, Asynchronous Mode (Asynchronous implies that STD and SRD are two different clocks)
i ck s = Internal Clock, Synchronous Mode (Synchronous implies that STD and SRD are the same clock)
bl = bit length
wl = word length

Table 2-11 SSI Timing

Num	Characteristics	40 MHZ or 66 MHz		80 MHz		Case	Unit
		Min	Max	Min	Max		
80	Clock Cycle–t_{SSICC}[1]	$4T_C$ $3T_C$	— —	$4T_C$ $3T_C$	— —	i ck x ck	ns
81	Clock High Period	$t_{SSICC}/2 - 10.8$ $T_C + T_L$	— —	$T_C + 5$ $T_C + 5$	— —	i ck x ck	ns
82	Clock Low Period	$t_{SSICC}/2 - 10.8$ $T_C + T_L$	— —	$T_C + 5$ $T_C + 5$	— —	i ck x ck	ns
84	RXC Rising Edge to FSR Out (bl) High	— —	40.8 25.8	— —	30 25.8	x ck i ck a	ns
85	RXC Rising Edge to FSR Out (bl) Low	— —	35.8 25.8	— —	30 25.8	x ck i ck a	ns
86	RXC Rising Edge to FSR Out (wl) High	— —	35.8 20.8	— —	30 20.8	x ck i ck a	ns
87	RXC Rising Edge to FSR Out (wl) Low	— —	35.8 20.8	— —	30 20.8	x ck i ck a	ns
88	Data In Setup Time Before RXC (SCK in Synchronous Mode) Falling Edge	3.3 15.8 13	— — —	3.3 15.8 13	— — —	x ck i ck a i ck s	ns

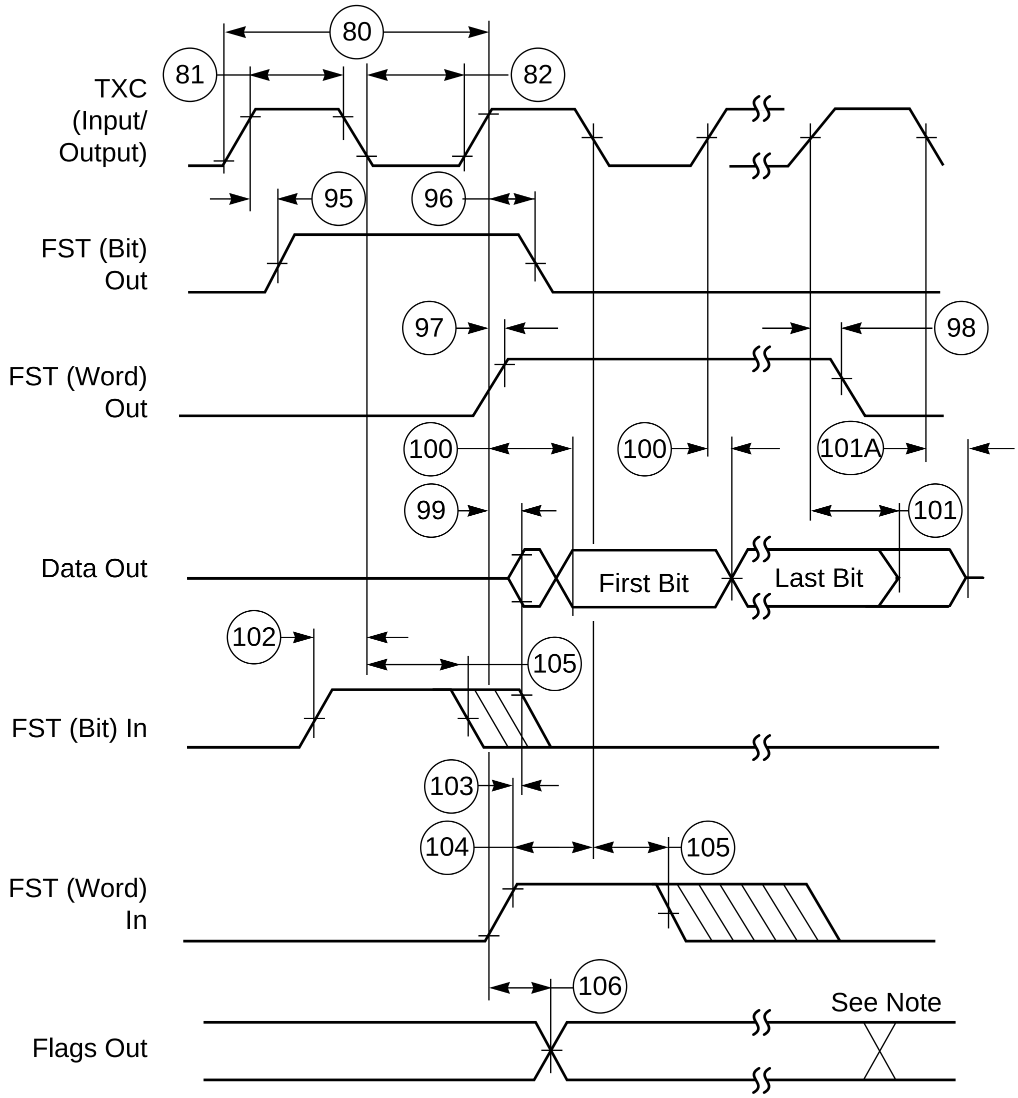
Table 2-11 SSI Timing (Continued)

Num	Characteristics	40 MHZ or 66 MHz		80 MHz		Case	Unit
		Min	Max	Min	Max		
89	Data In Hold Time After RXC Falling Edge	18 3.3	— —	18 3.3	— —	x ck i ck	ns
90	FSR Input (bl) High Before RXC Falling Edge	0.8 17.4	— —	0.8 17.4	— —	x ck i ck a	ns
91	FSR Input (wl) High Before RXC Falling Edge	3.3 18.3	— —	3.3 18.3	— —	x ck i ck a	ns
92	FSR Input Hold Time After RXC Falling Edge	18.3 3.3	— —	18.3 3.3	— —	x ck i ck	ns
93	Flags Input Setup Before RXC Falling Edge	0.8 16.7	— —	0.8 16.7	— —	x ck i ck s	ns
94	Flags Input Hold Time After RXC Falling Edge	18.3 3.3	— —	18.3 3.3	— —	x ck i ck s	ns
95	TXC Rising Edge to FST Out (bl) High	— —	31.6 15.8	— —	30 15.8	x ck i ck	ns
96	TXC Rising Edge to FST Out (bl) Low	— —	33.3 18.3	— —	30 18.3	x ck i ck	ns
97	TXC Rising Edge to FST Out (wl) High	— —	30.8 18.3	— —	30 18.3	x ck i ck	ns
98	TXC Rising Edge to FST Out (wl) Low	— —	33.3 18.3	— —	30 18.3	x ck i ck	ns
99	TXC Rising Edge to Data Out Enable from High Impedance	— —	33.3 + T_H 20.8	— —	30 20.8	x ck i ck	ns
100	TXC Rising Edge to Data Out Valid	— —	33.3 + T_H 22.4	— —	30 22.4	x ck i ck	ns
101	TXC Rising Edge to Data Out High Impedance [2]	— —	35.8 20.8	— —	30 20.8	x ck i ck	ns

Table 2-11 SSI Timing (Continued)

Num	Characteristics	40 MHZ or 66 MHz		80 MHz		Case	Unit
		Min	Max	Min	Max		
101A	TXC Falling Edge to Data Out High Impedance [2]	—	$T_C + T_H$	—	$T_C + T_H$	g ck	ns
102	FST Input (bl) Setup Time Before TXC Falling Edge	0.8 18.3	— —	0.8 18.3	— —	x ck i ck	ns
103	FST Input (wl) to Data Out Enable from High Impedance	—	30.8	—	30.8		ns
104	FST Input (wl) Setup Time Before TXC Falling Edge	0.8 20.0	— —	0.8 20.0	— —	x ck i ck	ns
105	FST Input Hold Time After TXC Falling Edge	18.3 3.3	— —	18.3 3.3	— —	x ck i ck	ns
106	Flag Output Valid After TXC Rising Edge	— —	32.5 20.8	— —	30 20.8	x ck i ck	ns

Notes:
1. For internal clock, External Clock Cycle is defined by I_{cyc} and SSI control register.
2. Periodically sampled and not 100% tested



Note: In the Network mode, output flag transitions can occur at the start of each time slot within the frame. In the Normal mode, the output flag state is asserted for the entire frame period.

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Figure 2-19 SSI Transmitter Timing

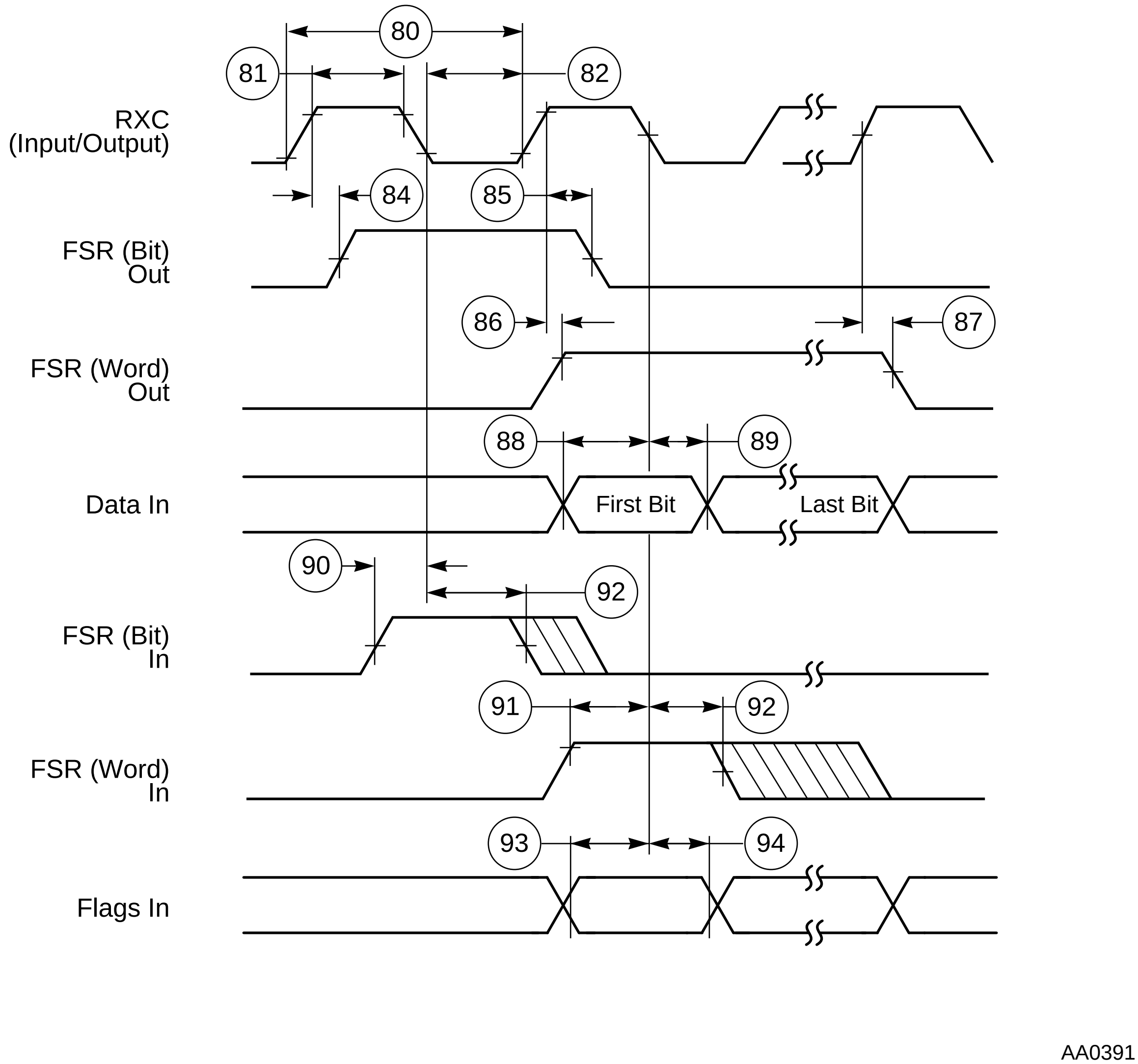


Figure 2-20 SSI Receiver Timing

EXTERNAL BUS ASYNCHRONOUS TIMING

C_L = 50 pF + 2 TTL loads
WS = Number of Wait States (0 to 15), as determined by BCR register

Capacitance Derating: The DSP56002 External Bus Timing Specifications are designed and tested at the maximum capacitive load of 50 pF, including stray capacitance. Typically, the drive capability of the External Bus pins (A0–A15, D0–D23, PS, DS, RD, WR, X/Y, EXTP) derates linearly at 1 ns per 12 pF of additional capacitance from 50 pF to 250 pF of loading. Port B and C pins (HI, SCI, SSI, and Timer) derate linearly at 1 ns per 5 pF of additional capacitance from 50 pF to 250 pF of loading. Active low lines should be “pulled up” in a manner consistent with the AC and DC specifications.

Table 2-12 External Bus Asynchronous Timing

No.	Characteristics	40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
115	Delay from $\overline{BR}$ Assertion to $\overline{BG}$ Assertion							
	• With no external access from the DSP	$2T_C + T_H$	$4T_C + T_H + 14$	$2T_C + T_H$	$4T_C + T_H + 14$	$2T_C + T_H$	$4T_C + T_H + 14$	ns
	• During external read or write access	$T_C + T_H$	$4T_C + T_H + (T_C \times WS) + 14$	$T_C + T_H$	$4T_C + T_H + (T_C \times WS) + 14$	$T_C + T_H$	$4T_C + T_H + (T_C \times WS) + 14$	ns
	• During external read-modify-write access	$T_C + T_H$	$6T_C + T_H + (2T_C \times WS) +14$	$T_C + T_H$	$6T_C + T_H + (2T_C \times WS) +14$	$T_C + T_H$	$6T_C + T_H + (2T_C \times WS) +14$	ns
	• During Stop mode—external bus will not be released and $\overline{BG}$ will not go low	∞	14	∞	14	∞	14	ns
	• During Wait mode	T_H	$T_C + T_H + 15$	T_H	$T_C + T_H + 15$	T_H	$T_C + T_H + 15$	ns
116	Delay from $\overline{BR}$ Deassertion to $\overline{BG}$ Deassertion	$2T_C$	$4T_C + 12.5$	$2T_C$	$4T_C + 12.5$	$2T_C$	$4T_C + 12.5$	ns

Table 2-12 External Bus Asynchronous Timing (Continued)

No.	Characteristics	40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
117	$\overline{BG}$ Deassertion Duration • During Wait mode • All other cases	 $T_C - 5.5$ $2T_C + T_H - 5.5$	 — —	 $T_C - 5.5$ $2T_C + T_H - 5.5$	 — —	 $T_C - 5.5$ $2T_C + T_H - 5.5$	 — —	 ns ns
118	Delay from Address, Data, and Control Bus High Impedance to $\overline{BG}$ Assertion	0	—	0	—	0	—	ns
119	Delay from $\overline{BG}$ Deassertion to Address and Control Bus Enabled	0	T_H	0	T_H	0	T_H	ns
120	Address Valid to $\overline{WR}$ Assertion • WS = 0 • WS > 0	 $T_L - 6$ $T_C - 6$	 — —	 $T_L - 4.5$ $T_C - 4.5$	 — —	 $T_L - 4.5$ $T_C - 4.5$	 — —	 ns ns
121	$\overline{WR}$ Assertion Width • WS = 0 • WS > 0	 $T_C - 4$ $WS \times T_C + T_L$	 — —	 $T_C - 4$ $WS \times T_C + T_L$	 — —	 $T_C - 2$ $WS \times T_C + T_L$	 — —	 ns ns
122	$\overline{WR}$ Deassertion to Address Not Valid	$T_H - 6$	—	$T_H - 4$	—	$T_H - 4$	—	ns
123	$\overline{WR}$ Assertion to Data Out Active From High Impedance • WS = 0 • WS > 0	 $T_H - 4$ 0	 — —	 $T_H - 4$ 0	 — —	 $T_H - 4$ 0	 — —	 ns ns
124	Data Out Hold Time from $\overline{WR}$ Deassertion (the maximum specification is periodically sampled, and not 100% tested)	$T_H - 7$	$T_H - 2.5$	$T_H - 5$	$T_H - 1.5$	$T_H - 5$	$T_H - 1.5$	ns
125	Data Out Setup Time to $\overline{WR}$ Deassertion • WS = 0 • WS > 0	 $T_L - 0.8$ $WS \times T_C + T_L - 0.8$	 — —	 $T_L - 0.4$ $WS \times T_C + T_L - 0.4$	 — —	 $T_L - 0.5$ $WS \times T_C + T_L - 0.5$	 — —	 ns ns

Table 2-12 External Bus Asynchronous Timing (Continued)

No.	Characteristics	40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
126	$\overline{RD}$ Deassertion to Address Not Valid	T_H	—	$T_H - 1$	—	T_H	—	ns
127	Address Valid to $\overline{RD}$ Deassertion • WS = 0 • WS > 0	$T_C + T_L - 6$ $((WS + 1) \times T_C) + T_L - 6$	— —	$T_C + T_L - 6$ $((WS + 1) \times T_C) + T_L - 6$	— —	$T_C + T_L - 6$ $((WS + 1) \times T_C) + T_L - 6$	— —	ns ns
128	Input Data Hold Time to $\overline{RD}$ Deassertion	0	—	0	—	0	—	ns
129	$\overline{RD}$ Assertion Width • WS = 0 • WS > 0	$T_C - 4$ $((WS + 1) \times T_C) - 4$	— —	$T_C - 4$ $((WS + 1) \times T_C) - 4$	— —	$T_C - 4$ $((WS + 1) \times T_C) - 4$	— —	ns ns
130	Address Valid to Input Data Valid • WS = 0 • WS > 0	— —	$T_C + T_L - 9.5$ $((WS+1)\times T_C) + T_L - 9.5$	— —	$T_C + T_L - 7$ $((WS+1)\times T_C) + T_L - 7$	— —	$T_C + T_L - 6$ $((WS+1) \times T_C) + T_L - 6$	ns ns
131	Address Valid to $\overline{RD}$ Assertion	$T_L - 4.5$	—	$T_L - 4.5$	—	$T_L - 4.5$	—	ns
132	$\overline{RD}$ Assertion to Input Data Valid • WS = 0 • WS > 0	— —	$T_C - 7.5$ $((WS+1)\times T_C) - 7.5$	— —	$T_C - 5.5$ $((WS+1)\times T_C) - 5.5$	— —	$T_C - 5.5$ $((WS+1)\times T_C) - 5.5$	ns ns
133	$\overline{WR}$ Deassertion to $\overline{RD}$ Assertion	$T_C - 7$	—	$T_C - 5$	—	$T_C - 5$	—	ns
134	$\overline{RD}$ Deassertion to $\overline{RD}$ Assertion	$T_C - 4$	—	$T_C - 2.5$	—	$T_C - 2.5$	—	ns
135	$\overline{WR}$ Deassertion to $\overline{WR}$ Assertion • WS = 0 • WS > 0	$T_C - 4$ $T_C + T_H - 4$	— —	$T_C - 3$ $T_C + T_H - 3$	— —	$T_C - 3$ $T_C + T_H - 3$	— —	ns ns

Table 2-12 External Bus Asynchronous Timing (Continued)

No.	Characteristics	40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
136	$\overline{RD}$ Deassertion to $\overline{WR}$ Assertion • WS = 0 • WS > 0	 $T_C - 4$ $T_C + T_H - 4$	 — —	 $T_C - 2.5$ $T_C + T_H - 2.5$	 — —	 $T_C - 2.5$ $T_C + T_H - 2.5$	 — —	 ns ns

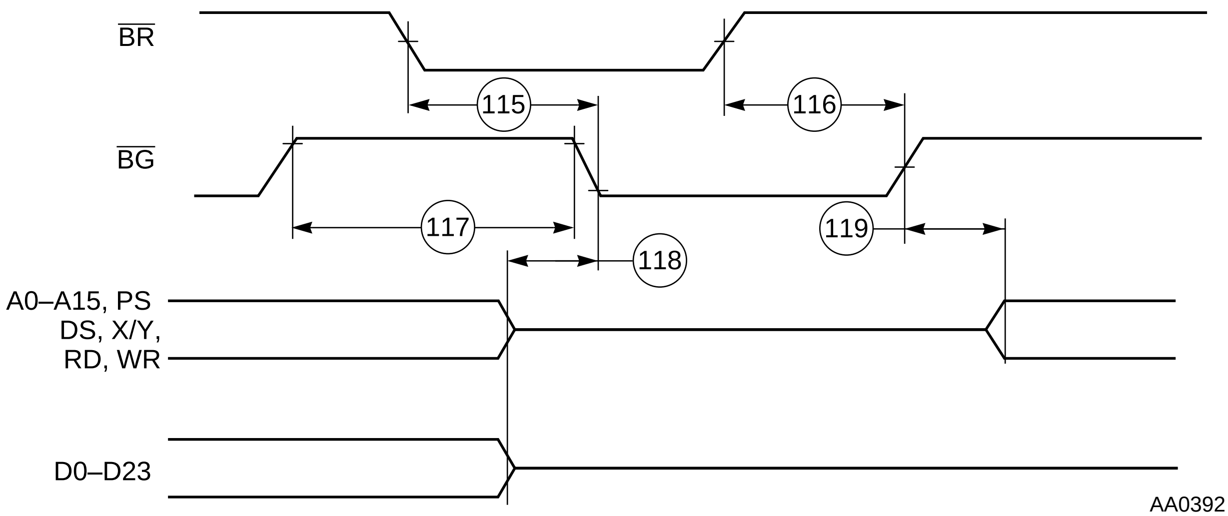
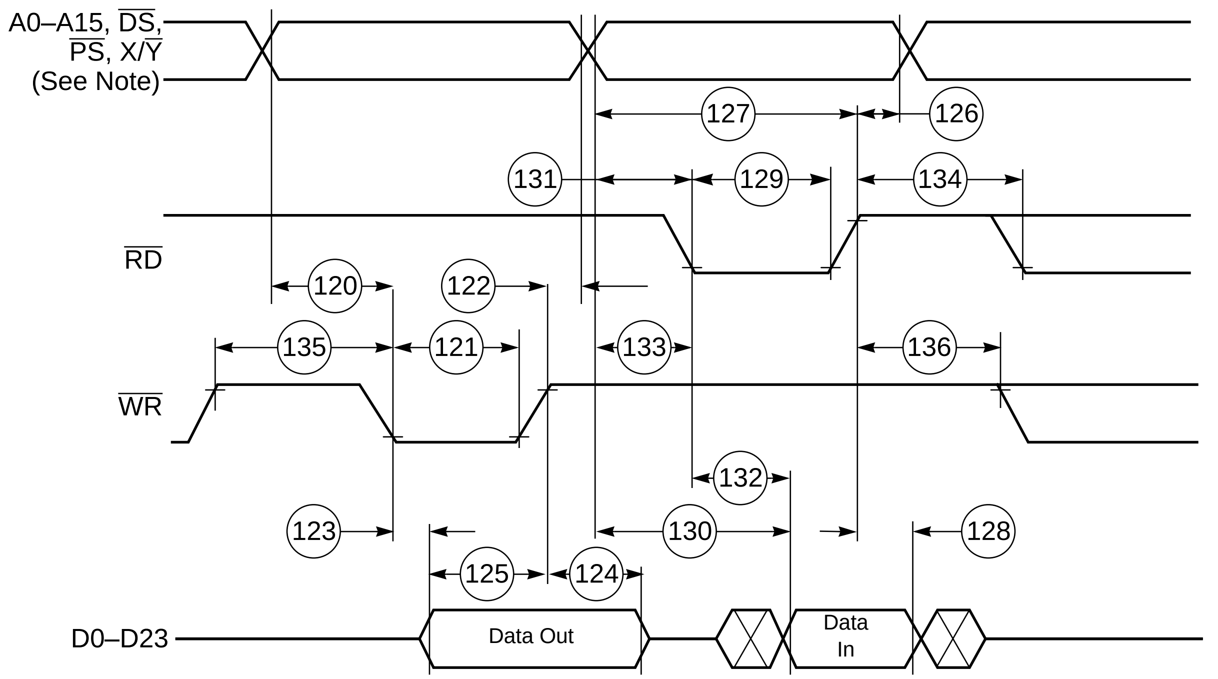


Figure 2-21 Bus Request / Bus Grant Timing

External Bus Asynchronous Timing



Note: During Read-Modify-Write instructions, the address lines do not change state.

Figure 2-22 External Bus Asynchronous Timing

EXTERNAL BUS SYNCHRONOUS TIMING

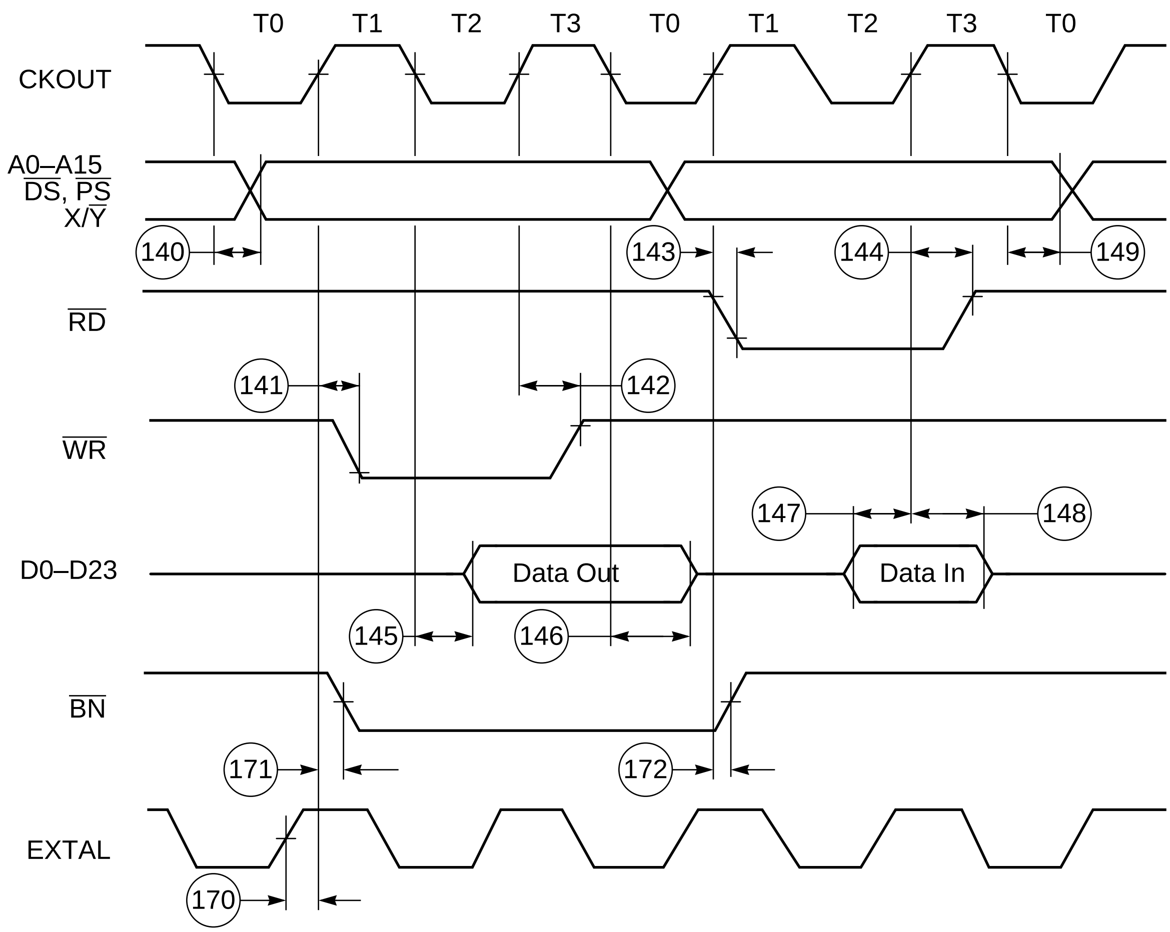
C_L = 50 pF + 2 TTL loads

Capacitance Derating: The DSP56002 external bus timing specifications are designed and tested at the maximum capacitive load of 50 pF, including stray capacitance. Typically, the drive capability of the external bus pins (A0–A15, D0–D23, $\overline{PS}$, $\overline{DS}$, $\overline{RD}$, $\overline{WR}$, X / $\overline{Y}$) derates linearly at 1 ns per 12 pF of additional capacitance from 50 pF to 250 pF of loading. Port B and C pins (HI, SCI, SSI, and Timer) derate linearly at 1 ns per 5 pF of additional capacitance from 50 pF to 250 pF of loading. Active-low lines should be “pulled up” in a manner consistent with the ac and dc specifications.

Table 2-13 External Bus Synchronous Timing

Num	Characteristics	40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
140	First CKOUT transition to Address Valid	—	6.2	—	5	—	5	ns
141	Second CKOUT transition to $\overline{WR}$ Assertion[1]							ns
	• WS = 0	—	4.4	—	4	—	4	ns
	• WS > 0	—	T_H + 4.4	—	T_H + 4	—	T_H + 4	
142	Second CKOUT transition to $\overline{WR}$ Deassertion	1.3	9.1	1	5	1	5	ns
143	Second CKOUT transition to $\overline{RD}$ Assertion	—	3.9	—	3.9	—	3.9	ns
144	Second CKOUT transition to $\overline{RD}$ Deassertion	0	3.4	–3	3	–3	3	ns
145	First CKOUT transition to Data-Out Valid	—	5.4	—	4.5	—	4.5	ns
146	First CKOUT transition to Data-Out Invalid[3]	0	—	0	—	0	—	ns
147	Data-In Valid to second CKOUT transition (Setup)	3.4	—	3.4	—	3.4	—	ns
148	Second CKOUT transition to Data-In Invalid (Hold)	0	—	0	—	0	—	ns
149	First CKOUT transition to Address Invalid[3]	0	—	0	—	0	—	ns

Notes:
1. AC timing specifications which are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal’s transition.
2. WS are wait state values specified in the BCR.
3. First CKOUT transition to data-out invalid (specification # T146) and first CKOUT transition to address invalid (specification # T149) indicate the time after which data / address are no longer guaranteed to be valid.
4. Timings are given from CKOUT midpoint to V_{OL} or V_{OH} of the corresponding pin(s).
5. First CKOUT transition is a falling edge of CKOUT for CKP = 0.



Note: During Read-Modify-Write Instructions, the address lines do not change states.

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Figure 2-23 Synchronous Bus Timing

Table 2-14 Bus Strobe / Wait Timing

No.	Characteristics	40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
150	First CKOUT transition to $\overline{BS}$ Assertion	—	5.6	—	5.6	—	5.6	ns
151	WT Assertion to first CKOUT transition (setup time)	5.3	—	5.3	—	5.3	—	ns
152	First CKOUT transition to $\overline{WT}$ Deassertion for Minimum Timing	0	$T_C - 7.9$	0	$T_C - 7.9$	0	$T_C - 6$	ns
153	$\overline{WT}$ Deassertion to first CKOUT transition for Maximum Timing (2 wait states)	7.9	—	7.9	—	6	—	ns
154	Second CKOUT transition to $\overline{BS}$ Deassertion	—	5.2	—	5.2	—	5.2	ns
155	$\overline{BS}$ Assertion to Address Valid	0	2.4	0	2.4	0	2.4	ns
156	$\overline{BS}$ Assertion to $\overline{WT}$ Assertion[1]	0	$T_C - 10.9$	0	$T_C - 10.9$	0	$T_C - 8.8$	ns
157	$\overline{BS}$ Assertion to $\overline{WT}$ Deassertion[1,3]	$(WS–1) \times T_C$	$WS \times T_C - 13.5$	$(WS–1) \times T_C$	$WS \times T_C - 13.5$	$(WS–1) \times T_C$	$WS \times T_C - 10.9$	ns
158	$\overline{WT}$ Deassertion to $\overline{BS}$ Deassertion	$T_C + T_L + 3.3$	$2 \times T_C + T_L + 7.8$	$T_C + T_L + 3.3$	$2 \times T_C + T_L + 7.8$	$T_C + T_L + 3.3$	$2 \times T_C + T_L + 7.8$	ns
159	Minimum $\overline{BS}$ Deassertion Width for Consecutive External Accesses	$T_H - 1$	—	$T_H - 1$	—	$T_H - 1$	—	ns
160	$\overline{BS}$ Deassertion to Address Invalid[2]	$T_H - 4.6$	—	$T_H - 4.6$	—	$T_H - 4.6$	—	ns
161	Data-In Valid to $\overline{RD}$ Deassertion (Set Up)	3.4	—	3.4	—	3.4	—	ns
162	$\overline{BR}$ Assertion to second CKOUT transition for Minimum Timing	9.5	T_C	9.5	T_C	9.5	T_C	ns

Table 2-14 Bus Strobe / Wait Timing (Continued)

No.	Characteristics	40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
163	$\overline{BR}$ Deassertion to second CKOUT transition for Minimum Timing	8	T_C	8	T_C	8	T_C	ns
164	First CKOUT transition to $\overline{BG}$ Assertion	—	8.8	—	8.8	—	8.8	ns
165	First CKOUT transition to $\overline{BG}$ Deassertion	—	5.3	—	5.3	—	5.3	ns
170	EXTAL to CKOUT with PLL Disabled EXTAL to CKOUT[5] with PLL Enabled and MF < 5	3 0.3	9.7 3.7	3 0.3	9.7 3.7	3 0.3	9.7 3.7	ns ns
171	Second CKOUT transition to $\overline{BN}$ Assertion	—	5.7	—	5.7	—	5.7	ns
172	Second CKOUT transition to $\overline{BN}$ Deassertion	—	5	—	5	—	5	ns

Notes:
1. If wait states are also inserted using the BCR and if the number of wait states is greater than 2, then specification numbers T156 and T157 can be increased accordingly.
2. $\overline{BS}$ deassertion to address invalid indicates the time after which the address are no longer guaranteed to be valid.
3. The minimum number of wait states when using $\overline{BS}$ / $\overline{WT}$ is two (2).
4. For read-modify-write instructions, the address lines will not change states between the read and the write cycle. However, $\overline{BS}$ will deassert before asserting again for the write cycle. If wait states are desired for each of the read and write cycle, the $\overline{WT}$ pin must be asserted once for each cycle.
5. When EXTAL frequency is less than 33 MHz, then timing T170 is not guaranteed for a period of 1000 × T_C after PLOCK assertion following the events below:
   - when enabling the PLL operation by software,
   - when changing the Multiplication Factor,
   - when recovering from the Stop state if the PLL was turned off and it is supposed to turn, on
   - when exiting the Stop state.

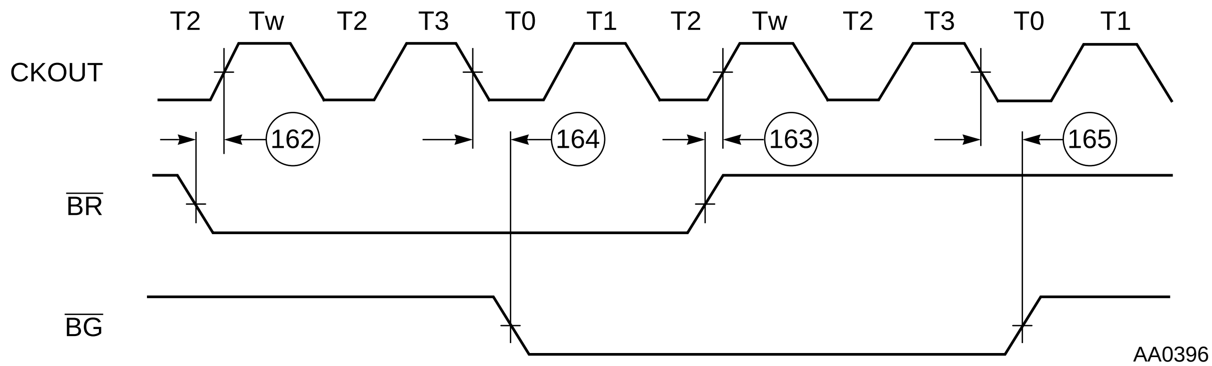
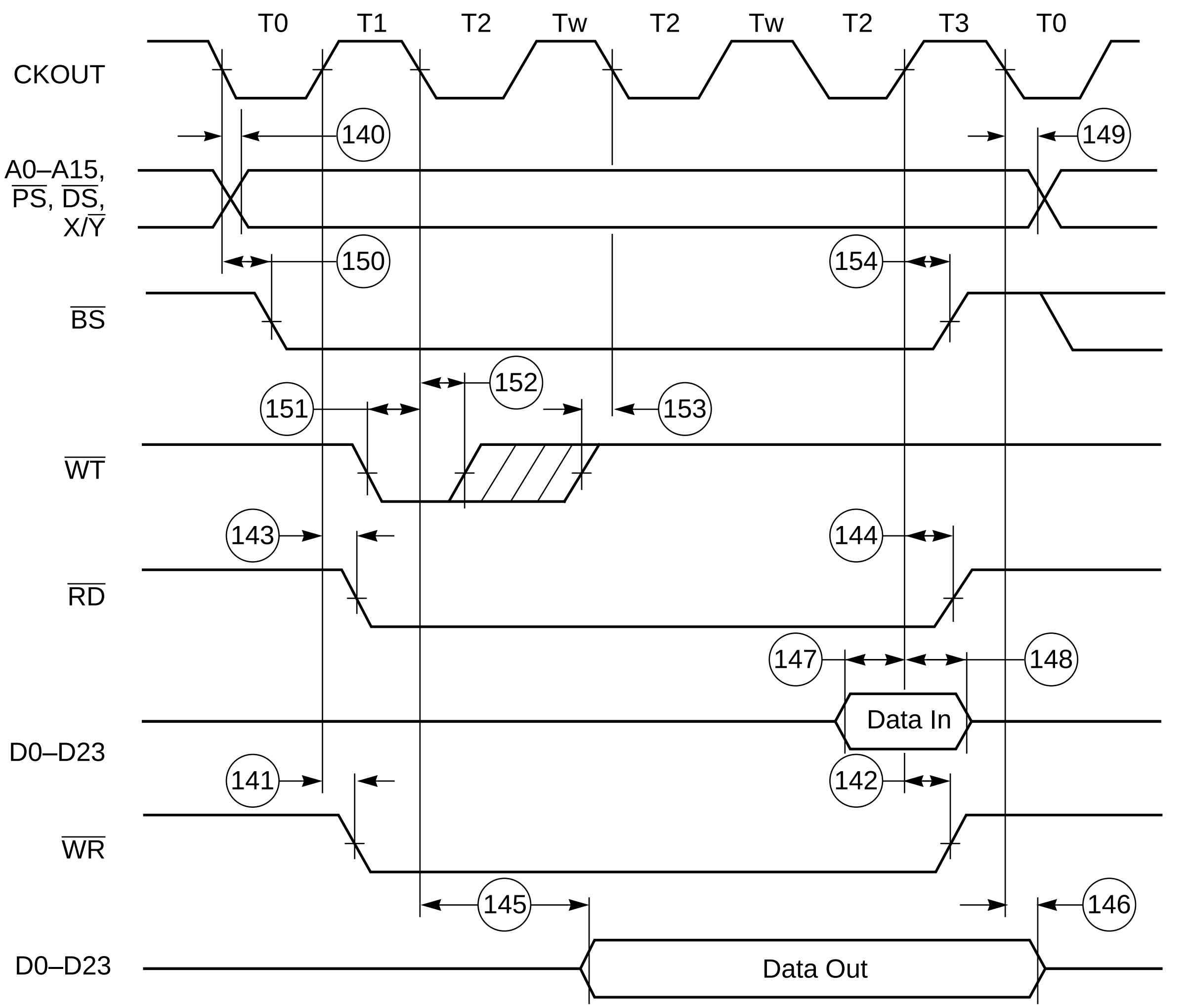
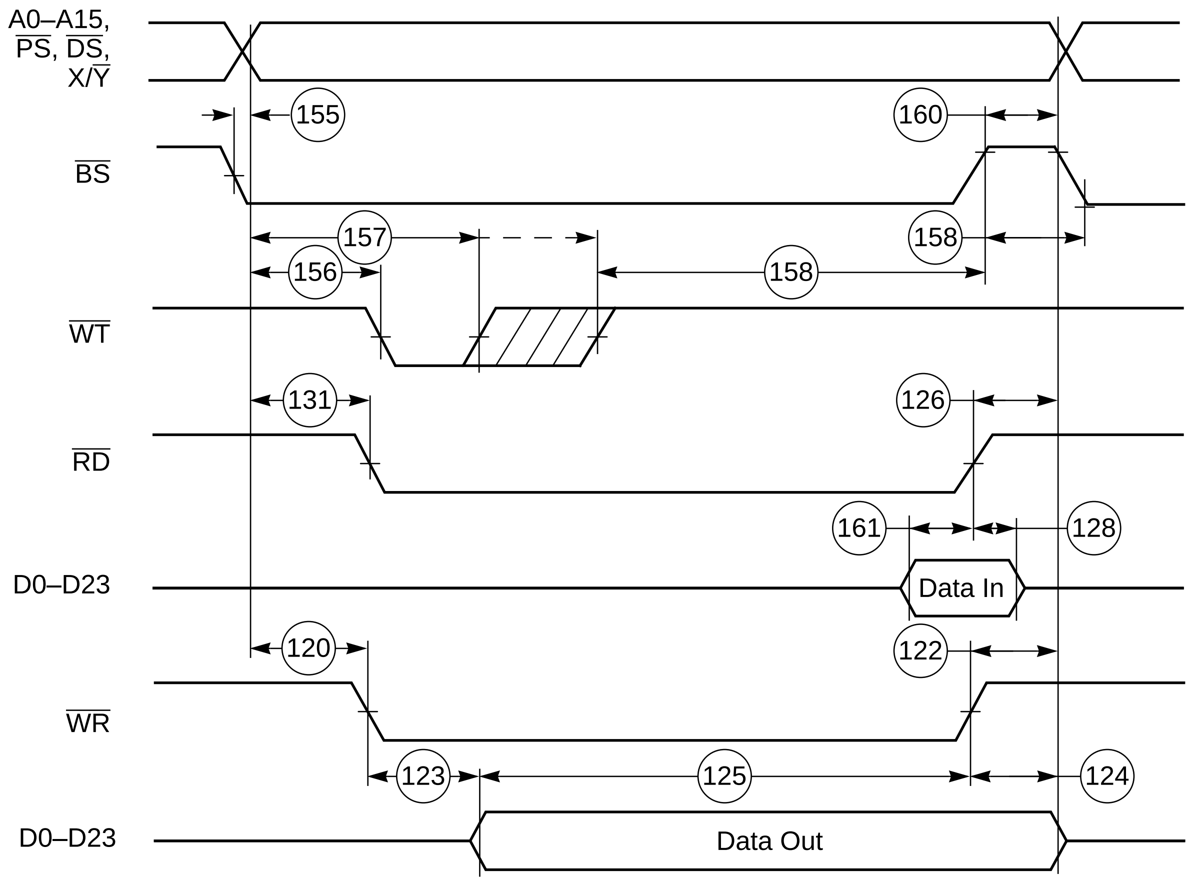


Figure 2-24 Synchronous Bus Request / Bus Grant Timing



Note: During Read-Modify-Write instructions, the address lines do not change state. However, $\overline{BS}$ will deassert before asserting again for the write cycle.

Figure 2-25 Synchronous $\overline{BS}$ / $\overline{WT}$ Timings



Note: During Read-Modify-Write instructions, the address lines do not change state. However, $\overline{\text{BS}}$ will deassert before asserting again for the write cycle.

Figure 2-26 Asynchronous $\overline{\text{BS}}$ / $\overline{\text{WT}}$ Timings

OnCE PORT TIMING

C_L = 50 pF + 2 TTL loads

Table 2-15 OnCE Port Timing

Num	Characteristics	Min	Max	Unit
230	DSCK Low	40	—	ns
231	DSCK High	40	—	ns
232	DSCK Cycle Time	200	—	ns
233	$\overline{DR}$ Asserted to DSO ($\overline{ACK}$) Asserted	$5T_C$	—	ns
234	DSCK High to DSO Valid	—	42	ns
235	DSCK High to DSO Invalid	3	—	ns
236	DSI Valid to DSCK Low (Setup)	15	—	ns
237	DSCK Low to DSI Invalid (Hold)	3	—	ns
238	Last DSCK Low to OS0–OS1, $\overline{ACK}$ Active	$3T_C + T_L$	—	ns
239	DSO ($\overline{ACK}$) Asserted to First DSCK High	$2T_C$	—	ns
240	DSO ($\overline{ACK}$) Assertion Width	$4T_C + T_H – 3$	$5T_C + 7$	ns
241	DSO ($\overline{ACK}$) Asserted to OS0–OS1 High Impedance[2]	—	0	ns
242	OS0–OS1 Valid to second CKOUT transition	$T_C – 21$	—	ns
243	Second CKOUT transition to OS0–OS1 Invalid	0	—	ns
244	Last DSCK Low of Read Register to First DSCK High of Next Command	$7T_C + 10$	—	ns
245	Last DSCK Low to DSO Invalid (Hold)	3	—	ns
246	$\overline{DR}$ Assertion to second CKOUT transition for Wake Up from Wait state	12	T_C	ns
247	Second CKOUT transition to DSO after Wake Up from Wait state	$17T_C$	—	ns
248	$\overline{DR}$ Assertion Width • To recover from Wait state • To recover from Wait state and enter Debug mode	 15 $13T_C + 15$	 $12T_C – 15$ —	 ns
249	$\overline{DR}$ Assertion to DSO ($\overline{ACK}$) Valid (enter Debug mode) After Asynchronous Recovery from Wait State	$17T_C$	—	ns
250A	$\overline{DR}$ Assertion Width to Recover from Stop state[1] • Stable External Clock, OMR Bit 6 = 0 • Stable External Clock, OMR Bit 6 = 1 • Stable External Clock, PCTL Bit 17= 1	 15 15 15	 $65548T_C + T_L$ $20T_C + T_L$ $13T_C + T_L$	 ns ns ns

Table 2-15 OnCE Port Timing

Num	Characteristics	Min	Max	Unit
250B	$\overline{DR}$ Assertion Width to Recover from Stop state and enter Debug mode[1] • Stable External Clock,OMR Bit 6 = 0 • Stable External Clock,OMR Bit 6 = 1 • Stable External Clock,PCTL Bit 17= 1	 $65549T_C + T_L$ $21T_C + T_L$ $14T_C + T_L$	 — — —	 ns ns ns
251	$\overline{DR}$ Assertion to DSO ($\overline{ACK}$) Valid (enter Debug mode) after recovery from Stop state[1] • Stable External Clock, OMR Bit 6 = 0 • Stable External Clock, OMR Bit 6 = 1 • Stable External Clock, PCTL Bit 17= 1	 $65553T_C + T_L$ $25T_C + T_L$ $18T_C + T_L$	 — — —	 ns ns ns

Notes:
1. A clock stabilization delay is required when using the on-chip crystal oscillator in two cases:
   - after power-on Reset, and
   - when recovering from Stop mode.

   During this stabilization period, T_C, T_H, and T_L will not be constant. Since this stabilization period varies, a delay of $75{,}000 \times T_C$ is typically allowed to assure that the oscillator is stable before executing programs. While it is possible to set OMR bit 6 = 1 when using the internal crystal oscillator, it is not recommended and these specifications do not guarantee timings for that case.
2. The maximum specified is periodically sampled and not 100% tested.

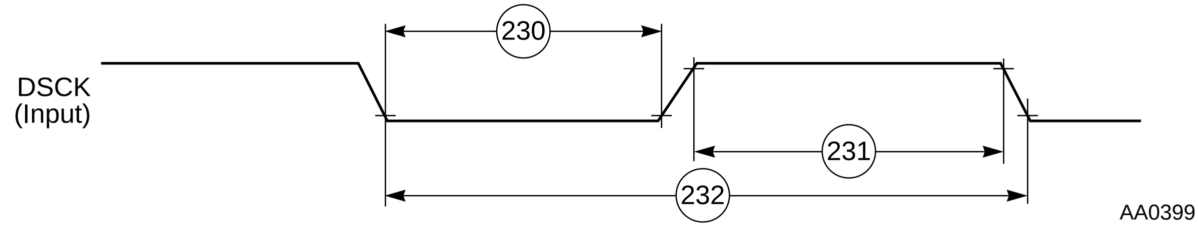


Figure 2-27 OnCE Serial Clock Timing

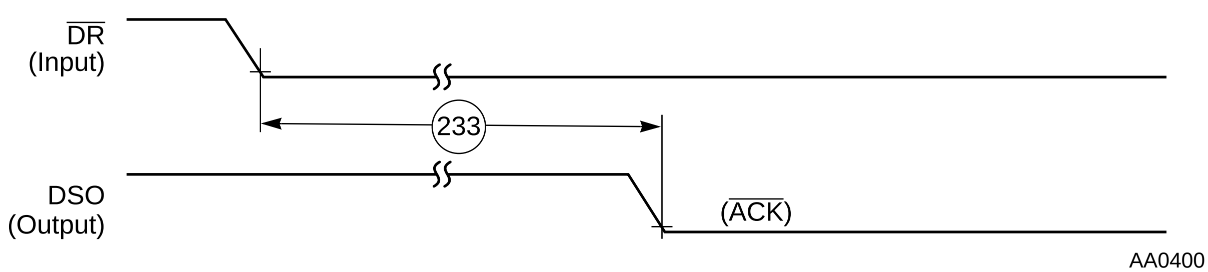


Figure 2-28 OnCE Acknowledge Timing

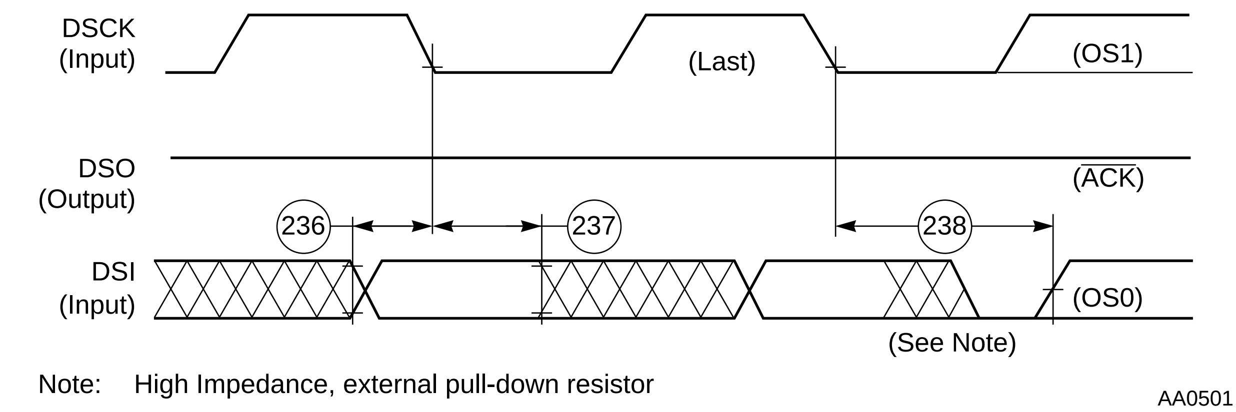


Figure 2-29 OnCE Data I/O To Status Timing

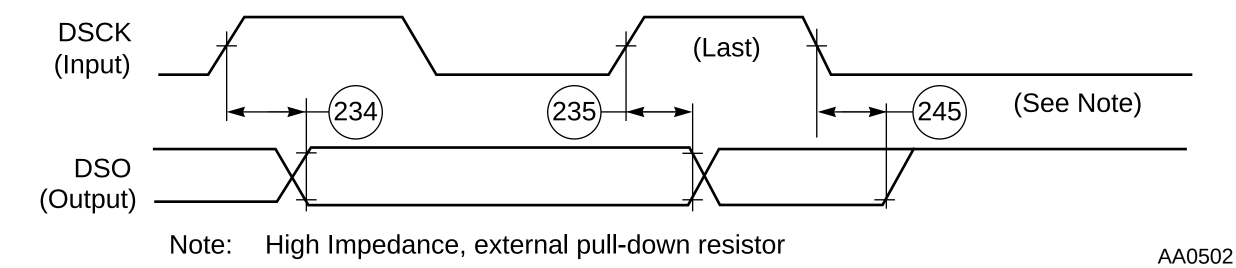


Figure 2-30 OnCE Read Timing

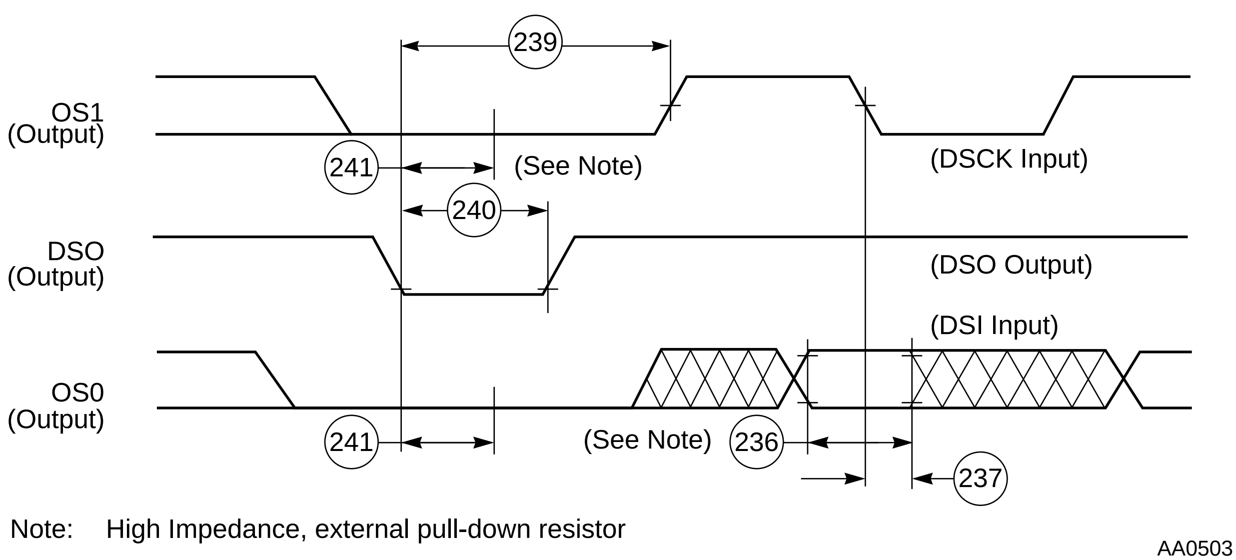


Figure 2-31 OnCE Data I/O To Status Timing

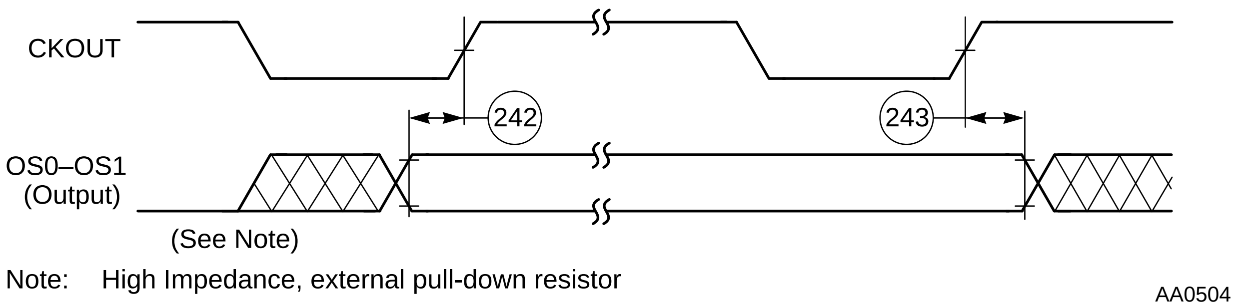


Figure 2-32 OnCE CKOUT To Status Timing

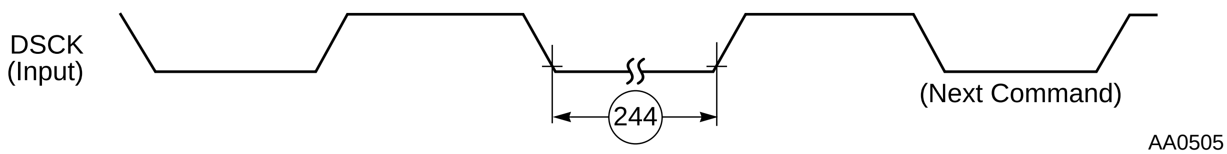


Figure 2-33 OnCE Read Register to Next Command Timing

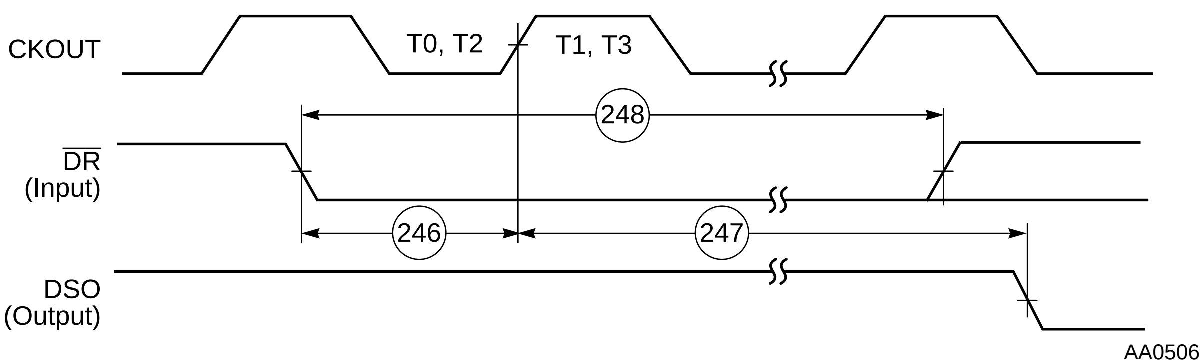


Figure 2-34 Synchronous Recovery from Wait State

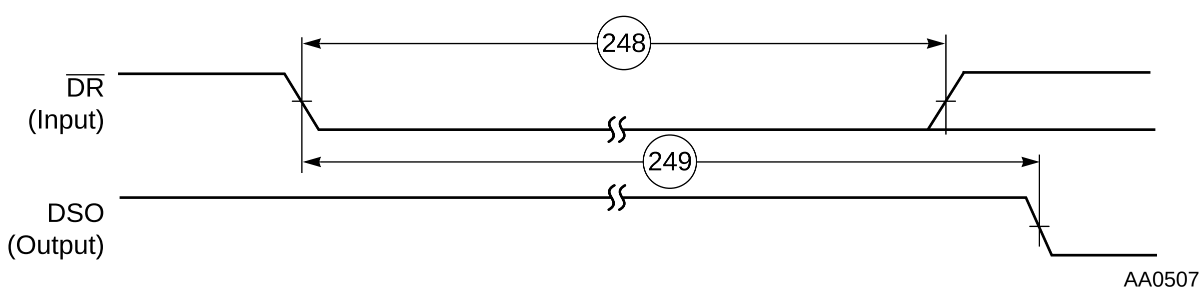


Figure 2-35 Asynchronous Recovery from Wait State

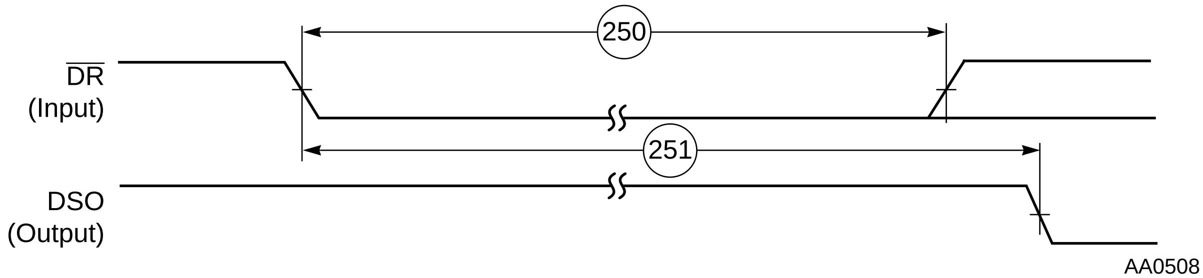


Figure 2-36 Asynchronous Recovery from Stop State

TIMER TIMING

C_L = 50 pF + 2 TTL loads

Table 2-16 Timer Timing

Num	Characteristics	Min	Max	Unit
260	TIO Low	$2T_C + 7$	—	ns
261	TIO High	$2T_C + 7$	—	ns
262	Synchronous Timer Setup Time from TIO (input) Assertion to CKOUT Rising Edge	10	T_C	ns
263	Synchronous Timer Delay Time from CKOUT Rising Edge to the External Memory Access Address Out Valid Caused by First Interrupt Instruction Execution	$5T_C + T_H$	—	ns
264	CKOUT Rising Edge to TIO (output) Assertion	0	8	ns
265	CKOUT Rising Edge to TIO (output) Deassertion	0	8	ns
266	CKOUT Rising Edge to TIO (General Purpose Output)	0	8	ns

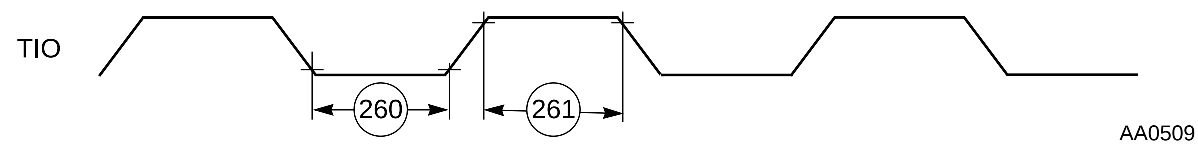


Figure 2-37 TIO Timer Event Input

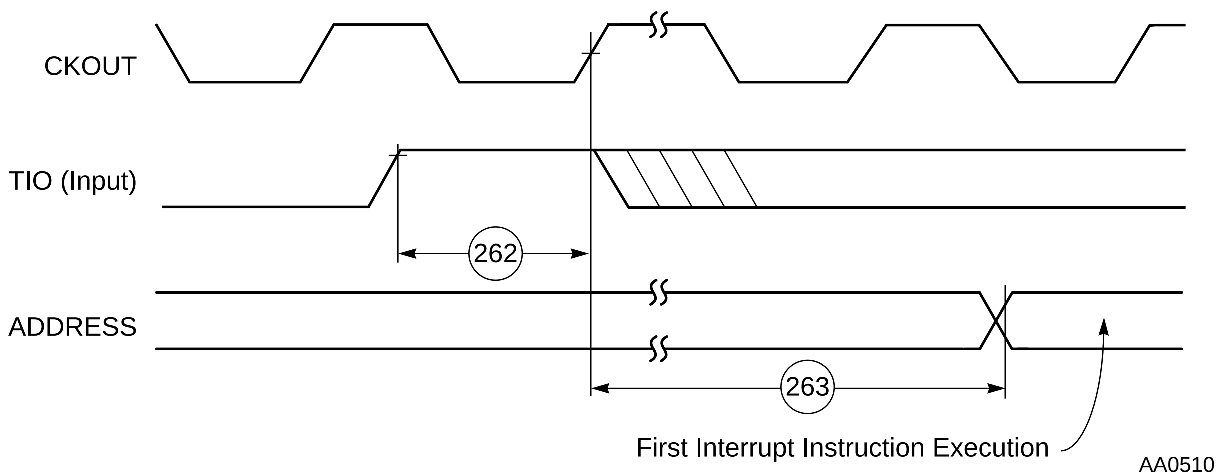


Figure 2-38 Timer Interrupt Generation

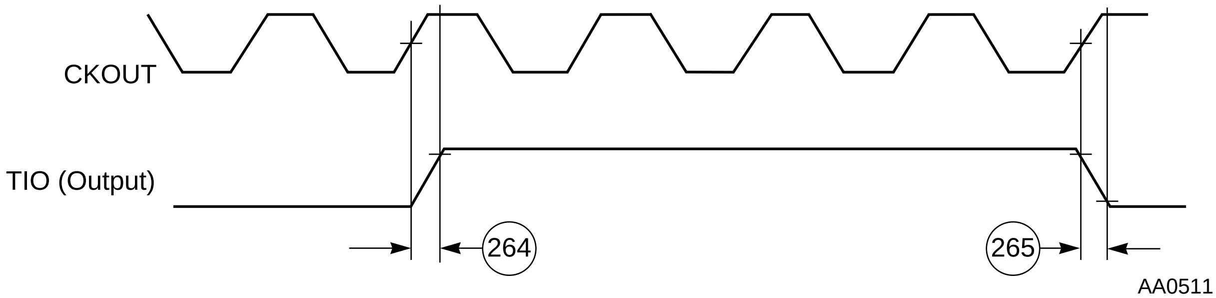


Figure 2-39 External Pulse Generation

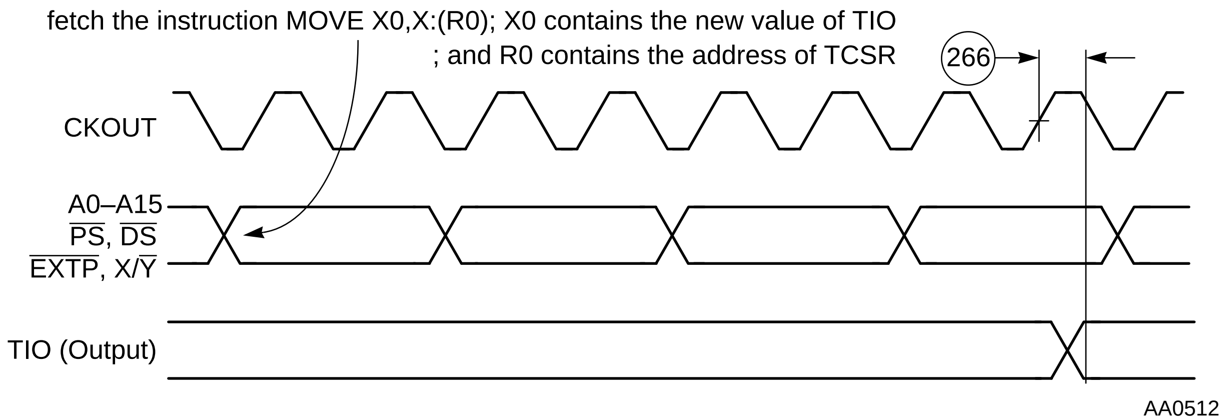


Figure 2-40 GPIO Output Timing

SECTION 3

PACKAGING

PIN-OUT AND PACKAGE INFORMATION

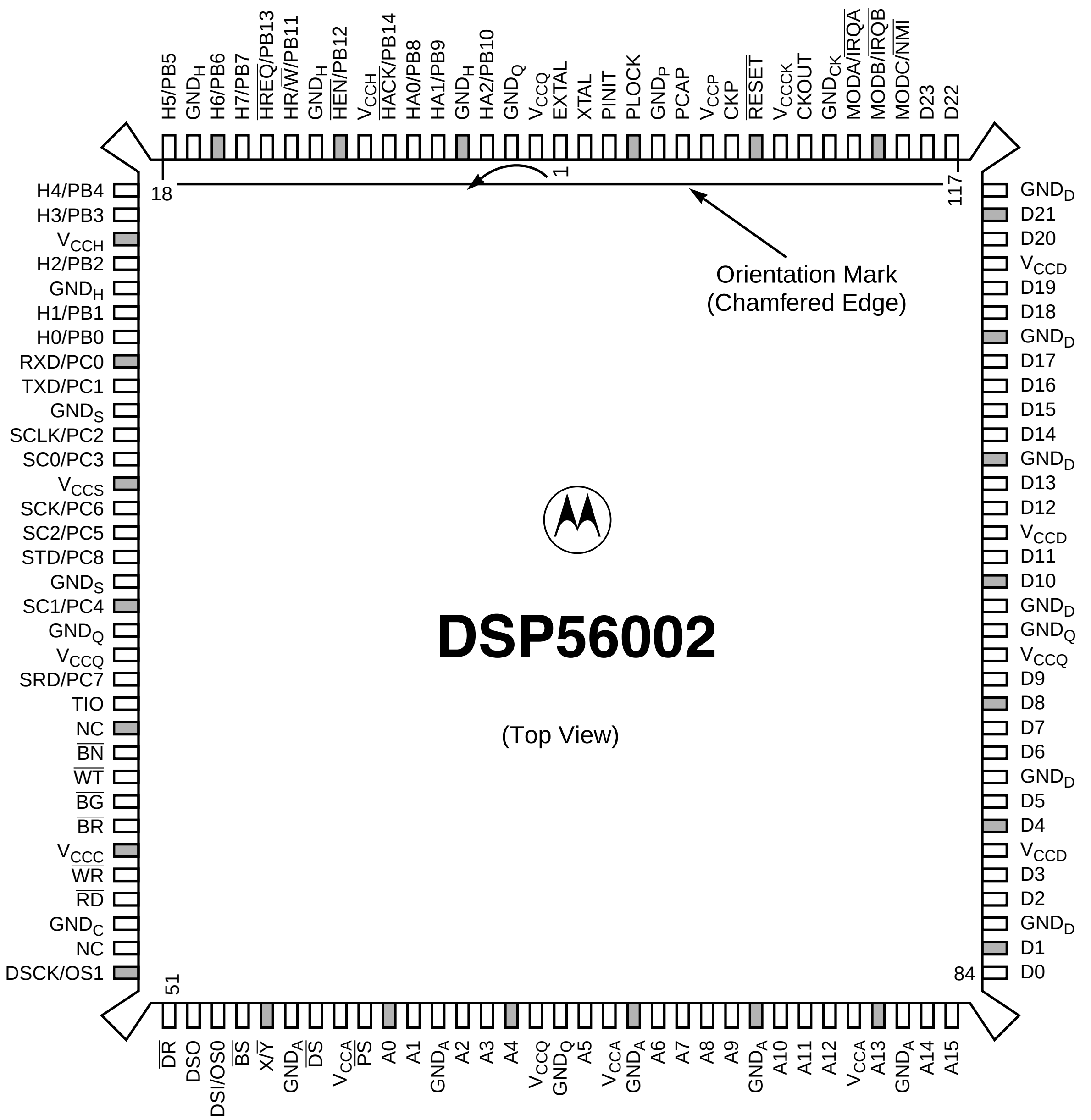
This sections provides information about the available packages for this product, including diagrams of the package pinouts and tables describing how the signals described in **Section 1** are allocated for each package.

The DSP56002 is available in three package types:

- 132-pin Plastic Quad Flat Pack (PQFP)
- 144-pin Thin Quad Flat Pack (TQFP)
- 132-pin Ceramic Pin Grid Array (PGA)

PQFP Package Description

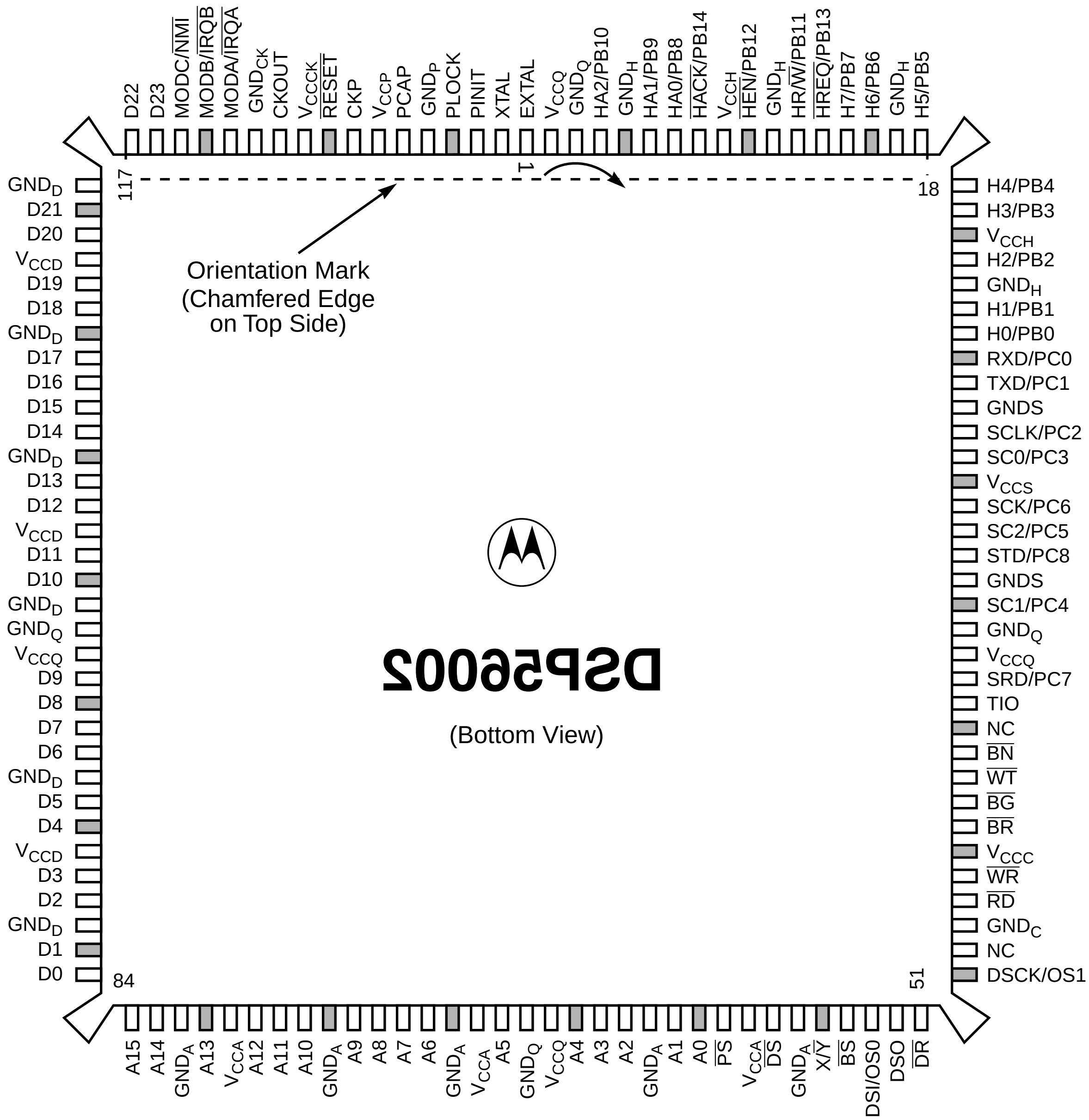
Top and bottom views of the PQFP package are shown in **Figure 3-1** and **Figure 3-2** with their pin-outs.



Note: 1. "NC" are No Connection pins that are reserved for possible future enhancements. Do not connect these pins to any power, ground, signal traces, or vias.
2. An $\overline{\text{OVERBAR}}$ indicates the signal is asserted when the voltage = ground (active low).
3. To simplify locating the pins, each fifth pin is shaded in the illustration.

AA0611

Figure 3-1 Top View of the 132-pin Plastic Quad Flat Pack (PQFP) Package



Note:
1. "NC" are No Connection pins that are reserved for possible future enhancements. Do not connect these pins to any power, ground, signal traces, or vias.
2. An OVERBAR indicates the signal is asserted when the voltage = ground (active low).
3. To simplify locating the pins, each fifth pin is shaded in the illustration.

AA0612

Figure 3-2 Bottom View of the 132-pin Plastic Quad Flat Pack (PQFP) Package

The DSP56002 signals that may be programmed as General Purpose I/O are listed with their primary function in **Table 3-9**.

Table 3-1 DSP56002 General Purpose I/O Pin Identification in PQFP Package

Pin Number	Primary Function	Port	GPIO ID
24	H0	B	PB0
23	H1		PB1
21	H2		PB2
19	H3		PB3
18	H4		PB4
17	H5		PB5
15	H6		PB6
14	H7		PB7
7	HA0		PB8
6	HA1		PB9
4	HA2		PB10
12	$\overline{\text{HR/W}}$		PB11
10	$\overline{\text{HEN}}$		PB12
13	$\overline{\text{HREQ}}$		PB13
8	$\overline{\text{HACK}}$		PB14
25	RXD	C	PC0
26	TXD		PC1
28	SCLK		PC2
29	SC0		PC3
35	SC1		PC4
32	SC2		PC5
31	SCK		PC6
38	SRD		PC7
33	STD		PC8
39	TIO	No port assigned	

Table 3-2 DSP56002 Signal Identification by PQFP Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	EXTAL	26	TXD / PC1	51	DR
2	V_{CCQ}	27	GND_S	52	DSO
3	GND_Q	28	SCLK / PC2	53	DSI / OS0
4	HA2 / PB10	29	SC0 / PC3	54	BS
5	GND_H	30	V_{CCS}	55	X / $\overline{\text{Y}}$
6	HA1 / PB9	31	SCK / PC6	56	GND_A
7	HA0 / PB8	32	SC2 / PC5	57	DS
8	$\overline{\text{HACK}}$ / PB14	33	STD / PC8	58	V_{CCA}
9	V_{CCH}	34	GND_S	59	PS
10	$\overline{\text{HEN}}$ / PB12	35	SC1 / PC4	60	A0
11	GND_H	36	GND_Q	61	A1
12	HR / $\overline{\text{W}}$ / PB11	37	V_{CCQ}	62	GND_A
13	$\overline{\text{HREQ}}$ / PB13	38	SRD / PC7	63	A2
14	H7 / PB7	39	TIO*	64	A3
15	H6 / PB6	40	NC	65	A4
16	GND_H	41	BN	66	V_{CCQ}
17	H5 / PB5	42	WT	67	GND_Q
18	H4 / PB4	43	BG	68	A5
19	H3 / PB3	44	BR	69	V_{CCA}
20	V_{CCH}	45	V_{CCC}	70	GND_A
21	H2 / PB2	46	WR	71	A6
22	GND_H	47	RD	72	A7
23	H1 / PB1	48	GND_C	73	A8
24	H0 / PB0	49	NC	74	A9
25	RXD / PC0	50	DSCK / OS1	75	GND_A

Table 3-2 DSP56002 Signal Identification by PQFP Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
76	A10	95	D8	114	D20
77	A11	96	D9	115	D21
78	A12	97	V_{CCQ}	116	GND_D
79	V_{CCA}	98	GND_Q	117	D22
80	A13	99	GND_D	118	D23
81	GND_A	100	D10	119	MODC / $\overline{\text{NMI}}$
82	A14	101	D11	120	MODB / $\overline{\text{IRQB}}$
83	A15	102	V_{CCD}	121	MODA / $\overline{\text{IRQA}}$
84	D0	103	D12	122	GND_{CK}
85	D1	104	D13	123	CKOUT
86	GND_D	105	GND_D	124	V_{CCCK}
87	D2	106	D14	125	RESET
88	D3	107	D15	126	CKP
89	V_{CCD}	108	D16	127	V_{CCP}
90	D4	109	D17	128	PCAP
91	D5	110	GND_D	129	GND_P
92	GND_D	111	D18	130	PLOCK
93	D6	112	D19	131	PINIT
94	D7	113	V_{CCD}	132	XTAL

Note:
1. "NC" are No Connection pins that are reserved for possible future enhancements. Do not connect these pins to any power, ground, signal traces, or vias.
2. An $\overline{\text{OVERBAR}}$ indicates the signal is asserted when the voltage = ground (active low).

Table 3-3 DSP56002 PQFP Pin Identification by Signal Name

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
A0	60	D3	114	DSO	52
A1	61	D4	116	EXTAL	1
A2	63	D5	117	GND_A	56
A3	64	D6	119	GND_A	62
A4	65	D7	94	GND_A	70
A5	68	D8	95	GND_A	75
A6	71	D9	96	GND_A	81
A7	72	D10	100	GND_C	48
A8	73	D11	101	GND_{CK}	122
A9	74	D12	103	GND_D	86
A10	76	D13	104	GND_D	92
A11	77	D14	106	GND_D	99
A12	78	D15	107	GND_D	105
A13	80	D16	108	GND_D	110
A14	82	D17	109	GND_D	116
A15	83	D18	111	GND_H	5
$\overline{BG}$	43	D19	112	GND_H	11
$\overline{BN}$	41	D20	114	GND_H	16
$\overline{BR}$	44	D21	115	GND_H	22
$\overline{BS}$	54	D22	117	GND_P	129
CKOUT	123	D23	118	GND_Q	3
CKP	126	$\overline{DR}$	51	GND_Q	36
D0	84	$\overline{DS}$	57	GND_Q	67
D1	85	DSCK	50	GND_Q	98
D2	87	DSI	53	GND_S	27

Table 3-3 DSP56002 PQFP Pin Identification by Signal Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
$\mathrm{GND_S}$	34	PB1	23	PLOCK	130
H0	24	PB2	21	$\overline{\mathrm{PS}}$	59
H1	23	PB3	19	$\overline{\mathrm{RD}}$	47
H2	21	PB4	18	$\overline{\mathrm{RESET}}$	125
H3	19	PB5	17	RXD	25
H4	18	PB6	15	SC0	29
H5	17	PB7	14	SC1	35
H6	15	PB8	7	SC2	32
H7	14	PB9	6	SCK	31
HA0	7	PB10	4	$\overline{\mathrm{SCLK}}$	28
HA1	6	PB11	12	SRD	38
HA2	4	PB12	10	STD	33
$\overline{\mathrm{HACK}}$	8	PB13	13	TIO	39
$\overline{\mathrm{HEN}}$	10	PB14	8	TXD	26
$\mathrm{HR}/\overline{\mathrm{W}}$	12	PC0	25	$\mathrm{V_{CCA}}$	58
$\overline{\mathrm{HREQ}}$	13	PC1	26	$\mathrm{V_{CCA}}$	69
$\overline{\mathrm{IRQA}}$	121	PC2	28	$\mathrm{V_{CCA}}$	79
$\overline{\mathrm{IRQB}}$	120	PC3	29	$\mathrm{V_{CCC}}$	45
MODA	121	PC4	35	$\mathrm{V_{CCCK}}$	124
MODB	120	PC5	32	$\mathrm{V_{CCD}}$	89
MODC	119	PC6	31	$\mathrm{V_{CCD}}$	102
$\overline{\mathrm{NMI}}$	119	PC7	38	$\mathrm{V_{CCD}}$	113
OS0	53	PC8	33	$\mathrm{V_{CCH}}$	9
OS1	50	PCAP	128	$\mathrm{V_{CCH}}$	20
PB0	24	PINIT	131	$\mathrm{V_{CCP}}$	127
$\mathrm{V_{CCQ}}$	2	$\mathrm{V_{CCS}}$	30	XTAL	132
$\mathrm{V_{CCQ}}$	37	$\overline{\mathrm{WR}}$	46	nc	40
$\mathrm{V_{CCQ}}$	66	$\overline{\mathrm{WT}}$	42	nc	49
$\mathrm{V_{CCQ}}$	97	$\mathrm{X}/\overline{\mathrm{Y}}$	55		

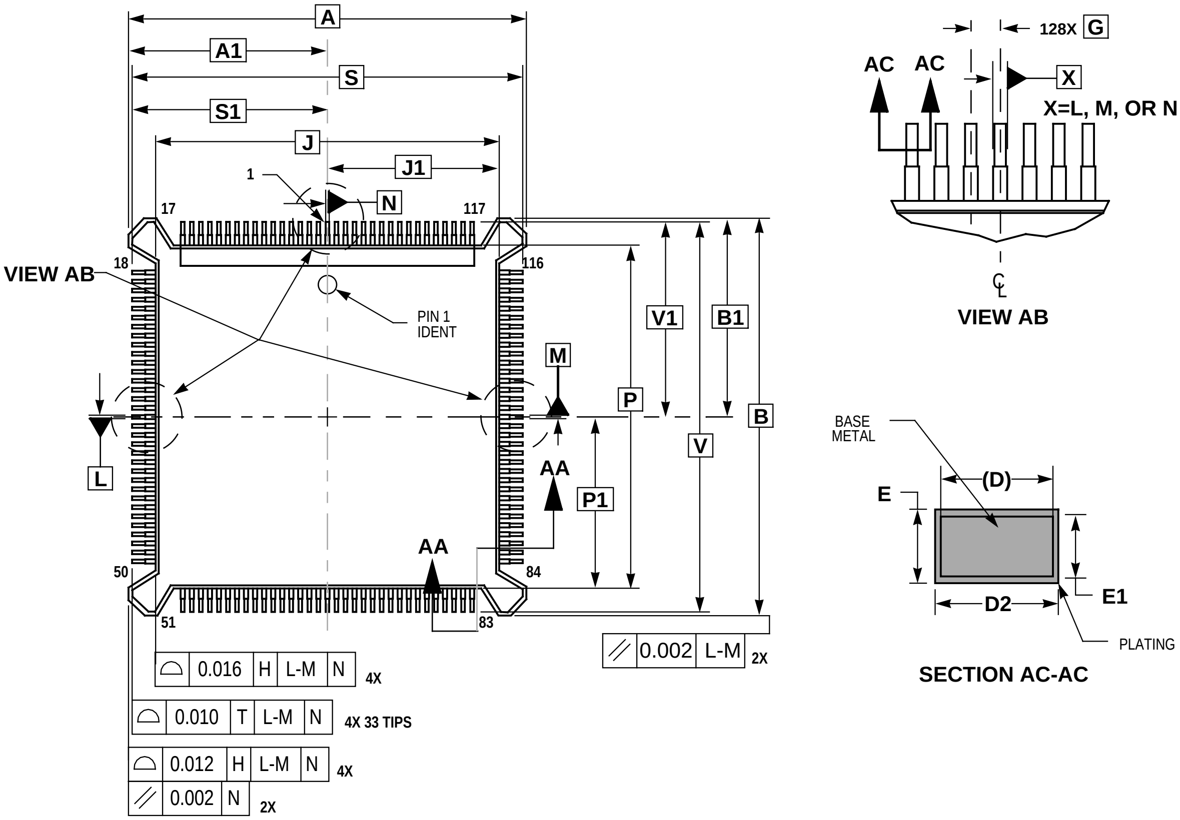
Power and ground pins have special considerations for noise immunity. See **Section 4 Design Considerations**.

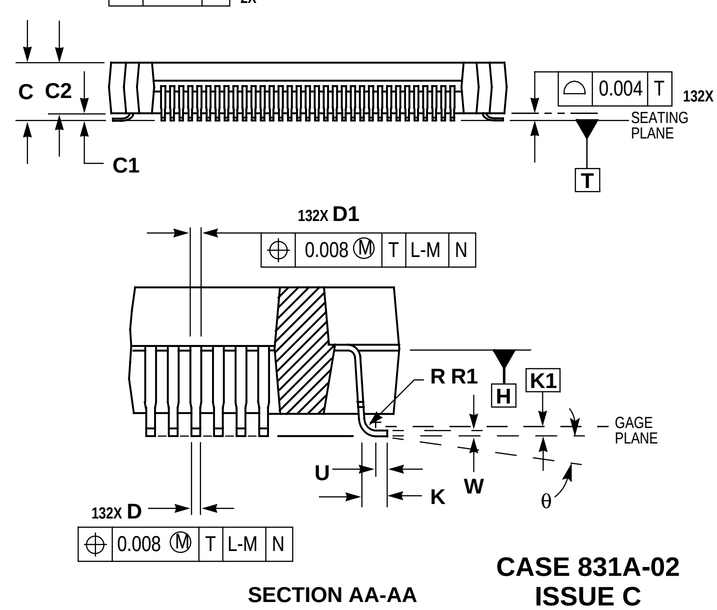
Table 3-4 DSP56002 Power Supply Pins in PQFP Package

Pin Number	Power Supply	Circuit Supplied
58	V_{CCA}	Address Bus Buffers
69		
79		
56	GND_A	
62		
70		
75		
81		
45	V_{CCC}	Bus Control Buffers
48	GND_C	
124	V_{CCCK}	Clock
122	GND_{CK}	
89	V_{CCD}	Data Bus Buffers
102		
113		
86	GND_D	
92		
99		
105		
110		
116		
9	V_{CCH}	Host Interface Buffers
20		
5	GND_H	
11		
16		
22		

Table 3-4 DSP56002 Power Supply Pins in PQFP Package (Continued)

Pin Number	Power Supply	Circuit Supplied
2	V_{CCQ}	Internal Logic
37		
66		
97		
3	GND_Q	
36		
67		
98		
127	V_{CCP}	PLL
129	GND_P	
30	V_{CCS}	Serial Port
27	GND_S	
34		





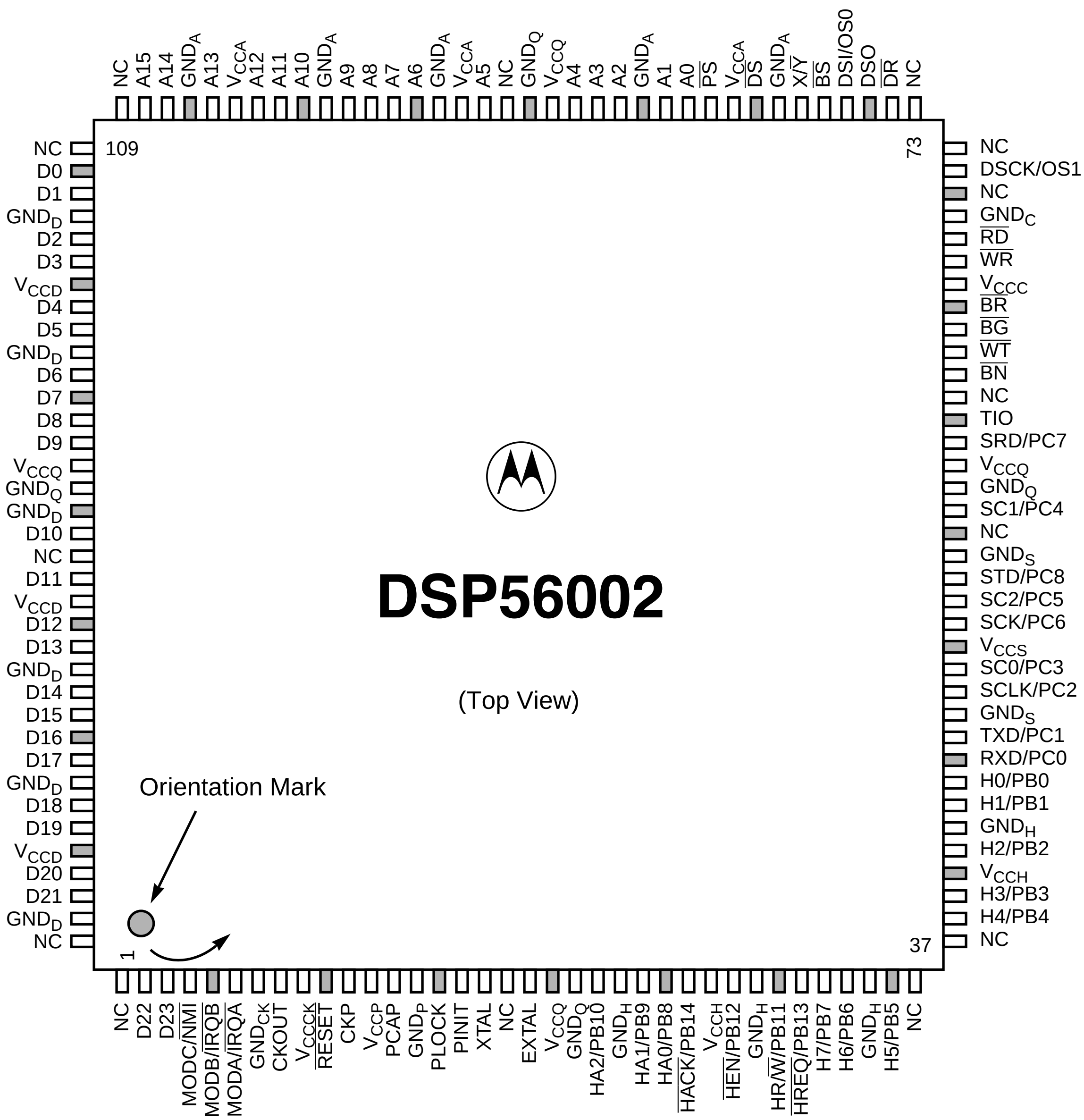
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1982.
2. DIMENSIONS IN INCHES.
3. DIMENSIONS A, B, J, AND P DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION FOR DIMENSIONS A AND B IS 0.007, FOR DIMENSIONS J AND P IS 0.010.
4. DATUM PLANE H IS LOCATED AT THE UNDERSIDE OF LEADS WHERE LEADS EXIT PACKAGE BODY.
5. DATUMS L, M, AND N TO BE DETERMINED WHERE CENTER LEADS EXIT PACKAGE BODY AT DATUM H.
6. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
7. DIMENSIONS A, B, J, AND P TO BE DETERMINED AT DATUM PLANE H.
8. DIMENSION F DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.019.

	INCHES	
DIM	MIN	MAX
A	1.100 BSC	
A1	0.550 BSC	
B	1.100 BSC	
B1	0.550 BSC	
C	0.160	0.180
C1	0.020	0.040
C2	0.135	0.145
D	0.008	0.012
D1	0.012	0.016
D2	0.008	0.011
E	0.006	0.008
E1	0.005	0.007
F	0.014	0.014
G	0.025 BSC	
J	0.950 BSC	
J1	0.475 BSC	
K	0.034	0.044
K1	0.010 BSC	
P	0.950 BSC	
P1	0.475 BSC	
R1	0.013 REF	
S	1.080 BSC	
S1	0.540 BSC	
U	0.025 REF	
V	1.080 BSC	
V1	0.540 BSC	
W	0.006	0.008
θ	0 °	8°

Figure 3-3 132-Pin Plastic Quad Flat Pack (PQFP) Mechanical Information

TQFP Package Description

Top and bottom views of the TQFP package are shown in **Figure 3-4** and **Figure 3-5** with their pin-outs.



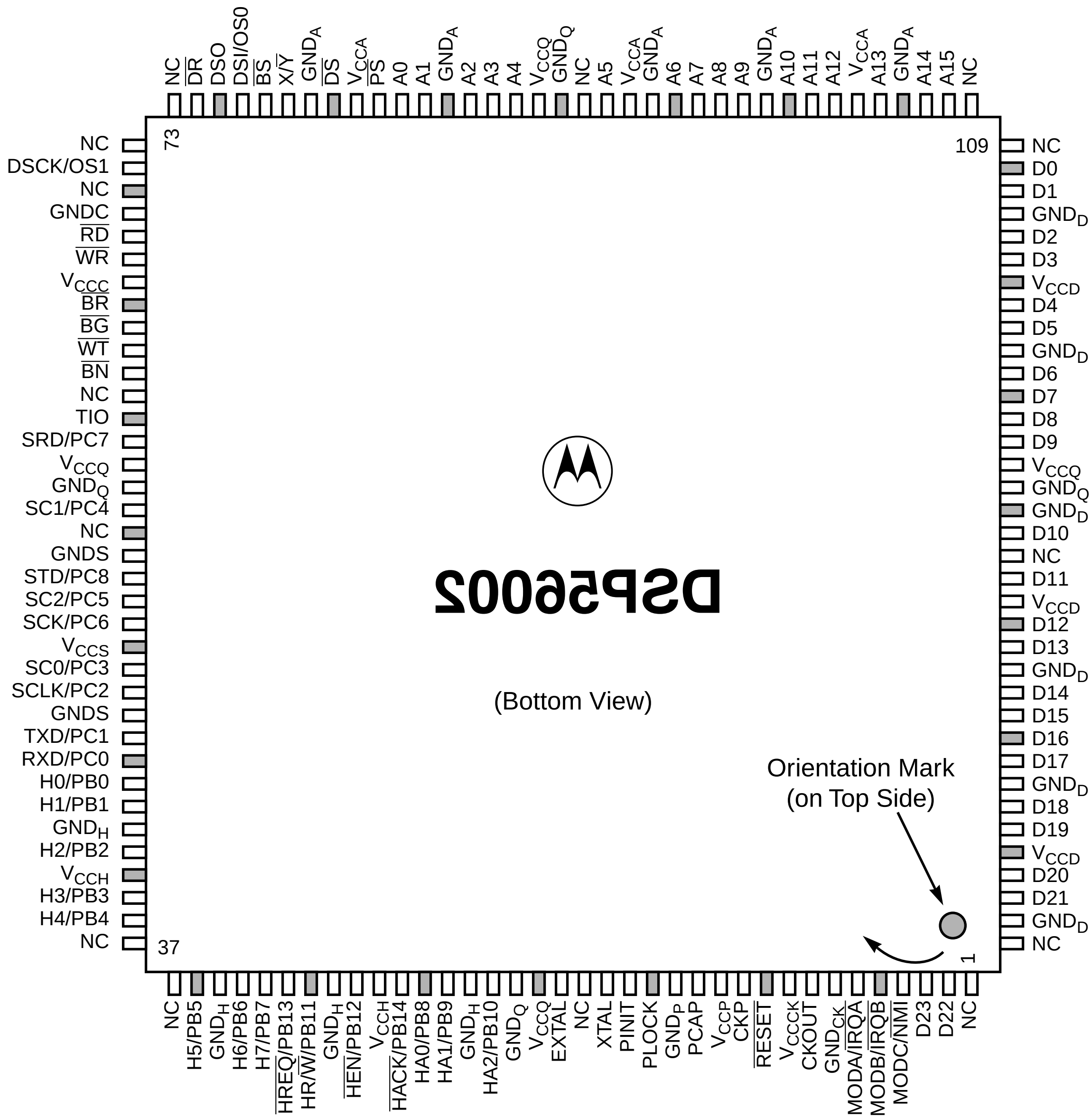
Note: 1. "NC" are No Connection pins that are reserved for possible future enhancements. Do not connect these pins to any power, ground, signal traces, or vias.

2. An $\overline{\text{OVERBAR}}$ indicates the signal is asserted when the voltage = ground (active low).

3. To simplify locating the pins, each fifth pin is shaded in the illustration.

AA0613

Figure 3-4 Top View of the 144-pin Thin Quad Flat Pack (TQFP) Package



Note:
1. “NC” are No Connection pins that are reserved for possible future enhancements. Do not connect these pins to any power, ground, signal traces, or vias.
2. An OVERBAR indicates the signal is asserted when the voltage = ground (active low).
3. To simplify locating the pins, each fifth pin is shaded in the illustration.

AA0614

Figure 3-5 Bottom View of the144-pin Thin Quad Flat Pack (TQFP) Package

The DSP56002 signals that may be programmed as General Purpose I/O are listed with their primary function in **Table 3-9**.

Table 3-5 DSP56002 General Purpose I/O Pin Identification in TQFP Package

Pin Number	Primary Function	Port	GPIO ID
44	H0	B	PB0
43	H1		PB1
41	H2		PB2
39	H3		PB3
38	H4		PB4
35	H5		PB5
33	H6		PB6
32	H7		PB7
25	HA0		PB8
24	HA1		PB9
22	HA2		PB10
30	$\overline{\text{HR/W}}$		PB11
28	$\overline{\text{HEN}}$		PB12
31	$\overline{\text{HREQ}}$		PB13
26	$\overline{\text{HACK}}$		PB14
45	RXD	C	PC0
46	TXD		PC1
48	SCLK		PC2
49	SC0		PC3
56	SC1		PC4
52	SC2		PC5
51	SCK		PC6
59	SRD		PC7
53	STD		PC8
60	TIO	No port assigned	

Table 3-6 DSP56002 Signal Identification by TQFP Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	NC	26	$\overline{\text{HACK}}$ / PB14	51	SCK / PC6
2	D22	27	V_{CCH}	52	SC2 / PC5
3	D23	28	$\overline{\text{HEN}}$ / PB12	53	STD / PC8
4	MODC / $\overline{\text{NMI}}$	29	GND_H	54	GND_S
5	MODB / $\overline{\text{IRQB}}$	30	HR / $\overline{\text{W}}$ / PB11	55	NC
6	MODA / $\overline{\text{IRQA}}$	31	$\overline{\text{HREQ}}$ / PB13	56	SC1 / PC4
7	GND_{CK}	32	H7 / PB7	57	GND_Q
8	CKOUT	33	H6 / PB6	58	V_{CCQ}
9	V_{CCCK}	34	GND_H	59	SRD / PC7
10	RESET	35	H5 / PB5	60	TIO
11	CKP	36	NC	61	NC
12	V_{CCP}	37	NC	62	BN
13	PCAP	38	H4 / PB4	63	WT
14	GND_P	39	H3 / PB3	64	BG
15	PLOCK	40	V_{CCH}	65	BR
16	PINIT	41	H2 / PB2	66	V_{CCC}
17	XTAL	42	GND_H	67	WR
18	NC	43	H1 / PB1	68	RD
19	EXTAL	44	H0 / PB0	69	GND_C
20	V_{CCQ}	45	RXD / PC0	70	NC
21	GND_Q	46	TXD / PC1	71	DSCK / OS1
22	HA2 / PB10	47	GND_S	72	NC
23	GND_H	48	SCLK / PC2	73	NC
24	HA1 / PB9	49	SC0 / PC3	74	DR
25	HA0 / PB8	50	V_{CCS}	75	DSO

Table 3-6 DSP56002 Signal Identification by TQFP Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
76	DSI / OS0	99	GND_A	122	D9
77	BS	100	A10	123	V_{CCQ}
78	X / $\overline{Y}$	101	A11	124	GND_Q
79	GND_A	102	A12	125	GND_D
80	DS	103	V_{CCA}	126	D10
81	V_{CCA}	104	A13	127	NC
82	PS	105	GND_A	128	D11
83	A0	106	A14	129	V_{CCD}
84	A1	107	A15	130	D12
85	GND_A	108	NC	131	D13
86	A2	109	NC	132	GND_D
87	A3	110	D0	133	D14
88	A4	111	D1	134	D15
89	V_{CCQ}	112	GND_D	135	D16
90	GND_Q	113	D2	136	D17
91	NC	114	D3	137	GND_D
92	A5	115	V_{CCD}	138	D18
93	V_{CCA}	116	D4	139	D19
94	GND_A	117	D5	140	V_{CCD}
95	A6	118	GND_D	141	D20
96	A7	119	D6	142	D21
97	A8	120	D7	143	GND_D
98	A9	121	D8	144	NC

Note: 1. "NC" are No Connection pins that are reserved for possible future enhancements. Do not connect these pins to any power, ground, signal traces, or vias.
2. An $\overline{\text{OVERBAR}}$ indicates the signal is asserted when the voltage = ground (active low).

Table 3-7 DSP56002 TQFP Pin Identification by Signal Name

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
A0	83	D3	114	DSO	75
A1	84	D4	116	EXTAL	19
A2	86	D5	117	GND_A	79
A3	87	D6	119	GND_A	85
A4	88	D7	120	GND_A	94
A5	92	D8	121	GND_A	99
A6	95	D9	122	GND_A	105
A7	96	D10	126	GND_C	69
A8	97	D11	128	GND_{CK}	7
A9	98	D12	130	GND_D	112
A10	100	D13	131	GND_D	118
A11	101	D14	133	GND_D	125
A12	102	D15	134	GND_D	132
A13	104	D16	135	GND_D	137
A14	106	D17	136	GND_D	143
A15	107	D18	138	GND_H	23
$\overline{BG}$	64	D19	139	GND_H	29
$\overline{BN}$	62	D20	141	GND_H	34
$\overline{BR}$	65	D21	142	GND_H	42
$\overline{BS}$	77	D22	2	GND_P	14
CKOUT	8	D23	3	GND_Q	21
CKP	11	$\overline{DR}$	74	GND_Q	57
D0	110	$\overline{DS}$	80	GND_Q	90
D1	111	DSCK	71	GND_Q	124
D2	113	DSI	76	GND_S	47

Table 3-7 DSP56002 TQFP Pin Identification by Signal Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
GND_S	54	PB1	43	PLOCK	15
H0	44	PB2	41	$\overline{PS}$	82
H1	43	PB3	39	$\overline{RD}$	68
H2	41	PB4	38	$\overline{RESET}$	10
H3	39	PB5	35	RXD	45
H4	38	PB6	33	SC0	49
H5	35	PB7	32	SC1	56
H6	33	PB8	25	SC2	52
H7	32	PB9	24	SCK	51
HA0	25	PB10	22	SCLK	48
HA1	24	PB11	30	SRD	59
HA2	22	PB12	28	STD	53
$\overline{HACK}$	26	PB13	31	TIO	60
$\overline{HEN}$	28	PB14	26	TXD	46
HR/$\overline{W}$	30	PC0	45	V_{CCA}	81
$\overline{HREQ}$	31	PC1	46	V_{CCA}	93
$\overline{IRQA}$	6	PC2	48	V_{CCA}	103
$\overline{IRQB}$	5	PC3	49	V_{CCC}	66
MODA	6	PC4	56	V_{CCCK}	9
MODB	5	PC5	52	V_{CCD}	115
MODC	4	PC6	51	V_{CCD}	129
$\overline{NMI}$	4	PC7	59	V_{CCD}	140
OS0	76	PC8	53	V_{CCH}	27
OS1	71	PCAP	13	V_{CCH}	40
PB0	44	PINIT	16	V_{CCP}	12

Table 3-7 DSP56002 TQFP Pin Identification by Signal Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
V_{CCQ}	20	XTAL	17	nc	72
V_{CCQ}	58	nc	70	nc	73
V_{CCQ}	89	nc	1	nc	91
V_{CCQ}	123	nc	18	nc	108
V_{CCS}	50	nc	36	nc	109
$\overline{WR}$	67	nc	37	nc	127
$\overline{WT}$	63	nc	55	nc	144
$X/\overline{Y}$	78	nc	61		

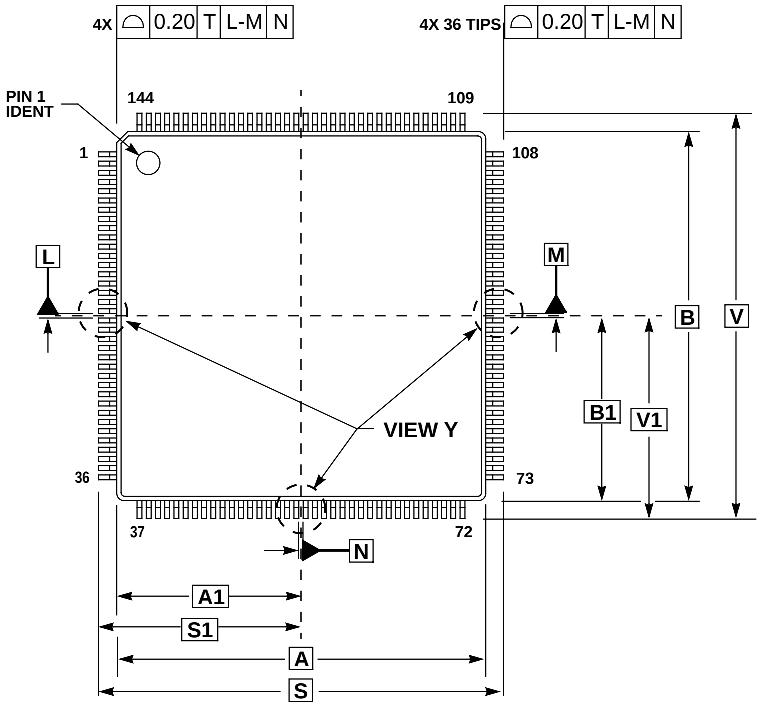
Power and ground pins have special considerations for noise immunity. See the section **Design Considerations**.

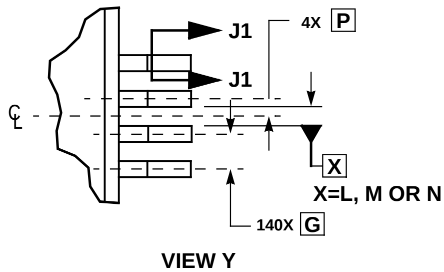
Table 3-8 DSP56002 Power Supply Pins in TQFP Package

Pin Number	Power Supply	Circuit Supplied
81	V_{CCA}	Address Bus Buffers
93		
103		
79	GND_A	
85		
94		
99		
105		
66	V_{CCC}	Bus Control Buffers
69	GND_C	
9	V_{CCCK}	Clock
7	GND_{CK}	
115	V_{CCD}	Data Bus Buffers
129		
140		
112	GND_D	
118		
125		
132		
137		
143		
27	V_{CCH}	Host Interface Buffers
40		
23	GND_H	
29		
34		
42		

Table 3-8 DSP56002 Power Supply Pins in TQFP Package (Continued)

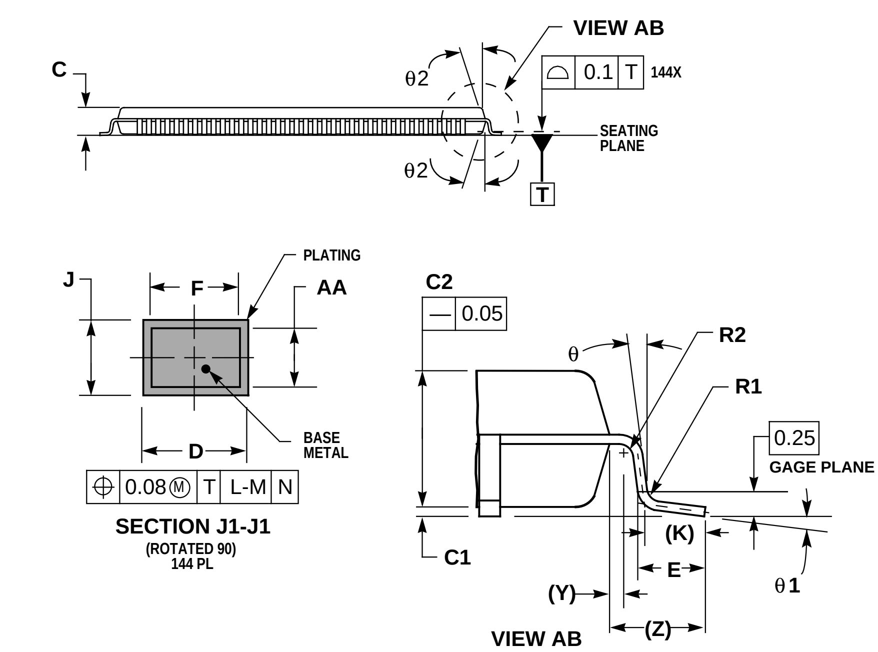
Pin Number	Power Supply	Circuit Supplied
20	V_{CCQ}	Internal Logic
58		
89		
123		
21	GND_Q	
57		
90		
124		
12	V_{CCP}	PLL
14	GND_P	
50	V_{CCS}	Serial Port
47	GND_S	
54		





NOTES:

9. DIMENSIONS AND TOLERANCING PER ASME Y14.5, 1994.
10. DIMENSIONS IN MILLIMETERS.
11. DATUMS L, M AND N TO BE DETERMINED AT THE SEATING PLANE, DATUM T.
12. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
13. DIMENSIONS A AND B DO NOT INCULDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
14. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLED DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.35.



DIM	MILLIMETERS	
	MIN	MAX
A	20.00 BSC	
A1	10.00 BSC	
B	20.00 BSC	
B1	10.00 BSC	
C	1.40	1.60
C1	0.05	0.15
C2	1.35	1.45
D	0.17	0.27
E	0.45	0.75
F	0.17	0.23
G	0.50 BSC	
J	0.09	0.20
K	0.50 REF	
P	0.25 BSC	
R1	0.13	0.20
R2	0.13	0.20
S	22.00 BSC	
S1	11.00 BSC	
V	22.00 BSC	
V1	11.00 BSC	
Y	0.25 REF	
Z	1.00 REF	
AA	0.09	0.16
θ	0°	
θ1	0°	7°
θ2	11°	13°

CASE 918-03
ISSUE C

Figure 3-6 144-pin Thin Plastic Quad Flat Pack (TQFP) Mechanical Information

PGA Package Description

Top and bottom views of the PGA package are shown in **Figure 3-7** and **Figure 3-8** with their pin-outs.

Orientation Mark

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	GND$_Q$	V$_{CCQ}$	GND$_Q$	V$_{CCQ}$	GND$_Q$	V$_{CCQ}$	GND$_Q$	V$_{CCQ}$	HA2	$\overline{\text{HACK}}$	H6	GND$_H$	GND$_H$
B	GND$_D$	V$_{CCCK}$	$\overline{\text{RESET}}$	CKP	V$_{CCP}$	PCAP	PLOCK	XTAL	HA1	$\overline{\text{HEN}}$	H7	H5	V$_{CCH}$
C	V$_{CCD}$	MODB/$\overline{\text{IRQB}}$	MODA/$\overline{\text{IRQA}}$	GND$_{CK}$	CKOUT	GND$_P$	PINIT	EXTAL	HA0	$\overline{\text{HREQ}}$	H2	RXD	GND$_H$
D	GND$_D$	D20	D21	D23	MODC/$\overline{\text{NMI}}$				HR/$\overline{\text{W}}$	H4	H1	TXD	V$_{CCH}$
E	GND$_D$	D18	D19	D22						H3	H0	SCLK	GND$_H$
F	D15	D16	D17								SC0	SCK	SC2
G	D14	D13	D12								STD	SC1	SRD
H	D11	D10	D9								TIO	NC	$\overline{\text{BN}}$
J	V$_{CCD}$	D8	D7	A15						$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{WT}}$	GNDS
K	GND$_D$	D6	D5	A14	A11				A0	X/$\overline{\text{Y}}$	$\overline{\text{DR}}$	$\overline{\text{BG}}$	V$_{CCS}$
L	GND$_D$	D4	D3	A13	A10	A8	A6	A3	A1	$\overline{\text{DS}}$	DSO	$\overline{\text{BR}}$	GNDS
M	V$_{CCD}$	D2	D1	A12	A9	A7	A5	A4	A2	$\overline{\text{PS}}$	DSI/OS0	NC	V$_{CCC}$
N	GND$_D$	D0	GND$_A$	V$_{CCA}$	GND$_A$	GND$_A$	V$_{CCA}$	GND$_A$	V$_{CCA}$	GND$_A$	$\overline{\text{BS}}$	DSCK/OS1	GNDC

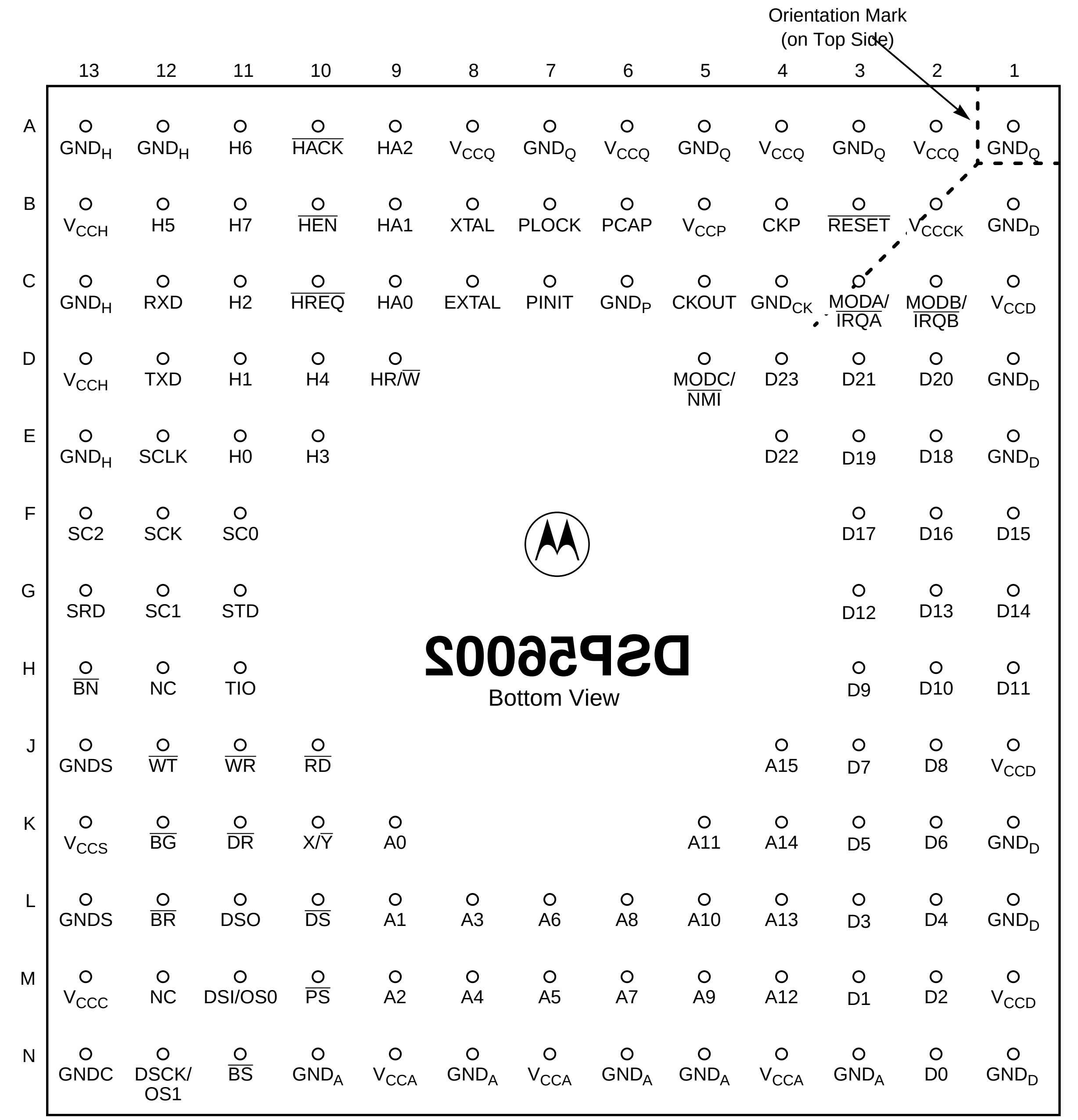
DSP56002

Top View

Note: 1. "NC" are No Connection pins that are reserved for possible future enhancements. Do not connect these pins to any power, ground, signal traces, or vias.
2. An $\overline{\text{OVERBAR}}$ indicates the signal is asserted when the voltage = ground (active low).

AA0615

Figure 3-7 Top View of the 132-pin Ceramic (RC) 13 ×13 Pin Grid Array Package



Note: 1. “NC” are No Connection pins that are reserved for possible future enhancements. Do not connect these pins to any power, ground, signal traces, or vias.

2. An $\overline{\text{OVERBAR}}$ indicates the signal is asserted when the voltage = ground (active low).

AA0616

Figure 3-8 Bottom View of the 132-pin Ceramic (RC) 13 ×13 Pin Grid Array Package

The DSP56008 signals that may be programmed as General Purpose I/O are listed with their primary function in **Table 3-9**.

Table 3-9 DSP56002 General Purpose I/O Pin Identification in PGA Package

Pin Number	Primary Function	Port	GPIO ID
E11	H0	B	PB0
D11	H1		PB1
C11	H2		PB2
E10	H3		PB3
D10	H4		PB4
B12	H5		PB5
A11	H6		PB6
B11	H7		PB7
C9	HA0		PB8
B9	HA1		PB9
A9	HA2		PB10
D9	$\overline{\text{HR/W}}$		PB11
B10	$\overline{\text{HEN}}$		PB12
C10	$\overline{\text{HREQ}}$		PB13
A10	$\overline{\text{HACK}}$		PB14
C12	RXD	C	PC0
D12	TXD		PC1
E12	SCLK		PC2
F11	SC0		PC3
G12	SC1		PC4
F13	SC2		PC5
F12	SCK		PC6
G13	SRD		PC7
G11	STD		PC8
H11	TIO	No port assigned	

Table 3-10 DSP56002 Signal Identification by PGA Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
A1	GND_Q	B13	V_{CCH}	E2	D18
A2	V_{CCQ}	C1	V_{CCD}	E3	D19
A3	GND_Q	C2	MODB / $\overline{\text{IRQB}}$	E4	D22
A4	V_{CCQ}	C3	MODA / $\overline{\text{IRQA}}$	E10	H3 / PB3
A5	GND_Q	C4	GND_{CK}	E11	H0 / PB0
A6	V_{CCQ}	C5	CKOUT	E12	SCLK / PC2
A7	GND_Q	C6	GND_P	E13	GND_H
A8	V_{CCQ}	C7	PINIT	F1	D15
A9	HA2 / PB10	C8	EXTAL	F2	D16
A10	$\overline{\text{HACK}}$ / PB14	C9	HA0 / PB8	F3	D17
A11	H6 / PB6	C10	$\overline{\text{HREQ}}$ / PB13	F11	SC0 / PC3
A12	GND_H	C11	H2 / PB2	F12	SCK / PC6
A13	GND_H	C12	RXD / PC0	F13	SC2 / PC5
B1	GND_D	C13	GND_H	G1	D14
B2	V_{CCCK}	D1	GND_D	G2	D13
B3	RESET	D2	D20	G3	D12
B4	CKP	D3	D21	G11	STD / PC8
B5	V_{CCP}	D4	D23	G12	SC1 / PC4
B6	PCAP	D5	MODC / $\overline{\text{NMI}}$	G13	SRD / PC7
B7	PLOCK	D9	HR / $\overline{\text{W}}$ / PB11	H1	D11
B8	XTAL	D10	H4 / PB4	H2	D10
B9	HA1 / PB9	D11	H1 / PB1	H3	D9
B10	$\overline{\text{HEN}}$ / PB12	D12	TXD / PC1	H11	TIO*
B11	H7 / PB7	D13	V_{CCH}	H12	NC
B12	H5 / PB5	E1	GND_D	H13	BN

Table 3-10 DSP56002 Signal Identification by PGA Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
J1	V_{CCD}	L2	D4	M8	A4
J2	D8	L3	D3	M9	A2
J3	D7	L4	A13	M10	PS
J4	A15	L5	A10	M11	DSI / OS0
J10	RD	L6	A8	M12	NC
J11	WR	L7	A6	M13	V_{CCC}
J12	WT	L8	A3	N1	GND_D
J13	GND_S	L9	A1	N2	D0
K1	GND_D	L10	DS	N3	GND_A
K2	D6	L11	DSO	N4	V_{CCA}
K3	D5	L12	BR	N5	GND_A
K4	A14	L13	GND_S	N6	GND_A
K5	A11	M1	V_{CCD}	N7	V_{CCA}
K9	A0	M2	D2	N8	GND_A
K10	$X/\overline{Y}$	M3	D1	N9	V_{CCA}
K11	DR	M4	A12	N10	GND_A
K12	BG	M5	A9	N11	BS
K13	V_{CCS}	M6	A7	N12	DSCK / OS1
L1	GND_D	M7	A5	N13	GND_C

Note:
1. NC” are No Connection pins that are reserved for possible future enhancements. Do not connect these pins to any power, ground, signal traces, or vias.
2. An $\overline{\text{OVERBAR}}$ indicates the signal is asserted when the voltage = ground (active low).

Table 3-11 DSP56002 PGA Pin Identification by Signal Name

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
A0	K9	D3	L3	DSO	L11
A1	L9	D4	L2	EXTAL	C8
A2	M9	D5	K3	GND_A	N10
A3	L8	D6	K2	GND_A	N8
A4	M8	D7	J3	GND_A	N6
A5	M7	D8	J2	GND_A	N5
A6	L7	D9	H3	GND_A	N3
A7	M6	D10	H2	GND_C	N13
A8	L6	D11	H1	GND_{CK}	C4
A9	M5	D12	G3	GND_D	N1
A10	L5	D13	G2	GND_D	L1
A11	K5	D14	G1	GND_D	K1
A12	M4	D15	F1	GND_D	E1
A13	L4	D16	F2	GND_D	D1
A14	K4	D17	F3	GND_D	B1
A15	J4	D18	E2	GND_H	A12
$\overline{BG}$	K12	D19	E3	GND_H	A13
$\overline{BN}$	H13	D20	D2	GND_H	C13
$\overline{BR}$	L12	D21	D3	GND_H	E13
$\overline{BS}$	N11	D22	E4	GND_P	C6
CKOUT	C5	D23	D4	GND_Q	A1
CKP	B4	$\overline{DR}$	K11	GND_Q	A2
D0	N2	$\overline{DS}$	L10	GND_Q	A5
D1	M3	DSCK	N12	GND_Q	A7
D2	M2	DSI	M11	GND_S	J13

Table 3-11 DSP56002 PGA Pin Identification by Signal Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
GND_S	L13	PB5	B12	SCK	F12
H0	E11	PB6	A11	$\overline{SCLK}$	E12
H1	D11	PB7	B11	SRD	G13
H2	C11	PB8	C9	STD	G11
H3	E10	PB9	B9	TIO	H11
H4	D10	PB10	A9	TXD	D12
H5	B12	PB11	D9	V_{CCA}	N9
H6	A11	PB12	B10	V_{CCA}	N7
H7	B11	PB13	C10	V_{CCA}	N4
HA0	C9	PB14	A10	V_{CCC}	M13
HA1	B9	PC0	C12	V_{CCCK}	B2
HA2	A9	PC1	D12	V_{CCD}	M1
$\overline{HACK}$	A10	PC2	E12	V_{CCD}	J1
$\overline{HEN}$	B10	PC3	F11	V_{CCD}	C1
HR/$\overline{W}$	D9	PC4	G12	V_{CCH}	B13
$\overline{HREQ}$	C10	PC5	F13	V_{CCH}	D13
$\overline{IRQA}$	C3	PC6	F12	V_{CCP}	B5
$\overline{IRQB}$	C2	PC7	G13	V_{CCQ}	A2
MODA	C3	PC8	G11	V_{CCQ}	A4
MODB	C2	PCAP	B6	V_{CCQ}	A6
MODC	D5	PINIT	C7	V_{CCQ}	A8
$\overline{NMI}$	D5	PLOCK	B7	V_{CCS}	K13
OS0	M11	$\overline{PS}$	M10	$\overline{WR}$	J11
OS1	N12	$\overline{RD}$	J10	$\overline{WT}$	J12
PB0	E11	$\overline{RESET}$	B3	X/$\overline{Y}$	K10
PB1	D11	RXD	C12	XTAL	B8
PB2	C11	SC0	F11	nc	H12
PB3	E10	SC1	G12	nc	M12
PB4	D10	SC2	F13		

Power and ground pins have special considerations for noise immunity. See the section **Design Considerations**.

Table 3-12 DSP56002 Power Supply Pins in PGA Package

Pin Number	Power Supply	Circuit Supplied
N9	V_{CCA}	Address Bus Buffers
N7		
N4		
N10	GND_A	
N8		
N6		
N5		
N3		
M13	V_{CCC}	Bus Control Buffers
N13	GND_C	
B2	V_{CCCK}	Clock
C4	GND_{CK}	
M1	V_{CCD}	Data Bus Buffers
J1		
C1		
N1	GND_D	
L1		
K1		
E1		
D1		
B1		
B13	V_{CCH}	Host Interface Buffers
D13		
A12	GND_H	
A13		
C13		
E13		

Table 3-12 DSP56002 Power Supply Pins in PGA Package (Continued)

Pin Number	Power Supply	Circuit Supplied
A8	V_{CCQ}	Internal Logic
A6		
A4		
A2		
A1	GND_Q	
A2		
A5		
A7		
B5	V_{CCP}	PLL
C6	GND_P	
K13	V_{CCS}	Serial Port
J13	GND_S	
L13		

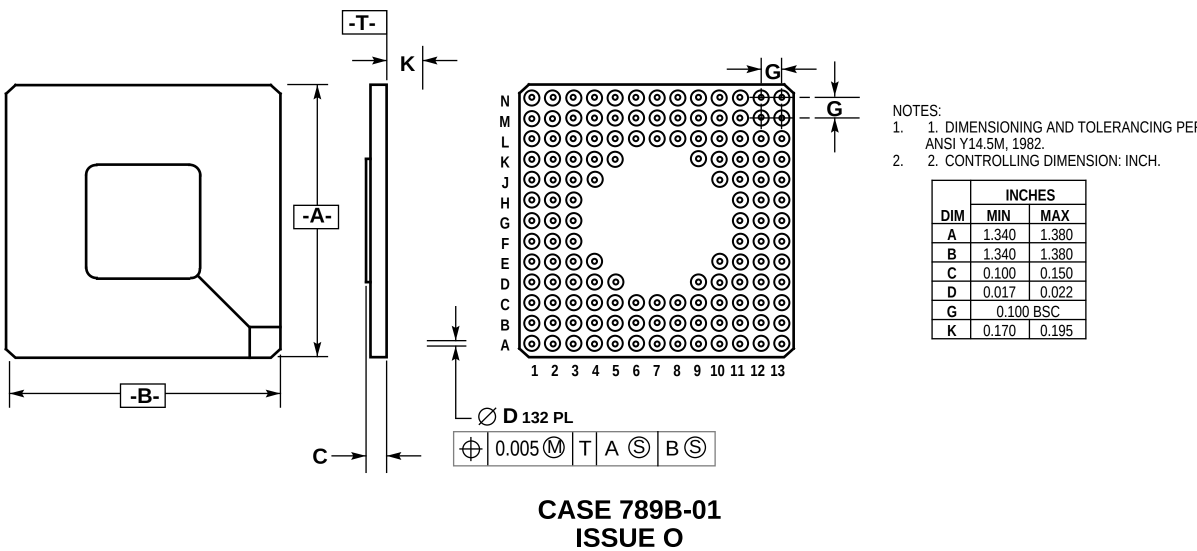


Figure 3-9 132-pin Ceramic Pin Grid Array (PGA) Package Mechanical Information

ORDERING DRAWINGS

Complete mechanical information regarding DSP56002 packaging is available by facsimile through Motorola's Mfax™ system. Call the following number to obtain information by facsimile:

(602) 244-6591

The Mfax automated system requests the following information:

- The receiving facsimile telephone number including area code or country code
- The caller’s Personal Identification Number (PIN)

Note: For first time callers, the system provides instructions for setting up a PIN, which requires entry of a name and telephone number.

- The type of information requested:
  - Instructions for using the system
  - A literature order form
  - Specific part technical information or data sheets
  - Other information described by the system messages

A total of three documents may be ordered per call.

The DSP56002 132-pin PQFP package mechanical drawing is referenced as 831A-02. The reference number for the 144-pin TQFP package is 918-03. The reference number for the 132-pin ceramic PGA package is 789B-01.

SECTION 4

DESIGN CONSIDERATIONS

HEAT DISSIPATION

An estimation of the chip junction temperature, T_J, in °C can be obtained from the equation:

Equation 1: $T_J = T_A + (P_D \times R_{\theta JA})$

Where:

T_A = ambient temperature ˚C
$R_{\theta JA}$ = package junction-to-ambient thermal resistance ˚C / W
P_D = power dissipation in package

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

Equation 2: $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

Where:

$R_{\theta JA}$ = package junction-to-ambient thermal resistance ˚C / W
$R_{\theta JC}$ = package junction-to-case thermal resistance ˚C / W
$R_{\theta CA}$ = package case-to-ambient thermal resistance ˚C / W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the Printed Circuit Board, or otherwise change the thermal dissipation capability of the area surrounding the device on a Printed Circuit Board. This model is most useful for ceramic packages with heat sinks; some 90% of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the Printed Circuit Board, analysis of the device thermal performance may need the additional modeling capability of a system level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the Printed Circuit Board to which the package is mounted. Again, if the estimations obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system level model may be appropriate.

A complicating factor is the existence of three common ways for determining the junction-to-case thermal resistance in plastic packages:

- To minimize temperature variation across the surface, the thermal resistance is measured from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink.
- To define a value approximately equal to a junction-to-board thermal resistance, the thermal resistance is measured from the junction to where the leads are attached to the case.
- If the temperature of the package case (T_T) as determined by a thermocouple, the thermal resistance is computed using the value obtained by the equation $(T_J - T_T) / P_D$.

As noted above, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable for determining the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, using the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will estimate a junction temperature slightly hotter than actual temperature. Hence, the new thermal metric, Thermal Characterization Parameter or Ψ_{JT}, has been defined to be $(T_J - T_T) / P_D$. This value gives a better estimate of the junction temperature in natural convection when using the surface temperature of the package. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

Note: **Table 2-2 Thermal Characteristics** on page 2-2 contains the package thermal values for this chip.

ELECTRICAL DESIGN CONSIDERATIONS

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

Use the following list of recommendations to assure correct DSP operation:

- Provide a low-impedance path from the board power supply to each V_{CC} pin on the DSP, and from the board ground to each GND pin.
- Use at least four 0.1 μF bypass capacitors positioned as close as possible to the four sides of the package to connect the V_{CC} power source to GND.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{CC} and GND pins are less than 0.5 inch per capacitor lead.
- Use at least a four-layer Printed Circuit Board (PCB) with two inner layers for V_{CC} and GND.
- Because the DSP output signals have fast rise and fall times, PCB trace lengths should be minimal. This recommendation particularly applies to the address and data buses as well as the $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{NMI}}$, $\overline{\text{HEN}}$, and $\overline{\text{HACK}}$ pins.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{CC} and GND circuits.
- All inputs must be terminated (i.e., not allowed to float) using CMOS levels.
- Take special care to minimize noise levels on the PLL supply pins (both V_{CC} and GND).

POWER CONSUMPTION

Power dissipation is a key issue in portable DSP applications. The following describes some factors which affect current consumption. Current consumption is described by the formula:

Equation 3: $I = C \times V \times f$

where: C = node / pin capacitance
V = voltage swing
f = frequency of node / pin toggle

For example, for an address pin loaded with a 50 pF capacitance and operating at 5.5 V with a 40 MHz clock, toggling at its maximum possible rate (which is 10 MHz), the current consumption is:

Equation 4: $I = 50 \times 10^{-12} \times 5.5 \times 10 \times 10^{6} = 2.75\text{mA}$

The maximum internal current value (I_{CCI}-max), reflects the maximum I_{CC} expected when running the code given below. This represents “typical” internal activity, and is included as a point of reference. Some applications may consume more or less current depending on the code used. The typical internal current value (I_{CCI}-typ) reflects what is typically seen when running the given code.

The following steps are recommended for applications requiring very low current consumption:

1. Minimize external memory accesses; use internal memory accesses instead.
2. Minimize the number of pins that are switching.
3. Minimize the capacitive load on the pins.
4. Connect the unused inputs to pull-up or pull-down resistors.

Current consumption test code:

```
        org     p:RESET
        jmp     MAIN
        org     p:MAIN
        movep   #$180000,x:$FFFD
        move    #0,r0
        move    #0,r4
        move    #$00FF, m0
        move    #$00FF, m4
        nop
        rep     #256
        move    r0,x:(r0)+
        rep     #256
        mov     r4,y:(r4)+
        clr     a
        move    l:(r0)+,a
        rep     #30
        mac     x0,y0,a x:(r0)+,x0 y:(r4)+,y0
        move    a,p:(r5)
        jmp     TP1
TP1     nop
        jmp     MAIN
```

HOST PORT CONSIDERATIONS

Careful synchronization is required when reading multibit registers that are written by another asynchronous system. This is a common problem when two asynchronous systems are connected. The situation exists in the host interface. The following paragraphs present considerations for proper operation.

Host Programming Considerations

UNSYNCHRONIZED READING OF RECEIVE BYTE REGISTERS

When reading receive byte registers (RXH, RXM, and RXL) the host programmer should use interrupts or poll the RXDF flag that indicates that data is available. This assures that the data in the receive byte registers will be stable.

OVERWRITING TRANSMIT BYTE REGISTERS

The host programmer should not write to the transmit byte registers (TXH, TXM, and TXL) unless the TXDE bit is set indicating that the transmit byte registers are empty. This guarantees that the transmit byte registers will transfer valid data to the HRX register.

SYNCHRONIZATION OF STATUS BITS FROM DSP TO HOST

HC, HREQ, DMA, HF3, HF2, TRDY, TXDE, and RXDF status bits are set or cleared from inside the DSP and read by the host processor. The host can read these status bits very quickly without regard to the clock rate used by the DSP, but the possibility exists that the state of the bit could be changing during the read operation. This is generally not a system problem, since the bit will be read correctly in the next pass of any host polling routine.

Note: Refer to *DSP56002 User’s Manual* sections describing the I/O Interface and Host/DMA Interface Programming Model for descriptions of these status bits.

OVERWRITING THE HOST VECTOR

The Host programmer should change the Host Vector register only when the Host Command bit (HC) is clear. This change guarantees that the DSP interrupt control logic will receive a stable vector.

CANCELLING A PENDING HOST COMMAND EXCEPTION

The host processor may elect to clear the HC bit to cancel the Host Command Exception request at any time before it is recognized by the DSP. Because the host does not know exactly when the exception will be recognized (due to exception processing synchronization and pipeline delays), the DSP may execute the Host Command Exception after the HC bit is cleared. For these reasons, the HV bits must not be changed at the same time the HC bit is cleared.

VARIANCE IN THE HI TIMING

HI timing may vary during initial startup during the time after reset before the PLL locks. Therefore, before a host attempt to load (i.e., bootstrap) the DSP, the host should first make sure that the HI port programming has been completed. The following steps can be used to ensure that the programming is complete:

1. Set the INIT bit in the ICR
2. Poll the INIT bit until it is cleared.
3. Read the ISR.

An alternate method is:

1. Write the TREQ/RREQ together with INIT.
2. Poll INIT, ISR, and the $\overline{\text{HREQ}}$ pin.

DSP Programming Considerations

SYNCHRONIZATION OF STATUS BITS FROM HOST TO DSP

DMA, HF1, HF0, and HCP, HTDE, and HRDF status bits are set or cleared by the host processor side of the interface. These bits are individually synchronized to the DSP clock.

Note: Refer to *DSP56002 User's Manual* sections describing the I/O Interface and Host/DMA Interface Programming Model for descriptions of these status bits.

READING HF0 AND HF1 AS AN ENCODED PAIR

A potential problem exists when reading status bits HF0 and HF1 as an encoded pair (i.e., the four combinations 00, 01, 10, and 11 each have significance). A very small probability exists that the DSP will read the status bits synchronized during transition. The solution to this potential problem is to read the HF0 and HF1 bits twice and check for consensus.

PACKAGE COMPATIBILITY

The PQFP and TQFP packages are designed so that a single Printed Circuit Board (PCB) can accommodate either package. The two package pinouts are similarly sequenced. Proper orientation of each package with the smaller TQFP footprint inside the PQFP footprint allow connection of PCB traces to either package. For example, the D0 pin is near the corner of both the PQFP package (pin 84) and the TQFP package (pin 109), and is adjacent to D1 on both packages.

Note: Some “no connect” pins in the TQFP pin sequence are excluded from the PQFP pin sequence.

SECTION 5

ORDERING INFORMATION

DSP56002 ordering information in the table below lists the pertinent information needed to place an order. Consult a Motorola Semiconductor sales office or authorized distributor to determine availability and to order parts.

Table 5-1 DSP56002 Ordering Information

<table>
<tr><th>Part</th><th>Supply Voltage</th><th>Package Type</th><th>Pin Count</th><th>Frequency (MHz)</th><th>Order Number</th></tr>
<tr><td rowspan="7">DSP56002</td><td rowspan="7">5 V</td><td rowspan="3">Plastic Quad Flat Pack (PQFP)</td><td rowspan="3">132</td><td>40</td><td>DSP56002FC40</td></tr>
<tr><td>66</td><td>DSP56002FC66</td></tr>
<tr><td>80</td><td>DSP56002FC80</td></tr>
<tr><td rowspan="3">Plastic Thin Quad Flat Pack (TQFP)</td><td rowspan="3">144</td><td>40</td><td>DSP56002PV40</td></tr>
<tr><td>66</td><td>DSP56002PV66</td></tr>
<tr><td>80</td><td>DSP56002PV80</td></tr>
<tr><td>Ceramic Pin Grid Array</td><td>132</td><td>40</td><td>DSP56002RC40</td></tr>
</table>

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US & Canada ONLY (800) 774-1848

Asia/Pacific:
Motorola Semiconductors H.K. Ltd.
8B Tai Ping Industrial Park
51 Ting Kok Road
Tai Po, N.T., Hong Kong
852-26629298

Technical Resource Center:
1 (800) 521-6274

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