Product Preview

FUNCTIONAL DIFFERENCES BETWEEN DSP56302 AND DSP56302A

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Preliminary Release 8/14/1997

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1 PURPOSE OF THIS DOCUMENT

To meet the increasing demands for higher performance and lower power consumption, an advanced DSP56302 is being designed and designated the DSP56302A. The new part is designed to be a functional replacement for the DSP56302. This document summarizes the differences between the DSP56302 and the DSP56302A.

2 DIFFERENCES OVERVIEW

Table 1 lists the primary functional differences between the DSP56302 and the DSP56302A, which are due to inherent differences between the two design technologies.

Table 1 Functional Comparison of DSP56302 and DSP56302A

Feature	DSP56302	DSP56302A
Operating frequency	≤ 66 MHz down to 0 Hz	≥ 66 MHz down to 0 Hz
Technology	0.5 micron	sub 0.4 micron
Input power	V_{CC} = 3.0–3.6 V combined core and I/O power and ground	Split power: • Core V_{CC} (3.0–3.6 V currently) • I/O V_{CC} (3.0–3.6 V currently) A pinout change is required to support the split power configuration. See page 4 for more information and a description of the 144-pin TQFP package pinout changes.
I/O pin inputs	5 V tolerant	tolerant up to 3.6 V
TTL output low current (I_{OL})	Standard output = 3.0 mA Open-drain output = 6.7 mA	Port A output = 1.6 mA Non-Port A standard output = 3.2 mA Open-drain output = 6.7 mA
Package	144-pin TQFP	144-pin TQFP or 196-pin PBGA
PLL input capacitor (C_{PCAP})	Uses the following rules: • For MF ≤ 4: C_{PCAP} = [(500 × MF) – 150] pF • For MF > 4: C_{PCAP} = (690 × MF) pF	Uses the following rules: • For MF < 3: C_{PCAP} = [(680 × MF) – 120] pF • For MF ≥ 3: C_{PCAP} = (1100 × MF) pF
Signal keepers	None	Keepers have been added to the following signals: • Port A Data Bus (D23–D0) • HI08 (All signal lines) • ESSI0 and ESSI1 (All signal lines) • SCI (All signal lines) • Timers (TIO0–TIO3)
Other functionality	All memory, control functions, and peripherals are identical. Refer to the *DSP56302 Technical Data* sheet (order by DSP56302/D) for a detailed description of these features.	
Note: MF = Multiplication Factor		

3 INPUT POWER REQUIREMENT CHANGES

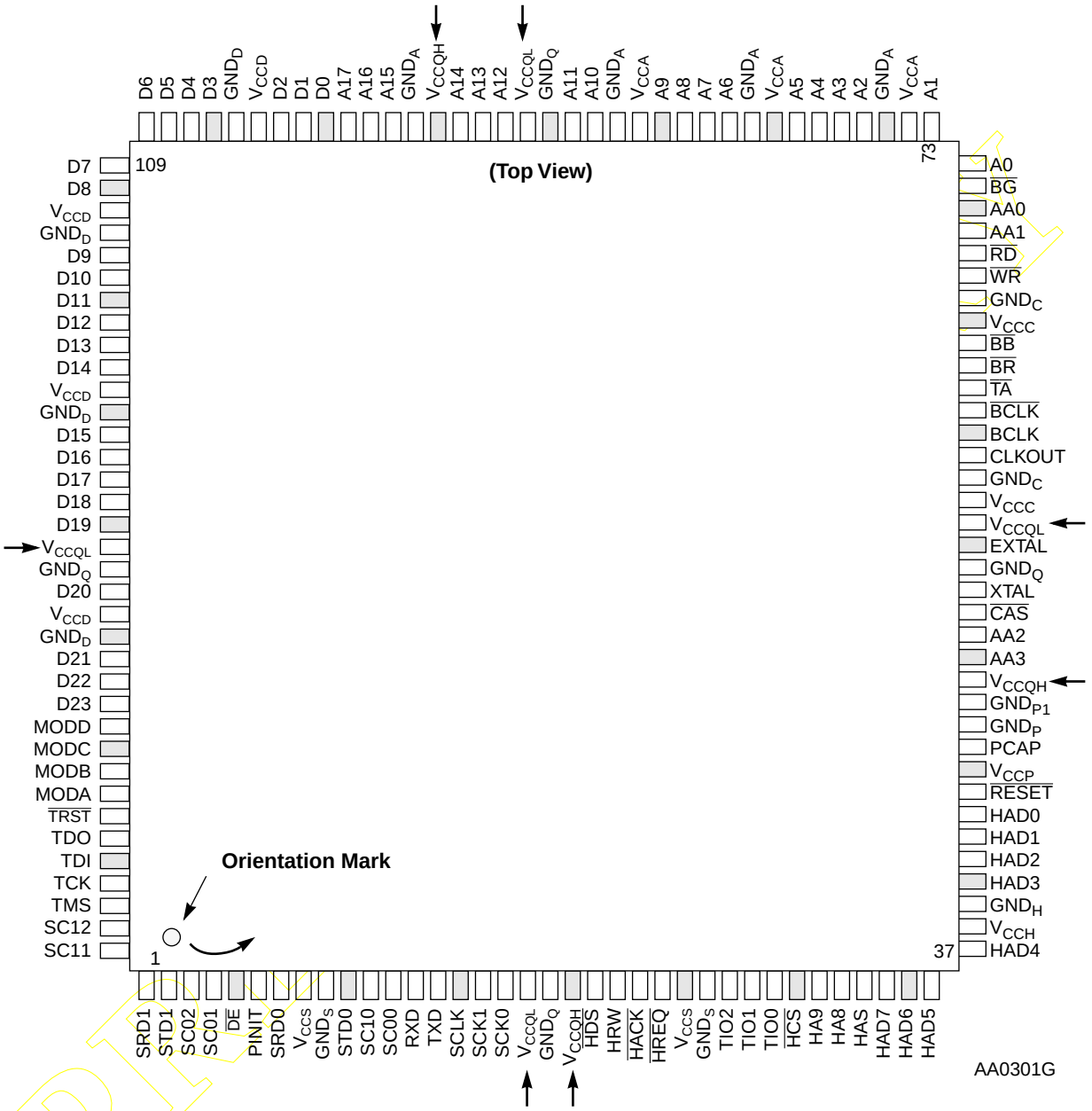
One method to increase the operating frequency of an integrated circuit is to “shrink” the die (i.e., reduce the die dimensions, both linearly and vertically). Reducing the die size can yield additional benefits, such as a reduction of power consumption, but can also result in other functional changes.

The DSP56302A is a “shrink” of the DSP56302. This die size reduction enables the DSP56302A to achieve higher operating frequencies than the DSP56302. Decreasing the die size, however, requires a reduction of the thickness of the oxide dielectrics, which also reduces the maximum allowable voltages across some oxides within the die.

To support future “shrinks” of the DSP56302A while maximizing system level compatibility, Motorola has elected to separate the power supply networks on the die. This split allows the I/O pins to operate over a voltage range which is different from that used by the core digital logic. Although the initial release of this product specifies the same voltage ranges for the I/O pins and the core logic, future versions of the DSP56302x are likely to have reduced core logic V_{CC} requirements (such as 2.5 V and lower voltages) while the I/O levels use a higher level (such as 3.3 V). This will allow Motorola to continue aggressively to “shrink” the device, while preserving the ability to maintain system level compatibility.

The split-power design requires a modification in the chip pinout. A top view of the DSP56302A TQFP package is shown in **Figure 1** on page 6. **Table 2** on page 7 lists the pin differences between the DSP56302 and the DSP56302A.

Note: The power input for the core logic is designated V_{CCQ} for the DSP56302. For the DSP56302A, the independent core logic input voltage is designated V_{CCQL}, while the independent I/O input voltage is designated V_{CCQH}. V_{CCQL} should be connected to the core input power supply. V_{CCQH} and all other input power (V_{CCA}, V_{CCC}, V_{CCD}, V_{CCH}, V_{CCP}, and V_{CCS}) should be connected to the external input power supply.



Note: Arrows (→) indicate the pins that are different from the DSP56302, as listed in **Table 2** on p. 6.

Figure 1 DSP56302A Thin Quad Flat Pack (TQFP), Top View

Table 2 Pin Differences between DSP56302 and DSP56302A (144-pin TQFP package)

Pin	Pin Name	
	DSP56302	**DSP56302A**
18	V_{CCQ}	V_{CCQL}
20	NC	V_{CCQH}
49	NC	V_{CCQH}
56	V_{CCQ}	V_{CCQL}
91	V_{CCQ}	V_{CCQL}
95	V_{CCA}	V_{CCQH}
126	V_{CCQ}	V_{CCQL}

Notes:
1. V_{CCQ} = input voltage for core logic
2. V_{CCQL} = independent input voltage for core logic
3. NC = not connected
4. V_{CCQH} = independent input voltage for I/O lines
5. V_{CCA} = voltage for external address lines
6. Unlisted pins are the same for both chips.

A pinout for the 196-pin PBGA package is included in the *DSP56302A Technical Data* sheet. This package will include the split power configuration described for the 144-pin TQFP package.

4 I/O INPUT POWER CHANGES

The DSP56302 supports 5 V inputs for its peripherals. Complete requirements are described in the *DSP56302 Technical Data* sheet.

The DSP56302A supports 3.3 V inputs. Detailed voltage requirements are included in the *DSP56302A Technical Data* sheet.

5 TTL OUTPUT LOW CURRENT CHANGES

The DSP56302 has the same output low current specifications for all TTL-compatible outputs. Complete requirements are described in the *DSP56302 Technical Data* sheet.

The DSP56302A has different requirements for the Port A outputs and the other TTL-compatible outputs. **Table 1** on page 4 lists the limits for the this specification.

6 PACKAGE AVAILABILITY

Because the new process yields a smaller die size, the DSP56302A can use both the 144-pin TQFP package or the 196-pin PBGA package. Because of die size constraints, the DSP56302 is limited to the 144-pin TQFP package.

7 PLL INPUT CAPACITOR (C_{PCAP})

The process change results in a changed requirement for computing the size of C_{PCAP}, the capacitor used with the PCAP input. **Table 1** on page 4 lists the new formulas for computing the value of this input capacitor for the DSP56302A.

8 SIGNAL LINE KEEPERS

Signal keepers have been added to several of the signal lines used on the DSP56302A. The purpose of a keeper is to hold the last logical value that was driven to the signal, to maintain the value in case all potential signal drivers are tri-stated. The keepers are weak enough so that if any potential driver does drive the signal, the keeper affects neither the correct driving of the signal nor the signal timing.

Note: A keeper may consume tens of µA during the Stop state if the power is not maintained at the required V_{IH} or V_{IL} levels during the Stop state, as specified in the *DSP56302A Technical Data sheet*. For minimal power consumption, the V_{IH} should never be lower than $0.9 \times V_{CC}$ and the V_{IL} should never be higher than $0.1 \times V_{CC}$.

The following pins have line keepers:

- Port A Data Bus (D23–D0)
- HI08 (all signals)
- ESSI0 (all signals)
- ESSI1 (all signals)
- SCI (all signals)
- Timers (all signals)

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