DSP

Technical Documentation

Main Menu

- New Products
- DSP Portfolio
- Technical Documentation
- Application Examples
- Development Tools
- Contact Information

MOTOROLA

DSP

New Products

DSP56362 24 bit Digital Audio DSP

The DSP56362 is a multimode, multichannel audio decoder for consumer applications such as Audio/Video (A/V) receivers, surround sound decoders, Digital Versatile Disk (DVD), digital TV, and other audio applications.

DSP56824 16 bit DSP

The DSP56824 is well-suited for cost-sensitive applications, such as digital wireless messaging, servo and motor control, digital answering machines/feature phones, modems, and digital cameras.

DSP56LF812 16 bit DSP

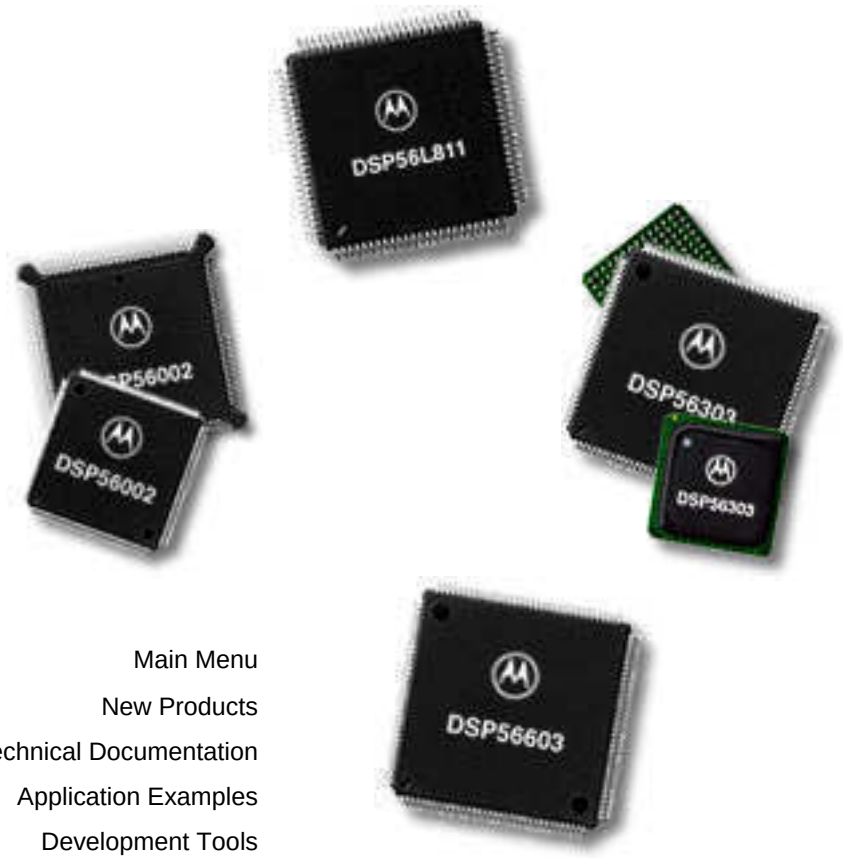
This general purpose DSP combines processing power with programming capability of Flash memories, making it an excellent choice for system code development for signal processing and control functions.

Main Menu
DSP Portfolio
Technical Documentation
Application Examples
Development Tools
Contact Information

MOTOROLA

DSP

DSP Portfolio



16-Bit DSPs

DSP56800 Family

24-Bit DSPs

DSP56000 Family

DSP56300 Family

DSP56600 Family

- Main Menu
- New Products
- Technical Documentation
- Application Examples
- Development Tools
- Contact Information

MOTOROLA

DSP

Technical Documentation

16-Bit DSPs

DSP56800 Family

24-Bit DSPs

DSP56000 Family

DSP56300 Family

DSP56600 Family

Application Notes

MOTOROLA

DSP

Application Examples

Audio

Cellular Infrastructure

Advanced Messaging

Digital Cordless

Video Conferencing
(Audio Subsystem)

Application Notes

Main Menu
New Products
DSP Portfolio
Technical Documentation
Development Tools
Contact Information

MOTOROLA

DSP

Development Tools

In addition to the thorough, detailed documentation available for each DSP product, Motorola offers a comprehensive stable of hardware and software development tools.

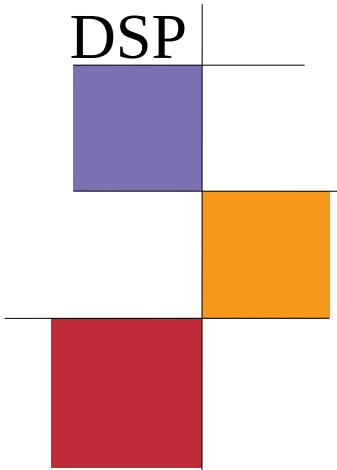
Motorola has upgraded the DSP Application Development System (ADS) to provide universal application development and emulation support for the DSP Family. The Universal Application Development System utilizes OnCE to provide a common hardware interface so that a single system now provides fullspeed emulation capabilities for every Motorola DSP product, on either a customer's target system or Motorola's Application Development Modules. The Application Development System hardware and a variety of third party boards are available for all three families of DSP products.

Motorola and third party partners offer an assortment of software development tools for all DSP products. Development software available for IBM PC and equivalents, Macintosh II and SUN-4 workstations includes simulators, assemblers, linkers, libraries and C compilers for DSP products as well as real-time operating systems for the DSP56000 and DSP96000 Families.

- Main Menu
- New Products
- DSP Portfolio
- Technical Documentation
- Application Examples
- Contact Information

DOCUMENTATION THIRD PARTY

MOTOROLA



Contact Information

ASIA/PACIFIC
Motorola Semiconductors H.K. Ltd.
8B Tai Ping Industrial Park
51 Ting Kok Road
Tai Po, N.T., Hong Kong
852-2662928

JAPAN
Nippon Motorola Ltd.
Tatsumi-SPD-JLDC
6F Seibu-Butsuryu-Center
3-14-2 Tatsumi Koto-Ku
Tokyo 135, Japan
03-3521-8315

USA/EUROPE
Motorola Literature Distribution
P.O. Box 20912
Phoenix, Arizona 85036
1 (800) 441-2447 or
1 (602) 303-5454

DSP Helpline
dsphelp@dsp.sps.mot.com

Technical Resource Center
1 (800) 521-6274

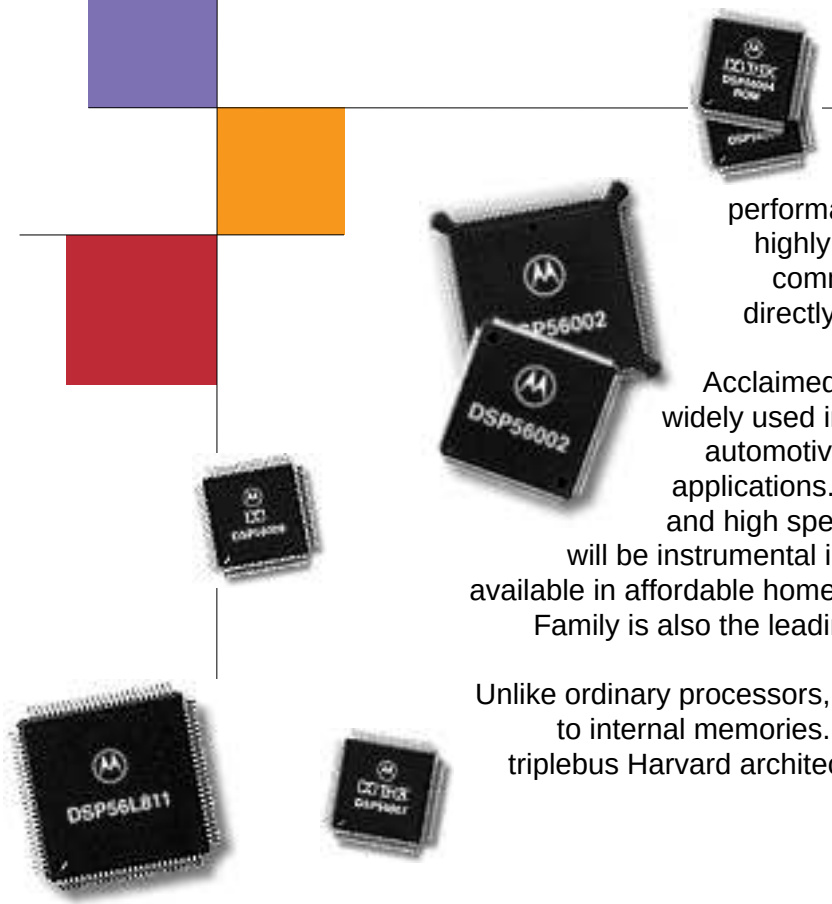
MFAX
RMFAX0@email.sps.mot.com
TOUCHTONE (602) 244-6609

Internet
http://www.motorola-dsp.com

Main Menu
New Products
DSP Portfolio
Technical Documentation
Development Tools
Application Examples

MOTOROLA

DSP



The DSP56000 Family

The DSP56000 Family boasts the industry's highest performance fixed point, 24 bit processors. It is also the most highly integrated family, with an array of on chip memories, communication ports, and a host interface that allows it to directly communicate to other processors or DMA channels.

Acclaimed for its proven performance, the DSP56000 Family is widely used in a variety of advanced communication, digital audio, automotive, robotic, military, medical, and sophisticated control applications. The chip's dynamic range, high accuracy, low noise, and high speed make it the preferred DSP for CD quality sound. It will be instrumental in making Compact Disk Interactive (CD I) technology available in affordable home entertainment systems of the future. The DSP56000 Family is also the leading architecture for voice/audio features in computers.

Unlike ordinary processors, the DSP56000 Family features three separate buses to internal memories. These processors were the first to have an extended triplebus Harvard architecture that can supply an instruction plus two pieces of data simultaneously.

CONTINUE

Back to DSP Portfolio

MOTOROLA

DSP

The DSP56000 Family

CORE ARCHITECTURE The DSP56000 24-bit core architecture is built around three separate execution units which function independently and simultaneously, allowing the processor to carry out as many as seven essential operations.

The family's linear, modulo, and reverse carry address arithmetic modes are tailored to specific DSP data organizations and can greatly accelerate addressing.

On chip resources featured in the DSP56000 Family simplify and economize system design, further enhancing overall system performance. Six memories are integrated on the processor, reducing or eliminating time consuming off chip memory fetches. DSP56000 processors can address off chip memory for applications that require additional storage.
The DSP56000s also incorporate five peripheral functions: a host processor interface, an asynchronous serial communications interface (SCI), a synchronous serial interface (SSI), 24 parallel I/O lines, and a timer.

POWER MANAGEMENT Like the DSP56100 and DSP96000 Families, the DSP56000 Family provides power saving wait and stop modes. The DSP56L002, identical in functionality to the DSP56002, is unique in its ability to operate as low as 3 V. This makes it ideal for battery powered portable products such as personal communications terminals and laptop computers.

DOCUMENTATION

Back to DSP Portfolio

MOTOROLA

DSP56000 Family Technical Documentation

Product	Product Brief	Data Sheet	User's Manual	Chip Errata
DSP56001		✓	✓	✓
DSP56001A		✓		
DSP56002	✓	✓	✓	✓
DSP56L002	✓	✓	✓	
DSP56004	✓	✓	✓	
DSP56005	✓	✓	✓	
DSP56007	✓	✓	✓	✓
DSP56L007	✓	✓	✓	
DSP56009	✓	✓	✓	
DSP56011	✓	✓	✓	
DSP56000 Family Manual	✓			

Back to Documentation

DSP56300 Family Technical Documentation

Product	Product Brief	Data Sheet	User's Manual	Chip Errata
DSP56301	✓	✓	✓	✓
DSP56302*	✓	✓	✓	✓
DSP56303	✓	✓	✓	✓
DSP56304	✓	✓	✓	✓
DSP56305*	✓	✓		✓
DSP56302A(309)	✓	✓		
DSP56362	✓			
DSP56000 Family Manual	✓			
Other Documents				
Functional differences between DSP56301 Rev A and Rev B				✓
Functional differences between DSP56302 and DSP56302A(309)				✓
DSP56302UM/AD Correction on Boundery Scan Registers				✓
DSP56303UM/AD Correction on Boundery Scan Registers				✓

* Not recommended for new design

Back to Documentation

DSP56600 Family Technical Documentation

Product	Product Brief	Data Sheet	User's Manual	Chip Errata
DSP56602	✔	✔	✔	
DSP56603	✔	✔	✔	
DSP56600 Family User's Manual		✔		

Back to Documentation

MOTOROLA

DSP56800 Family Technical Documentation

Product	Product Brief	Data Sheet	User's Manual	Chip Errata
DSP56L811	✓	✓	✓	
DSP56812	✓			
DSP56LF812	✓	✓	✓	✓
DSP56824	✓	✓	✓	✓
DSP56800 Family Manual	✓			
Other Documentation				
White Paper: Nover DSP Architechture with Microcontroller Features				✓
Technical Bulletin: DSP56L811				✓
Technical Bulletin: DSP56800 Family				✓

Back to Documentation

DSP

DSP56300 Family

The escalating performance demands of wireless communications, telecommunications, multimedia, and related applications have been limited by digital signal processing performance. Motorola's new DSP56300 core family of programmable 24-bit microprocessors drives these applications to new levels of performance. The broad DSP56300 family is based on the high-performance DSP56300 core, a design integrating advanced features that dramatically boost performance, simplify system design, and drive system costs down. The family also includes a complete set of time-saving development tools.

Raising The Speed Limit: The Fastest High-Performance DSP Expressly developed for the new generations of speed-hungry DSP applications, our DSP56300 core is the first programmable digital signal processor architecture to deliver true single-clock-cycle execution. This is the fastest high-performance DSP yet—twice as fast at equivalent clock speeds as Motorola's highly successful 24-bit DSP56000 core family—and represents a breakthrough in DSP architecture performance. The DSP56300 core offers 80 Million Instructions Per Second (MIPS) at 80 MHz, with a roadmap to 100 MIPS and beyond.

Powerful Instruction Set For Greater Functionality The DSP56300 core is code-compatible with the DSP56000 core family, and provides a wealth of new performanceBenhancing features including a barrel-shifter, 24-bit addressing, and high-speed Direct Memory Access (DMA). These features allow the programmer to accomplish a task with significantly fewer instructions.

Lower Power Consumption Means Even More Savings While the DSP56300 core architecture delivers unprecedented speed and functionality, its power requirements are uncommonly low. An innovative intelligent power management system and low-voltage process technology combine to provide the best power/performance ratio of any DSP.

DOCUMENTATION

Back to DSP Portfolio

MOTOROLA

DSP

DSP56600 Family

Members of the DSP56600 core, can execute one 24-bit instruction per clock cycle using 16-bit data. The 60 MHz chip includes a mixture of peripherals and memories optimized for processing-intensive, cost-effective, low power consumption digital mobile communications applications.

The DSP56600 core includes the Data ALU, Address Generation Unit, Program Controller, Program Patch Detector, Bus Interface Unit, On-Chip Emulation/JTAG port, and a PLL-based clock generator.

DOCUMENTATION

Back to DSP Portfolio

MOTOROLA

DSP

DSP56800 Family

A new generation of digital telecommunications and motor control products is in the works: Digital wireless messaging. Digital tapeless answering machines. Digital wireless modems. Digital AC motor controls and disk-drive servo controls. The performance and cost-sensitivity of these applications require a new breed of chip architecture: a cost-effective solution that combines the prodigious number crunching of a digital signal processor with the versatile functionality of a microcontroller Motorola drew on its long success in DSPs and microcontrollers to create the DSP56800, a core family of high-efficiency, low-power 16-bit programmable digital signal processors with control functionality. The DSP56800 core family is just what the market ordered, and then some.

The DSP56800 Core: Multiple Functionality, By Design Motorola's DSP56800 core family is not merely a set of control functions grafted onto a DSP architecture, but rather the first digital signal processing architecture designed from the ground up to integrate a powerful DSP architecture and instruction set with embedded microcontroller capabilities in a single chip. For functionality, efficiency , and price/performance, there's nothing else like the DSP56800 core family, whose first two members are the DSP56L811 and DSP56L812.

A Versatile Instruction Set For Maximum Efficiency The DSP56800 core family has a streamlined, efficient DSP instruction set with traditional microcontroller functionality. The flexible multiplier has been enhanced with a 16-bit bi-directional barrel shifter and a Bit Manipulation Unit (BMU). A mixed hardware/software stack provides high-speed hardware DO loops and the flexibility of an unlimited software stack for interrupts, subroutines, and structured programming.

DOCUMENTATION

Back to DSP Portfolio

MOTOROLA

APR1/D Rev. 2	Digital Sine-Wave Synthesis Using the DSP56001/2
APR2/D	Digital Stereo 10-Band Graphic Equalizer Using the DSP56001
APR3/D Rev. 1	Fractional and Integer Arithmetic Using the DSP56000 Family of General-Purpose Digital Signal Processors
APR4/D Rev. 3	Implementation of Fast Fourier Transforms on Motorola's Digital Signal Processors
APR5/D Rev. 1	Implementation of PID Controllers on the Motorola DSP56000/DSP56001
APR6/D	Convolutional Encoding and Viterbi Decoding Using the DSP56001 with a V.32 Modem Trellis Example
APR7/D Rev. 2	Implementing IIR/FIR Filters with Motorola's DSP56000/DSP56001
APR8/D Rev. 1	Principles of Sigma-Delta Modulation for Analog-to-Digital Converters
APR9/D Rev. 1	Full-Duplex 32-Kbit/s CCITT ADPCM Speech Coding on the Motorola DSP56001
APR10/D Rev. 1	DSP96002 Interface Techniques and Examples
APR11/D Rev. 1	DSP56001 Interface Techniques and Examples
APR14/D Rev. 1	Conference Bridging in the Digital Telecommunications Environment Using the Motorola DSP56001/2
APR15/D	Implementation of Adaptive Controllers on the Motorola DSP56000/DSP56001
APR16/D	Calculating Time Requirements of External SRAM for the 24-bit DSP56000 Family
APR20/D	DSP56300/DSP56600 Application Optimization for the Digital Signal Processors
APR21/D	DSP56L811 Software UART on the Using GPIO Port B
APR22/D	Application Conversion from the Digital Signal Processors DSP56100 Family to the DSP56300/600 Families

Continue

APR23/D	Using the DSP56300 Direct Memory Access Controller
APR30/D	DSP56300 Assembly Code Development Using the Motorola Toolsets
APR31/D	Booting and Simple Usage of the DSP56004/007/009 SHI Port in SPI Mode
APR33/D	ROM Software Patching on the Motorola DSP56304
APR34/D	MC68328 Microprocessor Application: FLEX™ Alphanumeric Chip MC68175 Interface for One-Way Pager
APR35/D	Designing Motorola DSP56xxx Software for Nonrealtime Tests File I/O Using SIM56xxx and ADS56xxx
APR36/D	Interfacing the DSP560xx/DSP563xx Families to the Crystal CS4226 Multichannel Codec
EB420/D	DSP56001-to-DSP56002 Conversion Document This document explains how to migrate from a DSP56001 to a DSP56002.

Back Main Menu