DSP56362

Advance Information
24-BIT AUDIO DIGITAL SIGNAL PROCESSOR

The DSP56362 is a multimode, multichannel audio decoder for consumer applications such as Audio/Video (A/V) receivers, surround sound decoders, Digital Versatile Disk (DVD), digital TV, and other audio applications. The DSP56362 supports all of the popular multichannel audio decoding formats, including Dolby Digital Surround, Moving Picture Experts Group Standard 2 (MPEG2), and Digital Theater Systems (DTS), in a single device with sufficient resources (MIPS and memory) for customer defined post-processing features such as bass management, 3D virtual surround, Lucasfilm THX5.1, soundfield processing, and advanced equalization.

The DSP56362 is the first device in the second generation Motorola Symphony™ DSP Family. The DSP56362 utilizes the single-clock-per-cycle DSP56300 core, while retaining code compatibility with the DSP56000 core family. The DSP56362 contains audio-specific peripherals and on-board software engines as shown in **Figure 1** and will be offered initially in an 80 MIPS version at a nominal 3.3 V.

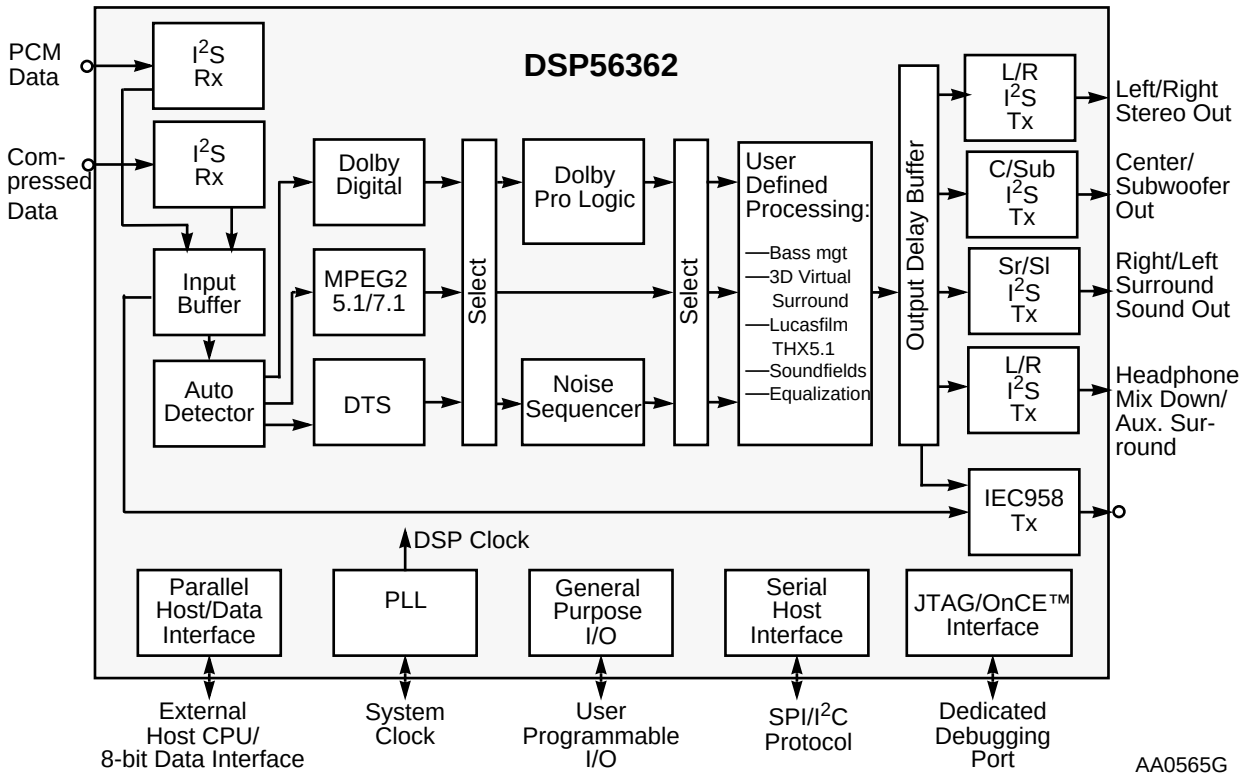

Figure 1 DSP56362 Surround Decoder Functionality

This document contains information on a new product. Specifications and information herein are subject to change without notice.

PRELIMINARY

FEATURES

- Multimode, multichannel decoder software functionality
  - Dolby Digital and Pro Logic
  - MPEG2 5.1/7.1
  - DTS
  - Bass management
- Digital audio post-processing capabilities
  - 3D Virtual surround sound
  - Lucasfilm THX5.1
  - Soundfield processing
  - Equalization
- Digital Signal Processing Core
  - 80 Million Instructions Per Second (MIPS) with an 80 MHz clock at a nominal 3.3 V
  - Object code compatible with the DSP56000 core with highly parallel instruction set
  - Data Arithmetic Logic Unit (Data ALU)
  - Program Control Unit (PCU)
  - Direct Memory Access (DMA)
  - Phase Lock Loop (PLL)
  - Hardware debugging support: On-Chip Emulation (OnCE™) module, Joint Action Test Group (JTAG) Test Access Port (TAP), and Address Trace mode
- On-Chip Memories
  - Modified Harvard architecture allows simultaneous access to program and data memories
  - Program, X data, and Y data ROMs that may be factory programmed with data/program provided by the application developer
  - 192 x 24-bit bootstrap ROM (disabled in Sixteen-Bit Compatibility mode)
- Off-Chip Memory Expansion
  - Data memory expansion to two 256 K × 24-bit word memory spaces (or up to two 4 M × 24-bit word memory spaces by using the Address Attribute AA0–AA3 signals)
  - Program memory expansion to one 256 K × 24-bit words memory space (or up to one 4 M × 24-bit word memory space by using the Address Attribute AA0–AA3 signals)
  - External memory expansion port (twenty-four data pins for high speed external memory access allowing for a large number of external accesses per sample)

  - Chip Select Logic for glueless interface to SRAMs
  - On-chip DRAM Controller for glueless interface to DRAMs
- Peripheral and Support Circuits
  - Enhanced Serial Audio Interface (ESAI) includes:
    - Up to four receivers and six transmitters
    - Master or slave capability
    - I^2S, Sony, AC97, and other audio protocol implementations
    - Configuration supports up to twelve General Purpose Input/Output (GPIO) lines
  - Serial Host Interface (SHI) features:
    - Multi-master capability
    - SPI and I^2C protocols
    - Ten-word receive FIFO
    - Support for 8-, 16-, and 24-bit words.
  - Byte-wide parallel Host Interface (HDI08) with DMA support; alternate configuration supports up to sixteen GPIO lines
  - DAX features one serial transmitter capable of supporting S/PDIF, IEC958, IEC1937, CP-340, and AES/EBU digital audio formats; configuration supports up to two GPIO lines
  - Triple Timer module with single external interface or one GPIO line
  - On-chip peripheral registers memory mapped in data memory space
- Reduced Power Dissipation
  - Very low power (3.3 V) CMOS design
  - Wait and Stop low-power standby modes
  - Fully-static logic, operation frequency down to 0 Hz (dc)
  - Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent)
- Additional Features
  - Software programmable PLL-based frequency synthesizer for the core clock
  - 144-pin plastic Thin Quad Flat Pack (TQFP) surface-mount package

DOCUMENTATION

Table 1 lists the documents that provide a complete description of the DSP56362 and are required to design properly with the part. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or (for the latest information) through the Motorola audio DSP home page on the Internet (see address below).

Table 1 Additional DSP56362 Documentation

Document Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the 56000-family architecture and the 24-bit core processor and instruction set	DSP56300FM/AD
DSP56362 User's Manual	Detailed description of memory, peripherals, and interfaces	DSP56362UM/AD
DSP56362 Technical Data Sheet	Electrical and timing specifications, and pin and package descriptions	DSP56362/D

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