Signal Descriptions for OCX_DLX_XLX_IF Module

This document provides a detailed description of the key input and output signals used in the OCX_DLX_XLX_IF module. Each signal is categorized based on its functionality and interfacing.

RX Interface Signals

Signal Name	Direction	Width	Description
ln0_rx_valid	Input	1-bit	Indicates if the data on lane 0 is valid.
ln0_rx_header	Input	2-bit	Header bits received on lane 0.
ln0_rx_data	Input	64-bit	Data received on lane 0.
ln0_rx_slip	Output	1-bit	Control signal to adjust the RX data alignment.
(Similar signals for ln1 to ln7)			

Signal Name	Direction	Width	Description
dlx_tlx_flit_valid	Output	1-bit	Indicates that the outgoing flit is valid.
dlx_tlx_flit	Output	512-bit	Flit data sent to the TLx interface.
dlx_tlx_flit_crc_err	Output	1-bit	Signals a CRC error in the outgoing flit.
dlx_tlx_link_up	Output	1-bit	Indicates that the link is active.
dlx_config_info ro_dlx_version	Output Output	32-bit 32-bit	Configuration information of the link. Version of the DLX module.

TX Interface Signals

Signal Name	Direction	Width	Description
tlx_dlx_flit_valid	Input	1-bit	Indicates the incoming flit is valid.
tlx_dlx_flit	Input	512-bit	Flit data received from the TLx interface.
tlx_dlx_debug_encode	Input	4-bit	Debug encoding signals for TX path.
tlx_dlx_debug_info	Input	32-bit	Debug information for TX path.
dlx_tlx_init_flit_depth	Output	3-bit	Initial depth of the flit buffer.
dlx_tlx_flit_credit	Output	1-bit	Credit signal for flit transfer.

Signal Name	Direction	Width	Description
dlx_lX_tx_data	Output	64-bit	Transmit data for each lane (l0 to l7).
dlx_lX_tx_header	Output	2-bit	Transmit header for each lane (l0 to l7).
dlx_lX_tx_seq	Output	6-bit	Sequence number for each lane (l0 to l7).

PHY Interface Signals

Signal Name	Direction	Width	Description
clk_156_25MHz	Input	1-bit	ain clock input at 156.25 MHz.
hb_gtwiz_reset_all_in	Input	1-bit	Global reset signal for the entire module.
gtwiz_reset_tx_done_in	Input	1-bit	Indicates TX reset completion.
gtwiz_reset_rx_done_in	Input	1-bit	Indicates RX reset completion.
gtwiz_buffbypass_tx_done_in	Input	1-bit	Signals TX buffer bypass completion.
gtwiz_buffbypass_rx_done_in	Input	1-bit	Signals RX buffer bypass completion.
gtwiz_userclk_tx_active_in	Input	1-bit	TX user clock activity status.
gtwiz_userclk_rx_active_in	Input	1-bit	RX user clock activity status.
send_first	Input	1-bit	Control signal to prioritize initial data send.
opt_gckn	Input	1-bit	Optional global clock signal input.
ocde	Input	1-bit	Optional clock domain enable.
gtwiz_reset_all_out	Output	1-bit	Reset status output for the entire module.
gtwiz_reset_rx_datapath_out	Output	1-bit	Reset signal for the RX datapath.

Internal Signals

Signal Name	Width	Description
dlx_reset	1-bit	Internal reset signal for the DLX logic.
pb_io_o0_rx_run_lane	8-bit	Indicates active RX lanes during operation.
io_pb_o0_rx_init_done	8-bit	Signals RX initialization completion per lane.

Signal Name	Width	Description
tx_rx_reset	1-bit	TX to RX reset synchronization signal.
train_ts2	1-bit	Training signal for TS2 state.
train_ts67	1-bit	Training signal for TS6/TS7 states.
rx_tx_crc_error	1-bit	Indicates CRC error during RX to TX transition.
rx_tx_retrain	1-bit	Retraining signal for RX to TX link.
rx_tx_nack	1-bit	Negative acknowledgment signal.
rx_tx_tx_ack_rtn	5-bit	TX acknowledgment return signal.
rx_tx_rx_ack_inc	4-bit	RX acknowledgment increment signal.
rx_tx_tx_ack_ptr_vld	1-bit	Validity signal for TX acknowledgment pointer.
rx_tx_tx_ack_ptr	7-bit	Pointer for TX acknowledgment.
rx_tx_tx_lane_swap	1-bit	Indicates lane swap during transmission.
rx_tx_deskew_done	1-bit	Signals completion of lane deskewing.
rx_tx_linkup	1-bit	Indicates that the link is successfully up.
lnX_rx_tx_last_byte_ts3	8-bit	Tracks the last byte in TS3 for each lane.
tx_rx_training	1-bit	Training control signal.
tx_rx_disabled_rx_lanes	8-bit	Indicates disabled RX lanes.
tx_rx_phy_training	1-bit	Physical training signal.
rx_tx_pattern_a	8-bit	Pattern A count for RX.
rx_tx_pattern_b	8-bit	Pattern B count for RX.
rx_tx_sync	8-bit	Synchronization signal for RX to TX.
rx_tx_TS1	8-bit	Indicates TS1 state across RX lanes.
rx_tx_TS2	8-bit	Indicates TS2 state across RX lanes.
rx_tx_TS3	8-bit	Indicates TS3 state across RX lanes.
rx_tx_block_lock	8-bit	Block lock status for each RX lane.