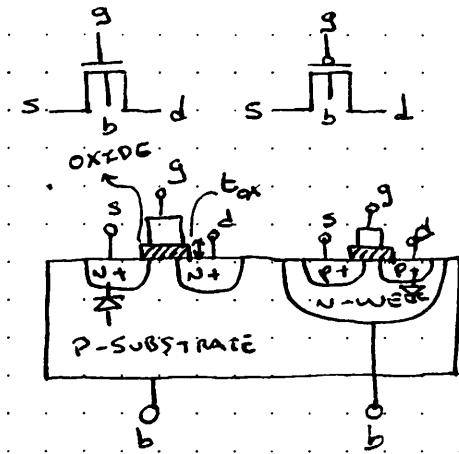


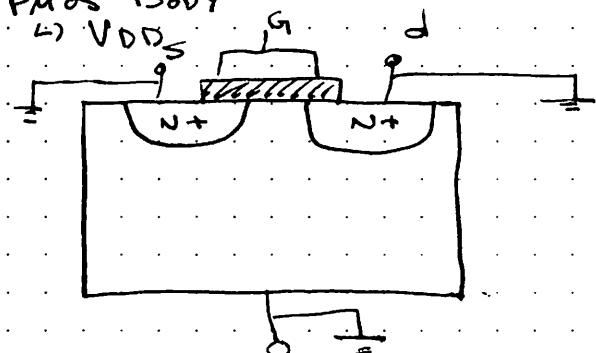
SEPT 5, 2018

PHYSICAL REALIZATION OF NMOS & PMOS



NMOS BODY
↳ GND

PMOS BODY
↳ VDD



CARRIER VELOCITY
 $V = \mu n E$

$$E = \frac{V_{ds}}{L}$$

$$I_{ds} = \frac{Q}{L/v} = \mu n C_{ox} \frac{W}{L} \left(V_{gs} - V_{th} - \frac{V_{ds}}{2} \right) V_{ds}$$

$$V_{ds} \ll V_{eff} \rightarrow I_{ds} = \beta_n V_{eff} V_{ds}$$

SUMMARY

REGION	CONDITIONS	CURRENT
CUTOFF	$V_{gs} < V_{th}$	$I_{ds} = 0$

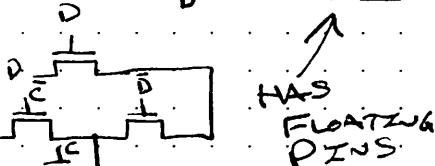
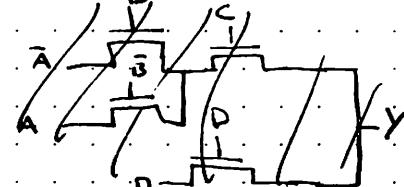
LINEAR
 $V_{gs} > V_{th}$
 $V_{ds} \ll V_{eff}$

LINEAR
 $V_{gs} \geq V_{th}$

SATURATION
 $V_{gs} \geq V_{th}$
 $V_{ds} \geq V_{eff}$

WARM UP: PASS LOGIC

$$y = (A \oplus B) C + D$$



HAS FLOATING PINS

DRAINED CURRENT DERIVATION

$$I_{ds} = f(V_{gs}, V_{ds}, \dots)$$

$$Q_L = (V_{gs} - V_{th}) C_g$$

$$C_g = C_{ox} W L$$

$$\frac{dQ_L}{dV_{ds}} = \frac{C_g}{C_{ox}}$$

$$K_{ox} = 3.9 \text{ fm}^{-2}$$

$$C_{ox} = \frac{\epsilon_0}{t_{ox}}$$

$$\epsilon_0 = 8.85 \text{ e-14 F/m}$$

$$I_{ds} \approx I_{ds0} + \frac{\partial I_{ds}}{\partial L} \frac{\partial L}{\partial V_{ds}} \Delta V_{ds}$$

$$\frac{\partial X_d}{\partial V_{ds}}$$

$$I_{ds} = \frac{1}{2} \beta_n V_{eff}^2 (1 + \lambda (V_{ds} - V_{eff}))$$

λ = CHANNEL LEN. MODULATION COEFF.

$$\lambda = \sqrt{J}$$

$$I_{ds} = \beta V_{eff} V_{ds}$$

$$I_{ds} = \beta (V_{eff} - \frac{V_{ds}}{2}) V_{ds}$$

$$I_{ds} = \gamma \beta V_{eff}^2$$

SEPT 12, 2018

WARM UP ~~A~~

$$Y = \overline{AB} + (\overline{CD} + E)(\overline{F} + G)$$

↳ DRAW CMOS SCHEMATIC

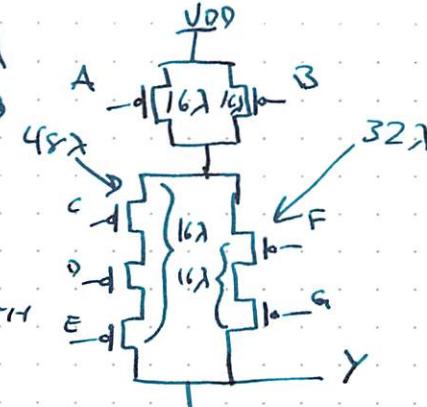
↳ SIZE THE TRANSISTORS

FOR EQUAL DRIVE STRENGTH

$$\hookrightarrow W_{NMOS, NMOS} = 4\lambda$$

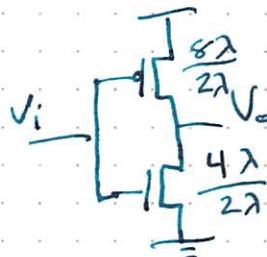
$$\hookrightarrow \mu_N = 2 \mu_D$$

(16-3) A



SIZE:

START w/ INVERTER



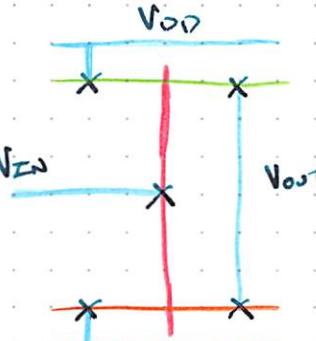
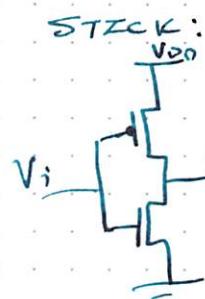
OF ~~SERIES~~
PATHS TO GND
FOR NMOS



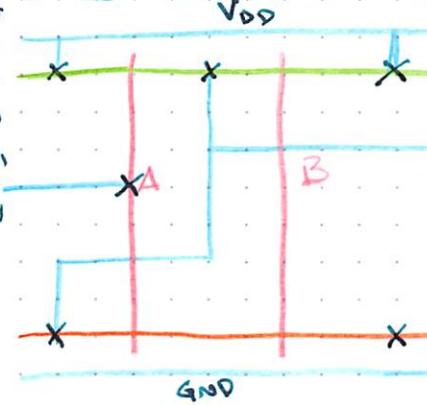
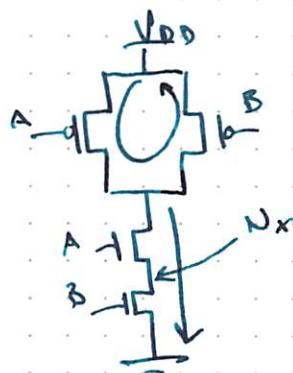
PMOS : (SEGMENTS IN) (BASE PMOS)
(SERIES)

CHECK : GO DOWN AUX PATH & ADD WIDTHS
↳ SHOULD ADD TO BASE WIDTH
FOR PATH

LAYOUT:



- METAL 1
- P-DIFFUSION
- N-DIFFUSION
- POLY
- CONTACT



CELL
EULER'S PATH
↳ PATH IN PULL UP
THAT CORRESPONDS
TO SAME ORDER IN
PULL DOWN

PUN:

VDD - A - VOUT - ~~B~~ - VDD

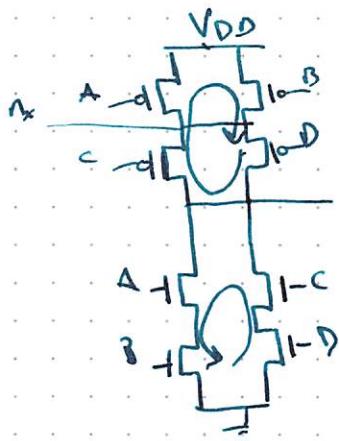
PDN:

VOUT - A - Nx - B - GND

SEP 17:

WARM UP:

DRAW A STACK DIAGRAM FOR $Y = \overline{AB} + CD$



PDN: D - C - Y - A - B - GND

PUN: D - Y - C - A - VDD - B - Nx

I TOOK LIKE NO NOTES
THIS DAY

RIPPERONI

Woot

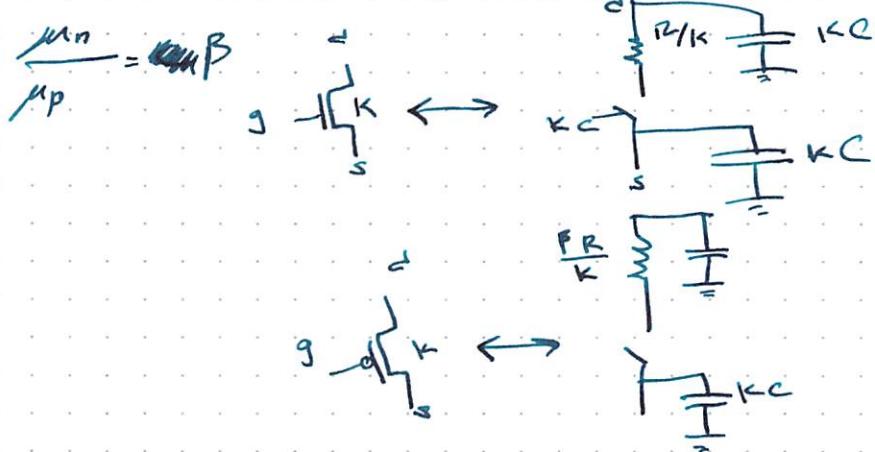
SEPT. 24.

EXAM 1: WED, OCT 3
CH #41-5

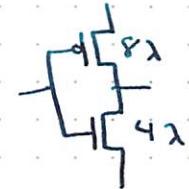
DELAY MODELS:

RC DELAY

- IDEA: MODEL EACH TRANS. AS AN IDEAL SWITCH IN SERIES w/ A RESISTOR



K = $\frac{I}{I_{\text{unit}}}$ OF TIMES LARGER THAN UNIT TRANSISTOR



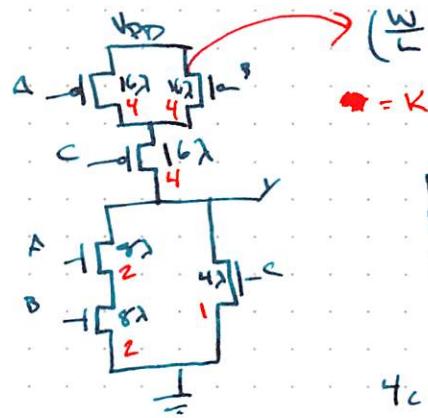
- DRAW EQ. CURRENT FOR t_{on} , t_{off} , t_{cr} , t_{tot}

3) $t = \sum_j \sum_i R_i C_j$

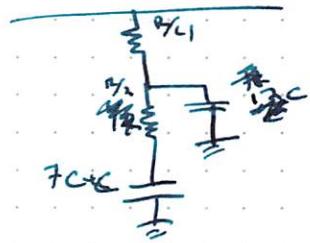
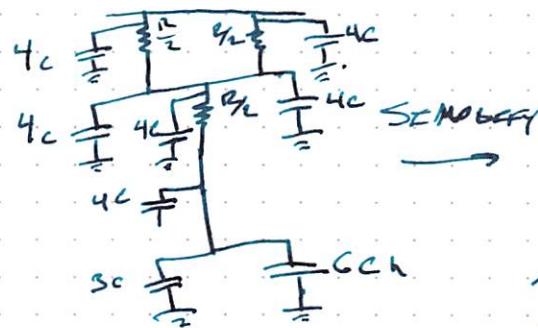
$i = \text{SOURCE} \rightarrow j$

HELLO

Ex: $Y = \overline{AB} + C$ $\mu n = 2 \mu p$



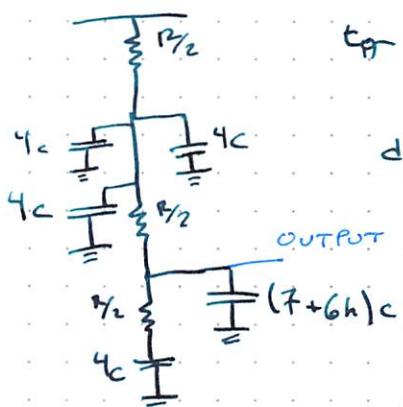
FIND t_{cr} WHEN Y IS CONNECTED TO h OTHER IDENTICAL GATED DRIVING INPUT A



$t_{\text{cr}} = \frac{R}{4} C_{\text{cr}} + (\gamma_{\text{q}} + \gamma_{\text{r}})(7h + h) C_{\text{tot}}$

FIND t_{pr}

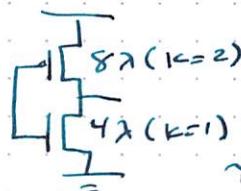
$A=1, B=0, C=0$



$$t_{pr} = R_2(4C) + ($$

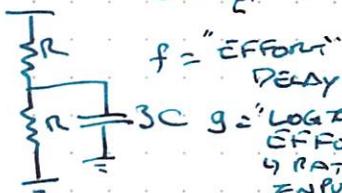
$$t_{pr} = \frac{R_2}{2}(4C) + (R_2 + R_2)(7+6h)c + R(4c)$$

$$= (7+6h)RC$$



$$\Sigma' = 3RC$$

$$d = \frac{t}{\Sigma'} = f + p = gh + p$$



f = "LOGICAL EFFORT"
DELAY
 g = "LOGICAL EFFORT"
INPUT CAP. OF GATE
TO INPUT CAP. OF UNIT INVERTER

h = "ELECTRICAL EFFORT"
AKA "FAN OUT"

Cout
Cin

P = "PARASITIC DELAY"
↳ NO LOAD DRIVING

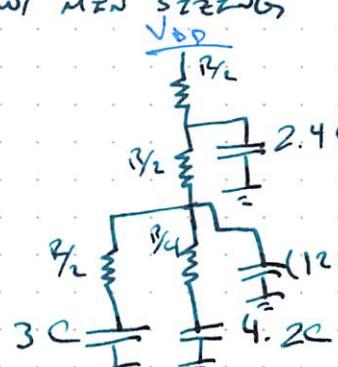
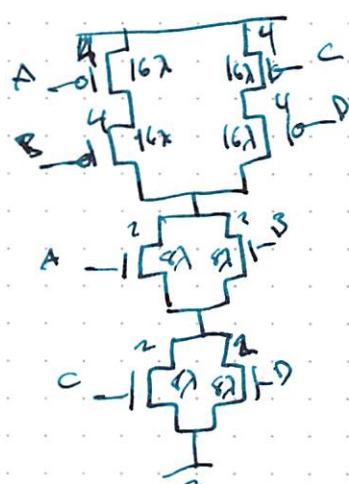
26 SEPT, 2018

CALC RISING PROP. DELAY OF $y = \overline{(A+B)(C+D)}$

↳ WHAT IS THE LOGICAL EFFORT

↳ WHAT IS THE PARASITIC DELAY

↳ WHAT IS THE DRIVE W/ MIN SIZING



$$(R_2)8C + R(12+8+8+6h)c$$

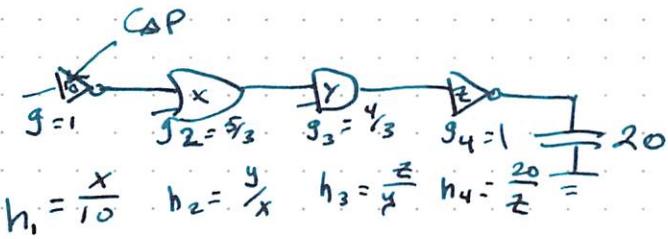
$$t_{pr} = 6hRC + 32RC$$

$$g = 2 = \frac{6RC}{\Sigma'}$$

$$P = \frac{32}{3}$$

$$\text{DRIVE: } X = \frac{C_{in}}{3g}$$

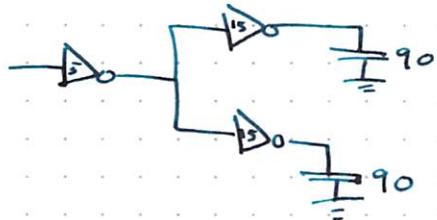
DELAY IN A MULTISTAGE NETWORK



PATH LOGICAL EFFORT: $G \equiv \prod g_i$

PATH ELECT. EFFORT: $H \equiv \frac{C_{OUT}(\text{PATH})}{C_{IN}(\text{PATH})}$

PATH EFFORT $\rightarrow F \equiv \prod f_i = \prod g_i h_i$



$$G = 1 \cdot 1 = 1$$

$$H = \frac{90}{5} = 18$$

$$F = (1 \cdot \frac{30}{5})(1 \cdot \frac{90}{15}) \\ = 3G \neq GH$$

BRANCHING EFFORT $\rightarrow b_i = \frac{C_{ON PATH} + C_{OFF PATH}}{C_{ON PATH}}$

PATH BRANCHING EFFORT $\rightarrow B = \prod b_i$

$$F = GBH$$

$$D = \sum d_i = D_F + P$$

D_F = PATH EFFORT DELAY
 $= \sum f_i$

P = PATH PARAMETRIC DELAY
 $= \sum p_i$

$$D = NF + P$$

OCT 1, 2018

WHAT IS POWER?

- $P(t) = \frac{dW}{dt} \rightarrow$ RATE OF WORK @ ANY GIVEN TIME
- $W = F(d) \rightarrow$ WORK = FORCE (DIST.)
- $P(t) = \frac{d}{dt} \int \vec{F} \cdot d\vec{s}$

WHAT IS VOLTAGE?

- $V(t) = \frac{W}{Q} \rightarrow$ work / charge

INSTANTANEOUS

$$P(t) = \frac{dW}{dt} = \frac{\text{POWER}}{\frac{d}{dt} V(t) Q} \equiv V(t) \frac{dQ}{dt} = V(I)$$

ENERGY:

$$E = \int_0^T P(t) dt$$

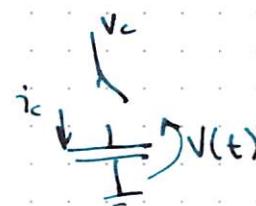
Avg. Power:

~~$$P_{\text{AVG}} = \frac{E}{T} = \frac{1}{T} \int_0^T P(t) dt$$~~

RESISTORS:

$$P_R = VI = I^2 R = V^2/R$$

POWER SUPPLY
POWER ZONE



CAPACITORS:

$$E_C = \int_0^\infty V(t) i(t) dt$$

$$= \int_0^\infty V(t) \frac{dV(t)}{dt} C dt$$

$$= C \int_0^\infty V(t) dV = \frac{1}{2} CV_c^2 = E_C$$

$$Q = V_C$$

$$i = \frac{dV}{dt} C$$

TOTAL Power Consumption

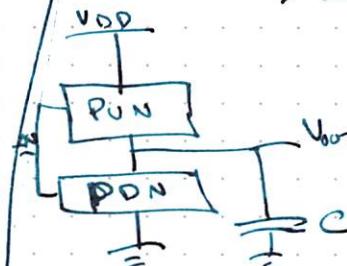
$$P_{\text{TOTAL}} = P_{\text{DYNAMIC}} + P_{\text{STATIC}}$$

P_{DYNAMIC} : Power consumed when circuit is "DOING STUFF"

P_{STATIC} : Power consumed when circuit is IDLE

$$P_{\text{DYNAMIC}} = P_{\text{SWITCHING}} + P_{\text{SHORT CIRCUIT}} + P_{\text{GATE}}$$

$\approx 90\%$



$$T = \frac{1}{\alpha f}$$

α : SWITCHING ACTIVITY PERIOD FACTOR

$$\begin{aligned} P_{\text{SWITCHING}} &= \frac{1}{T} \int_{-\infty}^{\infty} V_{DD}^2 i_{DD}(t) dt \\ &= \frac{1}{T} \int_0^{\infty} V_{DD} C \frac{dV_{out}}{dt} dt \\ &= \frac{1}{T} C V_{DD} \int_0^{\infty} dV_{out} \\ &= \frac{1}{T} C V_{DD}^2 = E_C \end{aligned}$$

$$P_{\text{SWITCHING}} = \alpha C V_{DD}^2 f$$

$$\alpha = \frac{P_{\text{on}}(\text{OUT} = '0') P_{\text{on}}(\text{OUT} = '1')}{P_Y P_Y} = (1 - P_Y) P_Y$$

Clouds HAVE $\alpha = 1$



$$P_Y = P_A P_B P_C$$

$$= (0.5)(0.5)(0.5) = \frac{1}{8}$$

$$(1 - P_Y) = \frac{7}{8} = \alpha$$

$P_{\text{short circuit}} = \text{POWER CONSUMED FROM } i_{VDD \rightarrow GND}$

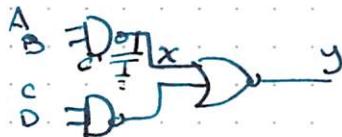
$$P_{\text{static}} = (I_{\text{sub}} + I_{\text{gate}} + I_{\text{drain}} + I_{\text{concentration}}) V_{DD}$$

$$\text{From } I_{\text{sub}} = \frac{(V_{GS} - V_{DS}) - R_s V_{DS}}{S}$$

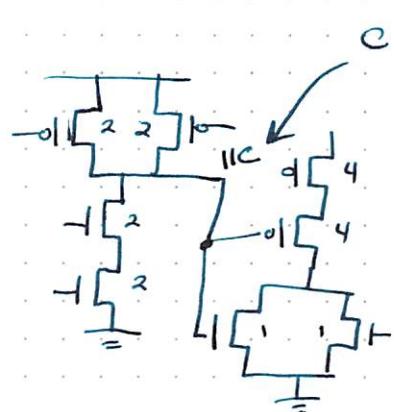
$$I_{\text{sub}} = I_{\text{off}} = 10^{-1}$$

25 LECTURE
OCT 16, 2018

WARM UP:



- A, B, C, D HAVE SWITCHING PROBABILITY OF 0.5
- $V_{DD} = 1V$
- $C = 2.24 \text{ fF}$
- $f = 1 \text{ GHz}$



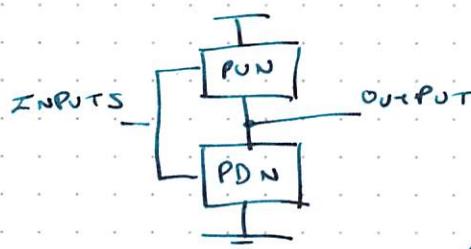
WHAT IS THE SWITCHING POWER @ X

$$P_x = 1 - P(A)P(B) = 0.75$$

$$\alpha = (0.75)(0.25) \\ = 0.1875$$

$$P = \alpha C V_{DD}^2 f \\ = (0.1875)(2.24 \times 10^{-15})(1)^2 (1 \text{ GHz}) \\ = 4.2 \text{ pW} = 4.20 \text{ nJ}$$

COMP. (STATIC) CMOS



Pros:

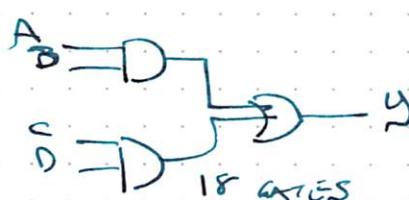
- GOOD NOISE MARGINS
- FAST
- GOOD POWER CONSUMPTION (STATIC)
- GOOD VARIATION TOLERANCE
- RELATIVELY SIMPLE TO DESIGN
- MOST WIDELY USED TODAY

Cons:

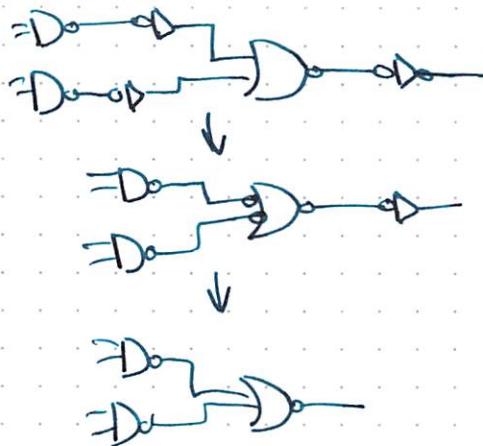
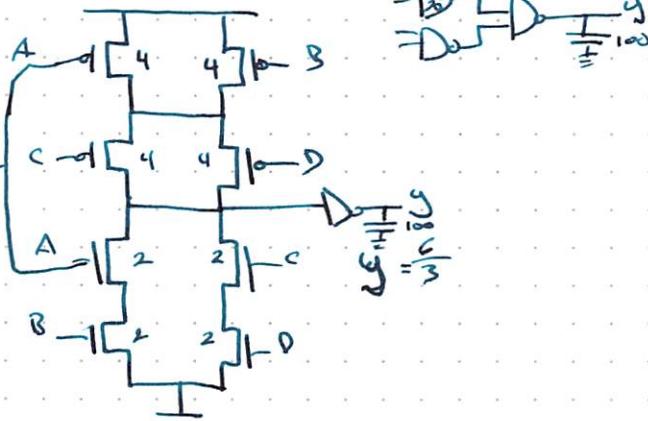
- LARGE AREA
- NOT ALWAYS BEST w/ POWER CONSUMPTION (DYNAMIC)

BUBBLE PUSHING

- IDEA: CONVERT AND-OR LOGIC TO NAND-NOR LOGIC USING DEMORGAN'S LAW
 $\neg(\bar{A}\bar{B}) = \bar{A} + \bar{B}$
 $\neg(\bar{A} + \bar{B}) = \bar{A}\bar{B}$



$$Y = AB + CD = \overline{AB + CD} \\ = (\overline{AB})(\overline{CD})$$



COMPOUND

$$H = \frac{100}{20} = 5$$

~~2019年4月22日~~

$$G = \{3\}$$

$$\text{so } p = \frac{12}{3} + 1 = 5$$

$$\text{PATH EFFORT} \rightarrow F = HGB = 10$$

MAXIMUM STAGE EFFORT

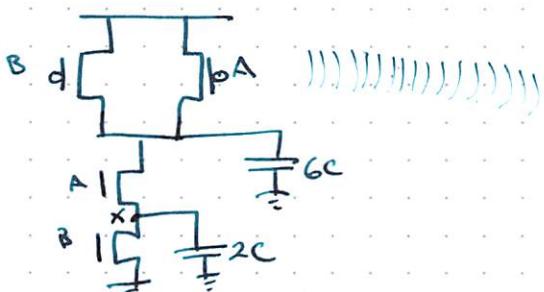
$$f = F \xrightarrow{\text{# OF STAGES}} = 10^{\frac{1}{2}} = 3.2$$

$$D = N_f \hat{f} + p \\ = 6.4 + 5 = 11.4 \approx$$

$$D = 10$$

GATE INPUT ORDERING

- ↳ DIFF. INPUTS HAVE
DIFF LOGICAL EFFORTS
& PARALLEL DELAYS
 - ↳ EVEN FOR SIMPLE GATES LIKE
NAND, ORDER OF INPUTS
MATTERS



CASE 1:

$$A = 1$$

B: 0 → 1

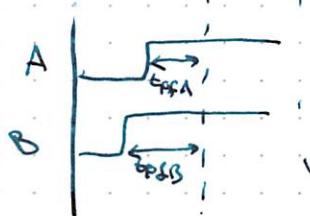
$$t_{pf} = \left(\frac{R}{2}\right)2C + R(6C) = 12.58 \text{ sec}$$

CASE 2:

$$A = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix}, B = \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix}$$

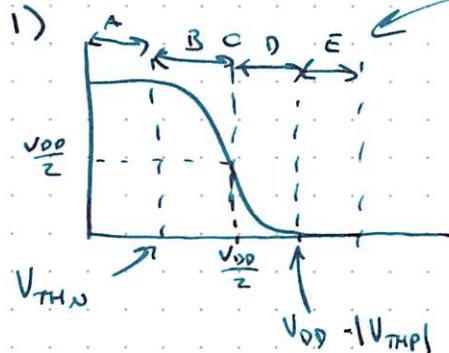
$$t_{\text{pf}} = R C = 2 \approx$$

- "OUTER INPUTS"
 - ↳ CLOSEST TO SUPPLY
- "INNER INPUTS"
 - ↳ CLOSEST TO OUTPUT
- PARASITIC DELAY IS LOWEST WHEN INNER INPUTS SWITCH LAST
- 2.33 • LATE SIGNALS SHOULD
 - 1 BE CONNECTED TO INNER INPUTS

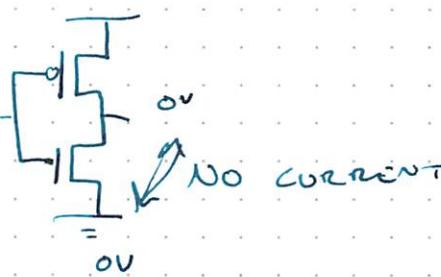


Oct 17, 2018

REVIEW EXAM 1:



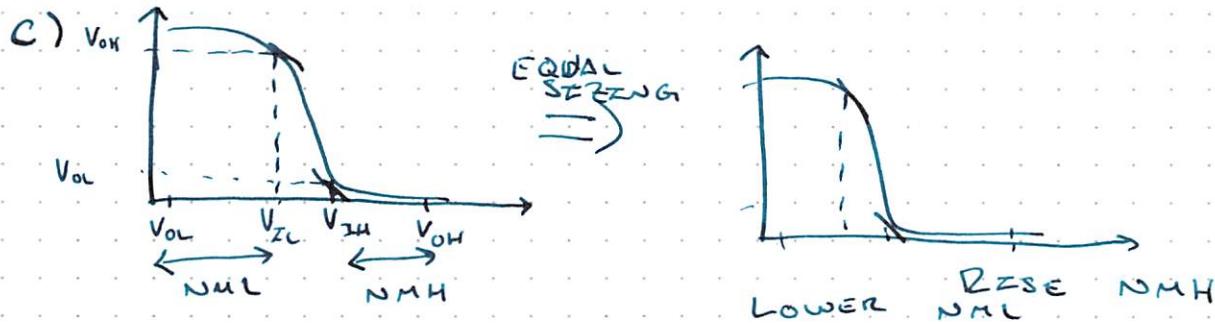
No current through NMOS @ E



$$1a) C \quad b) I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TN})^2$$

$$= \frac{1}{2} \beta \left(\frac{V_{DD}}{2} - V_{TN} \right)^2$$

$$= 21.9 \times 10^{-5} \frac{A}{V^2} (V_{EFF})^2$$



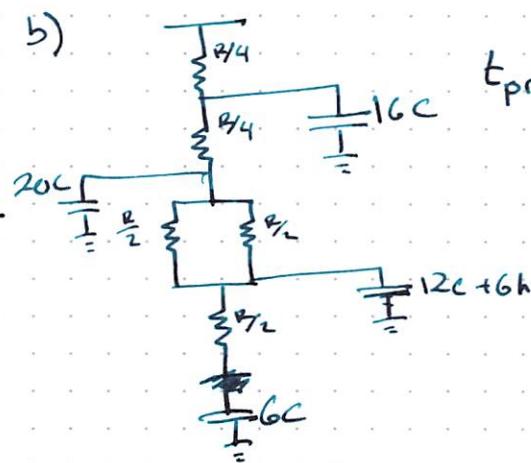
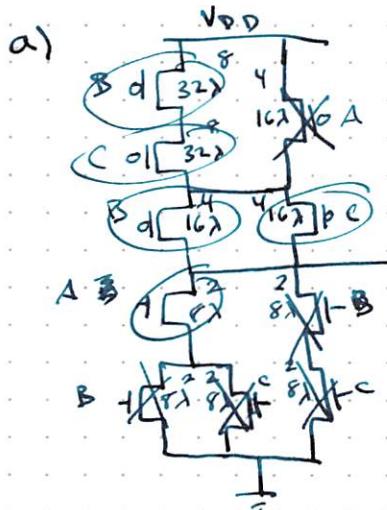
d) 1 - MEN METAL 1

2 - MN SURROUND OF WELL

3 - WIDTH OF POLY

4 → Surround of contact

$$3) \quad y = \overline{A(B+c) + BC} \quad A=1, \quad B=0, \quad C=0$$

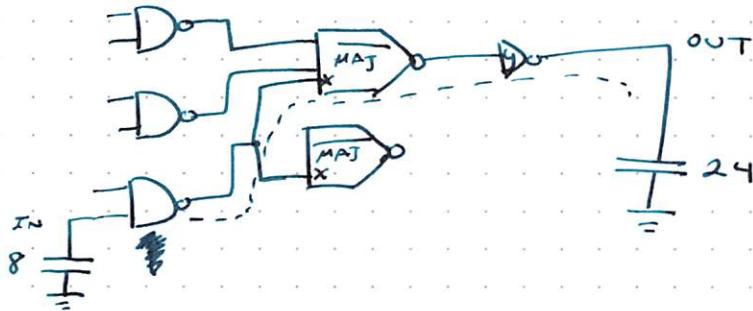


$$t_{pr} = \frac{\beta_4}{4}(16c) + \frac{\beta_2}{2}(20c) \\ + \frac{3\pi^2}{4}(12c + 6h) \\ + \frac{3\pi^2}{4}(6c)$$

$= 27.5 \text{ rc} + 4.5 \text{ rch} + 6h$

$$3. c) \quad g = \frac{4 \cdot 5}{3} = \frac{3}{2} \quad P = \frac{27 \cdot 5}{3} = \frac{55}{c}$$

4)



$$a) \quad D = N F^{\gamma_N} + P$$

$$\begin{array}{l} \text{SUM OF} \\ \text{DELAYS} \\ \text{ON PATH} \end{array} \quad N = 3 \quad P = 2 + \frac{55}{6} + 1 = \frac{91}{6}$$

NAND

$$F = G B H$$

$$H = \frac{24}{8}$$

$$B = (1) \left(\frac{x+x}{x} \right) (1)$$

$$= 2$$

$$G = \left(\frac{4}{3} \right) \left(\frac{5}{2} \right) (1) = 2$$

NAND

$$F = 12$$

$$D = (3)(12)^{\frac{1}{3}} + \frac{91}{6} \boxed{19.1}$$

$$b) \quad h_i = \frac{C_{out,i}}{C_{in,i}}$$

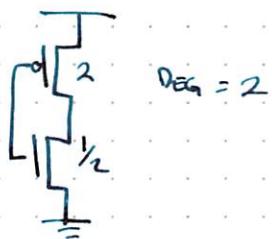
$$f_i = g_i h_i$$

$$C_{in,i} = \frac{g_i C_{out,i}}{f_i}$$

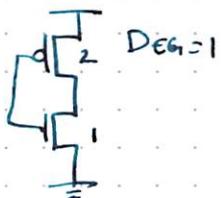
SKewed GATES

- ↳ USED WHEN ^{OUTPUT} TRANSITION IS MORE IMPORTANT THAN THE OTHER
- ↳ HI-SKew - FAVOR $0 \rightarrow 1$
- ↳ LO-SKew - FAVOR $1 \rightarrow 0$
- ↳ DEG. OF SKewing = $\frac{R_t}{R_s} \in [1, \infty)$

HI SKew



UNskewed



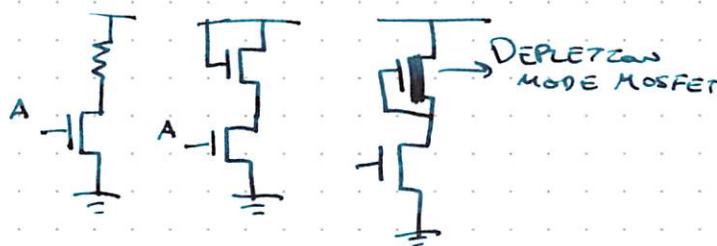
Lo SKew



LOG. EFFORT FOR RISING TRANSITION
 $g_d = \frac{2.5}{1.5}$

$$g_d = \frac{2.5}{1.5}$$

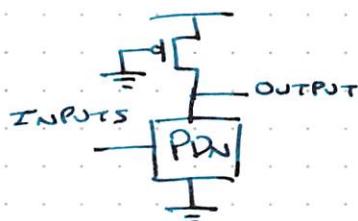
RATIOED CIRCUITS



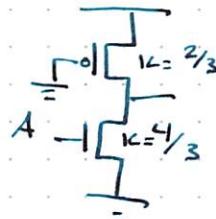
PROS

- ↳ REDUCED SIZE

"PSEUDO NMOS"



- USUALLY $\sim \frac{1}{3} - \frac{1}{6}$ SIZE OF MIN. NMOS IS GOOD FOR PUN PMOS



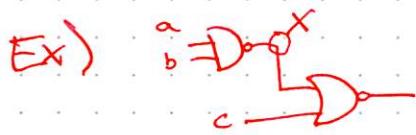
OCT 22, 2018

QUIZ NEXT WED (OCT 31)

~~TOPIC~~

↳ POWER

↳ COMB. LOGIC FAMILIES



$$P_{\text{Diss}} = P_{\text{SW}} + P_{\text{GATE}}$$

SHOULD BE

MOST \rightarrow ALL

$$\therefore P_{\text{Diss}} - P_{\text{SW}} = \alpha C V_f^2$$

$$= \sum P_{\text{SW},i}$$

To FIND Active Factor:

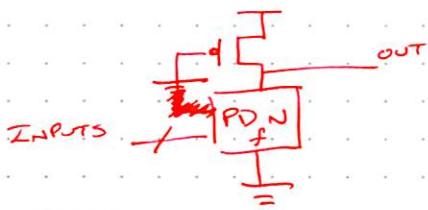
0	0	1
0	1	1
1	0	1
1	1	0

$$\alpha_x = P_1 (1 - P_0)$$

$$= \frac{3}{4} \left(\frac{1}{4} \right) = \frac{3}{16}$$

RATIOED CIRCUITS

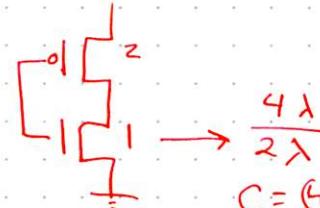
↳ PSEUDO-NMOS



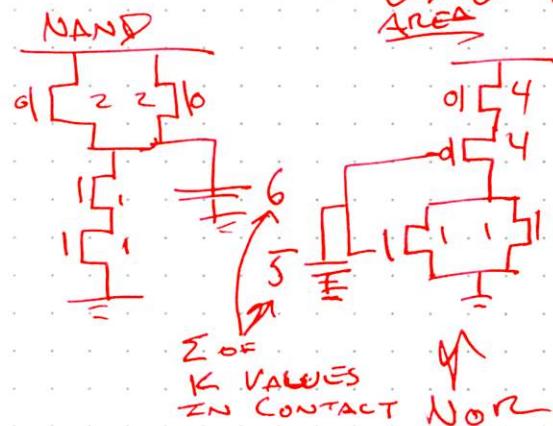
Pros:

- ↳ REDUCED SIZE
- ↳ REDUCED LOGICAL EFFORT

- Cons:
- ↳ WEAKISH '1's
 - ↳ WEAK '0' due to STRNGTH
 - ↳ CONSTANT
 - ↳ Power DISSIPATION
 - ↳ WHEN OUTPUT IS '0'

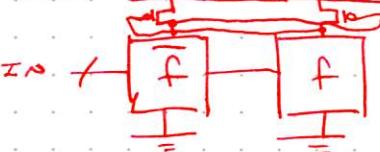


$$C = (4\lambda \times \lambda) \frac{k_{\text{ox}} \epsilon_0}{t_{\text{ox}}} \text{ AREA}$$



Σ OF K VALUES IN CONTACT NOR

CASCODE VOLTAGE SWITCH LOGIC (CVSL)



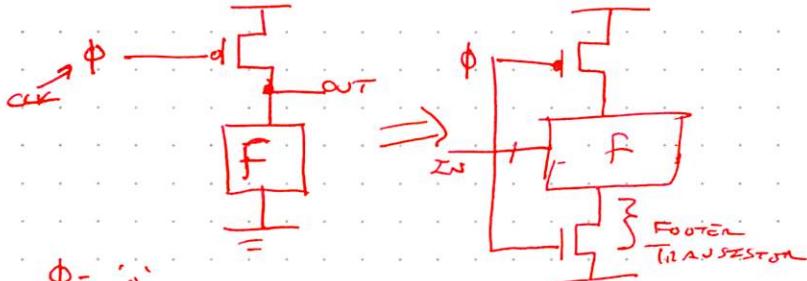
ADVANTAGE

- ↳ NO STATIC POWER

DISADVANTAGES

- ↳ NEED TRUE & COMP. NETWORKS
- ↳ REAL BIG
- ↳ STILL USUALLY SLOWER

DYNAMIC LOGIC



$$\phi = '0'$$

↳ PRE-CHARGE

$$\phi = '1'$$

↳ EVALUATE

- FASTEST COMMONLY

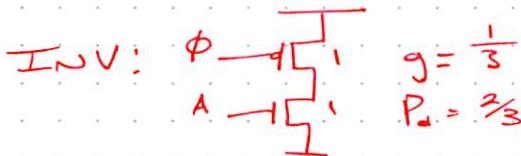
- USED LOGIC STYLE

- ↳ RAZED

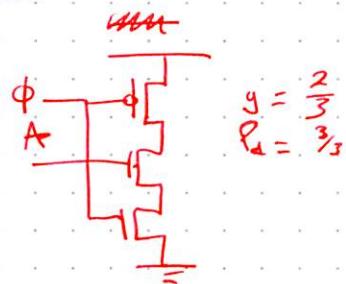
- ↳ NO CONTENTION

- ↳ NO SLOW RISING TRANS.

- PRE CHARGE TRANSISTOR $\approx 2 \times R$

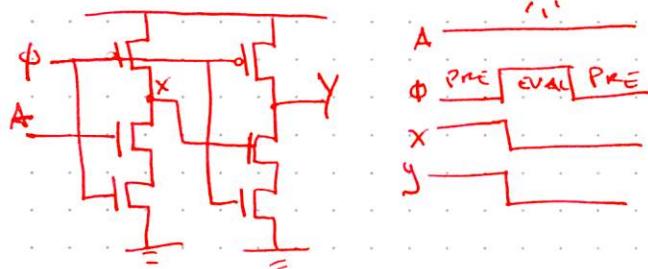


INFooted:

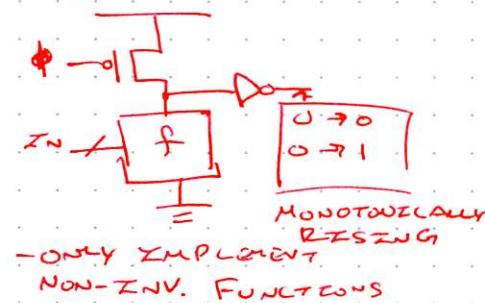


STATIC: $g_d = 1$
 $P_d = 1$

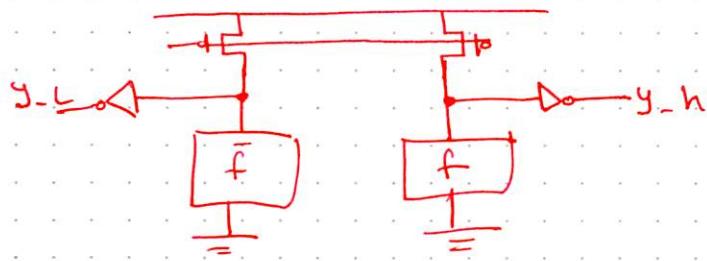
MONOTONICITY PROBLEM



Domino Logic



DUAL-RAIL DOMINO LOGIC

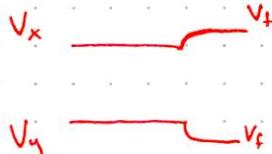
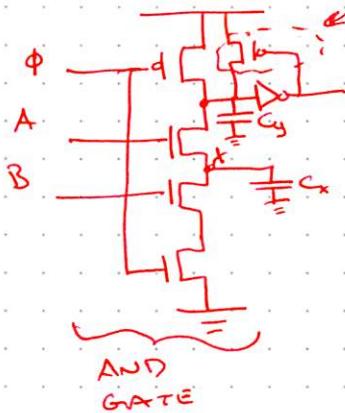


SIG-H	SIG-L	MEANING
0	0	PRE-CHARGED
0	1	'0'
1	0	'1'
1	1	FORBIDDEN (SHOULD NEVER HAPPEN)

DOMINO - CONT

CHARGE
KEEPER,
STOPS
CHARGE
SHARING

DURING EVAL:
 $B \rightarrow 0, A \rightarrow 1$



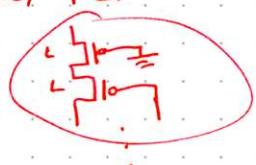
$$V_f = V_x = V_y \\ = \frac{C_y}{C_x + C_y} V_{dd}$$

WANT KEEPER TRANSISTOR

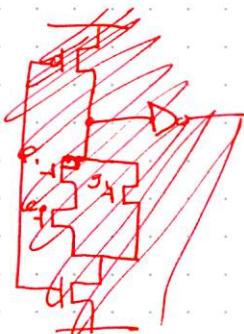
TO BE $\approx \frac{1}{2}$ STRENGTH OF
UNIT SIZED NMOS

- $W_P = W_{MIN}$
- INCREASE $L \rightarrow 2L$

\downarrow
CAN SPLIT TO
2 TRANSISTORS
w/ $1L$



$$\begin{aligned} C_1 &= g_1 + p_1 C_0 \\ C_2 &= g_2 + p_2(g_1 + p_1 C_0) \\ C_3 &= g_3 + p_3(g_2 + p_2(g_1 + p_1 C_0)) \\ C_4 &= g_4 + p_4(g_3 + p_3(g_2 + p_2(g_1 + p_1 C_0))) \end{aligned}$$



OCT 29, 2018

QUIZ WED. ~2-3 QUESTIONS

↳ Power

↳ COMB. CIRCUIT DESIGN

A	B	CIN	COUT	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
1	0	0	0	1
1	0	1	1	0
1	1	0	1	1
1	1	1	1	1

KILL $\rightarrow A=0, B=0$

PROPAGATE $\rightarrow A \oplus B = 1$

GENERATE $\rightarrow AB = 1$

$$S_i = \text{Prop}_i + \text{Generate}_{i-1:0} = P_i + C_{\text{in},i}$$

GROUP PG ADDENDS

$$G_{i:j} = G_{i:k} + G_{k-1:j} P_{i:k} \quad \text{Worst case ADDER: } P_i = 1 \quad i = 1 \dots n$$

$$C_{\text{out},i} = G_{i:i:0} = C_{\text{in},i+1}$$

$$P_{i:j} = P_{i:k} P_{k-1:j}$$

COST: $O(N)$

WORST THING
TO ADD B/C
THE CARRY
THROUGH PROPS
THROUGH THE
WHOLE THING.

BEST CASE:

$$\begin{array}{r} 10110111 \\ 10110111 \\ \hline 11011011 \end{array}$$

ALL PROPAGATE
BITS = 0

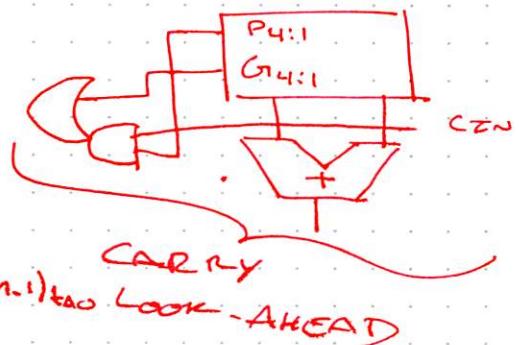
$$\begin{array}{r} 10101101 \\ 01100110 \\ \hline 11011011 \end{array}$$

PROP SIGNAL \rightarrow XOR

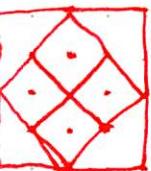
FIG 11.22 = Book

$$t_{cs} = t_{pg} + 2(n-1)t_{ao} + (k-1)t_{mux} + t_{xor}$$

$$t_{ca} = t_{pg} + t_{pg}(n) + (k-1)t_{ao} + t_{xor} + (n-1)t_{ao} \text{ LOOK-AHEAD}$$



PROJECT: EDGE DETECTION (YAY, EVEN MORE...)



IN VHDL??

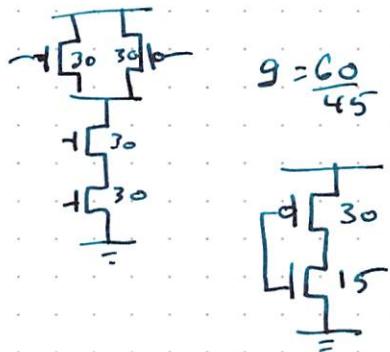
↳ JUST COMBINE RECONFIG & DECODE ...
 ↳ ~~NO CLASS WORK~~

Oct 31, 2018

QUIZ DAY

LOGICAL EFFORT: $g \equiv \frac{\text{INPUT GATE}}{\text{UNIT INV}^*}$

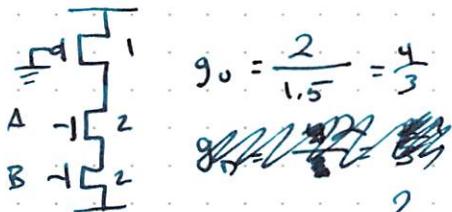
* UNIT INV. MUST HAVE SAME DRIVE STRENGTH



$$g = \frac{60}{45} = \frac{4}{3}$$

NOT DEPENDANT
ON TRANSISTOR
SIZES

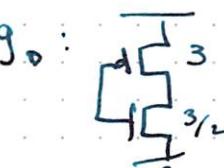
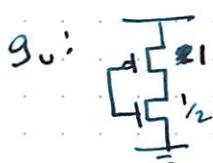
PSEUDO-NMOS



$$g_o = \frac{2}{1.5} = \frac{4}{3}$$

~~8/22/2018~~

$$g_o = \frac{2}{4.5} = \frac{4}{9}$$



$$2 - \frac{1}{2}(1) = \frac{3}{2}$$

~~Oct~~ Nov 5, 2018

ADDITION:

1) BITWISE P.G (PROPAGATE & GENERATE)

$$P_i = A_i \oplus B_i$$

$$G_1 = AB$$

2) Group P, G

$$P_{i:j} = P_{i:k} P_{k+1:j}$$

$$G_{i:j} = G_{i:k} + P_{i:k} G_{k+1:j}$$

$$3) \text{ Sum} = \sum S_i = P_i \oplus G_{i-1,0}$$

Czn

A	0 1 1 1 0 1 1 0 0 1 0 0 1 1 0 1
B	0 1 0 0 1 1 0 1 1 1 0 0 0 1
P	0 0 1 1 1 0 1 1 1 0 1 0 1 0 0 0 1 8
G	0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 1 0

$$P(\text{carry-zero}) = 0$$

$$G(c_{zn}) = c_{zn}$$

Group P	0	0	0	0	0
Group G	0	1	1	1	1
Group O	0	1	1	1	1

← AND OF ALL SIGNALS WITHIN GROUP

← PROPAGATE (xor) until GENERATE

$$G_{1,1:0} = G_{1,1} + P_1 G_{1,0}$$

$$\begin{array}{l} A : \boxed{1} \ 0 \ 1 \ 1 \ 0 \ 0 \ 1 \ 0 \ 0 \ 1 \ 1 \ 0 \ 0 \ 1 \ 0 \ 1 \\ B : \boxed{0} \ 1 \ 1 \ 0 \ 1 \ 1 \ 0 \ 1 \ 0 \ 1 \ 0 \ 0 \ 1 \ 1 \ 0 \\ P_1 : \boxed{1} \ 1 \ 0 \ 1 \ 1 \ 1 \ 1 \ 1 \ 0 \ 0 \ 0 \ 0 \ 0 \ 1 \ 1 \\ G_1 : \boxed{0} \ 0 \ 1 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 1 \ 1 \ 0 \ 0 \ 1 \ 0 \ 0 \\ LVP : \boxed{1} \ 0 \ 1 \ 1 \ 0 \ 0 \ 1 \ 0 \ 0 \ 1 \ 1 \ 0 \ 0 \ 1 \end{array}$$

LOOK @ THESE
FOR WHETHER A
BIT PROPS OR GENS
IGNORE A & B FROM NOW ON

SEQUENTIAL CIRCUIT DESIGN

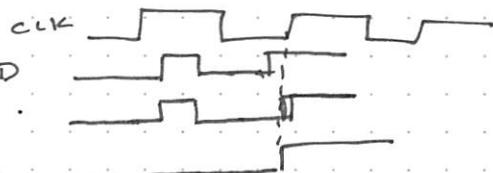
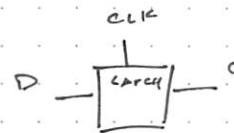
↳ DEPENDS ON CURRENT INPUT & STATE

LATCH

↳ LEVEL SENSITIVE

↳ TRANSPARENT LATCHES

↳ D - LATCHES



Flop

↳ EDGE SENSITIVE

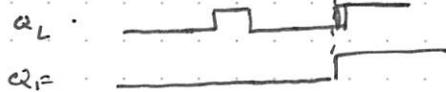
↳ TYPES

↳ MASTER-SLAVE CONFIGURATIONS

↳ DFF

↳ JKFF

↳ TFF

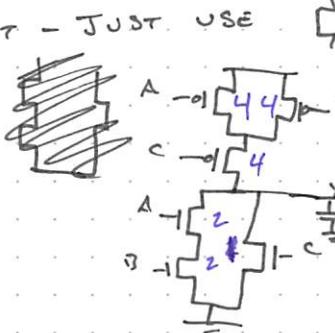


QUIZ 2 REVIEW: - EXAM (Possibly week after next)

$$1) Y = \overline{AB} + C$$

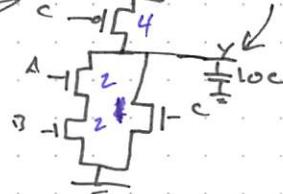


EASIEST - JUST USE



$$P_{SW} = \alpha C V_{dd}^2 f$$

PC (PARASITIC)



A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

$$\alpha = \left(\frac{3}{8}\right)\left(\frac{5}{8}\right) = \frac{15}{64}$$

C:



$$C' = A_{MN} C_{ox}$$

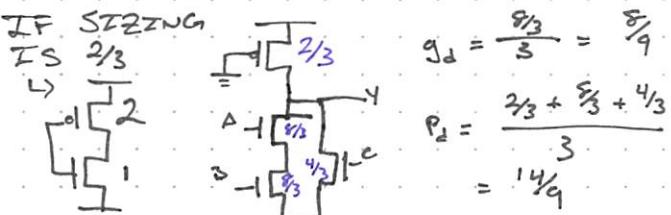
$$= A_{MN} K_{ox} E_0$$

$$= (180\text{ nm})(360\text{ nm}) \frac{C_{ox}}{4.1\text{ nm}} \left(\frac{3.9}{(8.85 \times 10^{-12})} \right)$$

$$= 0.546 \text{ fF}$$

$$P_{SW} = \frac{15}{64} (17 (0.546 \text{ fF}) (1.8V)^2 (1 \text{ GHz})) = 7.049 \mu\text{W}$$

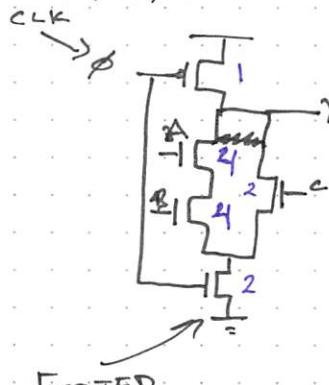
2) a) PSEUDO-NMOS



$$g_d = \frac{\frac{2}{3}}{3} = \frac{2}{9}$$

$$P_d = \frac{\frac{2}{3} + \frac{2}{3} + \frac{4}{3}}{3} = \frac{14}{9}$$

b) DYNAMIC LOGIC



GATE INPUT
SIZE

$$g_d = \frac{4}{3}$$

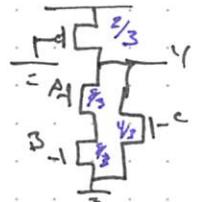
$$P_d = \frac{7}{3}$$

UNIT ZN.V.
SIZE

FOOTED

Q2 BONUS:

STATIC Power Consumption:



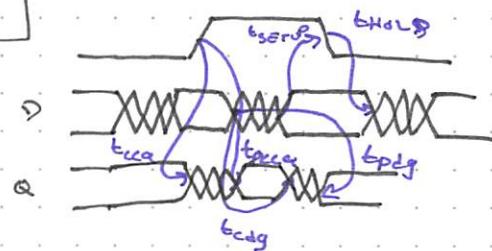
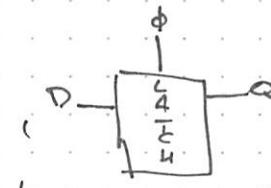
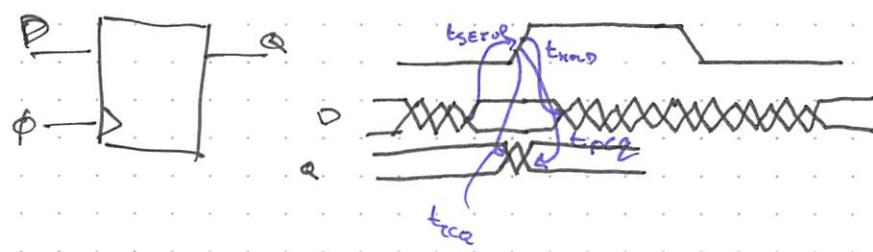
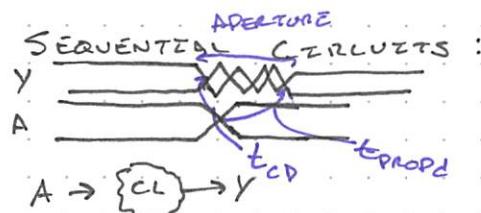
$$I_d(V_{dd})$$

$$\frac{1}{2} \mu_P C_{ox} \frac{W}{L} (|V_{gs}| - |V_{op}|)^2 (V_{dd})$$

$$\sim 590.7 \mu\text{W}$$

ASSUME
PMOS IS
SATURATED

B/C PULL-DOWN
SHOULD BE ON.
Vds WOULD BE
0V \therefore SAT



LATCH DESIGN:



CONS:

- WEAK '1' (V_t DROP)
- BACKDRIVING
- LEAKAGE
- DYNAMIC
(WHEN CLK = '0'
FLOATING NODE)
- NON-RESTORING
- OUTPUT NOISE
- DIFFUSION INPUT

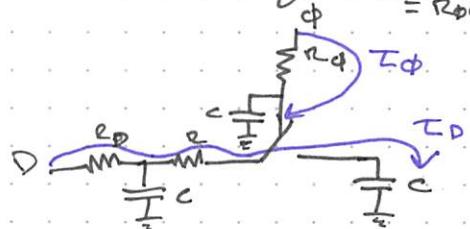
PROS:

- SMALL
- SMALL CAP. LOAD
- ON CLOCK

$$t_{pq} = \tau_\phi + \tau_0$$

$$= R_D C + R_D C$$

$$+ (R_D + R) C$$



$$t_{pdg} = \underbrace{R_D C + (R_D + R) C}_{\tau_0}$$

$$t_{setup} = K t_{pq}$$

$K = 3 \rightarrow 95\%$ OF FINAL VALUE

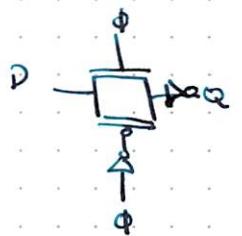
$$t_{hold} = R_\phi C - t_{pdg}$$

"NEGATIVE" HOLD TIME
POSSIBLE. (NO HOLD
TIME)

Nov 12, 2018

More Sequential Circuits

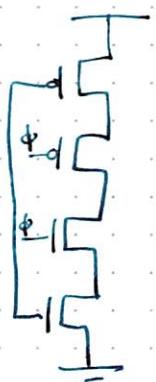
TRANSISTOR GATE LATCH



• NO MORE V_t DROP
↳ BUT WE NEED: Φ

$$t_{PCQ} = t_{CQ}$$

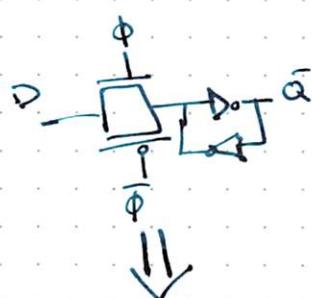
CLOCKED CMOS (C²MOS) :



Pros : DIFFUSION
• No RECESS INPUT
• SMALL

Cons :

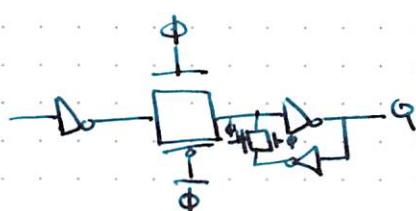
- DYNAMIC
- INVERTED Q
- CHARGE SHARING



Pros:
• NOT DYNAMIC

Cons

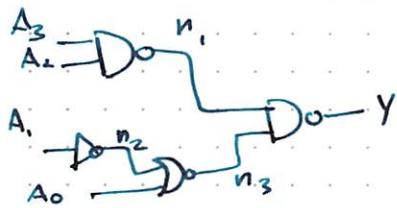
- BACKDRIVING
- POTENTIAL CONVENTION



Pros: TRUE OUTPUT
• NO DIFFUSION
Cons: • More TRANSISTORS

Nov 14

TESTING & VERIFICATION



n_1	n_3	Y
0	0	1
0	1	1
1	0	1
1	1	0

$$\text{SET } n_3 = 1$$

$$A_0 = 0$$

$$A_1 = 1$$

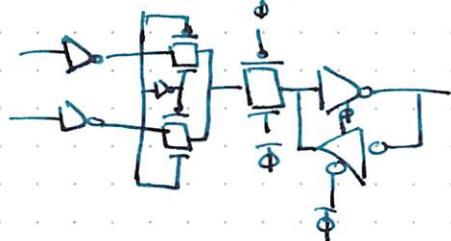
$$A_2 = 1$$

8

DESIGN FOR TEST

SCAN

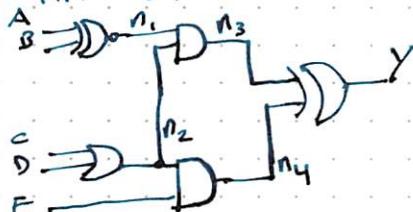
- Convert each FF to a scan register
- Scan Reg:



Nov 26
BEST

EXAM

WARM UP:



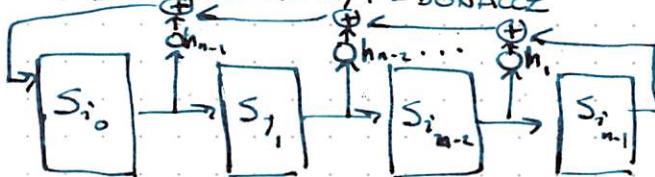
PATTERN	SAI	SAO
A {0, 1, 1, 1, 0}	{1, 0, 1, 0, 0}	
B {1, 0, 1, 1, 0}	0 1 1 0	
C {X, X, 0, 1, 1}	1 0 0 1	
D {X, X, 1, 0, 1}	1 0 0 1	
E {1, 0, 1, 1, 0}	1 0 1 0	
n1 1 0 1 1 0	0 0 1 1 0	
n2 0 0 0 0 0	1 0 1 0 1	
n3 0 1 0 0 0	0 1 1 0 1	
n4 0 0 1 1 0	1 0 1 1 1	
Y 1 1 1 1 1	0 1 1 1 1	



PRNG

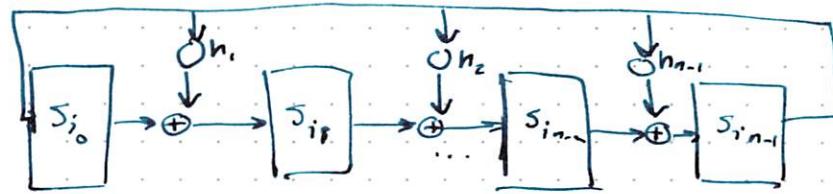
- LFSR

- External Xor, FIBONACCI



PRNG

• ~~FEEDBACK~~ MODULAR, INTERNAL, GALOIS LFSR



STRUCTURE OF LFSR:

$$f(x) = h_n x^n + h_{n-1} x^{n-1} + \dots + h_1 x + 1$$

→ AFTER i SHIFTS, THEN THE LFSR CONTENTS HAS

$$S_i(x) = S_{i_{n-1}} x^{n-1} + \dots + S_i x + S_{i_0}$$

↳ IF f W/ $h_j \in GF(2)$ & $f(0)=1$, THEN $\exists T$ SUCH THAT $f(x)$ DIVIDES $1+x^T$

Nov 24, 2018

EXAM 2 TOPICS :

- ↳ POWER
- ↳ LOGIC FAMILIES
- ↳ ADDERS
- ↳ SEQUENTIAL CIRCUITS
- ↳ TESTING
- ↳ MEMORY

GALOIS LFSR:

$$f(x) = x^n + h_{n-1} x^{n-1} + \dots + h_1 x + 1$$

$$h_i \in \{0, 1\}$$

$$S_i = S_{i_{n-1}} x^{n-1} + \dots + S_i x + S_{i_0}$$

$$S_i \in \{0, 1\}$$

IF A POLYNOMIAL W/ COEFFICIENTS $\in GF(2)$ IS IRREDUCIBLE,
THEN ITS PERIOD, T , DIVIDES 2^{n-1} PERFECTLY.

How long an LFSR can go before repetition?

Ex) WHAT IS THE PERIOD OF $f(x) = x^4 + x^2 + 1$?

$f(x)$ IS REDUCIBLE: $(x^2 + x + 1)^2 \bmod 2$

$$T > 4$$

$$T = 5:$$

$$\begin{array}{r} x^4 + x^2 + 1 \\ \hline x^5 + 1 \\ \vdots \\ 1 \end{array}$$

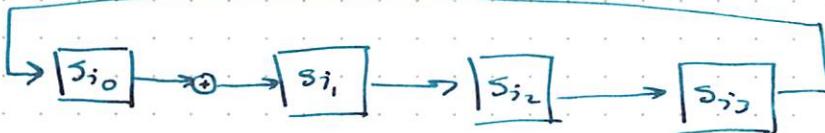
$$R = ?$$

$$\begin{array}{r} x^4 + x^2 + 1 \\ \hline x^6 + 1 \\ - (x^6 + x^4 + x^2) \\ \hline x^4 + x^2 + 1 \\ - (x^4 + x^4 + 1) \\ \hline 0 \end{array}$$

$$R = 0$$

$$\therefore \text{PERIOD} = 6$$

Ex)



SHOW THAT THE LFSR PRODUCES A MAX LENGTH SEQUENCE
 $f(x) = ?$

SHOW THAT $f(x)$ DIVIDES $x^{15} + 1$

$$\begin{array}{r} x^4 + x^2 + 1 \\ \hline x^{15} + 1 \\ - (x^{15} + x^{12} + x^9) \\ \hline 0 + x^{12} + x^9 + 1 \\ - (x^{12} + x^9 + x^6) \\ \hline 0 + x^9 + x^6 + x^3 + 1 \end{array}$$

$$x^{12} + x^9 + x^6 + x^3 + x^2 + x + 1$$



EXAM 2 REVIEW

1) $Y = \overline{A+B+C}$

ESTIMATE THE POWER CONSUMPTION FOR Y WITH:

a) STATIC CMOS

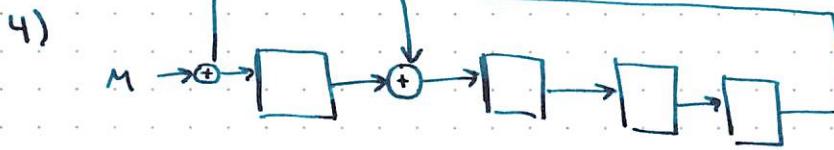
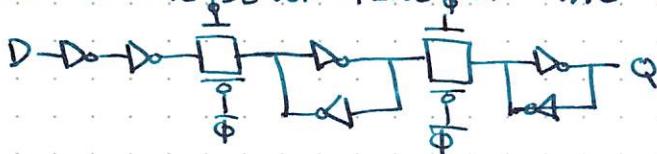
b) PSEUDO-NMOS

2) WHAT ARE THE BETWEEN & GROUP PG VALUES, C_{OUT} , & SUM FOR

$$A = 1011, B = 0110, C_{in} = 0$$

FOR A 4-BIT SLANSKY ADDER

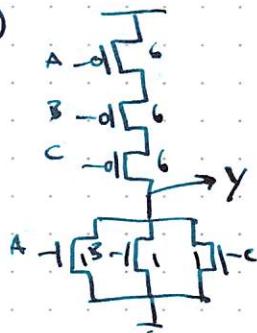
3) WHAT IS THE SETUP TIME OF THE FOLLOWING FF DESIGN?



$$\text{LET } M = \begin{matrix} 0 \\ 1 \\ 1 \\ 0 \\ 0 \\ 1 \\ 0 \end{matrix} \quad \begin{matrix} M_7 \\ M_6 \\ M_5 \\ M_4 \\ M_3 \\ M_2 \\ M_1 \end{matrix}$$

WHAT WILL THE SEED BE AFTER M IS SHIFTED IN?

1) a)



$$\text{OUTPUT: } q_C = C'$$

$$P_{SW} = \alpha C^2 V_{DD} f$$

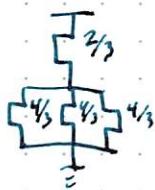
$$\begin{aligned} C &= C_{ox}(\Delta A) \\ &= \frac{k_{eg}}{C_{ox}} (360\text{nA})(180\text{nA}) \\ &= 0.546 \text{fF} \end{aligned}$$

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

$$\begin{aligned} \alpha &= \left(\frac{1}{8}\right)\left(\frac{1}{8}\right) \\ &= \frac{7}{64} \end{aligned}$$

$$\begin{aligned} P_{SW} &= \left(\frac{7}{64}\right) 9 (0.546 \text{fF}) (1.8V)^2 (16 \text{Hz}) \\ &= 1.741 \text{E}6 \text{W} \end{aligned}$$

b)

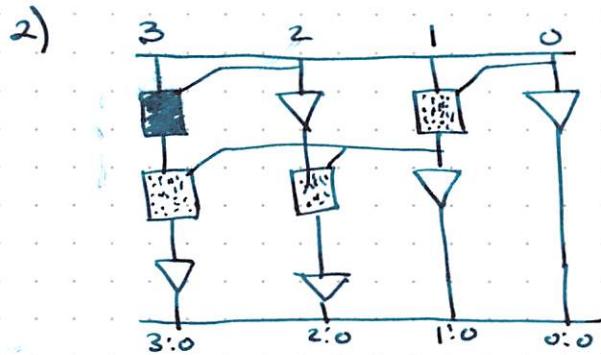


$$P = P_{SW2} + P_{S_{OUT}}$$

$$P_{SW2} = V_{DD}^2 f \left(\frac{4}{3}\right) (0.25)(3)(C')$$

$$P_{S_{OUT}} = (IV) = (V_{DD}) \left(\frac{1}{2} \mu_P C_{ox} \frac{w}{l} (N_{EFF})^2 \right) \left(\frac{7}{8} \right)$$

P(All zero)



$$P_i = A_i \oplus B_i$$

$$G_i = AB$$

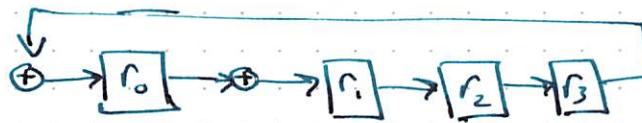
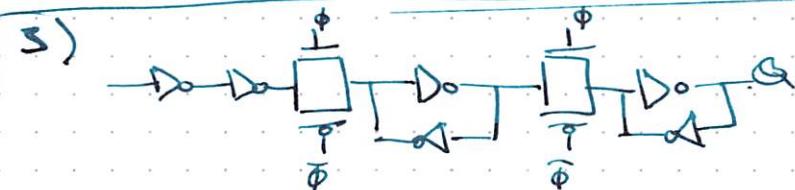
$$P_{ij} = P_{ik} P_{k-j}$$

$$G_{ij} = G_{ik} + P_{ik} G_{k-j}$$

$C_{out} \leftarrow \text{GENERATES}$

$$\text{Sum} \leftarrow P_i \oplus G_{i-1:0}$$

A	1 0 1 1
B	0 1 1 0
P _i	1 1 0 1
G _i	0 0 1 0
L _i	1
G _i	0 1
L ₂	1 1
S _c	1 0 0 0 1
C	1 1 1 0



WHAT WILL THE
SIGNATURE BE AFTER
M IS SHIFTED IN

$$M = 0 1 1 0 0 1 0 1$$

$$M_7 \quad M_0$$

$$\begin{array}{r} x^2 + x \\ \hline x^4 + x + 1 & | x^6 + x^5 + x^2 + 1 \\ & - (x^6 + x^3) \\ \hline & x^5 + x^3 + 1 \\ & - (x^7 + x^2 + x) \\ \hline r(x) & \rightarrow x^3 + x^2 + x + 1 \end{array}$$

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$$M(x) = g(x)f(x) + r(x)$$

$$\frac{M(x)}{f(x)}$$

$$f(x) = x^4 + x + 1$$

$$g(x) = x^6 + x^5 + x^2 + 1$$

0	0	0	0
1	0	0	0
0	1	0	0
0	0	1	0
0	1	0	1