

Jason Blocklove

COMPUTER ENGINEERING MS/BS CANDIDATE

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Education

Master of Science/Bachelor of Science in Computer Engineering | Rochester Institute of Technology

Graduation Date: May 2020

- GPA - 3.64/4.0

Rochester, NY

Master's Thesis Research | Hardware Obfuscation

- Investigating various methods of intellectual property protection on FPGA designs through hardware obfuscation
- Analyzing differences in popular hardware obfuscation methods to determine their effectiveness in common threat models

Experience

SICOM Systems | Research & Development Co-Op

May - August 2018

- Designed and developed a comprehensive testing system for order confirmation units
- Developed an ePayment system for university campuses with a point of sale terminal using external APIs
- Utilized a Linux subsystem to implement an HID card reader on a point of sale terminal system
- Worked on reverse engineering a device to determine how to modify the current system to interface with new hardware

Lansdale, PA

Johnson & Johnson | Computer Engineering Co-Op

June - December 2017

- Used Java to develop and disseminate creation tool for Outlook distribution lists
- Created numerous Excel and Outlook macros to streamline day-to-day work

Raritan, NJ

RIT Computer Engineering Department | Lab Instructor/Lead Teaching Assistant

January 2017 - Present

- Managed teams of up to 10 TAs, and helped students with technical problems encountered in lab
- Taught circuit troubleshooting principles, re-taught key lecture principles, addressed lab-related questions, graded labs
- Assisted students in Digital System Design I and II, Interfacing Digital Electronics, and Reconfigurable Computing labs

Rochester, NY

RIT Computer Engineering Department | Curriculum Developer

May 2017 - Present

- Identified structural issues with the Digital System Design II and Interfacing Digital Electronics lab courses
- Designed and developed replacement lab exercises that require students create a simplified MIPS Datapath in VHDL
- Restructured existing lab exercises and wrote new lab procedures for students to implement

Rochester, NY

Projects

L3Harris Hardware Obfuscation Method Investigation

September 2019 - Present

- Working with a team of RIT professors and L3Harris engineers to investigate hardware obfuscation methods
- Team goal is to protect a design on an FPGA from malicious reverse engineering attacks

VHDL Simplified MIPS Processor Design

August 2018 - Present

- Designed and developed a simplified MIPS datapath in VHDL
- Implemented the design on an FPGA with connections to several inputs and outputs for displaying proper functionality

MITRE eCTF Competition

January - April 2019

- Third place finish in competition to secure a Zynq System on Chip device and attack opposing teams' designs
- Collaborated with RIT Computing Security team to secure both hardware and software on the device
- Designed a system to reset the software of the device if the hardware detected a possible attack

Hardware Median Filter for CMPE-660

August - December 2018

- Designed a hardware system which transmitted an image through UART into DDR2 memory and then filtered the image
- Modified this hardware system to include a softcore processor and a median filter coprocessor
- Implemented the UART, FIFOs, median filter, and control logic for communication manually in VHDL
- Utilized Xilinx IP Cores for memory communication, AXI protocol conversion, and MicroBlaze processor instantiation

Personal Server

2016 - Present

- Built and configured a personal server using multiple distributions of Linux
- Set up the server with a hypervisor for easy management of multiple VMs for different tasks
- Managed multiple users and wrote installation scripts for most commonly used programs

Technical Skills

Languages VHDL, C, Java, C#, Python, Verilog, VBA, Bash, Assembly (MIPS and ARM ThumbII)

Hardware FPGA, SoC, ARM Microprocessors (Raspberry Pi, NXP K64F, STML32), Arduino

Software Xilinx Vivado & SDK, Xilinx ISE, Modelsim, Keil μ Vision

Operating Systems Linux (Arch, Debian, & Red Hat Based), Windows, macOS

Select Leadership Experience

RIT Engineering House | Vice President

2016 - 2017

- Executive Board member of an Engineering-focused student organization at RIT
- Responsible for Engineering House internal affairs and RIT liaison tasks
- Assumed role of President for last month of term

Rochester, NY