Jason Blocklove

MS Computer Engineering

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Education

Master of Science/Bachelor of Science in Computer Engineering | **Rochester Institute of Technology** — *Aug 2020*, *Rochester, NY*

- Undergraduate GPA – 3.65/4.0 Magna Cum Laude
- Graduate GPA – 4.0/4.0

Master's Thesis | **Hardware Obfuscation**

- Investigated IP protection methods on FPGAs and ASICs, focusing on netlist-level logic locking
- Determined a method of strengthening logic locking techniques against Boolean SAT attacks by inserting a modified SIMON block cipher to generate keys

Experience

Johns Hopkins University Applied Physics Lab | **Electrical Engineer 1** — *July 2020 - Present*, *Laurel, MD*

- Developed a control system and processing chain for an FPGA, utilizing multiple FIR filters to wake a device based on input signals
- Modified and updated PCB schematics to meet changing requirements and improve upon the initial board design
- Restructured and modified an existing embedded codebase to assist in a new use for a long established hardware design

SICOM Systems | **Research & Development Co-Op** — *May - August 2018*, *Lansdale, PA*

- Designed and developed a comprehensive testing system for order confirmation units
- Developed an ePayment system for university campuses with a point of sale terminal using external APIs
- Utilized a Linux subsystem to implement an HID card reader on a point of sale terminal system
- Worked on reverse engineering a device to determine how to modify the current system to interface with new hardware

Johnson & Johnson | **Computer Engineering Co-Op** — *June - December 2017*, *Raritan, NJ*

- Used Java to develop and disseminate creation tool for Outlook distribution lists
- Created numerous Excel and Outlook macros to streamline day-to-day work

RIT Computer Engineering Department | **Lab Instructor/Lead Teaching Assistant** — *January 2017 - Present*, *Rochester, NY*

- Managed teams of up to 10 TAs, and helped students with technical problems encountered in lab
- Taught circuit troubleshooting principles, re-taught key lecture principles, addressed lab-related questions, graded labs
- Assisted students in Digital System Design I and II, Interfacing Digital Electronics, and Reconfigurable Computing labs

RIT Computer Engineering Department | **Curriculum Developer** — *May 2017 - Present*, *Rochester, NY*

- Identified structural issues with the Digital System Design II and Interfacing Digital Electronics lab courses
- Designed and developed replacement lab exercises that require students create a simplified MIPS Datapath in VHDL
- Restructured existing lab exercises and wrote new lab procedures for students to implement

Projects

L3Harris Hardware Obfuscation Method Investigation — *September 2019 - Present*

- Working with a team of RIT professors and L3Harris engineers to investigate hardware obfuscation methods
- Team goal is to protect a design on an FPGA from malicious reverse engineering attacks

VHDL Simplified MIPS Processor Design — *August 2018 - Present*

- Designed and developed a simplified MIPS datapath in VHDL
- Implemented the design on an FPGA with connections to several inputs and outputs for displaying proper functionality

MITRE eCTF Competition — *January - April 2019*

- Third place finish in competition to secure a Zynq System on Chip device and attack opposing teams' designs
- Collaborated with RIT Computing Security team to secure both hardware and software on the device
- Designed a system to reset the software of the device if the hardware detected a possible attack

Hardware Median Filter for CMPE-660 — *August - December 2018*

- Designed a hardware system which transmitted an image through UART into DDR2 memory and then filtered the image
- Modified this hardware system to include a softcore processor and a median filter coprocessor
- Implemented the UART, FIFOs, median filter, and control logic for communication manually in VHDL
- Utilized Xilinx IP Cores for memory communication, AXI protocol conversion, and MicroBlaze processor instantiation

Personal Server — *2016 - Present*

- Built and configured a personal server using multiple distributions of Linux
- Set up the server with a hypervisor for easy management of multiple VMs for different tasks
- Managed multiple users and wrote installation scripts for most commonly used programs

Technical Skills

Languages	VHDL, C, Java, C#, Python, Verilog, VBA, Bash, Assembly (MIPS and ARM ThumbII)
Hardware	FPGA, Xilinx SoC, ARM & TI Microprocessors, Arduino
Software	Xilinx Vivado & SDK, Lattice Radiant, Altium Designer, Xilinx ISE, Modelsim, Aldec ActiveHDL, TI Code Composer Studio, Keil μVision
Operating Systems	Linux (Arch, Debian, & Red Hat Based), Windows, macOS

Select Leadership Experience

RIT Engineering House | **Vice President** *2016 - 2017*

Rochester, NY

- Executive Board member of an Engineering-focused student organization at RIT
- Responsible for Engineering House internal affairs and RIT liaison tasks
- Assumed role of President for last month of term