Jason Blocklove

Computer/Electrical Engineer
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Education

MS/BS in Computer Engineering | **Rochester Institute of Technology** *Aug. 2020*
Rochester, NY

- Undergraduate GPA – 3.65/4.0 | Magna Cum Laude
- Graduate GPA – 4.0/4.0

"Hardware Intellectual Property Protection Through Obfuscation Methods" | **MS Thesis**

- Analyzed the effectiveness of several existing logic locking techniques on a 16-bit substitution box against a boolean SAT attack
- Designed modified logic locking techniques to increase SAT attack resilience using a round-reduced SIMON cipher

Honors & Awards

Award for Excellence in Student Teaching, RIT Computer Engineering Department (Fall 2018, Spring 2020)
Dean's List, RIT Kate Gleason College of Engineering (6 Semesters from 2015 — 2019)

Publications

J. Blocklove, S. Farris, M. Kurdziel, M. Łukowiak, and S. Radziszowski, "Hardware Obfuscation of the 16-bit S-box in the MK-3 Cipher," in *2021 MIXDES – 28th International Conference "Mixed Design of Integrated Circuits and Systems",* 2021, pp. 0 – 0, doi:DOI STUFF

Research Experience

Bitstream Obfuscation for Securing IP on FPGAs | **Researcher** *Sep. 2019 - Jul. 2020*
Rochester, NY

- Investigated hardware obfuscation methods with a team of RIT professors and L3Harris engineers
- Identified methods to protect a design on an FPGA from malicious reverse engineering attacks
- Analyzed methods of implementing hardware protections on a Microsemi PolarFire FPGA

Dr. Shanchieh Yang Laboratory (RIT) | **Research & Development Team** *Apr. - Sep. 2016*
Rochester, NY

- Designed and developed a Java user interface for computing security-related research
- Extensively debugged an external API used for graph drawing

Special Qualifications

Security Clearance, Top Secret (Mar. 2021)

Experience

Johns Hopkins University Applied Physics Lab | **Computer/Electrical Engineer** *Jul. 2020 - Present*
Laurel, MD

- Designed a low power system on an FPGA to wake-up other devices in certain scenarios
- Integrated FPGA designs into a more comprehensive system
- Updated and improved board designs for a project
- Managed embedded systems designs and FPGA hardware for a different project
- FPGA DSP stuff

RIT Computer Engineering Department | **Curriculum Developer** *May 2017 - May 2020*
Rochester, NY

- Identified structural issues with the Digital System Design II and Interfacing Digital Electronics lab courses
- Designed and developed replacement lab exercises that require students create a simplified MIPS Datapath in VHDL
- Restructured existing lab exercises and wrote new lab procedures

RIT Computer Engineering Department | **Lab Instructor/Lead Teaching Assistant** *Jan. 2017 - May 2020*
Rochester, NY

- Managed teams of up to 10 teaching assistants
- Taught circuit troubleshooting principles, reinforced key lecture topics, addressed lab-related questions, and graded labs
- Assisted students in Digital System Design I, Digital System Design II, Interfacing Digital Electronics, Reconfigurable Computing, and Hardware/Software Design for Cryptographic Applications labs

SICOM Systems | **Research & Development Co-Op** *May - Aug. 2018*
Lansdale, PA

- Designed and developed a comprehensive testing system for order confirmation units
- Developed an ePayment system for university campuses with a point of sale terminal using external APIs
- Utilized a Linux subsystem to implement an HID card reader on a point of sale terminal system
- Contributed to reverse engineering the functionality of a device to determine how to modify a current system to interface with new hardware

Johnson & Johnson | **Computer Engineering Co-Op** *Jun. - Dec. 2017*
Raritan, NJ

- Used Java to develop and disseminate creation tool for Outlook distribution lists
- Created numerous Excel and Outlook macros to streamline day-to-day work

Projects

VHDL Simplified MIPS Processor Design *Aug. 2018 - May 2020*

- Designed and developed a simplified MIPS datapath in VHDL for use in a digital system design lab curriculum
- Implemented the design on an FPGA with connections to several inputs and outputs for displaying proper functionality

MITRE eCTF Competition *Jan. - Apr. 2019*

- Third place finish in competition to secure a Zynq System on Chip device and attack opposing teams' designs
- Collaborated with RIT Computing Security team to secure both hardware and software on the device
- Designed a hardware system to reset an on-chip ARM processor if a possible side-channel attack was detected

Hardware Median Filter for Reconfigurable Computing Graduate Course *Aug. - Dec. 2018*

- Designed a system on an FPGA which transmitted an image through UART into DDR2 memory and filtered the image
- Implemented the UART, FIFOs, median filter, and control logic for communication in VHDL
- Utilized Xilinx IP Cores for memory communication, AXI protocol conversion, and MicroBlaze processor instantiation
- Modified this hardware system to include a softcore processor and a median filter coprocessor

Technical Skills

Languages	VHDL, Verilog, C++, C, Java, C#, Python, VBA, Bash, Assembly (MIPS and ARM)
Hardware	FPGA, Xilinx SoC, ARM Microprocessors (Raspberry Pi, NXP K64F, STML32), Arduino
Software	Xilinx Vivado & SDK, Xilinx ISE, Modelsim, Lattice Radiant, Aldec Active-HDL, Altium Designer, Keil μVision, TI Code Composer Studio
Operating Systems	Linux (Arch, Debian, & Red Hat Based), Windows, macOS

Select Leadership Experience

Sigma Alpha Mu – Delta Omega Chapter | **Vice President** *2019*

Rochester, NY

- Executive Board member for a fraternity at RIT
- Oversaw execution of officer responsibilities to ensure each member's duties were being met
- Managed potential risks at events so all participants were safe and all guidelines were appropriately followed

Sigma Alpha Mu – Delta Omega Chapter | **Various Officer Positions** *2016 - 2019*

Rochester, NY

- Held several officer positions within fraternity including: Philanthropy Chair, Sergeant at Arms, Webmaster, and Historian
- Organized and oversaw numerous events to raise money for various charities
- Managed the organization's rules and regulations to ensure our proceedings ran well
- Created and updated the fraternity's website and managed user emails

RIT Engineering House | **Vice President** *2016 - 2017*

Rochester, NY

- Executive Board member of an Engineering-focused student organization at RIT
- Responsible for Engineering House internal affairs and RIT liaison tasks
- Assumed role of President for last month of term