Processor Prototyping Laboratory
Midterm Report Specifications

Fall 2022

1 Overview

The purpose of this report is to provide a comparison of the single-cycle and pipeline processors. The report should be written so that a technically competent reader can read it quickly and understand what you accomplished. Detail is expected, but must be at a level that can be digested with a single read. If you are working in a group select one of your single-cycle designs and your group's pipeline design. If you are working by yourself use your own designs.

The final report, which will be due closer to the end of the semester, will be very similar in format to this report and will include some of what you are going to do for this report. Therefore doing a good job on this report will save you some time on your final report.

2 Report Sections

2.1 Cover Page

- Title
- Course
- Your name
- Lab Section
- Teaching assistant name
- Due date

2.2 Overview

This section should be about two paragraphs in length, but not longer than a single page. Give a short overview of what you are comparing with both designs, and the benefits of each design. Mention the benefit of the selected test program in comparing designs, and how you would analyze the data gathered for each processor. Finally, give a brief summary of the conclusion you arrived at when comparing the processors.

2.3 Design

Block diagrams should be included for both of your processors, make sure they are readable, labeled, and appropriately sized. Also, be sure they carry sufficient detail to show your implementation and design choices. *If needed for readability, diagrams should be sectioned into logical hierarchical diagram sets.*

2.4 Results

For this section you will use the mapped version with gate timing of your designs. Use the command: 'synthesize -t -f 200 system' to enable timing and to set an effort of 200 MHz for quartus. Use the test program 'mergesort.asm' to collect performance data from your designs. Compare the designs by analyzing the data collected from the test program. Memory latencies should be equal for both designs. Mention the latency used in both designs.

Prepare a table for each processor (one single-cycle and one pipeline) summarizing:

- The frequency of your designs (max possible from logs).
- The average clocks per instruction (averaged over all the dynamic instructions).
- The latency of one instruction (how long one instruction takes to complete).
- The performance of the designs in MIPS.
- FPGA resources required for your design (separate amounts for each resource type).

The max possible frequency should be obtained from either 'system.log', or from the '.sta' report under the '._system folder'. Look for the CLK and CPUCLK frequency and for the 85 degree analysis results. The max possible frequency for CLK is min(CLK/2, CPUCLK). Mention if you are reporting the max frequency for CLK or CPUCLK next to the column. The latency corresponds to 1 clock period in single-cycle, and 5 clock periods in pipeline. The other results should be fairly obvious to attain.

Note on CPI and MIPS Calculations (repeated from Lab4 manual): The total clock cycles can be found using the "make system.sim" command. Note, the clock cycles reported by this command is the testbench clock cycle count. To obtain the equivalent CPU clock cycle count, divide the number obtained by two because CPUCLK = 2*CLK.

IMPORTANT: Mention the formulae used to calculate the various parameters asked and where you obtained the numbers from. E.g. total number of instructions obtained from running 'sim' which reports it at the end.

Should neither of your designs work, no points will be awarded for the result section of this report.

2.5 Conclusions

This section should be two paragraphs, but not longer than a single page. Summarize and reason out your results.

2.6 Contributions

For this section, you will detail the individual contributions for each team member. Individual contribution documentation is necessary, but not sufficient by itself, for credit on the design and report outcomes.

3 Formatting

- The length of the report will be approximately 3 to 5 pages of text. Diagrams are in addition to that.
- Block diagrams must be digitally drawn. Hand drawn and scanned will not be accepted, nor will copies of the diagram in the book. You can use software tools like visio, dia, or inkscape to draw your diagram.
- Text should be 12 point font.
- Line spacing should be 1.5 lines.

4 Turning In Your Report

This report is due by *Sunday, at 11:59 PM* of Week 8 as a single PDF file. There is also a LaTeX Template provided, feel free to use it. Name your report *midtermreport.pdf*.

Submission will be done via an appropriately named Brightspace assignment. Only one team member should submit the team's report.

5 Grading

0 pts	**Cover page** (5 point penalty if it does not meet specification)
5 pts	**Overview**
5 pts	**Processor Design**
15 pts	**Results**
5 pts	**Conclusions**
5 pts	**TA subjective evaluation for overall report quality** (Up to a 5 point penalty if individual contributions are missing)
35 pts	**Max Total**