Si5350, Si5351 Frequently Asked Questions

This FAQ document answers the most frequently asked questions for the Si5350 and the Si5351 CMOS Clock Generator products.

Si5350/51 Product Family Outline

Si5350 (Pin Controlled)
Si5350A – XTAL only
Si5350B – XTAL & VCXO capability
Si5350C – XTAL & CLKIN

Si5351 (I2C Programmable)
Si5351A – XTAL only
Si5351B – XTAL & VCXO capability
Si5351C – XTAL & CLKIN

Table 1. Si5350, Si5351 Product Links

Link Type	Link
Si5350/Si5351 Product Pages	https://www.silabs.com/products/timing/clocks/cmos-clock-generators
Evaluation Board / Development Kit	https://www.silabs.com/products/development-tools/timing/clock/si535x-b20qfn-evb-development-kit
ClockBuilder Pro Software	https://www.silabs.com/products/development-tools/software/clock
Quality and Reliability Reports	www.silabs.com/quality
Request Technical Support	www.silabs.com/support (Go to "E-Mail Support Request" link)

Table 2. Si5350, Si5351 Relevant Application Notes

Document	Link
AN619: Manually Generating an Si5351 Reg Map • For 10-MSOP and 20-QFN Si5351 Devices	https://www.silabs.com/documents/public/application-notes/AN619.pdf
AN1234: Manually Generating an Si5351 Reg Map • For 16-QFN Si5351 Devices	https://www.silabs.com/documents/public/application-notes/an1234.pdf
AN554: Si5350/51 PCB Layout Guide	https://www.silabs.com/documents/public/application-notes/AN554.pdf
AN551: Crystal Selection Guide for Si5350/51 Devices	https://www.silabs.com/documents/public/application-notes/AN551.pdf

Table of Contents

1 Where is the RoHs, REACH, or other material related compliance information for the Si5350 or the Si5351?

- Please refer to our Corporate, Product and Environmental Data Search (by Part Number) webpage for full RoHS, REACH and other material composition information.

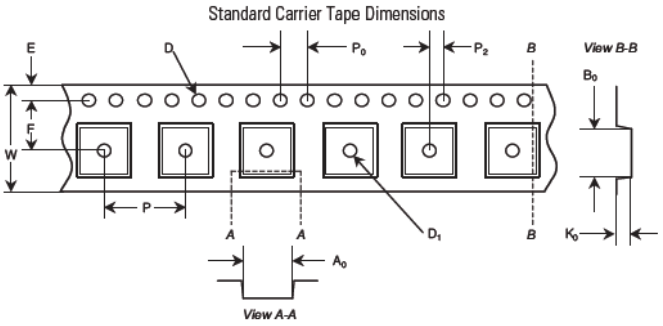
2 Where is the FIT information for the Si5350 or the Si5351?

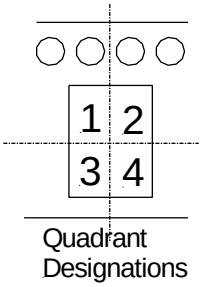
- FIT information for all Silicon Labs products can be found on the Corporate Commitment to Quality Page.
  - Look for the Quality and Reliability Monitor Report near the bottom.
- Look for the Si535X part number.
  - The Si5350 and the Si5351 both use 0.13um technology.

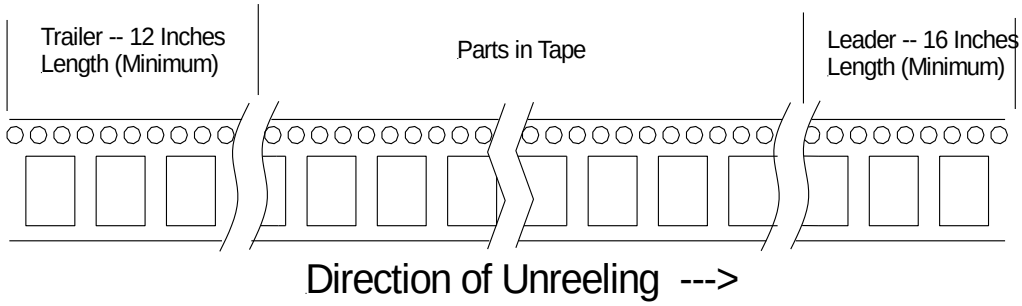
3 What are the Tape & Reel Specs for the Si5350/51?

- To specify Tape & Reel, please include the "R" suffix on the part number when you place an order.

Package	Lead Count	Package Description	Carrier Tape									Reel Size Diameter (inch)	Reel Hub Diameter (inch)	Pin-1 Orientation (Quadrant)
			Supplier	Carrier Tape P/N	Width	Pitch	Pocket Size				Parts Per Meter			
					W (mm)	P (mm)	A0 (mm)	B0 (mm)	K0 (mm)	K1 (mm)				
QFN	20	4X4	C-PAK	QFN0400X0400G	12	8	4.35	4.35	1.1	N/A	125	13	4	1
QFN	20	4X4	Advantek	ML0404-A	12	8	4.35	4.35	1.1	N/A	125	13	4	1
QFN	20	4X4	Kostat	ML0404-A	12	8	4.35	4.35	1.1	N/A	125	13	4	1
QFN	20	4X4	HwaShu	ECF0404-A20	12	8	4.25	4.25	1.1	N/A	125	13	4	1
QFN	20	4X4	Shin-Etsu	SP4.25-12QFN0	12	8	4.25	4.25	1.35	N/A	112	10	4	1
MSOP	10	3X3	C-PAK	MSOP8-13	12	8	5.2	3.3	1.6	1.2	125	13	4	1
MSOP	10	3X3	C-PAK	MSOP8-12	12	8	5.3	3.4	1.4	N/A	125	13	4	1







Tape Pitch	8mm
Minimum Number of pockets for leader	51
Minimum Number of pockets for trailer	39

4 How can I get a Si5350 or Si5351 with a custom startup frequency?

- You can use ClockBuilder Pro to create a custom part number.
- After you create your custom plan, you will have the option to submit the configuration to us. This will officially create the part number in our system. You will then be able to contact your local distributor to order this new part number.
- Here is a link to our ClockBuilder Pro software: https://www.silabs.com/products/development-tools/software/clock

5 What is the default I2C Address of the Si5351 when the part does not have an A0 pin?

- The default address of the Si5351 will always be 0x60h.
- The A0 bit described in figure 8 in the datasheet is only an option for the Si5351A. All other Si5351 devices will either have 0x60h as their default address, or they can have a custom I2C address defined by a custom configuration from ClockBuilder Pro.
- When you create a custom part number for the Si5351, you will have the option to define a new I2C address if you want to.

6 What finish is used on the contacts of the Si5350 or the Si5351?

- 10-Pin MSOP, 3x4.9mm is Matte Sn with 10um min. Thickness
- 16-Pin QFN, 3x3mm is Matte Sn with 10um min. Thickness
- 20-Pin QFN, 4x4mm is NiPdAu, with:
    - Ni: 10um min
    - Pd: 0.1um min
    - Ag-Au alloy: 0.2um min

7 How can I burn the NVM on a blank Si5351 part?

- Silicon Labs does not currently support customer NVM burning for this product family.
- However, you can easily create a new custom part with a newly defined default startup state using ClockBuilder Pro. Once the part is submitted at the end of the process, you will be able to contact your local distributor to order the new part number.

8 What if I want a feature in my custom Si5350 or Si5351 that is not configurable in ClockBuilder Pro?

- If ClockBuilder Pro is currently missing a configuration option for your Si5350 or Si5351 that you would like included in your custom part, just create a new support ticket and we will be able to add your new settings for you.
    - An example of a configuration option currently missing in ClockBuilder Pro might be the ability to buffer external references like an xtal or CLKIN directly to an output.
- Just remember to include your existing ClockBuilder Pro Project and a description of the functionality you would like added. We can then send a new updated ClockBuilder Pro Project file back to you. Just submit the new modified configuration and your new part number will include your desired functionality.

9 Can a CMOS clock be driven into the XA or XB pins of the Si5350 or Si5351?

- Yes, just drive the clock into XA and leave XB unconnected. However, limit the signal level into XA to <1Vpp.

10 What is the output-to-output skew of the Multisynth outputs?

- All outputs are within +/- 500ps of one another at power up (if pre-programmed) or if PLLA and PLLB are reset simultaneously via register 177.
    - If only PLLA or PLLB is reset, then only the outputs associated with the PLL in question will be guaranteed to be within +/-500ps of each other.
- If an output frequency is dynamically changed, output-to-output skew of that clock is not guaranteed until a soft reset is performed.
- If you are using a Si5351 in a 16-QFN package, please see Why does CLK3 on a 16-QFN Si5350/51 show a phase shift from the other outputs?

11 How long does a glitch-less frequency transition take?

- The Int, R and N register values inside the Interpolative Dividers are updated when the LSB of R is written via I2C.
- A good rule for calculating the transition time is: $5 * Multisynth\_Period + 200ns$.
- Using the frequency select pin, the transition time is on the order of 100us.

12 What is the power-up sequence of the Si5350 or the Si5351?

- All VDDO need to come up no later than VDD when the phase relationship between multiple outputs is concerned

13 Can the Si5350 or Si5351 duplicate a PWM input?

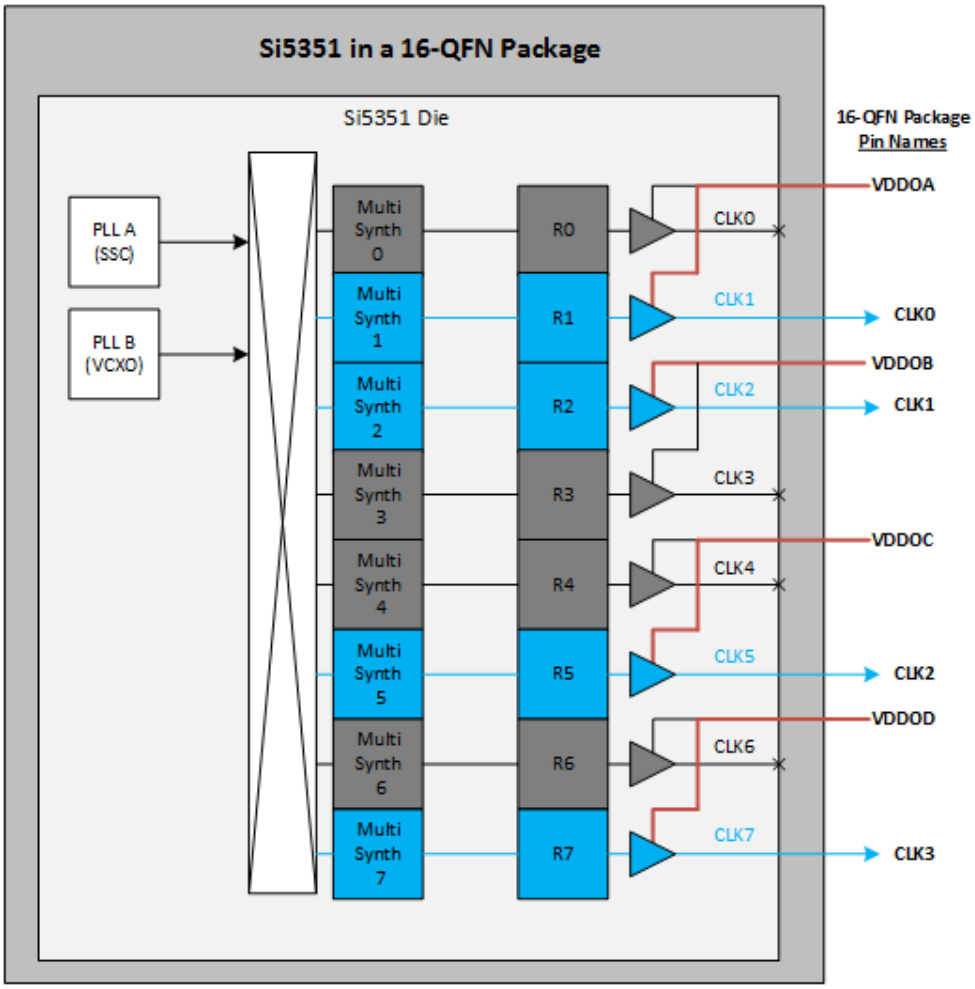
- Yes, just set the output to buffer the CLKIN signal. The Si5350 or Si5351 will not have an issue buffering a PWM input.
- Set the CLKx_SRC[1:0] bits in the CLKx Control register to 01.
    - This will bypass the PLL/VCXO and MultiSynth synthesis stages and connect CLKx directly to the CLKIN input.
    - See AN619 for more details for 10-MSOP and 20-QFN parts and AN1234 for more details on a 16-QFN part

14 Will changing the Drive Strength through the control registers change the output slew rate?

- Yes, decreasing the drive strength from 8mA will increase the rise/fall times and subsequently decrease the slew rate.
- **Note:** The datasheet rise/fall times are all based on an 8mA drive strength.

15 Why is there a separate programming guide (AN1234) for the 16-QFN Si5351?

- The 3x3mm 16-QFN Si5351 is a special four output version of the original 4x4mm 20-QFN Si5351. Each output on the 16-QFN part, has its own individual VDDO supply. This isolation of the outputs from one another dramatically reduces crosstalk which improves the jitter performance of the device.
- The 16-QFN Si5351 uses the same die as the 20-QFN Si5351. For the 20-QFN package, all 8 outputs are bonded out to external pins on the package. However, for the new 16-QFN package, only a subset of the original 8 outputs were bonded out to pins.
- The below diagram shows the relationship between the outputs of a 20-QFN and a 16-QFN Si5351. CLK0, CLK3, CLK4, and CLK6 are no longer used **(Outlined in Gray)**. Instead, CLK1, CLK2, CLK5, and CLK7 are used **(Outlined in blue)**, and they become the new CLK0, CLK1, CLK2, and CLK3 for the 16-QFN part.



- This concept becomes important when programming the Si5351 by hand, without the help of ClockBuilder Pro. CLK0, CLK1, CLK2, and CLK3 of the 16-QFN part still use the registers assigned to the original CLK1, CLK2, CLK5, and CLK7 referred to in AN619. This crossover could become very confusing very quickly. Especially when configuring the numerous output dividers.
- AN1234 was created to simplify this crossover. All register names were converted over to match the 16-QFN nomenclature. For example, register 17 now refers to CLK0 Control instead of CLK1 Control. Besides that, all of the same 20-QFN formulas and design concepts still apply to the 16-QFN.
- In the end, it is always recommended to use ClockBuilder Pro to configure any Si5351, either by creating custom orderable part numbers, or by creating register exports for in-system volatile programming. However, for those that want to still program the 16-QFN device by hand, AN1234 will hopefully make that easier.

16 Why does CLK3 on a 16-QFN Si5350/51 show a phase shift from the other outputs?

- For output frequencies below 3.5MHz, CLK3 can demonstrate a phase shift from CLK0, CLK1, CLK2 on the 16-QFN Si5350/51 even if those outputs are programmed to the same output frequency.
- Multisynth3 (MS3), which is the output divider for CLK3 in a 16-QFN package, (also the same as MS7 for CLK7 for a 20-QFN package), can only be set to divide ratios of even integers between 6 and 254. See AN1234. The Multisynths for CLK0, CLK1, and CLK2 do not have this limitation as they can be set to 4, 6, 8, and any fractional value between 8 and 2048.

16-QFN Si5351 Output Multisynth Dividers	Allowed Divide Values
MS0, MS1, MS2	4,6,8, and fractional values between 8-2048
MS3	Even integer between 6 and 254

- This difference can come into play for output frequencies less than 3.5MHz. To achieve those lower frequencies, CLK3 is forced to begin using its R divider in conjunction with MS3, while the other clock outputs are still able to use their Multisynth's much larger range. This means there can be different output divider solutions for the same frequency.
- If the output divider solution between two clocks at the same frequency is different, we cannot guarantee that they will be phase aligned due to the differences in delay caused by the different divide values.

17 What is the minimum PLL lock range of the Si5350/51?

- The PLL can track any abrupt input frequency changes of 3–4% without losing lock to it. Any input frequency changes greater than this amount will not necessarily track from the input to the output.

18 Is there a ppm/degreeC output error or ppm output error over time spec for the Si5350/51 devices?

- No, depending on the frequencies needed, most outputs can be generated with a 0ppm error. Essentially this means any error at the output will be due to inaccuracies in the crystal you select and not from the Si5351A.
- The device works on multiply/divide ratios and has a resolution of 20 bits, which translates roughly to 0.1ppm worst case frequency synthesis error.

19 What are the Si5350/51 power-up sequencing requirements for VDD/VDDO? What if I can't meet it?

- If output-to-output phase skew is a concern, then VDDOx should come up either before or at the same time as VDD. Otherwise, power-supply sequencing is not required.
- If output-to-output phase skew is important, and the above sequence can't be met, then a PLLA_RST and PLLB_RST must be performed by writing a 1 to reg177, bits 5 and 7 respectively
- Note that the Si5351 (I2C-controlled version) is required to perform PLL reset. This is not possible with the Si5350. With the Si5350, the sequence must be met if output skew is important to the application.

20 How do you interface Si5350/51 clock outputs to HCSL, LVDS, and LVPECL receivers?

- The Si5350/51 clock outputs can emulate some of the most common differential I/O interface standards.
- To generate a differential signal, two clock outputs of the same frequency must be used. In addition, one clock must be inverted, 180° out of phase, with respect to the other.
    - By default, all clock outputs are in phase. Invert one of the two output clocks by setting CLKx_INV = 1. For 20-QFN and 10-MSOP devices, see AN619 and for 16-QFN devices, see AN1234 for programming instructions.
- The circuits required to interface to each of the three standards mentioned above can be seen below.