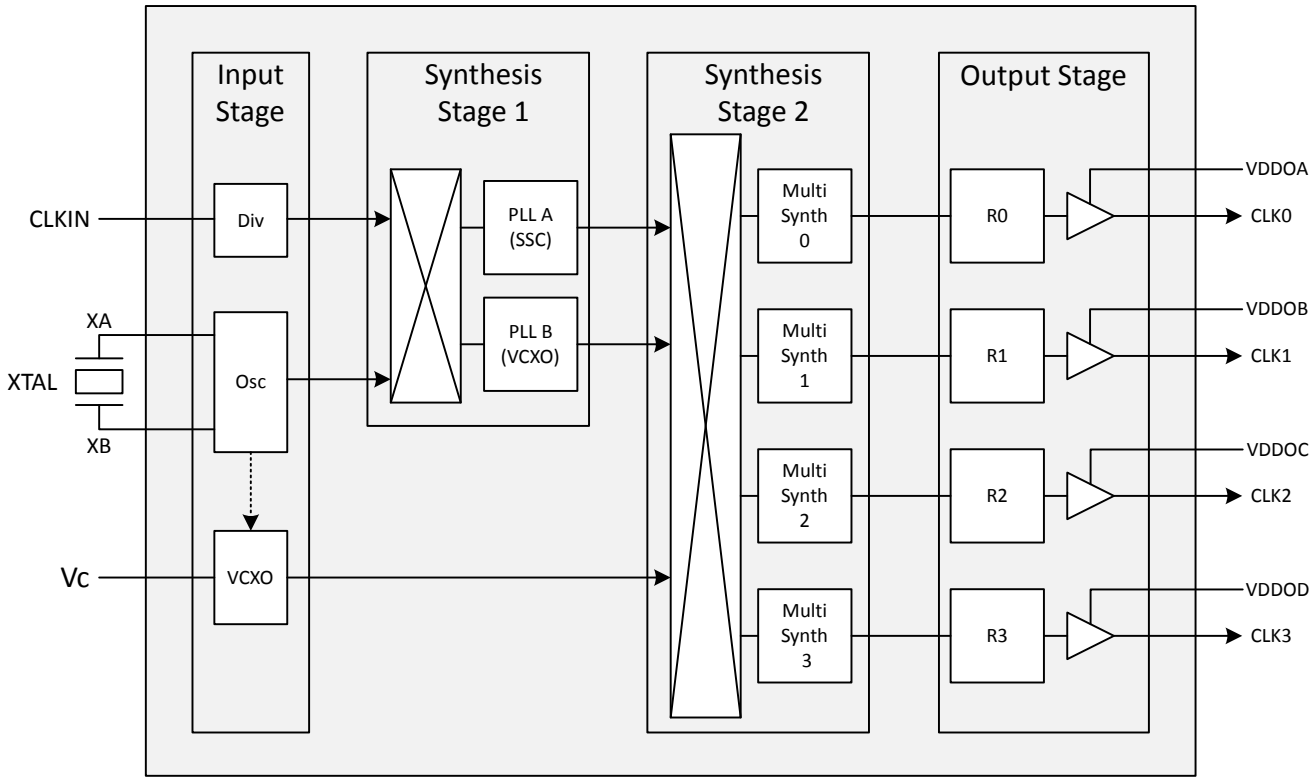
AN1234
Manually Generating an Si5351 Register Map for 16QFN Devices

The Si5351 is a highly flexible and configurable clock generator and VCXO. To support this flexibility, Silicon Labs has created ClockBuilder Pro to create register maps automatically and easily for a given configuration. Since programming with ClockBuilder Pro may not always be well suited for every system's requirements, this document presents the procedures and equations for determining a complete register set from a frequency plan. Section 2 highlights the overall frequency plan algorithm, and sections 3 and beyond detail all the necessary register calculations. This application note focuses only on programming a 16-QFN Si5351 device. Similar programming guidelines for 10-MSOP and 20-QFN devices can be found in AN619: Manually Generating an Si5351 Register Map.

KEY POINTS

- 4-output I2C programmable CMOS clock generator
- Generates any frequency between 2.5kHz and 200MHz
- Available in three variants
  - Si5351A - XTAL only device
  - Si5351B - XTAL + VCXO
  - Si5351C - XTAL + CLKIN
- Double PLL architecture allows additional frequency plan flexibility.
- Configurable spread spectrum selectable at each output.
- MultiSynth dividers allow exact frequency synthesis at each output
- Easily create frequency plans, export register maps, and create custom pre-burned orderable part numbers using ClockBuilder Pro.
- For more information, refer to the Si5351 Datasheet.



16-QFN Generalized Block Diagram

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1. Conceptualizing a Frequency Plan

The device consists of two PLLs—PLLA and PLLB. Each PLL consists of a Feedback Multisynth used to generate an intermediate VCO frequency in the range of 600 to 900 MHz. Either of these two VCO frequencies can be divided down by the individual output Multisynth dividers to generate a Multisynth frequency between 500 kHz and 200 MHz. Additionally, the R dividers can be used to generate any output frequency down to 2.5 kHz. The relationship between the VCO and output frequencies is given below.

$$fout_x = \frac{fvco}{Output\_Multisynth_x \times R_x}$$

$$fvco = fin \times Feedback\_Multisynth$$

Use the steps in the sections below to draw out a conceptual frequency plan map.

1.1 PLL Selection

If spread spectrum is not enabled, either of the two PLLs may be used as the source for any outputs of the Si5351A. If both XTAL and CLKIN input options are used simultaneously (Si5351C only), then one PLL must be reserved for use with CLKIN and one for use with the XTAL.

Note: PLLA must be used for any spread spectrum-enabled outputs. PLLB must be used for any VCXO outputs.

1.1.1 Selecting the Proper VCO Frequencies and Divide Ratios

The general criteria below may be used to set the VCO frequencies. This is a general model, and individual applications may require some modification.

1. Valid Multisynth divider ratios are 4, 6, 8, and any fractional value between 8 + 1/1,048,575 and 2048. This means that if any output is greater than 112.5 MHz (900 MHz/8), then this output frequency sets one of the VCO frequencies.
2. For the frequencies where jitter is a concern make the output Multisynth divide ratio an integer. If possible, make both output and feedback Multisynth ratios integers.
3. Once criteria 1 and 2 are satisfied, try to select as many integer output Multisynth ratios as possible.

1.2 Output Clock Pin Assignment (Optional)

The 16-QFN Si5351 is desiged so every output has its own individual VDDO bank. This helps minimizes jitter due to PCB crosstalk.

If possible, place output frequencies that are integer multiples of one another close to eachother. Attempt to either isolate non-integer related frequencies, or place them next to the output with the least sensitive jitter requirements.

Note: The only valid divide ratio for the CLK3 Multisynth divider is even integers between 6 and 254 inclusive. This could potentially limit the two VCO frequencies if all 4 output clocks are used.

2. Configuring Input and PLL Register Parameters (Synthesis Stage 1)

This section describes register parameters related to the input reference and the two PLLs.

2.1 PLL Input Source

The input source for each PLL must be selected. For the Si5351A and Si5351B devices, the only possible source is the XTAL, but for the Si5351C device, each PLL can be synchronized to either an XTAL or a CMOS clock on the CLKIN pin.

2.1.1 XTAL Source

If the source for the PLL is a crystal, PLLx_SRC must be set to 0 in register 15. XTAL_CL[1:0] must also be set to match the crystal load capacitance (see register 183).

2.1.2 CMOS Clock Source

If a PLL needs to be synchronized to a CMOS clock, PLLx_SRC must be 1. The input frequency range of the PLL is 10 to 40 MHz. If CLKIN is > 40 MHz, the CLKIN input divider must be used to bring the PLL input within the 10–40 MHz range. See CLKIN_DIV[1:0], register 15, bits [7:6].

2.2 Feedback Multisynth Divider Equations

Once the input source for each PLL and (if necessary) CLKIN_DIV are determined, the two VCO frequencies selected in Section 2 above can be generated using the following equations. Each feedback divider essentially multiplies the source frequency such that

$$f_{VCO} = f_{XTAL} \times \left(a + \frac{b}{c}\right)$$

and/or

$$f_{VCO} = \frac{f_{CLKIN}}{CLKIN\_DIV} \times \left(a + \frac{b}{c}\right)$$

The fractional ratio

$$a + \frac{b}{c}$$

has a valid range of 15 + 0/1,048,575 and 90 and is represented in the Si5351 register space using the equations below.

$$MSNx\_P1[17:0] = 128 \times a + Floor\left(128 \times \frac{b}{c}\right) - 512$$

$$MSNx\_P2[19:0] = 128 \times b - c \times Floor\left(128 \times \frac{b}{c}\right)$$

$$MSNx\_P3[19:0] = c$$

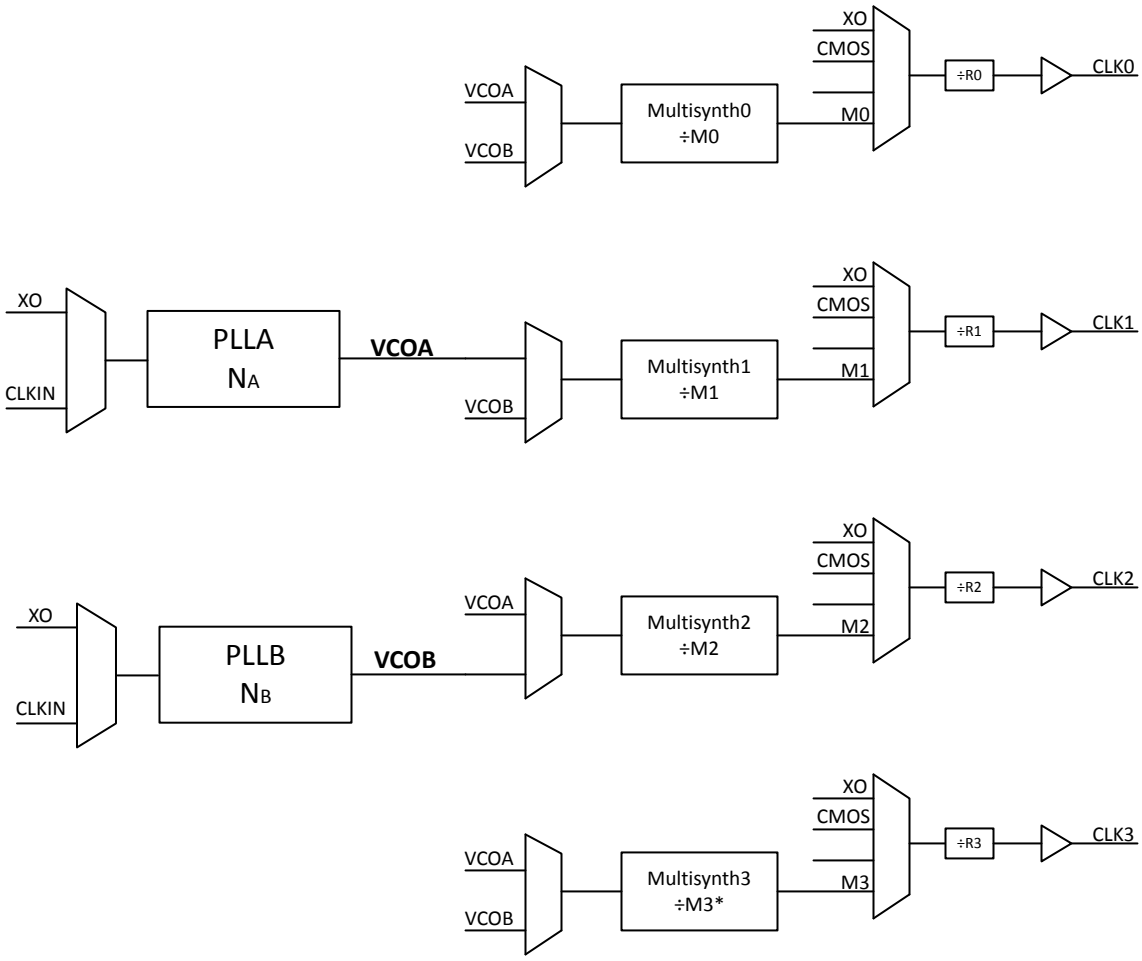
In the equations above, x is used to represent MSNA and MSNB, the PLLA and PLLB Multisynth dividers respectively. The equations above must be repeated for Multisynths MSNA and MSNB. As mentioned earlier in Section 1.1 PLL Selection, spread spectrum is only supported by PLLA, and the VCXO functionality is only supported by PLLB. When using the VCXO function, set the MSNB divide ratio a + b/c such that c = 10^6. This must be taken into consideration when configuring a frequency plan.

2.2.1 Integer Divide Values (FBx_INT)

If a + b/c is an even integer, integer mode may be enabled for PLLA or PLLB by setting parameter FBA_INT or FBB_INT respectively. In most cases setting this bit will improve jitter when using even integer divide values. Whenever spread spectrum is enabled, FBA_INT must be set to 0.

3. Configuring the Output Register Parameters

This section covers the Multisynth and output driver settings necessary for each output. As shown in Figure 3.1, one of the two VCO frequencies is divided down by each Multisynth divider. This is followed by an output driver state. See 3.2 Output Driver Settings.



*The Multisynth 3 divide ratio can only be an even integer between 6 and 254

Figure 3.1. Detailed Dividers and Output Drivers Block Diagram

3.1 Output Multisynth Settings (Synthesis Stage 2)

This section describes the settings related to the individual Multisynths. The 16-QFN Si5351 consists of three fractional Multisynth divider (MS0-MS2) and one even-integer divider (MS3).

3.1.1 Output Multisynth Source (MSx_SRC)

Each of these dividers can be set to use PLLA or PLLB as its reference by setting MSx_SRC to 0 or 1 respectively. See the bit 5 description of registers 17, 18, and 21.

3.1.2 Output Multisynth Divider Equations (Fout <= 150 MHz)

Once the PLL source for the output Multisynth is selected, the divide ratio can be set using the equations below.

Divider represented as fractional number,

$$a + \frac{b}{c}$$

between 8 + 1/1,048,575 and 2048.

$$MSx\_P1[17:0] = 128 \times a + Floor\left(128 \times \frac{b}{c}\right) - 512$$

$$MSx\_P2[19:0] = 128 \times b - c \times Floor\left(128 \times \frac{b}{c}\right)$$

$$MSx\_P3[19:0] = c$$

In the equations above, x=0, 1, 2. As previously noted, MS3 is an integer-only divider, with a valid range of all even integers between 6 and 254 inclusive. For MS3, set MS3_P1 directly (e.g., MS3_P1=divide value).

3.1.2.1 Integer Divide Values(MSx_INT)

If any of the MS0-MS2 dividers is an even integer, Multisynth integer mode may be enabled by setting MSx_INT=1 (see registers 17,18, and 21, bit 6). In most cases setting this bit will improve jitter when using even integer divide values. Multisynth 3 inherently operates in integer mode, and so there is no register to turn integer mode on or off. However, it's important to note that Multisynth integer mode cannot be used when adding phase offsets in NVM. In other words, MSx_INT needs to be set to 0 if phase offsets need to be enabled.

3.1.3 Output Multisynth Divider Equations (150 MHz <Fout<=200 MHz)

Output frequencies greater than 150 MHz are available on Multisynths 0-2. For this frequency range a divide value of 4 must be used by setting

- MSx_P1=0,
- MSx_P2=0,
- MSx_P3=1,
- MSx_INT=1, and
- MSx_DIVBY4[1:0]=11b.

Set the appropriate feedback Multisynth to generate f_{VCO}=Fout*4.

3.2 Output Driver Settings

Once the Multisynth registers are assembled, the output driver settings can be modified according to the information in this section.

3.2.1 Clock Source (CLKx_SRC)

Generally, Multisynth x should be output on CLKx, however XO, CLKIN, or a divided version of either (see section 3.2.2 R Dividers on R dividers) may also be output on each of the CLKx pins. See CLKx_SRC description for details.

3.2.2 R Dividers

The R dividers can be used to generate frequencies below about 500 kHz. Each individual output R divider can be set to 1, 2, 4, 8,....128 by writing the proper setting for Rx_DIV. Set this parameter to generate frequencies down to 2.5kHz.

3.2.3 (CLKx_INV)

In some cases, the user may need to invert the polarity (i.e., 180° phase offset) of one or more outputs with respect to the other outputs. This is achieved by setting CLKx_INV=1.

3.2.4 (CLKx_DIS_STATE)

When a clock is disabled via the OEB pin or OEB control register (reg 3), the output driver may be set to present a logic low, logic high, or high-impedance at the device pin. See CLKx_DIS_STATE description for details.

3.2.5 Unused Clock Outputs

Any unused clock outputs should be powered down to reduce IDDO current consumption. Set CLKx_PDN=1 to power down unused clock output drivers. The 4-output 16-QFN Si5351 is a scaled down version of the 8-output 20-QFN Si5351. This means there are 4 additional unused un-bonded outputs that need to be powered off. This will be done automatically for any project created in ClockBuilder Pro. However, it will need to be done manually when programming a blank Si5351 by hand without the use of ClockBuilder Pro. If this is the case, the following four registers will need to be written after every power cycle, regardless of frequency plan.

Register Address (Decimal)	Write Value (Hex)
16	0x80
19	0x80
20	0x80
22	*Dependent on FBB_INT setting. See the Register 22 Description in Section 8.

4. Configuring Spread Spectrum Register Parameters

Spread spectrum can be enabled on any Multisynth output that uses PLLA as its reference. Valid ranges for spread spectrum include –0.1% to –2.5% down spread and up to ± 1.5% center spread. This spread modulation rate is fixed at approximately 31.5 kHz.

The following parameters must be known to properly set up spread spectrum:

- $f_{PFD(A)}$→ input frequency to PLLA in Hz (determined in Sec 2 above and referred to in 2.1.2 CMOS Clock Source). This is also listed in the ClockBuilder Pro generated register map file as "#PFD(MHz)=..."
- a + b/c →PLLA Multisynth ratio (determined in Sec 2 above).
- sscAMP→Spread amplitude (e.g., for down or center spread amplitude of 1%, sscAmp = 0.01).

Use the equations below to set up the desired spread spectrum profile.

Note: Make sure MSNA is set up in fractional mode when using the spread spectrum feature. See parameter FBA_INT in register 22.

4.1 Down Spread

For down spread, four spread spectrum parameters need to be written: SSUDP[11:0], SSDN_P1[11:0], SSDN_P2[14:0], and SSDN_P3[14:0].

Up/Down Parameter:

$$SSUDP[11:0] = Floor\left(\frac{f_{PFD}}{4 \times 31,500}\right)$$

Intermediate Equation (no register writes):

$$SSDN = 64 \times \left(a + \frac{b}{c}\right) \times \frac{sscAmp}{(1 + sscAmp) \times SSUDP}$$

Down-Spread Parameters:

$$SSDN\_P1[11:0] = Floor[SSDN]$$

$$SSDN\_P2[14:0] = 32,767 \times [SSDN - SSDN\_P1]$$

$$SSDN\_P3[14:0] = 32,767 = 0x7FFF$$

Up-Spread Parameters:

$$SSUP\_P1 = 0$$

$$SSUP\_P2 = 0$$

$$SSUP\_P3 = 1$$

4.2 Center Spread

For center spread, seven spread spectrum parameters need to be written: SSUDP[11:0], SSDN_P1[11:0], SSDN_P2[14:0], SSDN_P3[14:0], SSUP_P1[11:0], SSUP_P2[14:0], and SSUP_P3[14:0].

Up/Down Parameter:

$$SSUDP[11:0] = Floor\left(\frac{f_{PFD}}{4 \times 31,500}\right)$$

Intermediate Equations (no register writes):

$$SSUP = 128 \times \left(a + \frac{b}{c}\right) \times \frac{sscAmp}{(1 - sscAmp) \times SSUDP}$$

$$SSDN = 128 \times \left(a + \frac{b}{c}\right) \times \frac{sscAmp}{(1 + sscAmp) \times SSUDP}$$

Up-Spread Parameters:

$$SSUP\_P1[11:0] = Floor[SSUP]$$

$$SSUP\_P2[14:0] = 32,767 \times [SSUP - SSUP\_P1]$$

$$SSUP\_P3[14:0] = 32,767 = 0x7FFF$$

Down-Spread Parameters:

$$SSDN\_P1[11:0] = Floor[SSDN]$$

$$SSDN\_P2[14:0] = 32,767 \times [SSDN - SSDN\_P1]$$

$$SSDN\_P3[14:0] = 32767 = 0x7FFF$$

4.3 Spread Spectrum Enable Pin (SSEN)

The Spread Spectrum Enable control pin is available on the Si5351A and B devices. Spread spectrum enable functionality is a logical OR of the SSEN pin and SSC_EN register bit, so for the SSEN pin to work properly, the SSC_EN register bit must be set to 0.

5. Configuring Initial Phase Offset Register Parameters

Outputs 0-2 of the 16-QFN Si5351 can be programmed with an independent initial phase offset. The phase offset only works when MS0-2 are set as fractional dividers (divider values greater than 8). The phase offset parameter is an unsigned integer where each LSB represents a phase difference of a quarter of the VCO period, $T_{VCO}/4$. Use the equation below to determine the register value. Also, remember that any divider using the phase offset feature needs the MSx_INT bit set to 0.

$$CLKx\_PHOFF[4:0] = Round(DesiredOffset_{(sec)} \times 4 \times F_{VCO})$$

6. Configuring VCXO Parameters (Si5351 B only)

The Si5351B combines free-running clock generation and a VCXO in a single package. The VCXO architecture of the Si5350B eliminates the need for an external pullable crystal. The “pulling” is done at PLLB. Only a standard, low cost, fixed-frequency (25 or 27 MHz) AT-cut crystal is required and is used as the reference source for both PLLA and PLLB.

PLLB must be used as the source for any VCXO output clock. Feedback B Multisynth divider ratio must be set such that the denominator, c, in the fractional divider a + b/c is fixed to 10^6. Set VCXO_Param register value according to the equation below. Note that 1.03 is a margining factor to ensure the full desired pull range is achieved. For a desired pull-range of +/– 30 ppm, the value APR in the equation below is 30, for +/– 60 ppm APR is 60, and so on.

$$\text{VCXO\_Param}[21:0] = 1.03 \times \left[128a + \frac{b}{10^6}\right] \times \text{APR}$$

7. Si5351 Registers

This section describes the registers and their usage in detail. These values are easily configured using ClockBuilder Pro.

7.1 Register Map Summary

The following is a summary of the register map used to read status, control, and configure the Si5351.

Register	7	6	5	4	3	2	1	0
0	SYS_INIT	LOL_B	LOL_A	LOS_CLKIN	LOS_XTAL	Reserved	REVID[1:0]	
1	SYS_IN-IT_STKY	LOL_B_STKY	LOL_A_STKY	LOS_CLKIN_STKY	LOS_XTAL_STKY	Reserved		
2	Reserved							
3	CLK3_OEB	Reserved	CLK2_OEB	Reserved		CLK1_OEB	CLK0_OEB	Re-served
4-8	Reserved							
9	OEB_MASK3	Reserved	OEB_MASK2	Reserved		OEB_MASK1	OEB_MASK0	Re-served
10-14	Reserved							
15	CLKIN_DIV[1:0]		Reserved		PLLB_SRC	PLLA_SRC	Reserved	
16	1	Reserved						
17	CLK0_PDN	MS0_INT	MS0_SRC	CLK0_INV	CLK0_SRC[1:0]		CLK0_IDRV[1:0]	
18	CLK1_PDN	MS1_INT	MS1_SRC	CLK1_INV	CLK1_SRC[1:0]		CLK1_IDRV[1:0]	
19	1	Reserved						
20	1	Reserved						
21	CLK2_PDN	MS2_INT	MS2_SRC	CLK2_INV	CLK2_SRC[1:0]		CLK2_IDRV[1:0]	
22	1	FBA_INT	Reserved					
23	CLK3_PDN	FBB_INT	MS3_SRC	CLK3_INV	CLK3_SRC[1:0]		CLK3_IDRV[1:0]	
24	Reserved		CLK1_DIS_STATE[1:0]		CLK0_DIS_STATE[1:0]		Reserved	
25	CLK3_DIS_STATE[1:0]		Reserved		CLK2_DIS_STATE[1:0]		Reserved	
26	MSNA_P3[15:8]							
27	MSNA_P3[7:0]							
28	Reserved						MSNA_P1[17:16]	
29	MSNA_P1[15:8]							
30	MSNA_P1[7:0]							
31	MSNA_P3[19:16]				MSNA_P2[19:16]			
32	MSNA_P2[15:8]							
33	MSNA_P2[7:0]							
34	MSNB_P3[15:8]							
35	MSNB_P3[7:0]							
36	Reserved						MSNB_P1[17:16]	

Register	7	6	5	4	3	2	1	0
37	MSNB_P1[15:8]							
38	MSNB_P1[7:0]							
39	MSNB_P3[19:16]				MSNB_P2[19:16]			
40	MSNB_P2[15:8]							
41	MSNB_P2[7:0]							
42-49	Reserved							
50	MS0_P3[15:8]							
51	MS0_P3[7:0]							
52		R0_DIV[2:0]			MS0_DIVBY4[1:0]		MS0_P1[17:16]	
53	MS0_P1[15:8]							
54	MS0_P1[7:0]							
55	MS0_P3[19:16]				MS0_P2[19:16]			
56	MS0_P2[15:8]							
57	MS0_P2[7:0]							
58	MS1_P3[15:8]							
59	MS1_P3[7:0]							
60		R1_DIV[2:0]			MS1_DIVBY4[1:0]		MS1_P1[17:16]	
61	MS1_P1[15:8]							
62	MS1_P1[7:0]							
63	MS1_P3[19:16]				MS1_P2[19:16]			
64	MS1_P2[15:8]							
65	MS1_P2[7:0]							
66-81	Reserved							
82	MS2_P3[15:8]							
83	MS2_P3[7:0]							
84		R2_DIV[2:0]			MS2_DIVBY4[1:0]		MS2_P1[17:16]	
85	MS2_P1[15:8]							
86	MS2_P1[7:0]							
87	MS2_P3[19:16]				MS2_P2[19:16]			
88	MS2_P2[15:8]							
89	MS2_P2[7:0]							
90	Reserved							
91	MS3_P1[7:0]							
92	Reserved	R3_DIV[2:0]			Reserved			
93-148	Reserved							
149	SSC_EN	SSDN_P2[14:8]						
150	SSDN_P2[7:0]							

Register	7	6	5	4	3	2	1	0
151	SSC_MODE	SSDN_P3[14:8]						
152	SSDN_P3[7:0]							
153	SSDN_P1[7:0]							
154	SSUDP[11:8]				SSDN_P1[11:8]			
155	SSUDP[7:0]							
156		SSUP_P2[14:8]						
157	SSUP_P2[7:0]							
158		SSUP_P3[14:8]						
159	SSUP_P3[7:0]							
160	SSUP_P1[7:0]							
161	SS_NCLK[3:0]				SSUP_P1[11:8]			
162	VCXO_Param[7:0]							
163	VCXO_Param[15:8]							
164	Reserved		VCXO_Param[21:16]					
165	Reserved							
166	Reserved	CLK0_PHOFF[6:0]						
167	Reserved	CLK1_PHOFF[6:0]						
168	Reserved							
169	Reserved							
170	Reserved	CLK2_PHOFF[6:0]						
171-176	Reserved							
177	PLLB_RST	Reserved	PLLA_RST	Reserved				
178-182	Reserved							
183	XTAL_CL[1:0]		Reserved					
184-186	Reserved							
187	CLKIN_FAN-OUT_EN	XO_FAN-OUT_EN	Reserved					
188-255	Reserved							

8. Register Descriptions

Register 0. Device Status

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SYS_INIT	LOL_B	LOL_A	LOS_CLKIN	LOS_XTAL	Reserved	REVID[1:0]	
Type	R	R	R	R	R	R	R	

Reset value = 0000 0000

Bit	Name	Function
7	SYS_INIT	**System Initialization Status.** During power up the device copies the content of the NVM into RAM and performs a system initialization. The device is not operational until initialization is complete. It is not recommended to read or write registers in RAM through the I^2C interface until initialization is complete. 0: System initialization is complete. Device is ready. 1: Device is in system initialization mode.
6	LOL_B	**PLL B Loss Of Lock Status.** PLL B will operate in a locked state when it has a valid reference from CLKIN or XTAL. A loss of lock will occur if the frequency of the reference clock forces the PLL to operate outside of its lock range or if the reference clock fails to meet the minimum requirements of a valid input signal as specified in the Si5351 data sheet. 0: PLL B is locked. 1: PLL B is unlocked.
5	LOL_A	**PLL A Loss Of Lock Status.** PLL A will operate in a locked state when it has a valid reference from CLKIN or XTAL. A loss of lock will occur if the frequency of the reference clock forces the PLL to operate outside of its lock range as specified in the data sheet, or if the reference clock fails to meet the minimum requirements of a valid input signal as specified in the Si5351 data sheet. 0: PLL A is operating normally. 1: PLL A is unlocked.
4	LOS_CLKIN	**CLKIN Loss Of Signal (Si5351C Only).** A loss of signal status indicates that the reference clock failed to meet the minimum requirements of a valid input signal as specified in the Si5351 data sheet. 0: Valid clock signal at the CLKIN pin. 1: Loss of signal detected at the CLKIN pin.
3	LOS_XTAL	**Crystal Loss of Signal** A loss of signal status indicates that the XA/XB crystal input failed to meet the minimum requirements of a valid input signal as specified in the Si5351 datasheet. 0: Valid crystal signal at the XA and XB pins 1: Loss of crystal signal detected
2	Reserved	Reserved.
1:0	REVID[1:0]	**Revision number of the device.**

Register 1. Interrupt Status Sticky

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SYS_INIT_STKY	LOL_B_STKY	LOL_A_STKY	LOS_CLKIN_STKY	LOS_XTAL_STKY	Reserved		
Type	R/W	R/W	R/W	R/W	R/W	R/W		

Reset value = 0000 0000

Bit	Name	Function
7	SYS_INIT_STKY	**System Calibration Status Sticky Bit.** The SYS_INIT_STKY bit is triggered when the SYS_INIT bit (register 0, bit 7) is triggered high. It remains high until cleared. Writing a 0 to this register bit will cause it to clear. 0: No SYS_INIT interrupt has occurred since it was last cleared. 1: A SYS_INIT interrupt has occurred since it was last cleared.
6	LOL_B_STKY	**PLLB Loss Of Lock Status Sticky Bit.** The LOL_B_STKY bit is triggered when the LOL_B bit (register 0, bit 6) is triggered high. It remains high until cleared. Writing a 0 to this register bit will cause it to clear. 0: No PLL B interrupt has occurred since it was last cleared. 1: A PLL B interrupt has occurred since it was last cleared.
5	LOL_A_STKY	**PLLA Loss Of Lock Status Sticky Bit.** The LOL_A_STKY bit is triggered when the LOL_A bit (register 0, bit 5) is triggered high. It remains high until cleared. Writing a 0 to this register bit will cause it to clear. 0: No PLLA interrupt has occurred since it was last cleared. 1: A PLLA interrupt has occurred since it was last cleared.
4	LOS_CLKIN_STKY	**CLKIN Loss Of Signal Sticky Bit (Si5351C Only).** The LOS_CLKIN_STKY bit is triggered when the LOS_CLKIN bit (register 0, bit 4) is triggered high. It remains high until cleared. Writing a 0 to this register bit will cause it to clear. 0: No LOS_CLKIN interrupt has occurred since it was last cleared. 1: A LOS_CLKIN interrupt has occurred since it was last cleared.
3	LOS_XTAL_STKY	**Crystal Loss Of Signal Sticky Bit** The LOS_XTAL_STKY bit is triggered when the LOS_XTAL bit (register 0, bit 3) is triggered high. It remains high until cleared. Writing a 0 to this register bit will cause it to clear. 0: No LOS_XTAL interrupt has occurred since it was last cleared. 1: A LOS_XTAL interrupt has occurred since it was last cleared
2:0	Reserved	Leave as default.

Register 3. Output Enable Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLK3_OEB	Reserved	CLK2_OEB	Reserved		CLK1_OEB	CLK0_OEB	Reserved
Type	R/W	R/W	R/W	R/W		R/W	R/W	R/W

Reset value = 0000 0000

Bit	Name	Function
7	CLK3_OEB	**Output Disable for CLK3.** 0: Enable CLK3 output. 1: Disable CLK3 output.
6	Reserved	Leave as default
5	CLK2_OEB	**Output Disable for CLK2.** 0: Enable CLK2 output. 1: Disable CLK2 output.
4:3	Reserved	Leave as default
2	CLK1_OEB	**Output Disable for CLK1.** 0: Enable CLK1 output. 1: Disable CLK1 output.
1	CLK0_OEB	**Output Disable for CLK0.** 0: Enable CLK0 output. 1: Disable CLK0 output.
0	Reserved	Leave as default

Register 9. OEB Pin Enable Control Mask

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OEB_MASK3	Reserved	OEB_MASK2	Reserved		OEB_MASK1	OEB_MASK0	Reserved
Type	R/W	R/W	R/W	R/W		R/W	R/W	R/W

Reset value = 0000 0000

Bit	Name	Function
7	OEB_MASK3	**OEB pin enable control of CLK3.** 0: OEB pin controls enable/disable state of CLK3 output. 1: OEB pin does not control enable/disable state of CLK3 output.
6	Reserved	Leave as default
5	OEB_MASK2	**OEB pin enable control of CLK2.** 0: OEB pin controls enable/disable state of CLK2 output. 1: OEB pin does not control enable/disable state of CLK2 output.
4:3	Reserved	Leave as default
2	OEB_MASK1	**OEB pin enable control of CLK1.** 0: OEB pin controls enable/disable state of CLK1 output. 1: OEB pin does not control enable/disable state of CLK1 output.
1	OEB_MASK0	**OEB pin enable control of CLK0.** 0: OEB pin controls enable/disable state of CLK0 output. 1: OEB pin does not control enable/disable state of CLK0 output.
0	Reserved	Leave as default

Register 15. PLL Input Source

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLKIN_DIV[1:0]		Reserved		PLLB_SRC	PLLA_SRC	Reserved	
Type	R/W	R/W	R/W		R/W	R/W	R/W	

Reset value = 0000 0000

Bit	Name	Function
7:6	CLKIN_DIV[1:0]	**CIKIN Input Divider.** Valid PLL input range is 10-40 MHz. If CLKIN is > 40 MHz, CLKIN input divider, CLKIN_DIV, must be used to bring the PLL input within the 10-40 MHz range. 00b: Divide by 1. 01b: Divide by 2. 10b: Divide by 4. 11b: Divide by 8.
5:4	Reserved	Leave as default.
3	PLLB_SRC	**Input Source Select for PLLB.** 0: Select the XTAL input as the reference clock for PLLB. 1: Select the CLKIN input as the reference clock for PLLB (Si5351C only).
2	PLLA_SRC	**Input Source Select for PLLA.** 0: Select the XTAL input as the reference clock for PLLA. 1: Select the CLKIN input as the reference clock for PLLA (Si5351C only).
1:0	Reserved	Leave as default.

Register 16. Unused Output Power Down

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	1	Reserved						
Type	R/W	R/W						

Reset value = 0000 0000

Bit	Name	Function
7	**Please write this bit to a 1**	
6:0	Reserved	Leave as default

Register 17. CLK0 Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLK0_PDN	MS0_INT	MS0_SRC	CLK0_INV	CLK0_SRC[1:0]		CLK0_IDRV[1:0]	
Type	R/W	R/W	R/W	R/W	R/W		R/W	

Reset value = 0000 0000

Bit	Name	Function
7	CLK0_PDN	**Clock 0 Power Down.** This bit allows powering down the CLK0 output driver to conserve power when the output is unused. 0: CLK0 is powered up. 1: CLK0 is powered down.
6	MS0_INT	**MultiSynth 0 Integer Mode.** When the MS0 divider is an even integer, this bit can be used to force MS0 into integer mode to improve jitter performance. Not valid for odd integers. Note that the fractional mode is necessary when a delay offset is specified for CLK0. 0: MS0 operates in fractional division mode. 1: MS0 operates in integer mode.
5	MS0_SRC	**MultiSynth Source Select for CLK0.** 0: Select PLLA as the source for MultiSynth0. 1: Select PLLB (Si5351A/C only) or VCXO (Si5351B only) MultiSynth0.
4	CLK0_INV	**Output Clock 0 Invert.** 0: Output Clock 0 is not inverted. 1: Output Clock 0 is inverted.
3:2	CLK0_SRC[1:0]	**Output Clock 0 Input Source.** These bits determine the input source for CLK0. 00: Select the XTAL as the clock source for CLK0. This option by-passes both synthesis stages (PLL/VCXO & MultiSynth) and connects CLK0 directly to the oscillator which generates an output frequency determined by the XTAL frequency. 01: Select CLKIN as the clock source for CLK0. This by-passes both synthesis stages (PLL/VCXO & MultiSynth) and connects CLK0 directly to the CLKIN input. This essentially creates a buffered output of the CLKIN input. 10: Reserved. Do not select this option. 11: Select MultiSynth 0 as the source for CLK0. Select this option when using the Si5351 to generate free-running or synchronous clocks.
1:0	CLK0_IDRV[1:0]	**CLK0 Output Rise and Fall time / Drive Strength Control.** 00: 2 mA 01: 4 mA 10: 6 mA 11: 8 mA

Register 18. CLK1 Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLK1_PDN	MS1_INT	MS1_SRC	CLK1_INV	CLK1_SRC[1:0]		CLK1_IDRV[1:0]	
Type	R/W	R/W	R/W	R/W	R/W		R/W	

Reset value = 0000 0000

Bit	Name	Function
7	CLK1_PDN	**Clock 1 Power Down.** This bit allows powering down the CLK1 output driver to conserve power when the output is unused. 0: CLK1 is powered up. 1: CLK1 is powered down.
6	MS1_INT	**MultiSynth 1 Integer Mode.** When the MS1 divider is an even integer, this bit can be used to force MS1 into integer mode to improve jitter performance. Not valid for odd integers. Note that the fractional mode is necessary when a delay offset is specified for CLK1. 0: MS1 operates in fractional division mode. 1: MS1 operates in integer mode.
5	MS1_SRC	**MultiSynth Source Select for CLK1.** 0: Select PLLA as the source for MultiSynth1. 1: Select PLLB (Si5351A/C only) or VCXO (Si5351B only) MultiSynth1.
4	CLK1_INV	**Output Clock 1 Invert.** 0: Output Clock 1 is not inverted. 1: Output Clock 1 is inverted.
3:2	CLK1_SRC[1:0]	**Output Clock 1 Input Source.** These bits determine the input source for CLK1. 00: Select the XTAL as the clock source for CLK1. This option by-passes both synthesis stages (PLL/VCXO & MultiSynth) and connects CLK1 directly to the oscillator which generates an output frequency determined by the XTAL frequency. 01: Select CLKIN as the clock source for CLK1. This by-passes both synthesis stages (PLL/VCXO & MultiSynth) and connects CLK1 directly to the CLKIN input. This essentially creates a buffered output of the CLKIN input. 10: Reserved. Do not select this option. 11: Select MultiSynth 1 as the source for CLK1. Select this option when using the Si5351 to generate free-running or synchronous clocks.
1:0	CLK1_IDRV[1:0]	**CLK1 Output Rise and Fall time / Drive Strength Control.** 00: 2 mA 01: 4 mA 10: 6 mA 11: 8 mA

Register 19. Unused Output Power Down

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	1	Reserved						
Type	R/W	R/W						

Reset value = 0000 0000

Bit	Name	Function
7	**Please write this bit to a 1**	
6:0	Reserved	Leave as default

Register 20. Unused Output Power Down

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	1	Reserved						
Type	R/W	R/W						

Reset value = 0000 0000

Bit	Name	Function
7	**Please write this bit to a 1**	
6:0	Reserved	Leave as default

Register 21. CLK2 Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLK2_PDN	MS2_INT	MS2_SRC	CLK2_INV	CLK2_SRC[1:0]		CLK2_IDRV[1:0]	
Type	R/W	R/W	R/W	R/W	R/W		R/W	

Reset value = 0000 0000

Bit	Name	Function
7	CLK2_PDN	**Clock 2 Power Down.** This bit allows powering down the CLK2 output driver to conserve power when the output is unused. 0: CLK2 is powered up. 1: CLK2 is powered down.
6	MS2_INT	**MultiSynth 2 Integer Mode.** When the MS2 divider is an even integer, this bit can be used to force MS2 into integer mode to improve jitter performance. Not valid for odd integers. Note that the fractional mode is necessary when a delay offset is specified for CLK2. 0: MS2 operates in fractional division mode. 1: MS2 operates in integer mode.
5	MS2_SRC	**MultiSynth Source Select for CLK2.** 0: Select PLLA as the source for MultiSynth2. 1: Select PLLB (Si5351A/C only) or VCXO (Si5351B only) MultiSynth2.
4	CLK2_INV	**Output Clock 2 Invert.** 0: Output Clock 2 is not inverted. 1: Output Clock 2 is inverted.
3:2	CLK2_SRC[1:0]	**Output Clock 2 Input Source.** These bits determine the input source for CLK2. 00: Select the XTAL as the clock source for CLK2. This option by-passes both synthesis stages (PLL/VCXO & MultiSynth) and connects CLK2 directly to the oscillator which generates an output frequency determined by the XTAL frequency. 01: Select CLKIN as the clock source for CLK2. This by-passes both synthesis stages (PLL/VCXO & MultiSynth) and connects CLK2 directly to the CLKIN input. This essentially creates a buffered output of the CLKIN input. 10: Reserved. Do not select this option. 11: Select MultiSynth 2 as the source for CLK2. Select this option when using the Si5351 to generate free-running or synchronous clocks.
1:0	CLK2_IDRV[1:0]	**CLK2 Output Rise and Fall time / Drive Strength Control.** 00: 2 mA 01: 4 mA 10: 6 mA 11: 8 mA

Register 22. Feedback A Integer Mode Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	1	FBA_INT	Reserved					
Type	R/W	R/W	R/W					

Reset value = 0000 0000

Bit	Name	Function
7	**Please write this bit to 1**	
6	FBA_INT	**FBA MultiSynth Integer Mode.** This bit can be used to force Feedback A Multisynth into Integer mode to improve jitter performance. Note that the fractional mode is necessary when spread spectrum is specified for any output clocks. 0: MSNA operates in fractional division mode. 1: MSNA operates in integer mode.
5:0	Reserved	Reserved. Leave as default.

Register 23. CLK3 and Feedback B Integer Mode Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLK3_PDN	FBB_INT	MS3_SRC	CLK3_INV	CLK3_SRC[1:0]		CLK3_IDRV[1:0]	
Type	R/W	R/W	R/W	R/W	R/W		R/W	

Reset value = 0000 0000

Bit	Name	Function
7	CLK3_PDN	**Clock 3 Power Down.** This bit allows powering down the CLK3 output driver to conserve power when the output is unused. 0: CLK3 is powered up. 1: CLK3 is powered down.
6	FBB_INT	**FBB MultiSynth Integer Mode.** This bit can be used to force Feedback B into Integer mode to improve jitter performance. 0: MSNB operates in fractional division mode. 1: MSNB operates in integer mode.
5	MS3_SRC	**MultiSynth Source Select for CLK3.** 0: Select PLLA as the source for MultiSynth3. 1: Select PLLB (Si5351A/C only) or VCXO (Si5351B only) MultiSynth3.
4	CLK3_INV	**Output Clock 3 Invert.** 0: Output Clock 3 is not inverted. 1: Output Clock 3 is inverted.
3:2	CLK3_SRC[1:0]	**Output Clock 3 Input Source.** These bits determine the input source for CLK3. 00: Select the XTAL as the clock source for CLK3. This option by-passes both synthesis stages (PLL/VCXO & MultiSynth) and connects CLK3 directly to the oscillator which generates an output frequency determined by the XTAL frequency. 01: Select CLKIN as the clock source for CLK3. This by-passes both synthesis stages (PLL/VCXO & MultiSynth) and connects CLK3 directly to the CLKIN input. This essentially creates a buffered output of the CLKIN input. 10: Reserved. Do not select this option. 11: Select MultiSynth 3 as the source for CLK3. Select this option when using the Si5351 to generate free-running or synchronous clocks.
1:0	CLK3_IDRV[1:0]	**CLK3 Output Rise and Fall time / Drive Strength Control.** 00: 2 mA 01: 4 mA 10: 6 mA 11: 8 mA

Register 24. CLK1–0 Disable State

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved		CLK1_DIS_STATE[1:0]		CLK0_DIS_STATE[1:0]		Reserved	
Type	R/W		R/W		R/W		R/W	

Reset value = 0000 0000

Bit	Name	Function
7:6	Reserved	Reserved. Leave as default.
5:4	CLK1_DIS_STATE[1:0]	**Clock 1 Disable State.** These 2 bits determine the state of the CLK1 output when disabled. Individual output clocks can be disabled using register Output Enable Control located at address 3. Outputs are also disabled using the OEB pin. 00: CLK1 is set to a LOW state when disabled. 01: CLK1 is set to a HIGH state when disabled. 10: CLK1 is set to a HIGH IMPEDANCE state when disabled. 11: CLK1 is NEVER DISABLED.
3:2	CLK0_DIS_STATE[1:0]	**Clock 0 Disable State.** These 2 bits determine the state of the CLK0 output when disabled. Individual output clocks can be disabled using register Output Enable Control located at address 3. Outputs are also disabled using the OEB pin. 00: CLK0 is set to a LOW state when disabled. 01: CLK0 is set to a HIGH state when disabled. 10: CLK0 is set to a HIGH IMPEDANCE state when disabled. 11: CLK0 is NEVER DISABLED.
1:0	Reserved	Reserved. Leave as default.

Register 25. CLK3-2 Disable State

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLK3_DIS_STATE[1:0]		Reserved		CLK2_DIS_STATE[1:0]		Reserved	
Type	R/W		R/W		R/W		R/W	

Reset value = 0000 0000

Bit	Name	Function
7:6	CLK3_DIS_STATE[1:0]	**Clock 3 Disable State.** These 2 bits determine the state of the CLK3 output when disabled. Individual output clocks can be disabled using register Output Enable Control located at address 3. Outputs are also disabled using the OEB pin. 00: CLK3 is set to a LOW state when disabled. 01: CLK3 is set to a HIGH state when disabled. 10: CLK3 is set to a HIGH IMPEDANCE state when disabled. 11: CLK3 is NEVER DISABLED.
5:4	Reserved	Reserved. Leave as default.
3:2	CLK2_DIS_STATE[1:0]	**Clock 2 Disable State**. These 2 bits determine the state of the CLK2 output when disabled. Individual output clocks can be disabled using register Output Enable Control located at address 3. Outputs are also disabled using the OEB pin. 00: CLK2 is set to a LOW state when disabled. 01: CLK2 is set to a HIGH state when disabled. 10: CLK2 is set to a HIGH IMPEDANCE state when disabled. 11: CLK2 is NEVER DISABLED.
1:0	Reserved	Reserved. Leave as default.

Register 26. Multisynth NA Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSNA_P3[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSNA_P3[15:8]	**Multisynth NA Parameter 3.** This 20-bit number is an encoded representation of the denominator for the fractional part of the PLLA Feedback Multisynth Divider.

Register 27. Multisynth NA Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSNA_P3[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSNA_P3[7:0]	**Multisynth NA Parameter 3.** This 20-bit number is an encoded representation of the denominator for the fractional part of the PLLA Feedback Multisynth Divider.

Register 28. Multisynth NA Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Unused				Reserved		MSNA_P1[17:16]	
Type					R/W		R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7:4	Unused	Unused.
3:2	Reserved	Reserved. Leave as default, 0.
1:0	MSNA_P1[17:16]	**Multisynth NA Parameter 1.** This 18-bit number is an encoded representation of the integer part of the PLLA Feedback Multisynth divider.

Register 29. Multisynth NA Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSNA_P1[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSNA_P1[15:8]	**Multisynth NA Parameter 1.** This 18-bit number is an encoded representation of the integer part of the PLLA Feedback Multisynth divider.

Register 30. Multisynth NA Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSNA_P1[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSNA_P1[7:0]	**Multisynth NA Parameter 1.** This 18-bit number is an encoded representation of the integer part of the PLLA Feedback Multisynth divider.

Register 31. Multisynth NA Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSNA_P3[19:16]				MSNA_P2[19:16]			
Type	R/W				R/W			

Reset value = xxxx xxxx

Bit	Name	Function
7:4	MSNA_P3[19:16]	**Multisynth NA Parameter 3.** This 20-bit number is an encoded representation of the denominator for the fractional part of the PLLA Feedback Multisynth divider.
3:0	MSNA_P2[19:16]	**Multisynth NA Parameter 2.** This 20-bit number is an encoded representation of the numerator for the fractional part of the PLLA Feedback Multisynth divider.

Register 32. Multisynth NA Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSNA_P2[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSNA_P2[15:8]	**Multisynth NA Parameter 2.** This 20-bit number is an encoded representation of the numerator for the fractional part of the PLLA Feedback Multisynth divider.

Register 33. Multisynth NA Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSNA_P2[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSNA_P2[7:0]	**Multisynth NA Parameter 2.** This 20-bit number is an encoded representation of the numerator for the fractional part of the PLLA Feedback Multisynth divider.

Register 34. Multisynth NB Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSNB_P3[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSNB_P3[15:8]	**Multisynth NA Parameter 3.** This 20-bit number is an encoded representation of the denominator for the fractional part of the PLLA Feedback Multisynth divider.

Register 35. Multisynth NB Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSNB_P3[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSNB_P3[7:0]	**Multisynth NB Parameter 3.** This 20-bit number is an encoded representation of the denominator for the fractional part of the PLLB Feedback Multisynth divider.

Register 36. Multisynth NB Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Unused				Reserved		MSNB_P1[17:16]	
Type					R/W		R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7:4	Unused	
3:2	Reserved	Reserved. Leave as default, 0.
1:0	MSNB_P1[17:16]	**Multisynth NB Parameter 1.** This 18-bit number is an encoded representation of the integer part for the fractional part of the PLLB Feedback Multisynth divider.

Register 37. Multisynth NB Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSNB_P1[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSNB_P1[15:8]	**Multisynth NB Parameter 1.** This 18-bit number is an encoded representation of the integer part of the PLLB Feedback Multisynth divider.

Register 38. Multisynth NB Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSNB_P1[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSNB_P1[7:0]	**Multisynth NB Parameter 1.** This 18-bit number is an encoded representation of the integer part of the PLLB Feedback Multisynth divider.

Register 39. Multisynth NB Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSNB_P3[19:16]				MSNB_P2[19:16]			
Type	R/W				R/W			

Reset value = xxxx xxxx

Bit	Name	Function
7:4	MSNB_P3[19:16]	**Multisynth NB Parameter 3.** This 20-bit number is an encoded representation of the denominator for the fractional part of the PLLB Feedback Multisynth divider.
3:0	MSNB_P2[19:16]	**Multisynth NB Parameter 2.** This 20-bit number is an encoded representation of the numerator for the fractional part of the PLLB Feedback Multisynth divider.

Register 40. Multisynth NB Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSNB_P2[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSNB_P2[15:8]	**Multisynth NB Parameter 2.** This 20-bit number is an encoded representation of the numerator for the fractional part of the PLLB Feedback Multisynth divider.

Register 41. Multisynth NB Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSNB_P2[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSNB_P2[7:0]	**Multisynth NB Parameter 2.** This 20-bit number is an encoded representation of the numerator for the fractional part of the PLLB Feedback Multisynth divider.

Register 50. Multisynth0 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_P3[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_P3[15:8]	**Multisynth0 Parameter 3.** This 20-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth0 Divider.

Register 51. Multisynth0 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_P3[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_P3[7:0]	**Multisynth0 Parameter 3.** This 20-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth0 Divider.

Register 52. Multisynth0 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		R0_DIV[2:0]			MS0_DIVBY4[1:0]		MS0_P1[17:16]	
Type		R/W			R/W		R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7	Unused	
6:4	R0_DIV[2:0]	**R0 Output Divider.** 000b: Divide by 1 001b: Divide by 2 010b: Divide by 4 011b: Divide by 8 100b: Divide by 16 101b: Divide by 32 110b: Divide by 64 111b: Divide by 128
3:2	MS0_DIVBY4[1:0]	**MS0 Divide by 4 Enable.** 11: Divide by 4 enabled. 00: Divide by a value other than 4.
1:0	MS0_P1[17:16]	**Multisynth0 Parameter 1.** This 18-bit number is an encoded representation of the integer part of the MultiSynth0 divider.

Register 53. Multisynth0 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_P1[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_P1[15:8]	**Multisynth0 Parameter 1.** This 18-bit number is an encoded representation of the integer part of the MultiSynth0 divider.

Register 54. Multisynth0 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_P1[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_P1[7:0]	**Multisynth0 Parameter 1.** This 18-bit number is an encoded representation of the integer part of the MultiSynth0 divider.

Register 55. Multisynth0 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_P3[19:16]				MS0_P2[19:16]			
Type	R/W				R/W			

Reset value = xxxx xxxx

Bit	Name	Function
7:4	MS0_P3[19:16]	**Multisynth0 Parameter 3.** This 20-bit number is an encoded representation of the denominator for the fractional part of the Multisynth0 Divider
3:0	MS0_P2[19:16]	**Multisynth0 Parameter 2.** This 20-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth0 Divider.

Register 56. Multisynth0 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_P2[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_P2[15:8]	**Multisynth0 Parameter 2.** This 20-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth0 divider.

Register 57. Multisynth0 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS0_P2[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS0_P2[7:0]	**Multisynth0 Parameter 2.** This 20-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth0 divider.

Register 58. Multisynth1 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_P3[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS1_P3[15:8]	**Multisynth1 Parameter 3.** This 20-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth1 divider.

Register 59. Multisynth1 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_P3[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS1_P3[7:0]	**Multisynth1 Parameter 3.** This 20-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth1 divider.

Register 60. Multisynth1 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		R1_DIV[2:0]			MS1_DIVBY4[1:0]		MS1_P1[17:16]	
Type		R/W			R/W		R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7	Unused	
6:4	R1_DIV[2:0]	**R1 Output Divider.** 000b: Divide by 1 001b: Divide by 2 010b: Divide by 4 011b: Divide by 8 100b: Divide by 16 101b: Divide by 32 110b: Divide by 64 111b: Divide by 128
3:2	MS1_DIVBY4[1:0]	**MS1 Divide by 4 Enable.** 11: Divide by 4 enabled. 00: Divide by a value other than 4.
1:0	MS1_P1[17:16]	**Multisynth1 Parameter 1.** This 18-bit number is an encoded representation of the integer part of the Multisynth1 divider.

Register 61. Multisynth1 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_P1[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS1_P1[15:8]	**Multisynth1 Parameter 1.** This 18-bit number is an encoded representation of the integer part of the Multisynth1 divider.

Register 62. Multisynth1 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_P1[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS1_P1[7:0]	**Multisynth1 Parameter 1.** This 18-bit number is an encoded representation of the integer part of the Multisynth1 divider.

Register 63. Multisynth1 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_P3[19:16]				MS1_P2[19:16]			
Type	R/W				R/W			

Reset value = xxxx xxxx

Bit	Name	Function
7:4	MS1_P3[19:16]	**Multisynth1 Parameter 3.** This 20-bit number is an encoded representation of the denominator for the fractional part of the Multisynth1 divider
3:0	MS1_P2[19:16]	**Multisynth1 Parameter 2.** This 20-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth1 divider.

Register 64. Multisynth1 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_P2[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS1_P2[15:8]	**Multisynth1 Parameter 2.** This 20-bit number is an encoded representation of the numerator for the fractional part of the Multisynth1 divider.

Register 65. Multisynth1 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS1_P2[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS1_P2[7:0]	**Multisynth1 Parameter 2.** This 20-bit number is an encoded representation of the numerator for the fractional part of the Multisynth1 divider.

Register 82. Multisynth2 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_P3[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS2_P3[15:8]	**Multisynth2 Parameter 3.** This 20-bit number is an encoded representation of the denominator for the fractional part of the Multisynth2 divider.

Register 83. Multisynth2 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_P3[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS2_P3[7:0]	**Multisynth2 Parameter 3.** This 20-bit number is an encoded representation of the denominator for the fractional part of the Multisynth2 divider.

Register 84. Multisynth2 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		R2_DIV[2:0]			MS2_DIVBY4[1:0]		MS2_P1[17:16]	
Type		R/W			R/W		R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7	Unused	
6:4	R2_DIV[2:0]	**R2 Output Divider.** 000b: Divide by 1 001b: Divide by 2 010b: Divide by 4 011b: Divide by 8 100b: Divide by 16 101b: Divide by 32 110b: Divide by 64 111b: Divide by 128
3:2	MS2_DIVBY4[1:0]	**MS2 Divide by 4 Enable.** 11: Divide by 4 enabled. 00: Divide by a value other than 4.
1:0	MS2_P1[17:16]	**Multisynth2 Parameter 1.** This 18-bit number is an encoded representation of the integer part of the Multisynth2 divider.

Register 85. Multisynth2 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_P1[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS2_P1[15:8]	**Multisynth2 Parameter 1.** This 18-bit number is an encoded representation of the integer part of the Multisynth2 divider.

Register 86. Multisynth2 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_P1[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS2_P1[7:0]	**Multisynth2 Parameter 1.** This 18-bit number is an encoded representation of the integer part of the Multisynth2 divider.

Register 87. Multisynth2 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_P3[19:16]				MS2_P2[19:16]			
Type	R/W				R/W			

Reset value = xxxx xxxx

Bit	Name	Function
7:4	MS2_P3[19:16]	**Multisynth2 Parameter 3.** This 20-bit number is an encoded representation of the denominator for the fractional part of the Multisynth2 divider
3:0	MS2_P2[19:16]	**Multisynth2 Parameter 2.** This 20-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth2 divider.

Register 88. Multisynth2 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_P2[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS2_P2[15:8]	**Multisynth2 Parameter 2.** This 20-bit number is an encoded representation of the numerator for the fractional part of the Multisynth2 Divider.

Register 89. Multisynth2 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS2_P2[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS2_P2[7:0]	**Multisynth2 Parameter 2.** This 20-bit number is an encoded representation of the numerator for the fractional part of the Multisynth2 Divider.

Register 91. Multisynth3 Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MS3_P1[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MS3_P1[7:0]	**Multisynth3 Parameter 1.** This 8-bit number is the Multisynth3 divide ratio. The multisynth3 divide ratio can only be even integers greater than or equal to 6. All other divide values are invalid.

Register 92. Clock 3 Output Divider

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved	R3_DIV[2:0]			Reserved			
Type	R/W	R/W			R/W			

Reset value = xxxx xxxx

Bit	Name	Function
7	Reserved	Leave as default.
6:4	R3_DIV[2:0]	**R3 Output Divider.** 000b: Divide by 1 001b: Divide by 2 010b: Divide by 4 011b: Divide by 8 100b: Divide by 16 101b: Divide by 32 110b: Divide by 64 111b: Divide by 128
3:0	Reserved	Leave as default.

Register 149. Spread Spectrum Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SSC_EN	SSDN_P2[14:8]						
Type	R/W	R/W						

Reset value = xxxx xxxx

Bit	Name	Function
7	SSC_EN	**Spread Spectrum Enable** 1: Enable 0: Disable Spread Spectrum Enable control pin is available on the Si5351A and B devices. Spread spectrum enable functionality is a logical OR of the SSEN pin and SSC_EN register bit, so for the SSEN pin to work properly, this register bit must be set to 0.
6:0	SSDN_P2[14:8]	**PLL A Spread Spectrum Down Parameter 2.**

Register 150. Spread Spectrum Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SSDN_P2[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	SSDN_P2[7:0]	**PLL A Spread Spectrum Down Parameter 2.**

Register 151. Spread Spectrum Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SSC_MODE	SSDN_P3[14:8]						
Type	R/W	R/W						

Reset value = xxxx xxxx

Bit	Name	Function
7	SSC_MODE	**Spread Spectrum Mode.** 0: Down Spread 1: Center Spread
6:0	SSDN_P3[14:8]	**PLL A Spread Spectrum Down Parameter 3.**

Register 152. Spread Spectrum Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SSDN_P3[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	SSDN_P3[7:0]	**PLL A Spread Spectrum Down Parameter 3.**

Register 153. Spread Spectrum Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SSDN_P1[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	SSDN_P1[7:0]	**PLL A Spread Spectrum Down Parameter 1.**

Register 154. Spread Spectrum Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SSUDP[11:8]				SSDN_P1[11:8]			
Type	R/W				R/W			

Reset value = xxxx xxxx

Bit	Name	Function
7:4	SSUDP[11:8]	**PLL A Spread Spectrum Up/Down Parameter.**
3:0	SSDN_P1[11:8]	**PLL A Spread Spectrum Down Parameter 1.**

Register 155. Spread Spectrum Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SSUDP[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	SSUDP[7:0]	**PLL A Spread Spectrum Up/Down Parameter.**

Register 156. Spread Spectrum Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		SSUP_P2[14:8]						
Type		R/W						

Reset value = xxxx xxxx

Bit	Name	Function
7	Unused	Unused.
6:0	SSUP_P2[14:8]	**PLL A Spread Spectrum Up Parameter 2.**

Register 157. Spread Spectrum Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SSUP_P2[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	SSUP_P2[7:0]	**PLL A Spread Spectrum Up Parameter 2.**

Register 158. Spread Spectrum Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		SSUP_P3[14:8]						
Type		R/W						

Reset value = xxxx xxxx

Bit	Name	Function
7	Unused	Unused.
6:0	SSUP_P3[14:8]	**PLL A Spread Spectrum Up Parameter 3.**

Register 159. Spread Spectrum Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SSUP_P3[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	SSUP_P3[7:0]	**PLL A Spread Spectrum Up Parameter 3.**

Register 160. Spread Spectrum Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SSUP_P1[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	SSUP_P1[7:0]	**PLL A Spread Spectrum Up Parameter 1.**

Register 161. Spread Spectrum Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SS_NCLK[3:0]				SSUP_P1[11:8]			
Type	R/W				R/W			

Reset value = xxxx xxxx

Bit	Name	Function
7:4	SS_NCLK[3:0]	Must write 0000b to these bits.
3:0	SSUP_P1[11:8]	**PLL A Spread Spectrum Up Parameter 1.**

Register 162. VCXO Parameter

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VCXO_Param[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	VCXO_Param[7:0]	**VCXO Parameter.**

Register 163. VCXO Parameter

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VCXO_Param[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	VCXO_Param[15:8]	**VCXO Parameter.**

Register 164. VCXO Parameter

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved		VCXO_Param[21:16]					
Type	R/W		R/W					

Reset value = xxxx xxxx

Bit	Name	Function
7:6	Reserved	Only write 00b to these bits.
5:0	VCXO_Param[21:16]	**VCXO Parameter.**

Register 166. CLK0 Initial Phase Offset

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved	CLK0_PHOFF[6:0]						
Type	R/W	R/W						

Reset value = 0000 0000

Bit	Name	Function
7	Reserved	Only write 0 to this bit.
6:0	CLK0_PHOFF[6:0]	**Clock 0 Initial Phase Offset.** CLK0_PHOFF[6:0] is an unsigned integer with one LSB equivalent to a time delay of Tvco/4, where Tvco is the period of the VCO/PLL associated with this output.

Register 167. CLK1 Initial Phase Offset

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved	CLK1_PHOFF[6:0]						
Type	R/W	R/W						

Reset value = 0000 0000

Bit	Name	Function
7	Reserved	Only write 0 to this bit.
6:0	CLK1_PHOFF[6:0]	**Clock 1 Initial Phase Offset.** CLK1_PHOFF[6:0] is an unsigned integer with one LSB equivalent to a time delay of Tvco/4, where Tvco is the period of the VCO/PLL associated with this output.

Register 170. CLK2 Initial Phase Offset

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved	CLK2_PHOFF[6:0]						
Type	R/W	R/W						

Reset value = 0000 0000

Bit	Name	Function
7	Reserved	Only write 0 to this bit.
6:0	CLK2_PHOFF[6:0]	**Clock 2 Initial Phase Offset.** CLK2_PHOFF[6:0] is an unsigned integer with one LSB equivalent to a time delay of Tvco/4, where Tvco is the period of the VCO/PLL associated with this output.

Register 177. PLL Reset

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PLLB_RST	Reserved	PLLA_RST	Reserved				
Type	R/W	R/W	R/W	R/W				

Reset value = 0000 0000

Bit	Name	Function
7	PLLB_RST	**PLLB_Reset.** Writing a 1 to this bit will reset PLLB. This is a self clearing bit.
6	Reserved	Leave as default.
5	PLLA_RST	**PLLA_Reset.** Writing a 1 to this bit will reset PLLA. This is a self clearing bit.
4:0	Reserved	Leave as default.

Register 183. Crystal Internal Load Capacitance

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	XTAL_CL[1:0]		Reserved					
Type	R/W		R/W					

Reset value = 11xx xxxx

Bit	Name	Function
7:6	XTAL_CL[1:0]	**Crystal Load Capacitance Selection.** These 2 bits determine the internal load capacitance value for the crystal. See the Crystal Inputs section in the Si5351 data sheet. 00: Reserved. Do not select this option. 01: Internal CL = 6 pF. 10: Internal CL = 8 pF. 11: Internal CL = 10 pF (default).
5:0	Reserved	Bits 5:0 should be written to 010010b.

Register 187. Fanout Enable

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLKIN_FANOUT_EN	XO_FANOUT_EN	Reserved					
Type	R/W	R/W	R/W					

Reset value = xxxx xxxx

Bit	Name	Function
7	CLKIN_FANOUT_EN	**Enable fanout of CLKIN to clock output multiplexers. Set this bit to 1b.**
6	XO_FANOUT_EN	**Enable fanout of XO to clock output multiplexers. Set this bit to 1b.**
5:0	Reserved	Reserved.

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